THE DATASHEET OF

LM2734ZMK/NOPB

TEXAS INSTRUMENTS

LM2734Z, LM2734Z-Q1

SNVS334F – JANUARY 2005 – REVISED JANUARY 2016

LM2734Z/-Q1 Thin SOT 1-A Load Step-Down DC-DC Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C6
- 6-pin SOT Package, or 6-Pin WSON Package
- 3.0-V to 20-V Input Voltage Range
- 0.8-V to 18-V Output Voltage Range
- 1-A Output Current
- 3-MHz Switching Frequency
- 300-mΩ NMOS Switch
- 30-nA Shutdown Current
- 0.8-V, 2% Internal Voltage Reference
- Internal Soft-Start
- Current-Mode, PWM Operation
- Thermal Shutdown

2 Applications

- DSL Modems
- Local Point of Load Regulation
- Battery-Powered Devices
- USB-Powered Devices
- Automotive

3 Description

The LM2734Z regulator is a monolithic, high-frequency, PWM step-down DC–DC converter assembled in a thick 6-pin SOT and a WSON non-pullback package. The device provides all the active functions to provide local DC–DC conversion with fast transient response and accurate regulation in the smallest possible PCB area.

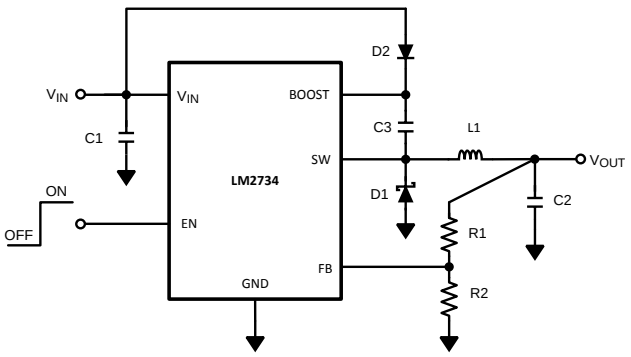
With a minimum of external components and online design support through WEBENCH™, the LM2734Z is easy to use. The ability to drive 1-A loads with an internal 300-mΩ NMOS switch using state-of-the-art 0.5-µm BiCMOS technology results in the best power density available. The world class control circuitry allows for ON-times as low as 13 ns, thus supporting exceptionally high-frequency conversion over the entire 3-V to 20-V input operating range down to the minimum output voltage of 0.8 V. Switching frequency is internally set to 3 MHz, allowing the use of extremely small surface mount inductors and chip capacitors. Even though the operating frequency is very high, efficiencies up to 85% are easy to achieve. External shutdown is included, featuring an ultra-low standby current of 30 nA. The LM2734Z uses current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, and output overvoltage protection.

Device Information(1)

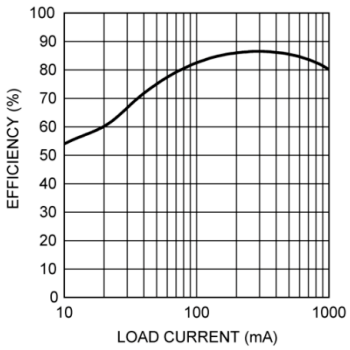
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2734Z	WSON (6)	3.00 mm × 3.00 mm
	SOT (6)	1.60 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Efficiency vs Load Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F **Page**

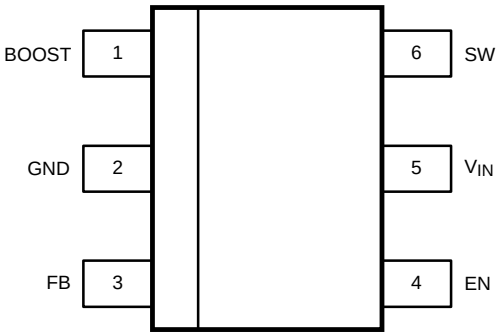
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed soldering information ... 4

Changes from Revision D (April 2013) to Revision E **Page**

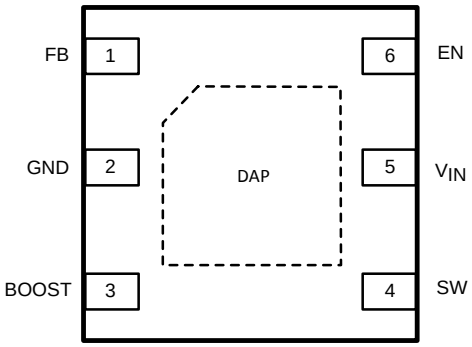
- Changed layout of National Data Sheet to TI format ... 25

5 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



NGG Package
6-Pin WSON
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	SOT	WSON		
BOOST	1	3	I	Boost voltage that drives the internal NMOS control switch. A bootstrap capacitor is connected between the BOOST and SW pins.
DAP	—	—	P	The die attach pad is internally connected to GND.
EN	4	6	I	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
FB	3	1	I	Feedback pin. Connect FB to the external resistor divider to set output voltage.
GND	2	2	P	Signal and Power ground pin. Place the bottom resistor of the feedback network as close as possible to this pin for accurate regulation.
SW	6	4	O	Output switch. Connects to the inductor, catch diode, and bootstrap capacitor.
V_{IN}	5	5	P	Input supply voltage. Connect a bypass capacitor to this pin.

(1) I –Input, O – Output, P – Power

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.5	24	V
	SW voltage	–0.5	24	V
	Boost voltage	–0.5	30	V
	Boost to SW voltage	–0.5	6	V
	FB voltage	–0.5	3	V
	EN voltage	–0.5	V_{IN} + 0.3	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)(2)	±2000	V
		Charged-device model (CDM), per AEC Q100-002	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Human-body model, 1.5 kΩ in series with 100 pF.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	3	20	V
	SW voltage	–0.5	20	V
	Boost voltage	–0.5	25	V
	Boost to SW voltage	1.6	5.5	V
T_J	Junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM2734Z		UNIT
		DDC (SOT)	NGG (WSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	180.3	56.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	52.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.7	30.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.3	30.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) Thermal shutdown occurs if the junction temperature exceeds 165°C. The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly onto a 3-in × 3-in printed-circuit-board with 2-oz. copper on 4 layers in still air. For a 2-layer board using 1-oz. copper in still air, $R_{\theta JA}$ = 204°C/W.

6.5 Electrical Characteristics

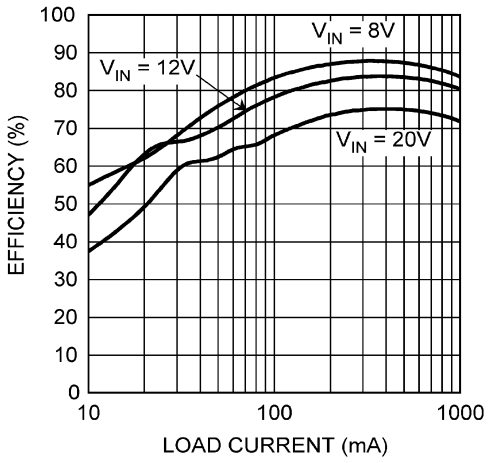
All typical specifications are for T_J = 25°C, and all maximum and minimum limits apply over the full operating temperature range (T_J = –40°C to 125°C). V_{IN} = 5 V, $V_{BOOST} – V_{SW}$ = 5 V (unless otherwise noted). Data sheet minimum and maximum specification limits are specified by design, test, or statistical analysis.

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
V_{FB}	Feedback voltage		0.784	0.8	0.816	V
$\Delta V_{FB}/\Delta V_{IN}$	Feedback voltage line regulation	V_{IN} = 3 V to 20 V		0.01		% / V
I_{FB}	Feedback input bias current	Sink and source		10	250	nA
UVLO	Undervoltage lockout	V_{IN} Rising		2.74	2.90	V
	Undervoltage lockout	V_{IN} Falling	2	2.3		
	UVLO hysteresis		0.30	0.44	0.62	
F_{SW}	Switching frequency		2.2	3.0	3.6	MHz
D_{MAX}	Maximum duty cycle		78%	85%		
D_{MIN}	Minimum duty Cycle			8%		
$R_{DS(ON)}$	Switch ON resistance	V_{BOOST} - V_{SW} = 3 V (SOT Package)		300	600	mΩ
		V_{BOOST} - V_{SW} = 3 V (WSON Package)		340	650	mΩ
I_{CL}	Switch current limit	V_{BOOST} - V_{SW} = 3 V	1.2	1.7	2.5	A
I_Q	Quiescent current	Switching		1.5	2.5	mA
	Quiescent current (shutdown)	V_{EN} = 0 V		30		nA
I_{BOOST}	Boost pin current	(Switching)		4.25	6	mA
V_{EN_TH}	Shutdown threshold voltage	V_{EN} Falling			0.4	V
	Enable threshold voltage	V_{EN} Rising	1.8			
I_{EN}	Enable pin current	Sink/source		10		nA
I_{SW}	Switch leakage			40		nA

(1) Specified to Texas Instruments' Average Outgoing Quality Level (AOQL).
(2) Typicals represent the most likely parametric norm.

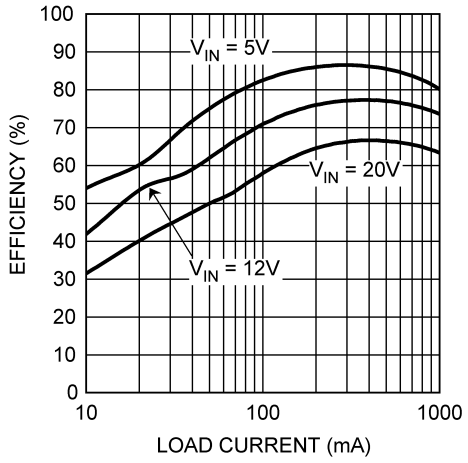
6.6 Typical Characteristics

at V_{IN} = 5 V, V_{BOOST} - V_{SW} = 5 V, L1 = 2.2 µH and T_A = 25°C (unless otherwise noted)



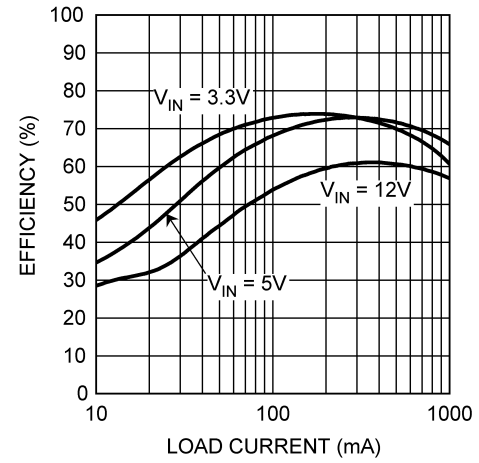
V_{OUT} = 5 V

Figure 1. Efficiency vs Load Current



V_{OUT} = 3.3 V

Figure 2. Efficiency vs Load Current



V_{OUT} = 1.5 V

Figure 3. Efficiency vs Load Current

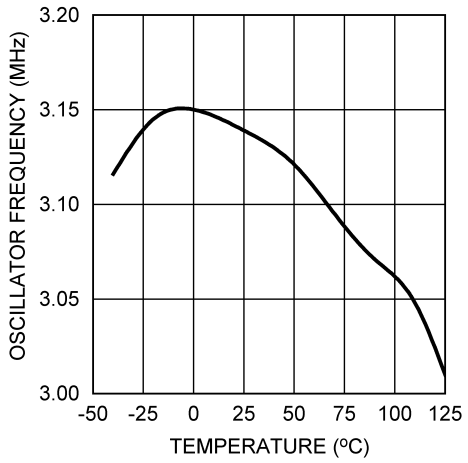
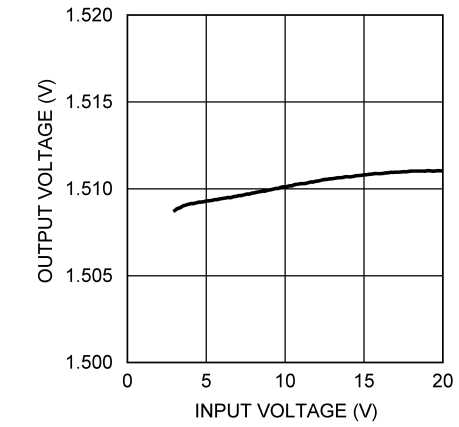
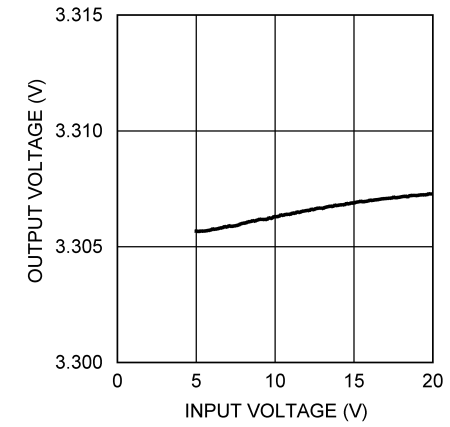


Figure 4. Oscillator Frequency vs Temperature



V_{OUT} = 1.5 V I_{OUT} = 500 mA

Figure 5. Line Regulation



V_{OUT} = 3.3 V I_{OUT} = 500 mA

Figure 6. Line Regulation

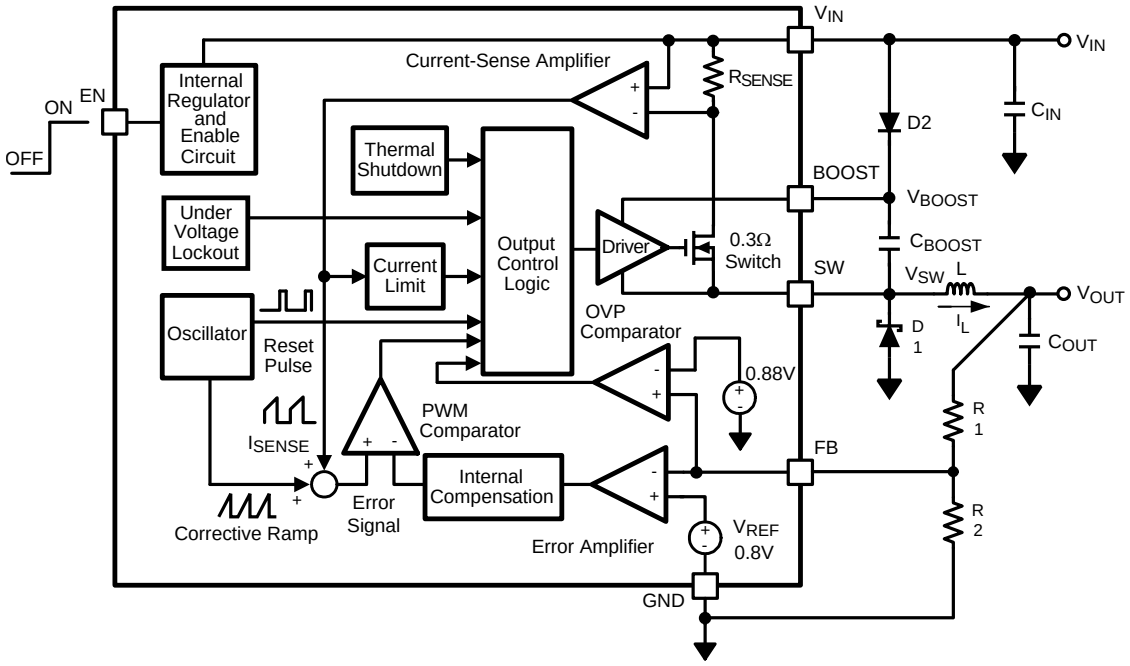
7 Detailed Description

7.1 Overview

The LM2734Z is a constant frequency buck regulator that can deliver load current of 1 A. Device is optimized for high-efficiency operation and includes a number of features that make it suitable for demanding applications. High switching frequency allows for use of small external components enabling small solution size and saving board space.

Device is designed to operate from wide input voltage range up to 20 V, making it ideal for wide range of applications (such as automotive, industrial, communications, and so forth). LM2734Z can be controlled through shutdown pin, consuming only 30 nA in standby mode, making it very appealing for applications that demand very low standby power consumption.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Theory of Operation

The LM2734Z is a constant frequency PWM buck regulator IC that delivers a 1-A load current. The regulator has a preset switching frequency of 3 MHz. This high frequency allows the LM2734Z to operate with small surface mount capacitors and inductors, resulting in a DC–DC converter that requires a minimum amount of board space. The LM2734Z is internally compensated, so it is simple to use, and requires few external components. The LM2734Z uses current-mode control to regulate the output voltage.

The following operating description of the LM2734Z refers to the *Functional Block Diagram* and to the waveforms in Figure 7. The LM2734Z supplies a regulated output voltage by switching the internal NMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS control switch. During this ON-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current-sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the corrective ramp of the

Feature Description (continued)

regulator and compared to the output of the error amplifier, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch OFF-time, inductor current discharges through Schottky diode D1, which forces the SW pin to swing below ground by the forward voltage (V_D) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

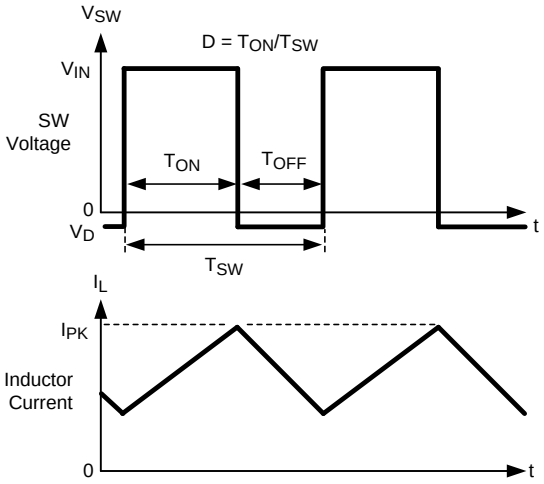


Figure 7. LM2734Z Waveforms of SW Pin Voltage and Inductor Current

7.3.2 Boost Function

Capacitor C_{BOOST} and diode D2 in Figure 8 are used to generate a voltage V_{BOOST}. V_{BOOST} - V_{SW} is the gate drive voltage to the internal NMOS control switch. To properly drive the internal NMOS switch during its ON-time, V_{BOOST} needs to be at least 1.6 V greater than V_{SW}. Although the LM2734Z operates with this minimum voltage, it may not have sufficient gate drive to supply large values of output current. Therefore, TI recommends that V_{BOOST} be greater than 2.5 V above V_{SW} for best efficiency. V_{BOOST} – V_{SW} must not exceed the maximum operating limit of 5.5 V.

5.5 V > V_{BOOST} – V_{SW} > 2.5 V for best performance.

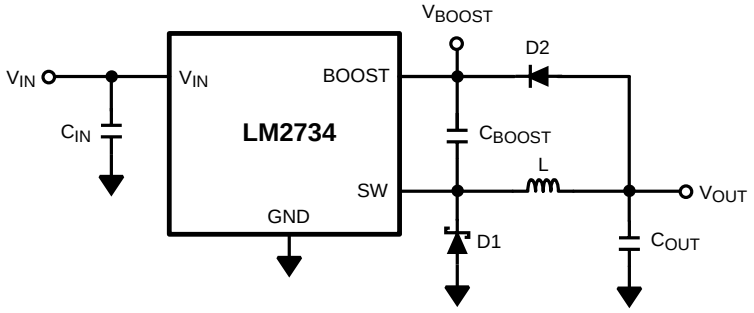


Figure 8. V_{OUT} Charges C_{BOOST}

When the LM2734Z starts up, internal circuitry from the BOOST pin supplies a maximum of 20 mA to C_{BOOST}. This current charges C_{BOOST} to a voltage sufficient to turn the switch on. The BOOST pin continues to source current to C_{BOOST} until the voltage at the feedback pin is greater than 0.76 V.

Feature Description (continued)

There are various methods to derive V_{BOOST}:

1. From the input voltage (V_{IN})
2. From the output voltage (V_{OUT})
3. From an external distributed voltage rail (V_{EXT})
4. From a shunt or series zener diode

In *Functional Block Diagram*, capacitor C_{BOOST} and diode D2 supply the gate-drive current for the NMOS switch. Capacitor C_{BOOST} is charged through diode D2 by V_{IN}. During a normal switching cycle, when the internal NMOS control switch is off (T_{OFF}) (refer to Figure 7), V_{BOOST} equals V_{IN} minus the forward voltage of D2 (V_{FD2}), during which the current in the inductor (L) forward biases the Schottky diode D1 (V_{FD1}). Therefore the voltage stored across C_{BOOST} is calculated using Equation 1.

$$V_{BOOST} - V_{SW} = V_{IN} - V_{FD2} + V_{FD1} \quad (1)$$

When the NMOS switch turns on (T_{ON}), the switch pin rises to:

$$V_{SW} = V_{IN} - (R_{DSON} \times I_L), \quad (2)$$

forcing V_{BOOST} to rise thus reverse biasing D2. The voltage at V_{BOOST} is then:

$$V_{BOOST} = 2\ V_{IN} - (R_{DSON} \times I_L) - V_{FD2} + V_{FD1} \quad (3)$$

which is approximately:

$$2\ V_{IN} - 0.4\ V \quad (4)$$

for many applications. Thus the gate-drive voltage of the NMOS switch is approximately:

$$V_{IN} - 0.2\ V \quad (5)$$

An alternate method for charging C_{BOOST} is to connect D2 to the output as shown in Figure 8. The output voltage must be between 2.5 V and 5.5 V, so that proper gate voltage is applied to the internal switch. In this circuit, C_{BOOST} provides a gate drive voltage that is slightly less than V_{OUT}.

In applications where both V_{IN} and V_{OUT} are greater than 5.5 V, or less than 3 V, C_{BOOST} cannot be charged directly from these voltages. If V_{IN} and V_{OUT} are greater than 5.5 V, C_{BOOST} can be charged from V_{IN} or V_{OUT} minus a Zener voltage by placing a Zener diode D3 in series with D2, as shown in Figure 9. When using a series Zener diode from the input, ensure that the regulation of the input supply does not create a voltage that falls outside the recommended V_{BOOST} voltage.

$$(V_{INMAX} - V_{D3}) < 5.5V \quad (6)$$

$$(V_{INMIN} - V_{D3}) > 1.6V \quad (7)$$

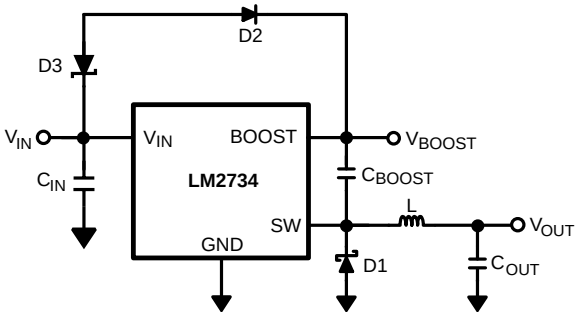


Figure 9. Zener Reduces Boost Voltage from V_{IN}

An alternative method is to place the Zener diode D3 in a shunt configuration as shown in Figure 10. A small 350-mW to 500-mW, 5.1-V Zener in a SOT or SOD package can be used for this purpose. A small ceramic capacitor such as a 6.3-V, 0.1-µF capacitor (C4) must be placed in parallel with the Zener diode. When the internal NMOS switch turns on, a pulse of current is drawn to charge the internal NMOS gate capacitance. The 0.1-µF parallel shunt capacitor ensures that the V_{BOOST} voltage is maintained during this time.

Feature Description (continued)

Resistor R3 must be chosen to provide enough RMS current to the Zener diode (D3) and to the BOOST pin. A recommended choice for the Zener current (I_{ZENER}) is 1 mA. The current I_{BOOST} into the BOOST pin supplies the gate current of the NMOS control switch and varies typically according to Equation 8.

$$I_{BOOST} = (D + 0.5) \times (V_{ZENER} - V_{D2}) \text{ mA} \quad (8)$$

where

- D is the duty cycle
- V_{ZENER} and V_{D2} are in volts
- I_{BOOST} is in milliamps
- V_{ZENER} is the voltage applied to the anode of the boost diode (D2)
- V_{D2} is the average forward voltage across D2

NOTE

Equation 8 for I_{BOOST} gives typical current.

For the worst case I_{BOOST}, increase the current by 25%. In that case, the worse-case boost current is:

$$I_{BOOST\text{-}MAX} = 1.25 \times I_{BOOST} \quad (9)$$

R3 is then given by Equation 10.

$$R3 = (V_{IN} - V_{ZENER}) / (1.25 \times I_{BOOST} + I_{ZENER}) \quad (10)$$

For example, let V_{IN} = 10 V, V_{ZENER} = 5 V, V_{D2} = 0.7 V, I_{ZENER} = 1 mA, and duty cycle D = 50%. Then:

$$I_{BOOST} = (0.5 + 0.5) \times (5 - 0.7) \text{ mA} = 4.3 \text{ mA} \quad (11)$$

$$R3 = (10 \text{ V} - 5 \text{ V}) / (1.25 \times 4.3 \text{ mA} + 1 \text{ mA}) = 787 \ \Omega \quad (12)$$

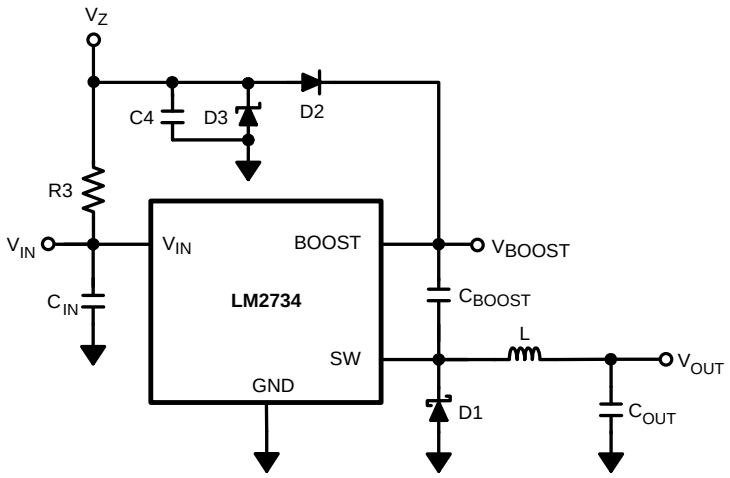


Figure 10. Boost Voltage Supplied from the Shunt Zener on V_{IN}

7.3.3 Soft-Start

This function forces V_{OUT} to increase at a controlled rate during start-up. During soft-start, the reference voltage of the error amplifier ramps from 0 V to its nominal value of 0.8 V in approximately 200 µs. This forces the regulator output to ramp up in a more linear and controlled fashion, which helps reduce inrush current.

7.3.4 Output Overvoltage Protection

The overvoltage comparator compares the FB pin voltage to a voltage that is 10% higher than the internal reference Vref. Once the FB pin voltage goes 10% above the internal reference, the internal NMOS control switch is turned off, which allows the output voltage to decrease toward regulation.

Feature Description (continued)

7.3.5 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LM2734Z from operating until the input voltage exceeds 2.74 V (typical).

The UVLO threshold has approximately 440 mV of hysteresis, so the part operates until V_{IN} drops below 2.3 V (typical). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

7.3.6 Current Limit

The LM2734Z uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 1.7 A (typical), and turns off the switch until the next switching cycle begins.

7.4 Device Functional Modes

7.4.1 Enable Pin and Shutdown Mode

The LM2734Z has a shutdown mode that is controlled by the enable pin (EN). When a logic low voltage is applied to EN, the part is in shutdown mode and its quiescent current drops to typically 30 nA. Switch leakage adds another 40 nA from the input supply. The voltage at this pin must never exceed V_{IN} + 0.3 V.

7.4.2 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch doesn't turn on until the junction temperature drops to approximately 150°C.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This device operates with wide input voltage in the range of 3 V to 20 V and provides regulated output voltage in the range of 0.8 V to 18 V. This device is optimized for high-efficiency operation with a minimum number of external components, making it ideal for applications where board space is constrained.

8.2 Typical Applications

8.2.1 LM2734Z Design Example 1

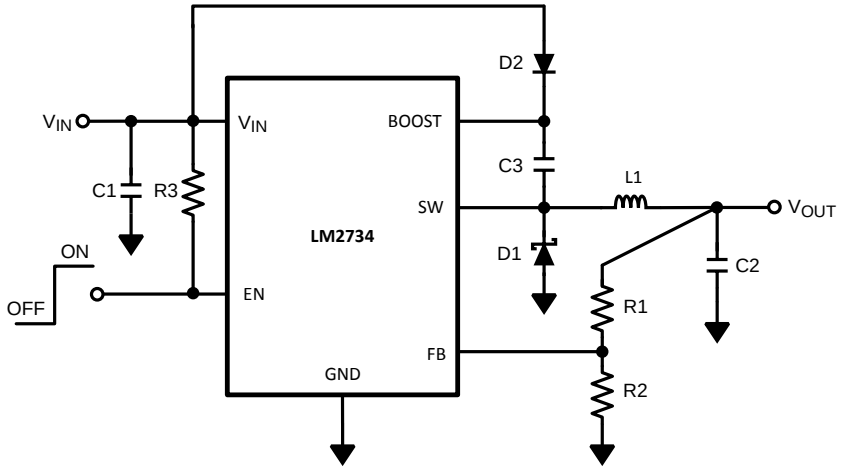


Figure 11. V_{BOOST} Derived from V_{IN}
Operating Conditions: 5 V to 1.5 V / 1 A

8.2.1.1 Design Requirements

Table 1 lists the operating conditions for the design example 1.

Table 1. Design Parameters

PARAMETER	VALUE		PARAMETER	VALUE
V_{IN}	5.0 V		P_{OUT}	2.5 W
V_{OUT}	2.5 V		P_{DIODE}	151 mW
I_{OUT}	1.0 A		P_{IND}	75 mW
V_D	0.35 V		P_{SWF}	53 mW
Freq	3 MHz		P_{SWR}	53 mW
I_Q	1.5 mA		P_{COND}	187 mW
T_{RISE}	8 ns		P_Q	7.5 mW
T_{FALL}	8 ns		P_{BOOST}	21 mW
R_{DSON}	330 mΩ		P_{LOSS}	548 mW
IND_{DCR}	75 mΩ			
D	56.8%			

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_O) to input voltage (V_{IN}) as shown in Equation 13.

$$D = \frac{V_O}{V_{IN}} \tag{13}$$

The catch diode (D1) forward voltage drop and the voltage drop across the internal NMOS must be included to calculate a more accurate duty cycle. Calculate D with Equation 14.

$$D = \frac{V_O + V_D}{V_{IN} + V_D - V_{SW}} \tag{14}$$

V_{SW} can be approximated by Equation 15.

$$V_{SW} = I_O \times R_{DS(ON)} \tag{15}$$

The diode forward drop (V_D) can range from 0.3 V to 0.7 V depending on the quality of the diode. The lower V_D is, the higher the operating efficiency of the converter.

The inductor value determines the output ripple current. Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value decreases the output ripple current. The ratio of ripple current (Δi_L) to output current (I_O) is optimized when it is set between 0.3 and 0.4 at 1 A. The ratio r is defined in Equation 16.

$$r = \frac{\Delta i_L}{I_O} \tag{16}$$

One must also ensure that the minimum current limit (1.2 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by Equation 17.

$$I_{LPK} = I_O + \Delta I_L/2 \tag{17}$$

If r = 0.5 at an output of 1 A, the peak current in the inductor is 1.25 A. The minimum specified current limit over all operating conditions is 1.2 A. One can either reduce r to 0.4 resulting in a 1.2-A peak current, or make the engineering judgement that 50 mA over is safe enough with a 1.7-A typical current limit and 6 sigma limits. When the designed maximum output current is reduced, the ratio r can be increased. At a current of 0.1 A, r can be made as high as 0.9. The ripple ratio can be increased at lighter loads because the net ripple is actually quite low, and if r remains constant the inductor value can be made quite large. An equation empirically developed for the maximum ripple ratio at any current below 2 A is:

$$r = 0.387 \times I_{OUT}^{-0.3667} \tag{18}$$

NOTE

Use this as a guideline.

The LM2734Z operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the *Output Capacitor* section for more details on calculating output voltage ripple.

Now that the ripple current or ripple ratio is determined, the inductance is calculated by Equation 19.

$$L = \frac{V_O + V_D}{I_O \times r \times f_S} \times (1\text{-}D) \tag{19}$$

where

- f_s is the switching frequency
- I_O is the output current

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation results in a sudden reduction in inductance and prevent the regulator from operating correctly. Because of the speed of the internal current limit, the peak current of the inductor need only be specified for the required maximum output current. For example, if the designed maximum output current is 0.5 A and the peak current is 0.7 A, then the inductor must be specified with a saturation current limit of >0.7 A. There is no need to specify the saturation or peak current of the inductor at the 1.7-A typical switch current limit. The difference in inductor size is a factor of 5. Because of the operating frequency of the LM2734Z, ferrite based inductors are preferred to minimize core losses. This presents little restriction because the variety of ferrite based inductors is huge. Lastly, inductors with lower series resistance (DCR) provides better operating efficiency. For recommended inductors, see the design examples in *Typical Applications*.

8.2.1.2.2 Input Capacitor

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and ESL (Equivalent Series Inductance). The recommended input capacitance is 10 µF, although 4.7 µF works well for input voltages below 6 V. The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating ($I_{RMS\text{-}IN}$) must be greater than:

$$I_{RMS\text{-}IN} = I_O \times \sqrt{D \times \left(1\text{-}D + \frac{r^2}{12}\right)} \tag{20}$$

As seen in Equation 20, the maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle, D, is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor has high ESL and a 0805 ceramic chip capacitor has very low ESL. At the operating frequencies of the LM2734Z, certain capacitors may have an ESL so large that the resulting impedance ($2\pi fL$) is higher than that required to provide stable operation. As a result, surface mount capacitors are strongly recommended. Sanyo POSCAP, Tantalum or Niobium, Panasonic SP or Cornell Dubilier ESR, and multilayer ceramic capacitors (MLCC) are all good choices for both input and output capacitors and have very low ESL. For MLCCs, TI recommends using X7R or X5R dielectrics. Consult capacitor manufacturer data sheet to see how rated capacitance varies over operating conditions.

8.2.1.2.3 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is shown in Equation 21.

$$\Delta V_O = \Delta i_L \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_O}\right) \tag{21}$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple is approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LM2734Z, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise couples through parasitic capacitances in the inductor

to the output. A ceramic capacitor bypasses this noise while a tantalum will not. Because the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum at 10 µF of output capacitance. Capacitance can be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R. Again, verify actual capacitance at the desired operating voltage and temperature.

Check the RMS current rating of the capacitor. The RMS current rating of the capacitor chosen must also meet Equation 22.

$$I_{RMS\text{-}OUT} = I_O \times \frac{r}{\sqrt{12}} \tag{22}$$

8.2.1.2.4 Catch Diode

The catch diode (D1) conducts during the switch OFF-time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode must be chosen so that its current rating is greater than Equation 23.

$$I_{D1} = I_O \times (1\text{-}D) \tag{23}$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency choose a Schottky diode with a low forward voltage drop.

8.2.1.2.5 Boost Diode

A standard diode such as the 1N4148 type is recommended. For V_{BOOST} circuits derived from voltages less than 3.3 V, a small-signal Schottky diode is recommended for greater efficiency. A good choice is the BAT54 small signal diode.

8.2.1.2.6 Boost Capacitor

A ceramic 0.01-µF capacitor with a voltage rating of at least 6.3 V is sufficient. The X7R and X5R MLCCs provide the best performance.

8.2.1.2.7 Output Voltage

The output voltage is set using Equation 24 where R2 is connected between the FB pin and GND, and R1 is connected between V_O and the FB pin. A good value for R2 is 10 kΩ.

$$R1 = \left(\frac{V_O}{V_{REF}} - 1\right) \times R2 \tag{24}$$

8.2.1.2.8 Calculating Efficiency, and Junction Temperature

The complete LM2734Z DC–DC converter efficiency can be calculated in the following manner:

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{25}$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \tag{26}$$

Calculations for determining the most significant power losses are shown below. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter, switching and conduction. Conduction losses usually dominate at higher output loads, where as switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D).

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \tag{27}$$

V_{SW} is the voltage drop across the internal NFET when it is on, and is equal to Equation 28.

$$V_{SW} = I_{OUT} \times R_{DSON} \quad (28)$$

V_D is the forward voltage drop across the Schottky diode. It can be obtained from the Electrical Characteristics section. If the voltage drop across the inductor (V_{DCR}) is accounted for, use Equation 29 to calculate the duty cycle.

$$D = \frac{V_O + V_D + V_{DCR}}{V_{IN} + V_D - V_{SW}} \quad (29)$$

This usually gives only a minor duty cycle change, and has been omitted in the examples for simplicity.

The conduction losses in the free-wheeling Schottky diode are calculated using Equation 30.

$$P_{DIODE} = V_D \times I_{OUT}(1-D) \quad (30)$$

Often this is the single most significant power loss in the circuit. Take care choosing a Schottky diode that has a low forward voltage drop.

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to Equation 31.

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (31)$$

The LM2734Z conduction loss is mainly associated with the internal NFET, as shown in Equation 32.

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D \quad (32)$$

Switching losses are also associated with the internal NFET. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measure the rise and fall times (10% to 90%) of the switch at the switch node using Equation 33 through Equation 35.

$$P_{SWF} = 1/2\ (V_{IN} \times I_{OUT} \times freq \times T_{FALL}) \quad (33)$$

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times freq \times T_{RISE}) \quad (34)$$

$$P_{SW} = P_{SWF} + P_{SWR} \quad (35)$$

Table 2. Typical Rise and Fall Times vs Input Voltage

V_{IN}	T_{RISE}	T_{FALL}
5 V	8 ns	4 ns
10 V	9 ns	6 ns
15 V	10 ns	7 ns

Another loss is the power required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN} \quad (36)$$

I_Q is the quiescent operating current, and is typically around 1.5 mA. The other operating power that needs to be calculated is that required to drive the internal NFET:

$$P_{BOOST} = I_{BOOST} \times V_{BOOST} \quad (37)$$

V_{BOOST} is normally between 3 VDC and 5 VDC. The I_{BOOST} rms current is approximately 4.25 mA. Total power losses are:

$$\Sigma P_{COND} + P_{SW} + P_{DIODE} + P_{IND} + P_Q + P_{BOOST} = P_{LOSS} \quad (38)$$

8.2.1.2.9 Calculating the LM2734Z Junction Temperature

Thermal Definitions:

T_J = Chip junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from chip junction to device case

$R_{\theta JA}$ = Thermal resistance from chip junction to ambient air

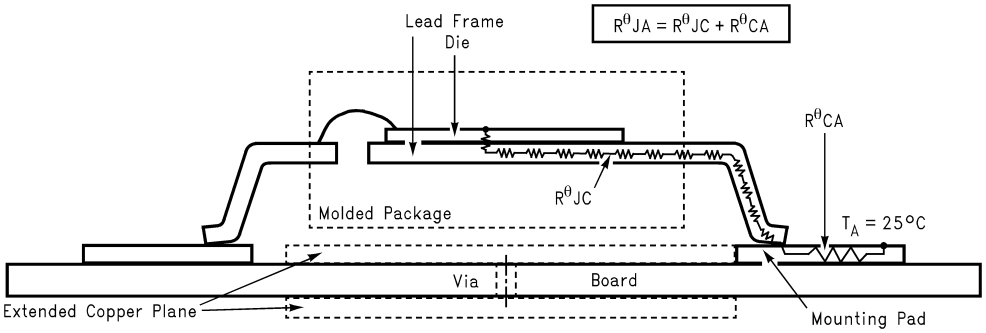


Figure 12. Cross-Sectional View of Integrated Circuit Mounted on a Printed Circuit Board

Heat in the LM2734Z due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs conductor).

Heat Transfer goes as:

silicon→package→lead frame→PCB.

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as shown in Equation 39.

$$R_{\theta} = \frac{\Delta T}{Power} \tag{39}$$

Thermal impedance from the silicon junction to the ambient air is defined as shown in Equation 40.

$$R_{\theta JA} = \frac{T_J - T_A}{Power} \tag{40}$$

This impedance can vary depending on the thermal properties of the PCB. This includes PCB size, weight of copper used to route traces and ground plane, and number of layers within the PCB. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Four to six thermal vias must be placed under the exposed pad to the ground plane if the WSON package is used. If the 6-pin SOT package is used, place two to four thermal vias close to the ground pin of the device.

The data sheet specifies two different $R_{\theta JA}$ numbers for the thin SOT–6 package. The two numbers show the difference in thermal impedance for a four-layer board with 2-oz. copper traces, versus a four-layer board with 1-oz. copper. $R_{\theta JA}$ equals 120°C/W for 2-oz. copper traces and GND plane, and 235°C/W for 1-oz. copper traces and GND plane.

The first method to accurately measure the silicon temperature for a given application, two methods can be used. The first method requires the user to know the thermal impedance of the silicon junction to case. ($R_{\theta JC}$) is approximately 80°C/W for the thin SOT-6 package. Knowing the internal dissipation from the efficiency calculation given previously, and the case temperature, which can be empirically measured on the bench:

$$R_{\theta JA} = \frac{T_J - T_C}{Power} \tag{41}$$

Therefore:

$$T_J = (R_{\theta JC} \times P_{LOSS}) + T_C \tag{42}$$

$$\Sigma P_{COND} + P_{SWF} + P_{SWR} + P_Q + P_{BOOST} = P_{INTERNAL}$$

$$P_{INTERNAL} = \mathbf{322\ mW}$$

$$T_J = (R_{\theta JC} \times \text{Power}) + T_C = 80^oC/W \times 322\ mW + T_C \quad (43)$$

The second method can give a very accurate silicon junction temperature. The first step is to determine $R_{\theta JA}$ of the application. The LM2734Z has overtemperature protection circuitry. When the silicon temperature reaches 165°C, the device stops switching. The protection circuitry has a hysteresis of 15°C. Once the silicon temperature has decreased to approximately 150°C, the device starts to switch again. Knowing this, the $R_{\theta JA}$ for any PCB can be characterized during the early stages of the design by raising the ambient temperature in the given application until the circuit enters thermal shutdown. If the SW-pin is monitored, it is obvious when the internal NFET stops switching indicating a junction temperature of 165°C. Knowing the internal power dissipation from the above methods, the junction temperature and the ambient temperature, $R_{\theta JA}$ can be determined using Equation 44.

$$R_{\theta JA} = \frac{165^oC - T_A}{P_{INTERNAL}} \quad (44)$$

Once this is determined, the maximum ambient temperature allowed for a desired junction temperature can be found using Equation 45.

$$\Sigma P_{COND} + P_{SWF} + P_{SWR} + P_Q + P_{BOOST} = P_{INTERNAL}$$

$$P_{INTERNAL} = \mathbf{322\ mW} \quad (45)$$

Using a standard Texas Instruments 6-pin SOT demonstration board to determine the $R_{\theta JA}$ of the board. The four layer PCB is constructed using FR4 with 1/2-oz copper traces. The copper ground plane is on the bottom layer. The ground plane is accessed by two vias. The board measures 2.5 cm × 3 cm. It was placed in an oven with no forced airflow.

The ambient temperature was raised to 94°C, and at that temperature, the device went into thermal shutdown.

$$R_{\theta JA} = \frac{165^oC - 94^oC}{322\ mW} = 220^oC/W \quad (46)$$

If the junction temperature was to be kept below 125°C, then the ambient temperature cannot go above 54.2°C.

$$T_J - (R_{\theta JA} \times P_{LOSS}) = T_A \quad (47)$$

The method described above to find the junction temperature in the thin 6-pin SOT package can also be used to calculate the junction temperature in the WSON package. The 6-pin WSON package has a $R_{\theta JC}$ = 20°C/W, and $R_{\theta JA}$ can vary depending on the application. $R_{\theta JA}$ can be calculated in the same manner as described in method 2 (see *LM2734Z Design Example 3*).

8.2.1.2.10 WSON Package

The LM2734Z is packaged in a thin, 6-pin SOT package and the 6-pin WSON. The WSON package has the same footprint as the thin, 6-pin SOT, but is thermally superior due to the exposed ground paddle on the bottom of the package.

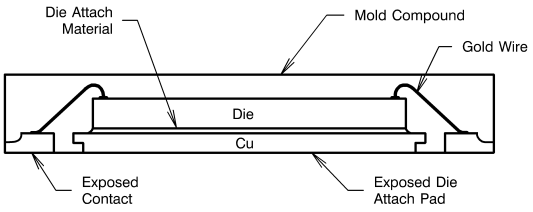


Figure 13. No Pullback WSON Configuration

$R_{\theta JA}$ of the WSON package is normally two to three times better than that of the thin, 6-pin SOT package for a similar PCB configuration (area, copper weight, thermal vias).

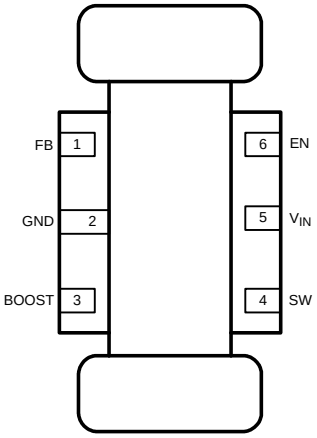


Figure 14. Dog Bone

For certain high power applications, the PCB land may be modified to a *dog bone* shape (see Figure 14). By increasing the size of ground plane, and adding thermal vias, the $R_{\theta JA}$ for the application can be reduced.

$$\Sigma P_{COND} + P_{SWF} + P_{SWR} + P_Q + P_{BOOST} = P_{INTERNAL}$$

$$P_{INTERNAL} = \mathbf{322\ mW} \tag{48}$$

This example follows *LM2734Z Design Example 2*, but uses the WSON package. Using a standard Texas Instruments 6-pin WSON demonstration board, use Method 2 to determine $R_{\theta JA}$ of the board. The four-layer PCB is constructed using FR4 with 1- or 2-oz copper traces. The copper ground plane is on the bottom layer. The ground plane is accessed by four vias. The board measures 2.5 cm × 3 cm. It was placed in an oven with no forced airflow.

The ambient temperature was raised to 113°C, and at that temperature, the device went into thermal shutdown.

$$R_{\theta JA}a = \frac{165^oC - 113^oC}{322\ mW} = 161^oC/W \tag{49}$$

If the junction temperature is to be kept below 125°C, then the ambient temperature cannot go above 73.2°C.

$$T_J - (R_{\theta JA} \times P_{LOSS}) = T_A \tag{50}$$

8.2.1.2.11 Package Selection

To determine which package you must use for your specific application, variables must be known before determining the appropriate package to use.

1. Maximum ambient system temperature
2. Internal LM2734Z power losses
3. Maximum junction temperature desired
4. $R_{\theta JA}$ of the specific application, or $R_{\theta JC}$ (WSON or 6-pin SOT)

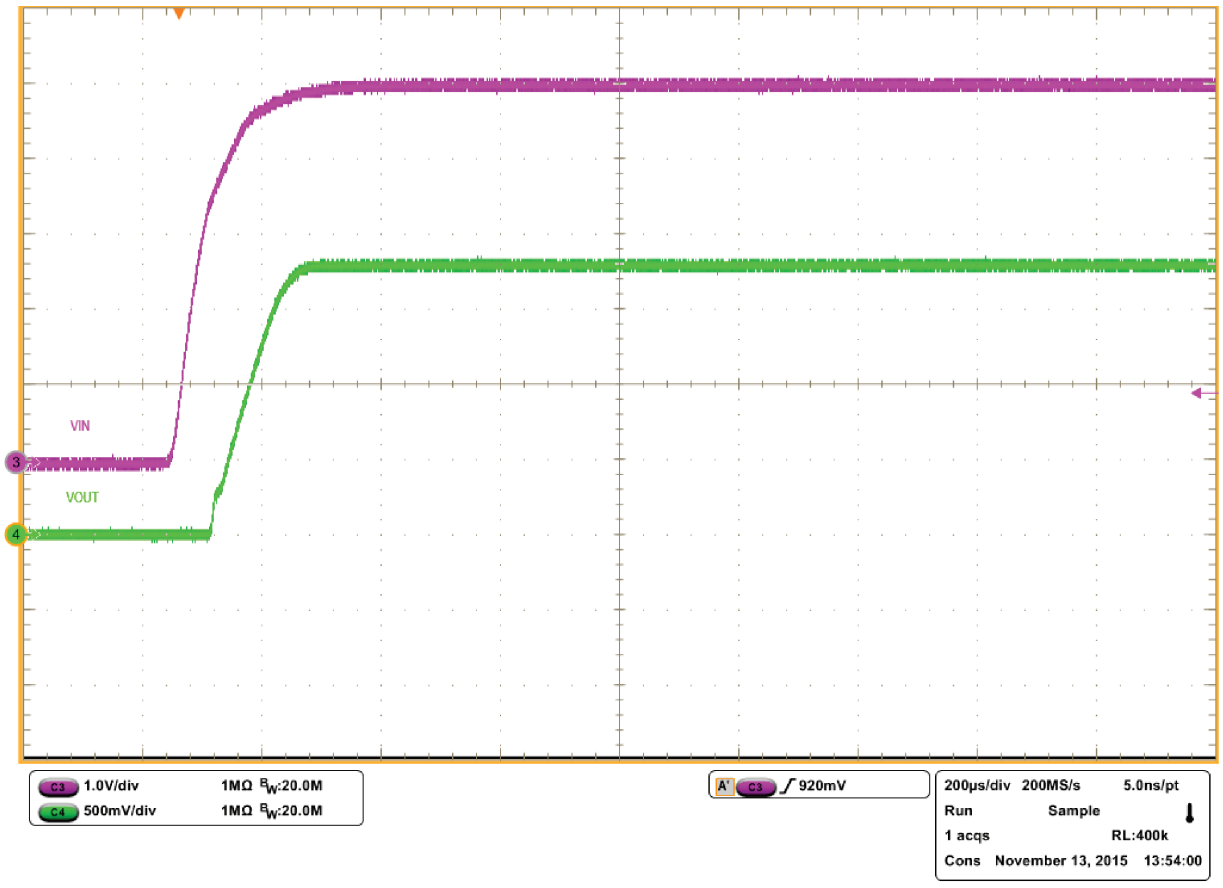
The junction temperature must be less than 125°C for the worst-case scenario.

Table 3 lists the bill of materials for LM2734Z design example 1.

Table 3. Bill of Materials for Figure 11

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A Buck Regulator	LM2734ZX	Texas Instruments
C1, Input Cap	10 µF, 6.3 V, X5R	C3216X5ROJ106M	TDK
C2, Output Cap	10 µF, 6.3 V, X5R	C3216X5ROJ106M	TDK
C3, Boost Cap	0.01 uF, 16 V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.3 V_F Schottky 1A, 10VR	MBRM110L	ON Semi
D2, Boost Diode	1 V_F at 50-mA Diode	1N4148W	Diodes, Inc.
L1	2.2 µH, 1.8 A	ME3220–222MX	Coilcraft
R1	8.87 kΩ, 1%	CRCW06038871F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.1.3 Application Curve



V_{IN}=5.0 V V_{OUT} = 1.5 V No load

Figure 15. Typical Start-Up Profile

8.2.2 LM2734Z Design Example 2

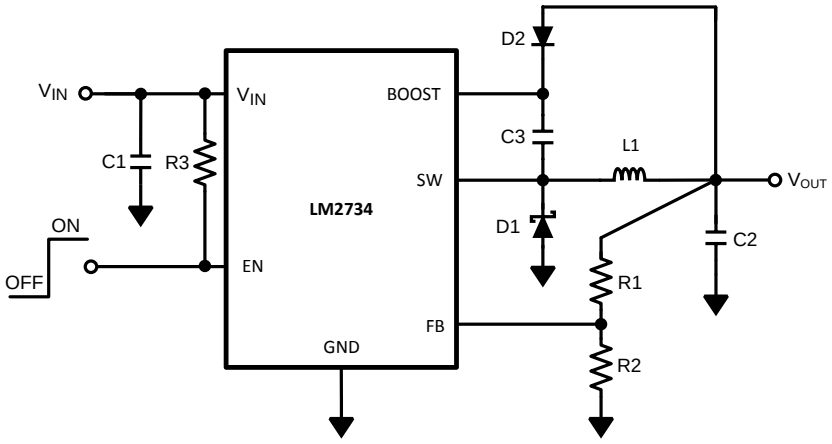


Figure 16. V_{BOOST} Derived from V_{OUT} 12 V to 3.3 V / 1 A

8.2.2.1 Design Requirements

Table 4 lists the operating conditions for design example 2.

Table 4. Design Parameters

PARAMETER	VALUE		PARAMETER	VALUE
V_{IN}	5.0 V		P_{OUT}	2.5 W
V_{OUT}	2.5 V		P_{DIODE}	151 mW
I_{OUT}	1.0 A		P_{IND}	75 mW
V_D	0.35 V		P_{SWF}	53 mW
Freq	3 MHz		P_{SWR}	53 mW
I_Q	1.5 mA		P_{COND}	187 mW
T_{RISE}	8 ns		P_Q	7.5 mW
T_{FALL}	8 ns		P_{BOOST}	21 mW
R_{DSON}	330 mΩ		P_{LOSS}	548 mW
IND_{DCR}	75 mΩ			
D	56.8%			

8.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*. Table 5 lists the bill of materials for LM2734Z design example 2.

Table 5. Bill of Materials for Figure 16

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A Buck Regulator	LM2734ZX	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22 µF, 6.3 V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01 µF, 16 V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.34 V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	0.6 V_F at 30-mA Diode	BAT17	Vishay
L1	3.3 µH, 1.3 A	ME3220–332MX	Coilcraft
R1	31.6 kΩ, 1%	CRCW06033162F	Vishay
R2	10.0 kΩ, 1%	CRCW06031002F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.3 LM2734Z Design Example 3

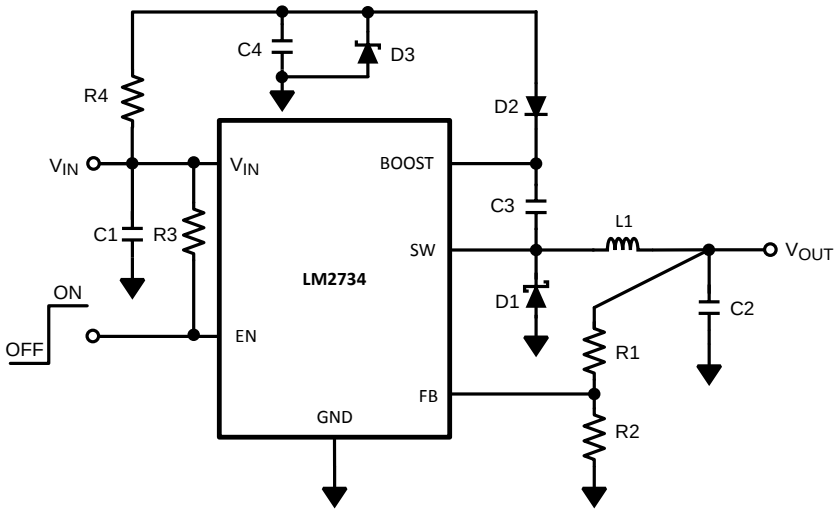


Figure 17. V_{BOOST} Derived from V_{SHUNT} 18 V to 1.5 V / 1 A

8.2.3.1 Design Requirements

Table 6 lists the operating conditions for design example 3.

Table 6. Design Parameters

PARAMETER	VALUE		PARAMETER	VALUE
Package	SOT-6		P_{OUT}	2.475 W
V_{IN}	12.0 V		P_{DIODE}	523 mW
V_{OUT}	3.30 V		P_{IND}	56.25 mW
I_{OUT}	750 mA		P_{SWF}	108 mW
V_D	0.35 V		P_{SWR}	108 mW
Freq	3 MHz		P_{COND}	68.2 mW
I_Q	1.5 mA		P_Q	18 mW
I_{BOOST}	4 mA		P_{BOOST}	20 mW
V_{BOOST}	5 V		P_{LOSS}	902 mW
T_{RISE}	8 ns			
T_{FALL}	8 ns			
R_{DSON}	400 mΩ			
IND_{DCR}	75 mΩ			
D	30.3%			

8.2.3.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

Table 7 lists the bill of materials for LM2734Z design example 3.

Table 7. Bill of Materials for Figure 17

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A Buck Regulator	LM2734ZX	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22 µF, 6.3 V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01 µF, 16 V, X7R	C1005X7R1C103K	TDK
C4, Shunt Cap	0.1 µF, 6.3 V, X5R	C1005X5R0J104K	TDK
D1, Catch Diode	0.4 V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	1 V_F at 50-mA Diode	1N4148W	Diodes, Inc.
D3, Zener Diode	5.1 V 250-Mw SOT	BZX84C5V1	Vishay
L1	3.3 µH, 1.3 A	ME3220–332MX	Coilcraft
R1	8.87 kΩ, 1%	CRCW06038871F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay
R4	4.12 kΩ, 1%	CRCW06034121F	Vishay

8.2.4 LM2734Z Design Example 4

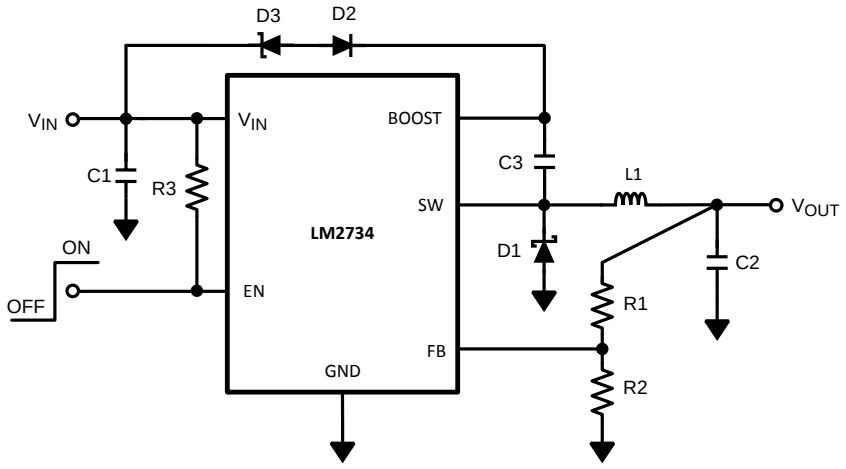


Figure 18. V_{BOOST} Derived from Series Zener Diode (V_{IN}) 15 V to 1.5 V / 1 A

8.2.4.1 Design Requirements

Table 8 lists the operating conditions for design example 4.

Table 8. Design Parameters

PARAMETER	VALUE		PARAMETER	VALUE
Package	WSON-6		P_{OUT}	2.475 W
V_{IN}	12.0 V		P_{DIODE}	523 mW
V_{OUT}	3.3 V		P_{IND}	56.25 mW
I_{OUT}	750 mA		P_{SWF}	108 mW
V_D	0.35 V		P_{SWR}	108 mW
Freq	3 MHz		P_{COND}	68.2 mW
I_Q	1.5 mA		P_Q	18 mW
I_{BOOST}	4 mA		P_{BOOST}	20 mW
V_{BOOST}	5 V		P_{LOSS}	902 mW
T_{RISE}	8 ns			
T_{FALL}	8 ns			
R_{DSON}	400 mΩ			
IND_{DCR}	75 mΩ			
D	30.3%			

8.2.4.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

Table 9 lists the bill of materials for LM2734Z design example 4.

Table 9. Bill of Materials for Figure 18

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A Buck Regulator	LM2734ZX	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22 µF, 6.3 V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.01 µF, 16 V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.4 V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	1 V_F at 50-mA Diode	1N4148W	Diodes, Inc.
D3, Zener Diode	11 V 350-Mw SOT	BZX84C11T	Diodes, Inc.
L1	3.3 µH, 1.3 A	ME3220–332MX	Coilcraft
R1	8.87 kΩ, 1%	CRCW06038871F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.5 LM2734Z Design Example 5

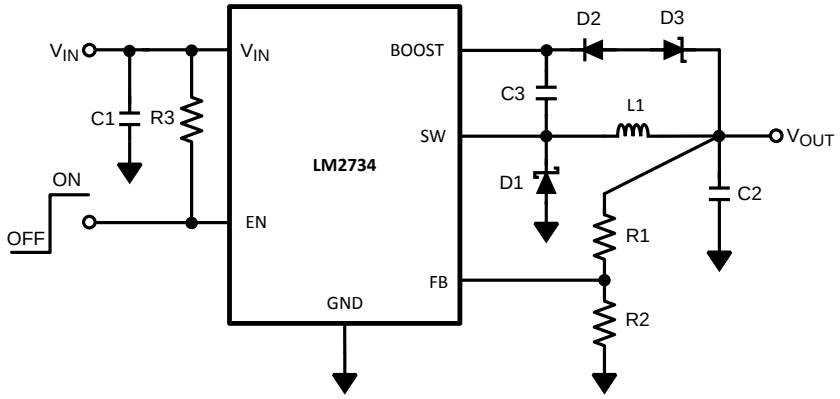


Figure 19. V_{BOOST} Derived from Series Zener Diode (V_{OUT}) 15 V to 9 V / 1 A

8.2.5.1 Design Requirements

Table 10 lists the operating conditions for design example 5.

Table 10. Design Parameters

PARAMETER	VALUE		PARAMETER	VALUE
Package	WSON-6			
V_{IN}	15.0 V		P_{OUT}	9 W
V_{OUT}	9.0 V		P_{DIODE}	130 mW
I_{OUT}	1.0 A		P_{IND}	104 mW
V_D	0.35 V		P_{COND}	186 mW
Freq	3 MHz		P_{SW}	382.5 mW
I_Q	1.5 mA		P_Q	22.5 mW
T_{RISE}	10 ns		P_{LOSS}	825 mW
T_{FALL}	7 ns			
R_{DSON}	300 mΩ			
IND_{DCR}	104 mΩ			
D	62%			

8.2.5.2 Detailed Design Procedure

Refer to *Detailed Design Procedure*.

Table 11 lists the bill of materials for the LM2734Z design example 5.

Table 11. Bill of Materials for Figure 19

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1-A Buck Regulator	LM2734ZX	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22 µF, 16 V, X5R	C3216X5R1C226M	TDK
C3, Boost Cap	0.01 µF, 16 V, X7R	C1005X7R1C103K	TDK
D1, Catch Diode	0.4 V_F Schottky 1A, 30VR	SS1P3L	Vishay
D2, Boost Diode	1 V_F at 50-mA Diode	1N4148W	Diodes, Inc.
D3, Zener Diode	4.3 V 350-mw SOT	BZX84C4V3	Diodes, Inc.
L1	2.2 µH, 1.8 A	ME3220–222MX	Coilcraft
R1	102 kΩ, 1%	CRCW06031023F	Vishay

Table 11. Bill of Materials for Figure 19 (continued)

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

9 Power Supply Recommendations

The LM2734Z is designed to operate from an input voltage supply range between 3 to 20 V. This input supply must be able to withstand the maximum input current and maintain voltage above 3.0 V. In case where input supply is located farther away (more than a few inches) from LM2734Z additional bulk capacitance may be required in addition to ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration when completing the layout is the close coupling of the GND connections of the C_{IN} capacitor and the catch diode D1. These ground ends must be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the IC as possible. Next in importance is the location of the GND connection of the C_{OUT} capacitor, which must be near the GND connections of C_{IN} and D1.

There must be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island.

The FB pin is a high impedance node and care must be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors must be placed as close as possible to the IC, with the GND of R2 placed as close as possible to the GND of the IC. The V_{OUT} trace to R1 must be routed away from the inductor and any other traces that are switching.

High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they must be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor.

The remaining components must also be placed as close as possible to the IC. Please see the *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines* Application Note (SNVA054) for further considerations and the LM2734Z demo board as an example of a four-layer layout.

10.2 Layout Examples

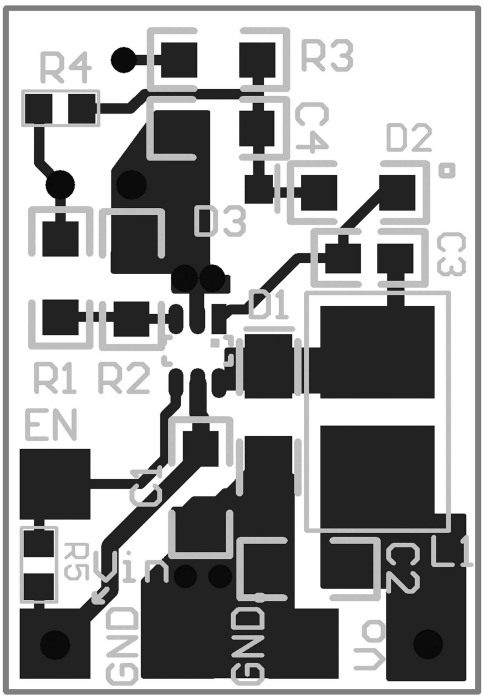


Figure 20. Top Layer

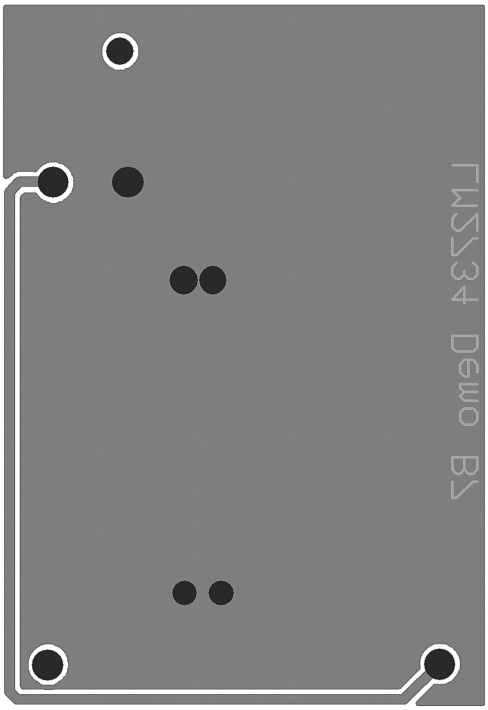


Figure 21. Bottom Layer

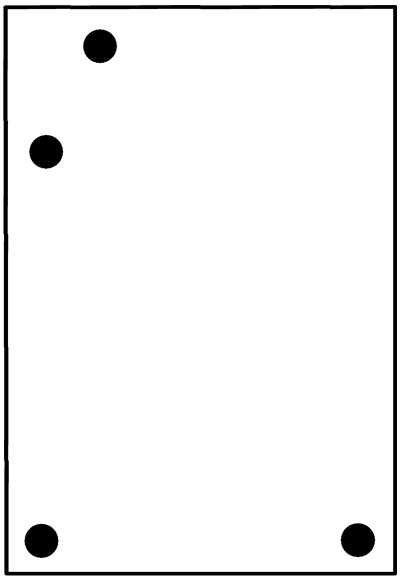


Figure 22. Internal Plane 1 (GND)

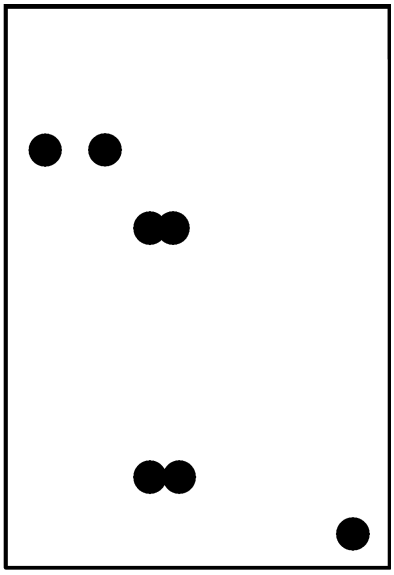


Figure 23. Internal Plane 2 (VIN)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines* Application Note (SNVA054)
- *AN-1350 LM2734 Evaluation Board* User's Guide (SNVA100)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2734ZMK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SFTB	Samples
LM2734ZMKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SFTB	Samples
LM2734ZQMKE/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SVBB	Samples
LM2734ZQSDE/NOPB	ACTIVE	WSON	NGG	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L238B	Samples
LM2734ZSD/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L163B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM2734Z, LM2734Z-Q1 :

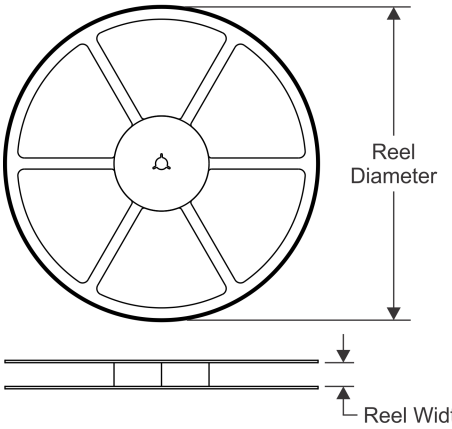
- Catalog: LM2734Z
- Automotive: LM2734Z-Q1

NOTE: Qualified Version Definitions:

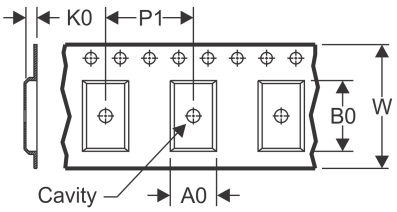
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

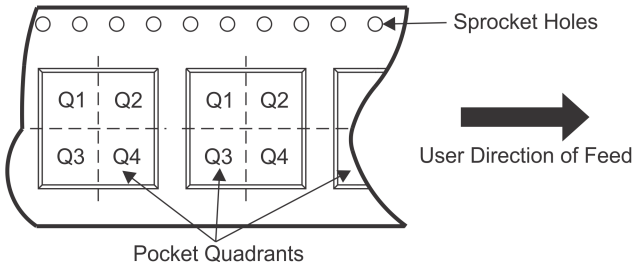


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

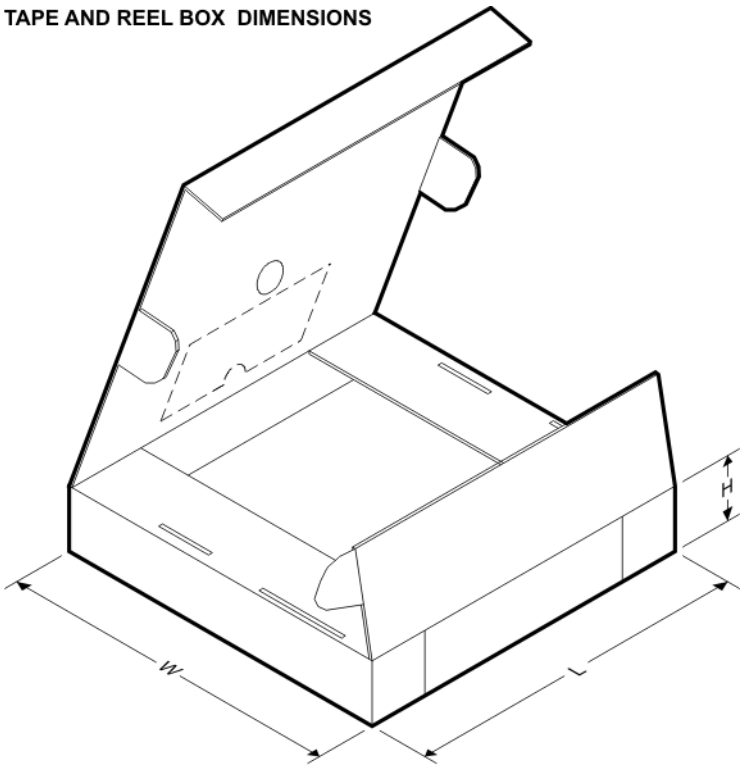
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2734ZMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2734ZMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2734ZQMKE/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2734ZQSDE/NOPB	WSON	NGG	6	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM2734ZSD/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

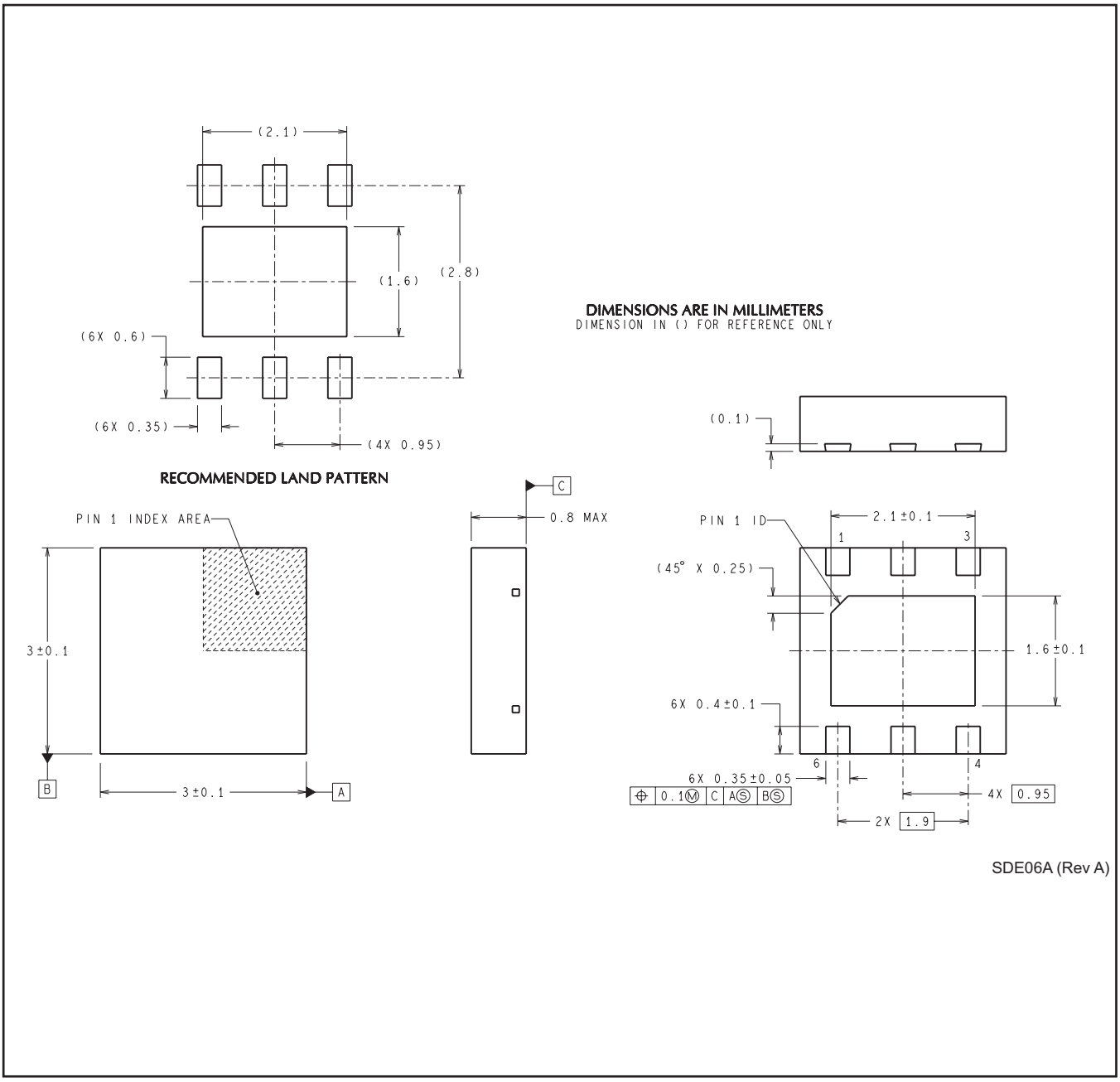
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

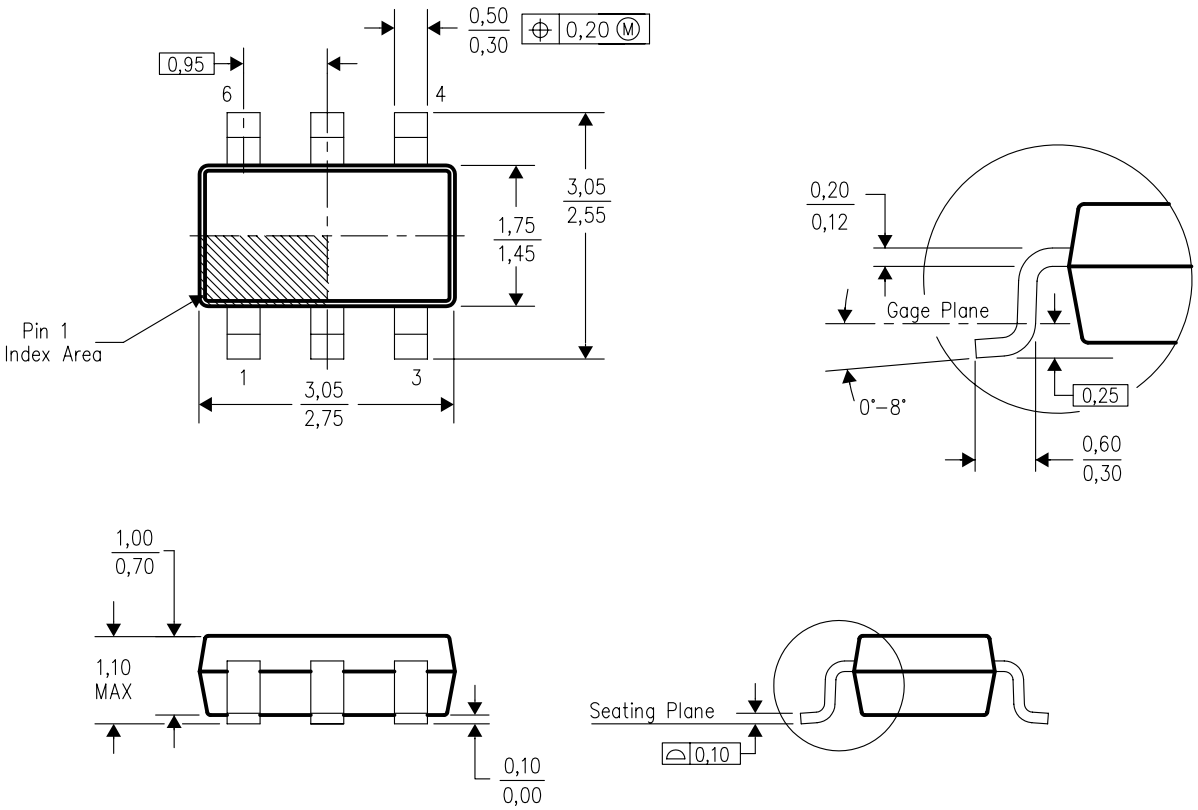
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2734ZMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LM2734ZMKX/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LM2734ZQMKE/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LM2734ZQSDE/NOPB	WSON	NGG	6	250	210.0	185.0	35.0
LM2734ZSD/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0

NGG0006A



SDE06A (Rev A)

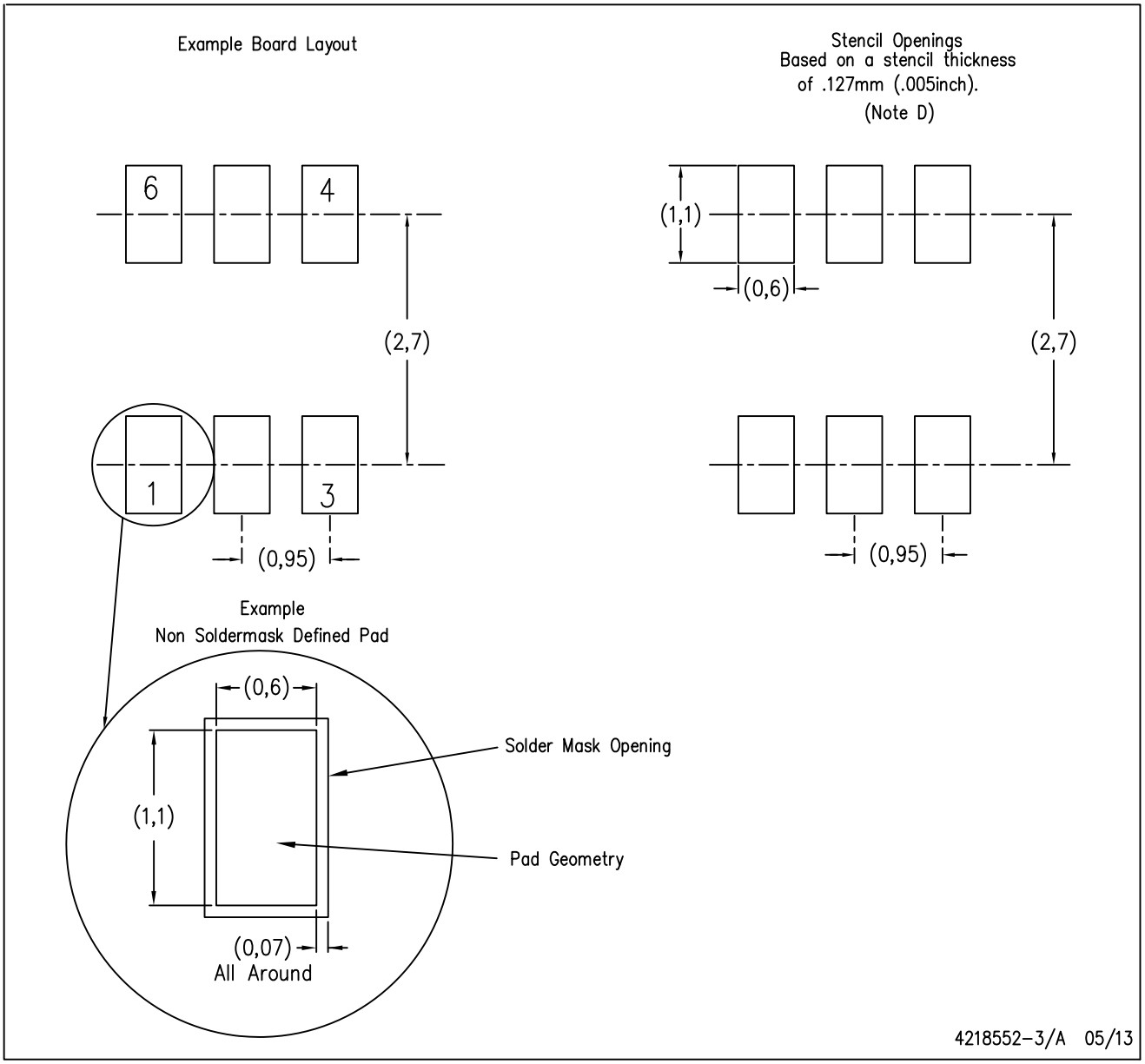
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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