



**THE DATASHEET OF  
AD9002AD**



### FEATURES

**150 MSPS ENCODE Rate**  
**Low Input Capacitance: 17 pF**  
**Low Power: 750 mW**  
**-5.2 V Single Supply**  
**MIL-STD-883 Compliant Versions Available**

### APPLICATIONS

**Radar Systems**  
**Digital Oscilloscopes/ATE Equipment**  
**Laser/Radar Warning Receivers**  
**Digital Radio**  
**Electronic Warfare (ECM, ECCM, ESM)**  
**Communication/Signal Intelligence**

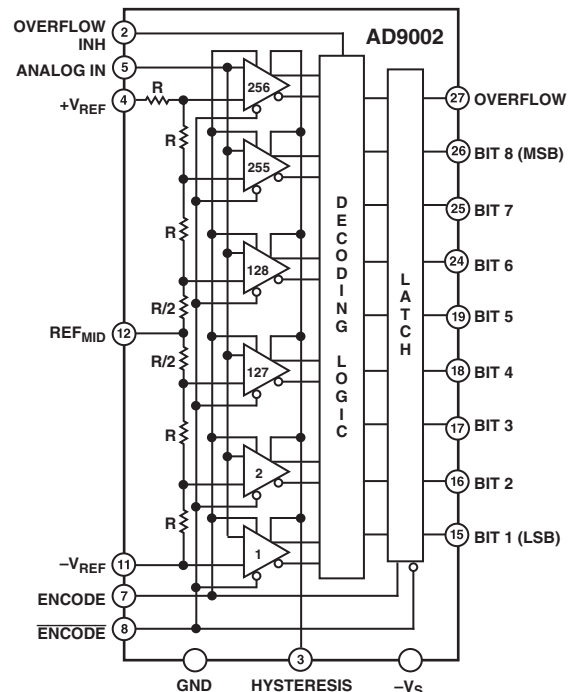
### GENERAL DESCRIPTION

The AD9002 is an 8-bit, high speed, analog-to-digital converter. The AD9002 is fabricated in an advanced bipolar process that allows operation at sampling rates in excess of 150 MSPS. Functionally, the AD9002 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the ECL compatible output latches.

An exceptionally wide, large signal, analog input bandwidth of 160 MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9002 allows very accurate acquisition of high speed pulse inputs without an external track-and-hold. The comparator output decoding scheme minimizes false codes, which is critical to high speed linearity.

The AD9002 provides an external hysteresis control pin that can be used to optimize comparator sensitivity to further improve performance. Additionally, the AD9002's low power dissipation of 750 mW makes it usable over the full extended temperature range. The AD9002 also incorporates an overflow bit to indicate overrange inputs. This overflow output can be disabled with the overflow inhibit pin.

### FUNCTIONAL BLOCK DIAGRAM



The AD9002 is available in two grades, one with 0.5 LSB linearity and one with 0.75 LSB linearity. Both versions are offered in an industrial grade,  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , packaged in a 28-lead DIP and a 28-lead JLC. The military temperature range devices,  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , are available in a ceramic DIP package and complies with MIL-STD-883 Class B.

REV. G

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# AD9002—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (−V<sub>S</sub> = −5.2 V, Differential Reference Voltage = 2.0 V, unless otherwise noted.)

Parameter	Temp	AD9002AD/AJ			AD9002BD/BJ			AD9002SD			AD9002TD			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION		8			8			8			8			Bits
DC ACCURACY														
Differential Linearity	25°C		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full			1.0			0.75			1.0			0.75	LSB
Integral Linearity	25°C		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full	Guaranteed			Guaranteed			Guaranteed			Guaranteed			
INITIAL OFFSET ERROR														
Top of Reference Ladder	25°C		8	14		8	14		8	14		8	14	mV
	Full			17			17			17			17	mV
Bottom of Reference Ladder	25°C		4	10		4	10		4	10		4	10	mV
	Full			12			12			12			12	mV
Offset Drift Coefficient	Full		20			20			20			20		μV/°C
ANALOG INPUT														
Input Bias Current <sup>1</sup>	25°C		60	200		60	200		60	200		60	200	μA
	Full			200			200			200			200	μA
Input Resistance	25°C	25	200		25	200		25	200		25	200		kΩ
Input Capacitance	25°C		17	22		17	22		17	22		17	22	pF
Large Signal Bandwidth <sup>2</sup>	25°C		160			160			160			160		MHz
Input Slew Rate <sup>3</sup>	25°C		440			440			440			440		V/μs
REFERENCE INPUT														
Reference Ladder Resistance	25°C	40	80	110	40	80	110	40	80	110	40	80	110	Ω
Ladder Temperature Coefficient			0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	25°C		10			10			10			10		MHz
DYNAMIC PERFORMANCE														
Conversion Rate	25°C	125	150		125	150		125	150		125	150		MSPS
Aperture Delay	25°C		1.3			1.3			1.3			1.3		ns
Aperture Uncertainty (Jitter)	25°C		15			15			15			15		ps
Output Delay (t <sub>PD</sub> ) <sup>4,5</sup>	25°C	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	ns
Transient Response <sup>6</sup>	25°C		6			6			6			6		ns
Overvoltage Recovery Time <sup>7</sup>	25°C		6			6			6			6		ns
Output Rise Time <sup>4</sup>	25°C			3.0			3.0			3.0			3.0	ns
Output Fall Time <sup>4</sup>	25°C			2.5			2.5			2.5			2.5	ns
Output Time Skew <sup>4,8</sup>	25°C		0.6			0.6			0.6			0.6		ns
ENCODE INPUT														
Logic “1” Voltage <sup>4</sup>	Full	−1.1			−1.1			−1.1			−1.1			V
Logic “0” Voltage <sup>4</sup>	Full		−1.5			−1.5			−1.5			−1.5		V
Logic “1” Current	Full			150			150			150			150	μA
Logic “0” Current	Full			120			120			120			120	μA
Input Capacitance	25°C		3			3			3			3		pF
ENCODE Pulsewidth (Low) <sup>9</sup>	25°C	1.5			1.5			1.5			1.5			ns
ENCODE Pulsewidth (High) <sup>9</sup>	25°C	1.5			1.5			1.5			1.5			ns
OVERFLOW INHIBIT INPUT														
0 V Input Current	Full		144	300		144	300		144	300		144	300	μA
AC LINEARITY <sup>10</sup>														
Effective Bits <sup>11</sup>	25°C		7.6			7.6			7.6			7.6		Bits
In-Band Harmonics														
DC to 1.23 MHz	25°C	48	55		48	55		48	55		48	55		dB
DC to 9.3 MHz	25°C		50			50			50			50		dB
DC to 19.3 MHz	25°C		44			44			44			44		dB
Signal-to-Noise Ratio <sup>12</sup>	25°C	46	47.6		46	47.6		46	47.6		46	47.6		dB
Two Tone Intermod Rejection <sup>13</sup>	25°C		60			60			60			60		dB
DIGITAL OUTPUTS <sup>4</sup>														
Logic “1” Voltage	Full	−1.1			−1.1			−1.1			−1.1			V
Logic “0” Voltage	Full		−1.5			−1.5			−1.5			−1.5		V
POWER SUPPLY <sup>14</sup>														
Supply Current (−5.2 V)	25°C		145	175		145	175		145	175		145	175	mA
	Full			200			200			200			200	mA
Nominal Power Dissipation	25°C		750			750			750			750		mW
Reference Ladder Dissipation	25°C		50			50			50			50		mW
Power Supply Rejection Ratio <sup>15</sup>	25°C		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	mV/V

### NOTES

<sup>1</sup>Measured with AIN = 0 V.

<sup>2</sup>Measured by FFT analysis where fundamental is −3 dBc.

<sup>3</sup>Input slew rate derived from rise time (10% to 90%) of full-scale input.

<sup>4</sup>Outputs terminated through 100 Ω to −2 V.

<sup>5</sup>Measured from ENCODE in to data out for LSB only.

<sup>6</sup>For full-scale step input, 8-bit accuracy is attained in specified time.

<sup>7</sup>Recovers to 8-bit accuracy in specified time after 150% full-scale input overvoltage.

<sup>8</sup>Output time skew includes high-to-low and low-to-high transitions as well as

bit-to-bit time skew differences.

<sup>9</sup>ENCODE signal rise/fall times should be less than 10 ns for normal operation.

<sup>10</sup>Measured at 125 MSPS ENCODE rate.

<sup>11</sup>Analog input frequency = 1.23 MHz.

<sup>12</sup>RMS signal to rms noise, with 1.23 MHz analog input signal.

<sup>13</sup>Input signals 1 V p-p @ 1.23 MHz and 1 V p-p @ 2.30 MHz.

<sup>14</sup>Supplies should remain stable within ±5% for normal operation.

<sup>15</sup>Measured at −5.2 V ±5%.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Supply Voltage ( $-V_S$ )	−6 V
Analog-to-Digital Supply Voltage Differential	0.5 V
Analog Input Voltage	$-V_S$ to +0.5 V
Digital Input Voltage	$-V_S$ to 0 V
Reference Input Voltage ( $+V_{REF}$ , $-V_{REF}$ ) <sup>2</sup>	−3.5 V to +0.1 V
Differential Reference Voltage	2.1 V
Reference Midpoint Current	±4 mA
ENCODE to ENCODE Differential Voltage	4 V
Digital Output Current	20 mA
Operating Temperature Range	
AD9002AD/BD/AJ/BJ	−25°C to +85°C
AD9002SD/TD	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature <sup>3</sup>	150°C
Lead Soldering Temperature (10 sec)	300°C

## NOTES

<sup>1</sup>Absolute Maximum Ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

<sup>2</sup> $+V_{REF} \geq -V_{REF}$  under all circumstances.

<sup>3</sup>Maximum junction temperature ( $T_J$  max) should not exceed 175°C for ceramic packages, and 150°C for plastic packages:

$$T_J = PD (\theta_{JA}) + T_A$$

$$= PD (\theta_{JC}) + T_C$$

where

$PD$  = power dissipation

$\theta_{JA}$  = thermal impedance from junction to ambient (°C/W)

$\theta_{JC}$  = thermal impedance from junction to case (°C/W)

$T_A$  = ambient temperature (°C)

$T_C$  = case temperature (°C)

Typical thermal impedances are:

Ceramic DIP  $\theta_{JA} = 56^\circ\text{C/W}$ ;  $\theta_{JC} = 20^\circ\text{C/W}$

PLCC  $\theta_{JA} = 60^\circ\text{C/W}$ ;  $\theta_{JC} = 19^\circ\text{C/W}$

## Recommended Operating Conditions

Parameter	Input Voltage (V)		
	Min	Nominal	Max
$-V_S$	−5.46	−5.20	−4.94
$+V_{REF}$	$-V_{REF}$	0.0	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
Analog Input	$-V_{REF}$		$+V_{REF}$

## EXPLANATION OF TEST LEVELS

- Test Level I – 100% production tested.
- Test Level II – 100% production tested at 25°C and sample tested at specified temperatures.
- Test Level III – Sample tested only.
- Test Level IV – Parameter is guaranteed by design and characterization testing.
- Test Level V – Parameter is a typical value only.
- Test Level VI – All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

## ORDERING GUIDE

Model	Linearity	Temperature Range	Package Option*
AD9002AD	0.75 LSB	−25°C to +85°C	D-28
AD9002BD	0.50 LSB	−25°C to +85°C	D-28
AD9002AJ	0.75 LSB	−25°C to +85°C	J-28
AD9002BJ	0.50 LSB	−25°C to +85°C	J-28
AD9002SD/883B	0.75 LSB	−55°C to +125°C	D-28
AD9002TD/883B	0.50 LSB	−55°C to +125°C	D-28

\*D = Ceramic DIP; J = Ceramic Chip Carrier, J-Formed Leads.

## CAUTION

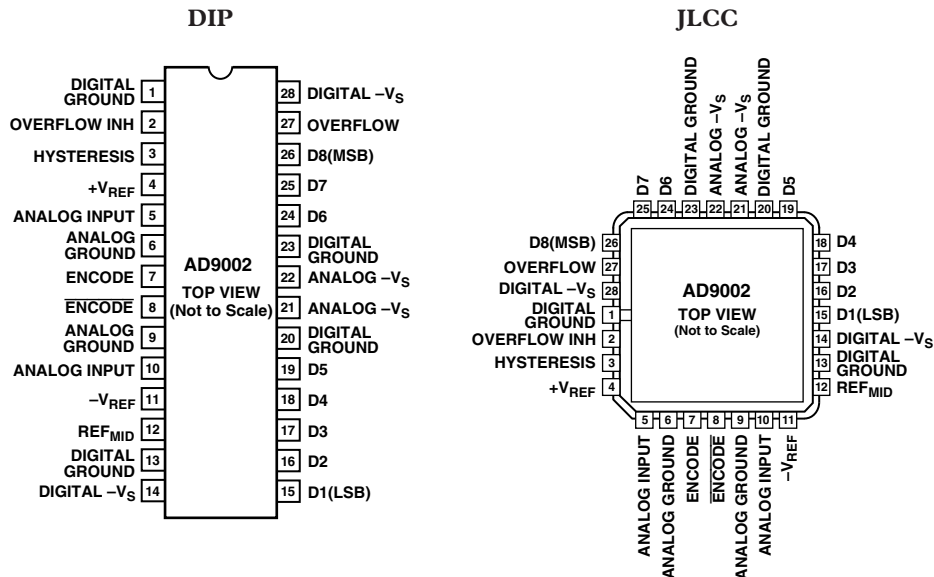
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9002 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## FUNCTIONAL DESCRIPTION

Pin No.	Mnemonic	Description									
1	DIGITAL GROUND	<p>One of Four Digital Ground Pins. All digital ground pins should be connected together.</p> <p>OVERFLOW INHIBIT controls the data output polarity for overvoltage inputs.</p> <table border="1"> <thead> <tr> <th>Analog Input</th> <th>Overflow Enabled (Floating or -5.2 V) of D1-D8</th> <th>Overflow Inhibited (GND) of D1-D8</th> </tr> </thead> <tbody> <tr> <td><math>V_{IN} &gt; +V_{REF}</math></td> <td>1 0 0 0 0 0 0 0</td> <td>0 1 1 1 1 1 1 1</td> </tr> <tr> <td><math>V_{IN} \leq +V_{REF}</math></td> <td>0 X X X X X X X</td> <td>0 X X X X X X X</td> </tr> </tbody> </table>	Analog Input	Overflow Enabled (Floating or -5.2 V) of D1-D8	Overflow Inhibited (GND) of D1-D8	$V_{IN} > +V_{REF}$	1 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1	$V_{IN} \leq +V_{REF}$	0 X X X X X X X	0 X X X X X X X
Analog Input	Overflow Enabled (Floating or -5.2 V) of D1-D8		Overflow Inhibited (GND) of D1-D8								
$V_{IN} > +V_{REF}$	1 0 0 0 0 0 0 0		0 1 1 1 1 1 1 1								
$V_{IN} \leq +V_{REF}$	0 X X X X X X X	0 X X X X X X X									
2	OVERFLOW INH										
3	HYSTERESIS	The hysteresis control voltage varies the comparator hysteresis from 0 mV to 10 mV, for a change from -5.2 V to -2.2 V at the hysteresis control pin. Normally converted to -5.2 V.									
4	+V <sub>REF</sub>	The Most Positive Reference Voltage for the Internal Resistor Ladder									
5	ANALOG INPUT	One of Two Analog Input Pins. Both analog input pins should be connected together.									
6	ANALOG GROUND	One of Two Analog Ground Pins. Both analog ground pins should be connected together.									
7	ENCODE	Noninverted Input of the Differential ENCODE Input. This pin is driven in conjunction with ENCODE.									
8	ENCODE	Inverted Input of the Differential ENCODE Input. This pin is driven in conjunction with ENCODE.									
9	ANALOG GROUND	One of Two Analog Ground Pins. Both analog ground pins should be connected together.									
10	ANALOG INPUT	One of Two Analog Input Pins. Both analog inputs should be connected together.									
11	-V <sub>REF</sub>	The Most Negative Reference Voltage for the Internal Resistor Ladder									
12	REF <sub>MID</sub>	The Midpoint Tap on the Internal Resistor Ladder									
13	DIGITAL GROUND	One of Four Digital Ground Pins. All digital ground pins should be connected together.									
14	DIGITAL -V <sub>S</sub>	One of Two Negative Digital Supply Pins (Nominally -5.2 V). Both digital supply pins should be connected together.									
15	D1 (LSB)	Digital Data Output									
16-19	D2-D5	Digital Data Output									
20	DIGITAL GROUND	One of Four Digital Ground Pins. All digital ground pins should be connected together.									
21, 22	ANALOG -V <sub>S</sub>	One of Two Negative Analog Supply Pins (Nominally -5.2 V). Both analog supply pins should be connected together.									
23	DIGITAL GROUND	One of Four Digital Ground Pins. All digital ground pins should be connected together.									
24, 25	D6, D7	Digital Data Output									
26	D8 (MSB)	Digital Data Output									
27	OVERFLOW	Overflow Data Output. Logic high indicates an input overvoltage ( $V_{IN} > +V_{REF}$ ) if OVERFLOW INH is enabled (overflow enabled, -5.2 V). See OVERFLOW INH.									
28	DIGITAL -V <sub>S</sub>	One of Two Negative Digital Supply Pins (Nominally -5.2 V). Both digital supply pins should be connected together.									

## PIN DESIGNATIONS



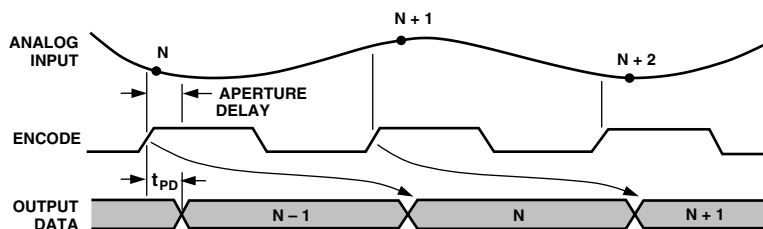


Figure 1. Timing Diagram

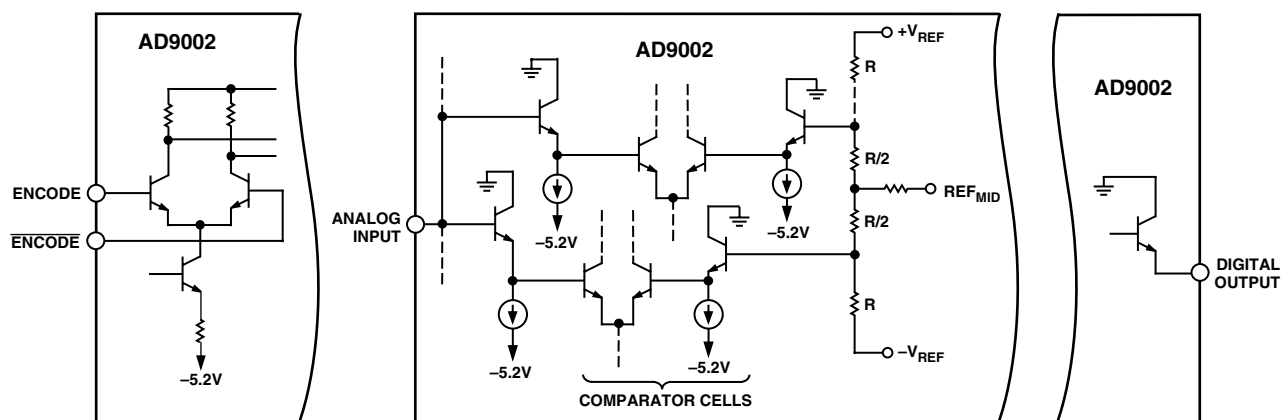


Figure 2. Input/Output Circuits

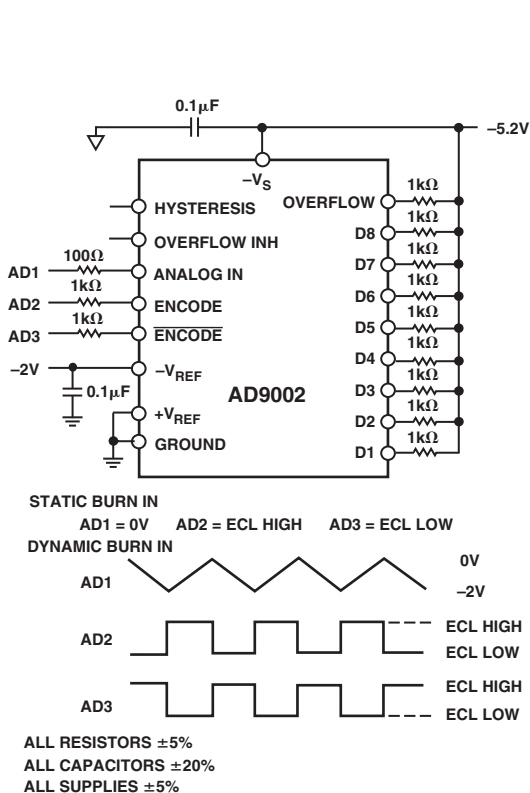


Figure 3. Burn-In Diagram

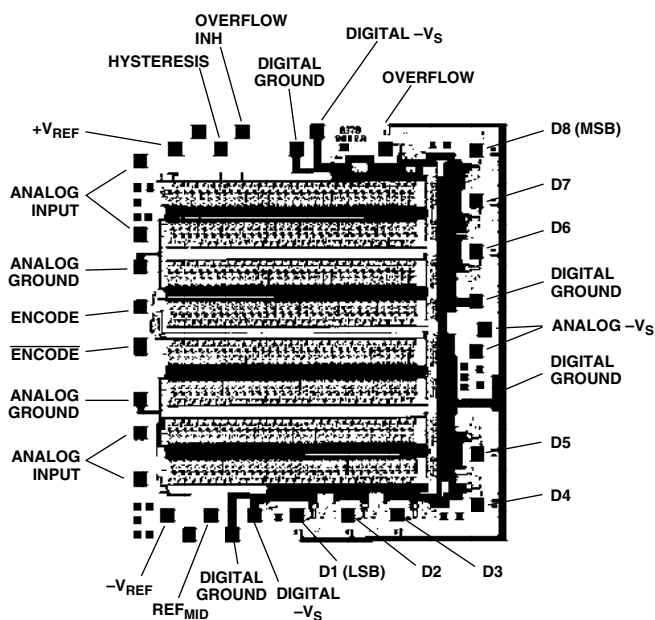


Figure 4. Die Layout and Mechanical Information

Die Dimensions	106 mils $\times$ 114 mils $\times$ 15 mils ( $\pm 2$ mils)
Pad Dimensions	4 mils $\times$ 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic (Ceramic)
	Epoxy (Plastic)
Bond Wire	1 mil–1.3 mil Gold; Gold Ball Bonding



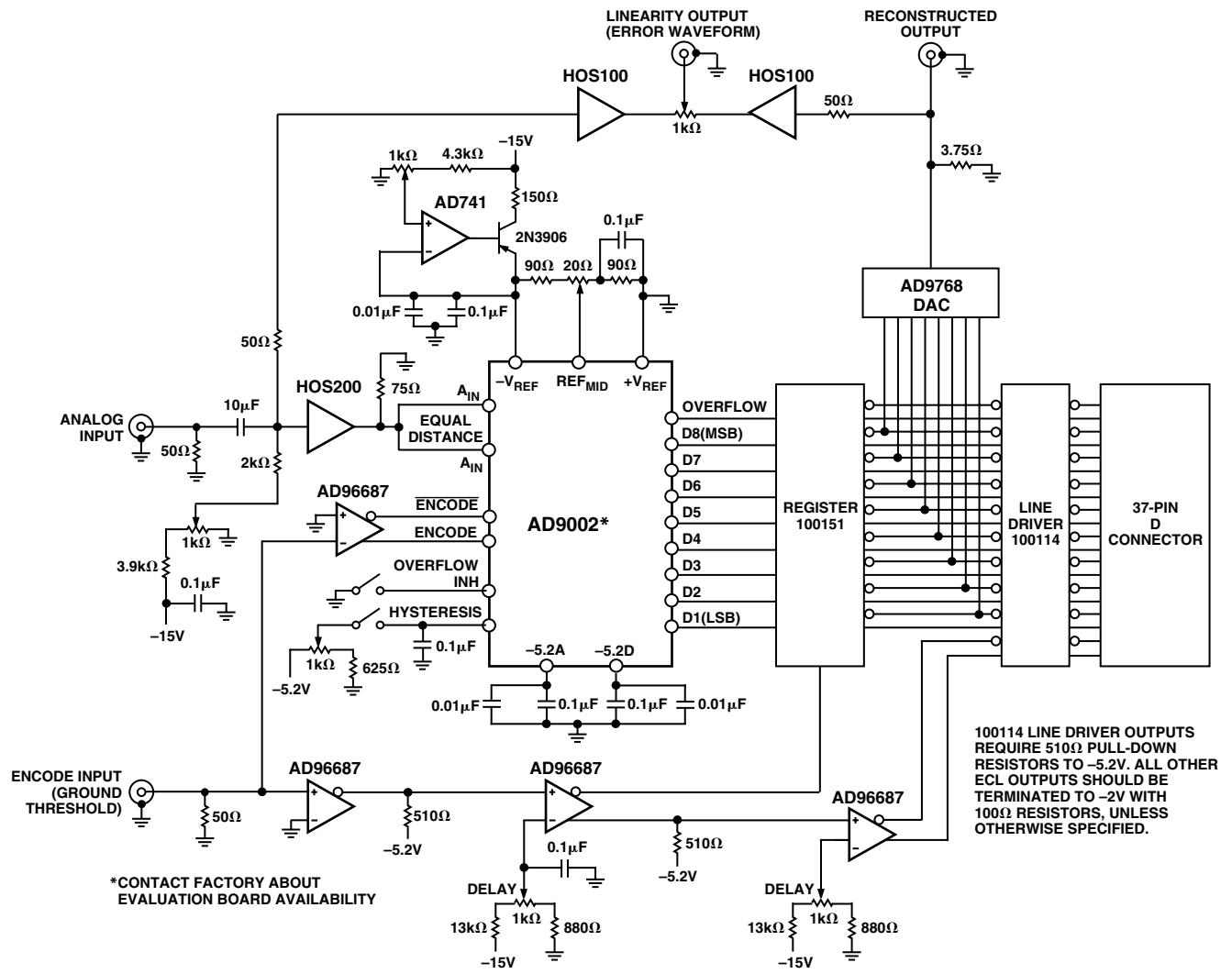


Figure 6. AD9002 Evaluation Circuit

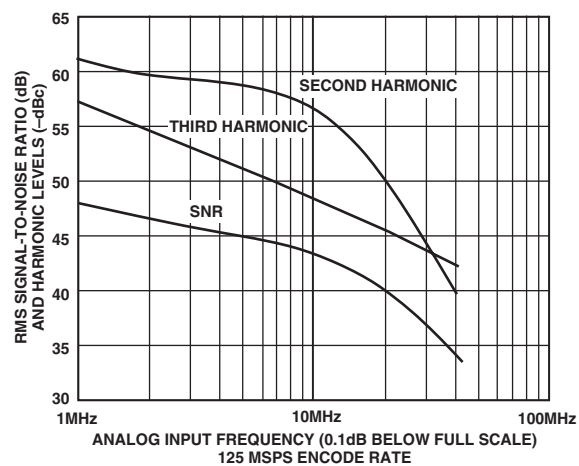
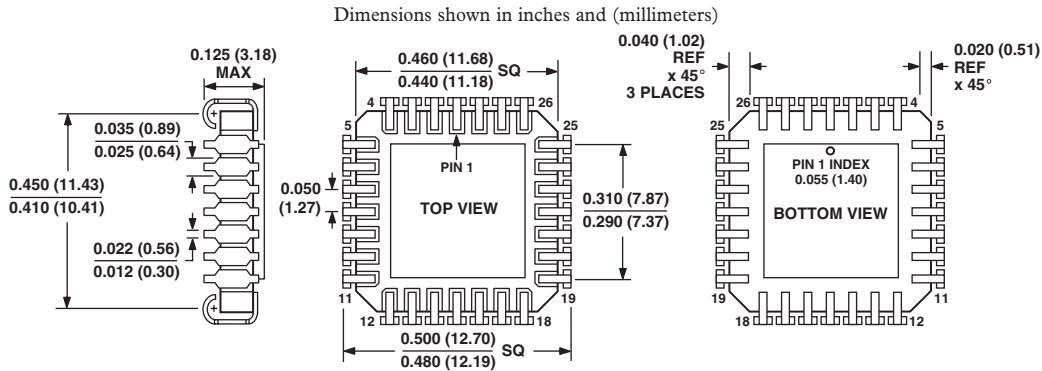


Figure 7. Dynamic Performance

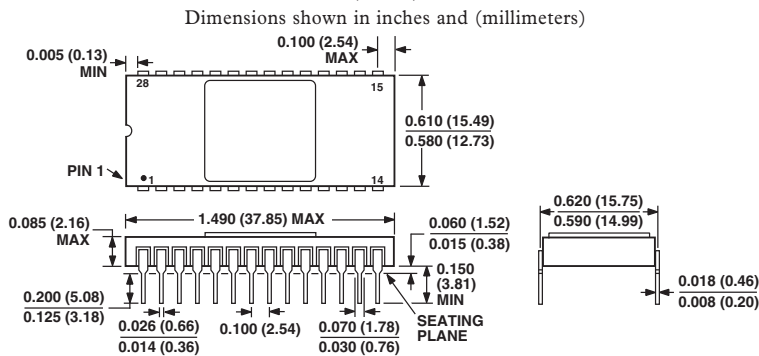
OUTLINE DIMENSIONS

28-Lead Ceramic Chip Carrier - J-Formed Leads [JLCC]  
(J-28A)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]  
(D-28)





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Revision History

Location	Page
5/03—Data Sheet changed from REV. F to REV. G.	
Deleted the E-28A	Universal
Changes to OUTLINE DIMENSIONS	8
Data Sheet changed from REV. E to REV. F.	
Edit to ABSOLUTE MAXIMUM RATINGS	3

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