THE DATASHEET OF

AD652KPZ

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Monolithic Synchronous Voltage-to-Frequency Converter

AD652

FEATURES

Full-scale frequency (up to 2 MHz) set by external system clock
Extremely low linearity error (0.005% max at 1 MHz FS, 0.02% max at 2 MHz FS)
No critical external components required
Accurate 5 V reference voltage
Low drift (25 ppm/°C max)
Dual- or single-supply operation
Voltage or current input
MIL-STD-883 compliant versions available

PRODUCT DESCRIPTION

The AD652 synchronous voltage-to-frequency converter (SVFC) is a powerful building block for precision analog-to-digital conversion, offering typical nonlinearity of 0.002% (0.005% maximum) at a 100 kHz output frequency. The inherent monotonicity of the transfer function and wide range of clock frequencies allow the conversion time and resolution to be optimized for specific applications.

The AD652 uses a variation of the charge-balancing technique to perform the conversion function. The AD652 uses an external clock to define the full-scale output frequency, rather than relying on the stability of an external capacitor. The result is a more stable, more linear transfer function, with significant application benefits in both single- and multichannel systems.

Gain drift is minimized using a precision low drift reference and low TC, on-chip, thin-film scaling resistors. Furthermore, initial gain error is reduced to less than 0.5% by the use of laser-wafer-trimming.

The analog and digital sections of the AD652 have been designed to allow operation from a single-ended power source, simplifying its use with isolated power supplies.

The AD652 is available in five performance grades. The 20-lead PLCC-packaged JP and KP grades are specified for operation over the 0°C to +70°C commercial temperature range. The 16-lead CERDIP-packaged AQ and BQ grades are specified for operation over the −40°C to +85°C industrial temperature range. The AD652SQ is available for operation over the full −55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. The use of an external clock to set the full-scale frequency allows the AD652 to achieve linearity and stability far superior to other monolithic VFCs. By using the same clock to drive the AD652 and set the counting period (through a suitable divider), conversion accuracy is maintained independent of variations in clock frequency.
2. The AD652 synchronous VFC requires only one external component (a noncritical integrator capacitor) for operation.
3. The AD652 includes a buffered, accurate 5 V reference.
4. The AD652's clock input is TTL and CMOS compatible and can also be driven by sources referred to the negative power supply. The flexible open-collector output stage provides sufficient current sinking capability for TTL and CMOS logic, as well as for optical couplers and pulse transformers. A capacitor-programmable one-shot is provided for selection of optimum output pulse width for power reduction.
5. The AD652 can also be configured for use as a synchronous F/V converter for isolated analog signal transmission.
6. The AD652 is available in versions compliant with MILSTD-883. Refer to the Analog Devices Military Products Databook or current AD652/883B data sheet for detailed specifications.

FUNCTIONAL BLOCK DIAGRAM

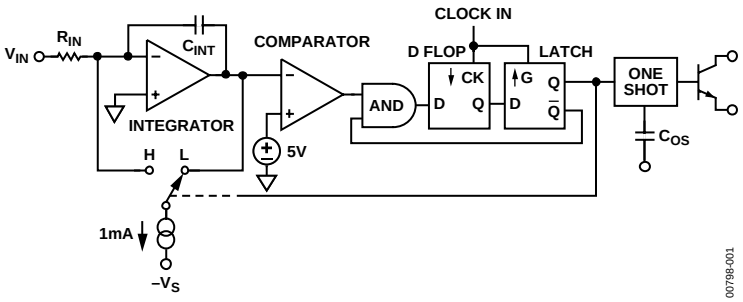

Figure 1.

Rev. C

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REVISION HISTORY

5/04—Data Sheet Changed from Rev. B to Rev. C

Updated Format ... Universal
Changes to Gain and Offset Calibration section ... 11
Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 26

2/00—Data Sheet Changed from Rev. A to Rev. B

SPECIFICATIONS

Typical @ T_A = 25°C, V_S = ±15 V, unless otherwise noted. Specifications in **boldface** are **100%** tested at final test and are used to measure outgoing quality levels.

Table 1.

	AD652JP/AQ/SQ			AD652KP/BQ			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
VOLTAGE-TO-FREQUENCY MODE							
Gain Error							
f_{CLOCK}= 200 kHz		±0.5	±1		±0.25	±0.5	%
f_{CLOCK} = 1 MHz		±0.5	**±1**		±0.25	**±0.5**	%
f_{CLOCK} = 4 MHz		±0.5	**±1.5**		±0.25	**±0.75**	%
Gain Temperature Coefficient							
f_{CLOCK} = 200 kHz		±25	±50		±15	±25	ppm/°C
f_{CLOCK} = 1 MHz		±25	**±50**		±15	**±25**	ppm/°C
		±10	**±50**		±10	**±30**	ppm/°C[1]
f_{CLOCK} = 4 MHz		±25	**±75**		±15	**±50**	ppm/°C
Power Supply Rejection Ratio		0.001	**0.01**		0.001	**0.01**	%/V
Linearity Error							
f_{CLOCK} = 200 kHz		±0.002	±0.02		±0.002	±0.005	%
f_{CLOCK} = 1 MHz		±0.002	**±0.02**		±0.002	**±0.005**	%
f_{CLOCK} = 2 MHz		±0.01	±0.02		±0.002	±0.005	%
f_{CLOCK} = 4 MHz		±0.02	**±0.05**		±0.01	**±0.02**	%
Offset (Transfer Function, RTI)		± 1	**±3**		±1	**±2**	mV
Offset Temperature Coefficient		±10	**±50**		±10	**±25**	µV/°C
Response Time	One Period of New Output Frequency Plus One Clock Period.						
FREQUENCY-TO-VOLTAGE MODE							
Gain Error, f_{IN} = 100 kHz FS		±0.5	±1		±0.25	±0.5	%
Linearity Error, f_{IN} = 100 kHz FS		±0.002	±0.02		±0.002	±0.01	%
INPUT RESISTORS							
CERDIP (Figure 2)(0 to 10 V FS Range)	19.8	20	20.2	19.8	20	20.2	kΩ
PLCC (Figure 3)							
Pin 8 to Pin 7	9.9	10	10.1	9.9	10	10.1	kΩ
Pin 7 to Pin 5 (0 V to 5 V FS Range)	9.9	10	10.1	9.9	10	10.1	kΩ
Pin 8 to Pin 5 (0 V to 10 V FS Range)	19.8	20	20.2	19.8	20	20.2	kΩ
Pin 9 to Pin 5 (0 V to 8 V FS Range)	15.8	16	16.2	15.8	16	16.2	kΩ
Pin 10 to Pin 5 (Auxiliary Input)	19.8	20	20.2	19.8	20	20.2	kΩ
Temperature Coefficient (All)		±50	**±100**		±50	**±100**	ppm/°C
INTEGRATOR OP AMP							
Input Bias Current							
Inverting Input (Pin 5)		±5	**±20**		±5	**±20**	nA
Noninverting Input (Pin 6)		20	**50**		20	**50**	nA
Input Offset Current		20	**70**		20	**70**	nA
Input Offset Current Drift		1	3		1	2	nA/°C
Input Offset Voltage		±1	**±3**		±1	**±2**	mV
Input Offset Voltage Drift		±10	±25		±10	±15	µV/°C
Open-Loop Gain		86			86		dB
Common-Mode Input Range	$-V_S + 5$		$+V_S - 5$	$-V_S + 5$		$+V_S - 5$	V
CMRR	80			80			dB
Bandwidth	14	95			14	95	MHz
Output Voltage Range	**−1**		**($+V_S$ − 4)**	**−1**		**($+V_S$ − 4)**	V
(Referred to Pin 6, R1 > = 5 kΩ)							

Parameter	AD652JP/AQ/SQ Min	AD652JP/AQ/SQ Typ	AD652JP/AQ/SQ Max	AD652KP/BQ Min	AD652KP/BQ Typ	AD652KP/BQ Max	Unit
COMPARATOR							
Input Bias Current		0.5	5		0.5	5	µA
Common-Mode Voltage	$-V_S + 4$		$+V_S - 4$	$-V_S + 4$		$+V_S - 4$	V
CLOCK INPUT							
Maximum Frequency	**4**	5		**4**	5		MHz
Threshold Voltage (Referred to Pin 12)		1.2			1.2		V
T_{MIN} to T_{MAX}	**0.8**		**2.0**	**0.8**		**2.0**	V
Input Current							
$(-V_S < V_{CLK} < +V_S)$		5	**20**		5	**20**	µA
Voltage Range	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Rise Time			2			2	µs
OUTPUT STAGE							
V_{OL} (I_{OUT} = 10 mA)			**0.4**			**0.4**	V
I_{OL}							
V_{OL} < 0.8 V			**15**			**15**	mA
V_{OL} < 0.4 V, T_{MIN} to T_{MAX}			**8**			**8**	mA
I_{OH} (Off Leakage)		0.01	**10**		0.01	**10**	µA
Delay Time, Positive Clock Edge to Output Pulse	**150**	200	**250**	**150**	200	**250**	ns
Fall Time (Load = 500 pF and I_{SINK} = 5 mA)		100			100		ns
Output Capacitance		5			5		pF
OUTPUT ONE-SHOT							
Pulse Width, t_{OS}							
C_{OS} = 300 pF	**1**	1.5	**2**	1	1.5	**2**	µs
C_{OS} = 1000 pF	4	5	6	4	5	6	µs
REFERENCE OUTPUT							
Voltage	**4.950**	5.0	**5.050**	**4.975**	5.0	**5.025**	V
Drift			**100**			**50**	ppm/°C
Output Current							
Source T_{MIN} to T_{MAX}	**10**			**10**			mA
Sink	100	500		100	500		µA
Power Supply Rejection							
Supply Range = ±12.5 V to ±17.5 V			0.015			0.015	%/V
Output Impedance (Sourcing Current)		0.3	**2**		0.3	**2**	Ω
POWER SUPPLY							
Rated Voltage		±15			±15		V
Operating Range							
Dual Supply	±6	±15	±18	±6	±15	±18	V
Single Supply ($-V_S$ = 0)	+12		+36	+12		+36	V
Quiescent Current		±11	**±15**		±11	**±15**	mA
Digital Common	$-V_S$		$+V_S - 4$	$-V_S$		$+V_S - 4$	V
Analog Common	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
TEMPERATURE RANGE							
Specified Performance							
JP, KP Grade	0		+70	0		+70	°C
AQ, BQ Grade	−40		+85	−40		+85	°C
SQ Grade	−55		+125				°C

[1] Referred to internal V_{REF}. In PLCC package, tested on 10 V input range only.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Ratings
Total Supply Voltage $+V_S$ to $-V_S$	36 V
Maximum Input Voltage (Figure 6)	36 V
Maximum Output Current (Open Collector Output)	50 mA
Amplifier Short-Circuit to Ground	Indefinite
Storage Temperature Range: CERDIP	−65°C to +150°C
Storage Temperature Range: PLCC	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS OF SPECIFICATIONS

Gain Error

The gain of a voltage-to-frequency converter is the scale factor setting that provides the nominal conversion relationship, e.g., 1 MHz full scale. The gain error is the difference in slope between the actual and ideal transfer functions for the V-F converter.

Linearity Error

The linearity error of a V-F is the deviation of the actual transfer function from a straight line passing through the endpoints of the transfer function.

Gain Temperature Coefficient

The gain temperature coefficient is the rate of change in full-scale frequency as a function of the temperature from +25°C to T_{MIN} or T_{MAX}.

Table 3. Pin Configurations

Pin No.	Q-16 Package	P-20A Package
1	$+V_S$	NC
2	TRIM	$+V_S$
3	TRIM	NC
4	OP AMP OUT	OP AMP OUT
5	OP AMP "−"	OP AMP "−"
6	OP AMP "+"	OP AMP "+"
7	10 VOLT INPUT	5 VOLT INPUT
8	$-V_S$	10 VOLT INPUT
9	C_{OS}	8 VOLT INPUT
10	CLOCK INPUT	OPTIONAL 10 V INPUT
11	FREQ OUT	$-V_S$
12	DIGITAL GND	C_{OS}
13	ANALOG GND	CLOCK INPUT
14	COMP "−"	FREQ OUT
15	COMP "+"	DIGITAL GND
16	COMP REF	ANALOG GND
17		COMP "−"
18		COMP "+"
19		NC
20		COMP REF

THEORY OF OPERATION

A synchronous VFC is similar to other voltage-to-frequency converters in that an integrator is used to perform a charge-balance of the input signal with an internal reference current. However, rather than using a one-shot as the primary timing element, which requires a high quality and low drift capacitor, a synchronous voltage-to-frequency converter (SVFC) uses an external clock. This allows the designer to determine the system stability and drift based upon the external clock selected. A crystal oscillator may also be used if desired.

The SVFC architecture provides other system advantages besides low drift. If the output frequency is measured by counting pulses gated to a signal that is derived from the clock, the clock stability is unimportant and the device simply performs as a voltage-controlled frequency divider, producing a high resolution A/D. If a large number of inputs must be monitored simultaneously in a system, the controlled timing relationship between the frequency output pulses and the user-supplied clock greatly simplifies this signal acquisition. Also, if the clock signal is provided by a VFC, the output frequency of the SVFC is proportional to the product of the two input voltages. Therefore, multiplication and A-to-D conversion on two signals are performed simultaneously.

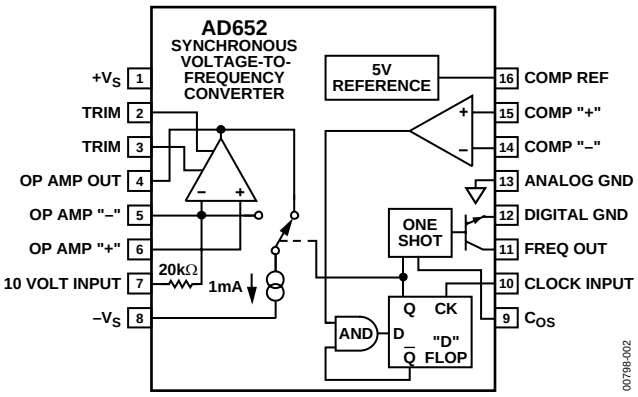


Figure 2. CERDIP Pin Configuration

The pinouts of the AD652 SVFC are shown in Figure 2 and Figure 3. A block diagram of the device configured as an SVFC, along with various system waveforms, is shown in Figure 4.

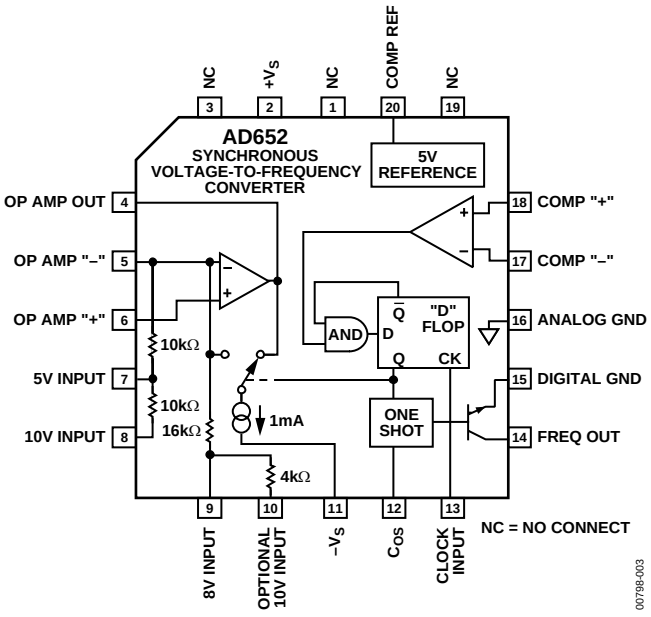


Figure 3. PLCC Pin Configuration

Figure 4 shows the typical up-and-down ramp integrator output of a charge-balance VFC. After the integrator output has crossed the comparator threshold and the output of the AND gate has gone high, nothing happens until a negative edge of the clock comes along to transfer the information to the output of the D FLOP. At this point, the clock level is low, so the latch does not change state. When the clock returns high, the latch output goes high and drives the switch to reset the integrator; at the same time, the latch drives the AND gate to a low output state. On the very next negative edge of the clock, the low output state of the AND gate is transferred to the output of the D FLOP. When the clock returns high, the latch output goes low and drives the switch back into the Integrate mode. At the same time, the latch drives the AND gate to a mode where it truthfully relays the information presented to it by the comparator.

Because the reset pulses applied to the integrator are exactly one clock period long, the only place where drift can occur is in a variation of the symmetry of the switching speed with temperature.

Since each reset pulse is identical, the AD652 SVFC produces a very linear voltage-to-frequency transfer relation. Also, because all reset pulses are gated by the clock, there are no problems with dielectric absorption causing the duration of a reset pulse to be influenced by the length of time since the last reset.

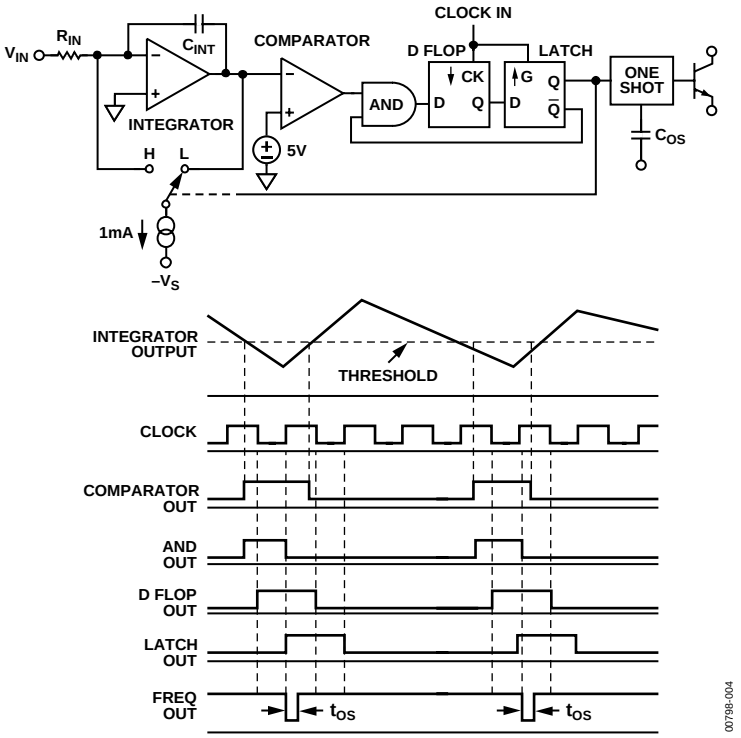


Figure 4. Block Diagram and System Waveforms

Figure 4 shows that the period between output pulses is constrained to be an exact multiple of the clock period. Consider an input current of exactly one quarter the value of the reference current. In order to achieve a charge balance, the output frequency equals the clock frequency divided by four: one clock period for reset and three clock periods of integrate. This is shown in Figure 5. If the input current is increased by a very small amount, the output frequency should also increase by a very small amount. Initially, however, no output change is observed for a very small increase in the input current. The output frequency continues to run at one quarter of the clock, delivering an average of 250 µA to the summing junction. Since the input current is slightly larger than this, charge accumulates in the integrator and the sawtooth signal starts to drift downward. As the integrator sawtooth drifts down, the comparator threshold is crossed earlier and earlier in each successive cycle, until finally, a whole cycle is lost. When the cycle is lost, the integrate phase lasts for two periods of the clock instead of the usual three periods. Thus, among a long string of divide-by-fours, an occasional divide-by-three occurs; the average of the output frequency is very close to one quarter of the clock, but the instantaneous frequency can be very different.

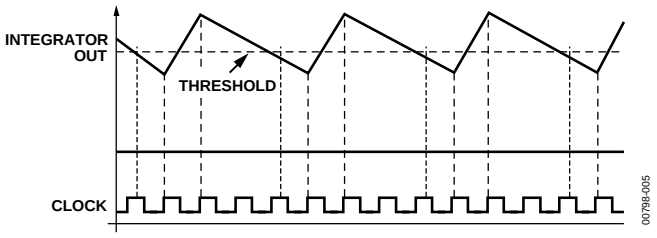


Figure 5. Integrator Output for I_{IN} = 250 µA

Because of this, it is very difficult to observe the waveform on an oscilloscope. During all of this time, the signal at the output of the integrator is a sawtooth wave with an envelope that is also a sawtooth. See Figure 6.

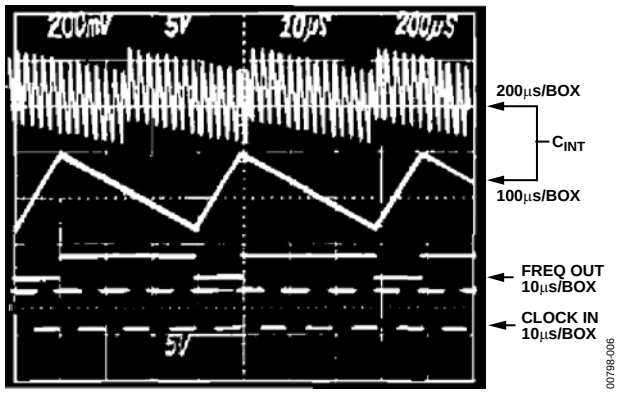


Figure 6. Integrator Output for I_{IN} Slightly Greater than 250 µs

Another way to view this is that the output is a frequency of approximately one-quarter of the clock that has been phase modulated. A constant frequency can be thought of as accumulating phase linearly with time at a rate equal to 2πf radians per second. Therefore, the average output frequency, which is slightly in excess of a quarter of the clock, requires phase accumulation at a certain rate. However, since the SVFC is running at exactly one-quarter of the clock, it does not accumulate enough phase (see Figure 7). When the difference between the required phase (average frequency) and the actual phase equals 2π, a step-in phase is taken where the deficit is made up instantaneously. The output frequency is then a steady carrier that has been phase modulated by a sawtooth signal (see Figure 7). The period of the sawtooth phase modulation is the time required to accumulate a 2π difference in phase between the required average frequency and one quarter of the clock frequency. The sawtooth phase modulation amplitude is 2π.

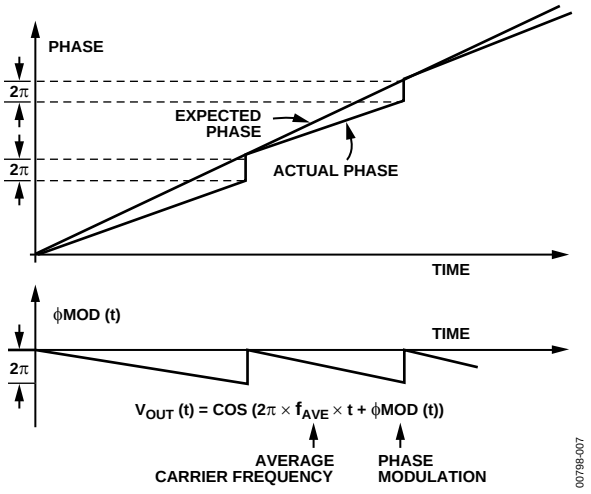


Figure 7. Phase Modulation

The result of this synchronism is that the rate at which data may be extracted from the series bit stream produced by the SVFC is limited. The output pulses are typically counted during a fixed gate interval and the result is interpreted as an average frequency. The resolution of such a measurement is determined by the clock frequency and the gate time. For example, if the clock frequency is 4 MHz and the gate time is 4.096 ms, a maximum count of 8,192 is produced by a full-scale frequency of 2 MHz. Thus, the resolution is 13 bits.

OVERRANGE

Since each reset pulse is only one clock period in length, the full-scale output frequency is equal to one-half the clock frequency. At full scale, the current steering switch spends half of the time on the summing junction; thus, an input current of 0.5 mA can be balanced. In the case of an overrange, the output of the integrator op amp drifts in the negative direction and the output of the comparator remains high. The logic circuits simply settle into a divide-by-two of the clock state.

SVFC CONNECTION FOR DUAL SUPPLY, POSITIVE INPUT VOLTAGES

Figure 8 shows the AD652 connection scheme for the traditional dual supply, positive input mode of operation. The $\pm V_S$ range is from ±6 V to ±18 V. When $+V_S$ is lower than 9.0 V, As shown in Figure 8, three additional connections are required The first connection is to short Pin 13 to Pin 8 (Analog Ground to $-V_S$) and add a pull-up resistor to $+V_S$ (as shown in Figure 21). The pull-up resistor is determined by the following equation:

$$R_{PULLUP} = \frac{2V_S - 5\text{ V}}{500\,\mu\text{A}}$$

These connections ensure proper operation of the 5 V reference. Tie Pin 16 to Pin 6 (as shown in Figure 21) to ensure that the integrator output ramps down far enough to trip the comparator.

The CERDIP-packaged AD652 accepts either a 0 V to 10 V or 0 mA to 0.5 mA full-scale input signal. The temperature drift of the AD652 is specified for a 0 V to 10 V input range using the internal 20 kΩ resistor. If a current input is used, the gain drift is degraded by a maximum of 100 ppm/°C (the TC of the 20 kΩ resistor). If an external resistor is connected to Pin 5 to establish a different input voltage range, drift is induced to the extent that the external resistor's TC differs from the TC of the internal resistor. The external resistor used to establish a different input voltage range should be selected to provide a full-scale current of 0.5 mA (i.e., 10 kΩ for 0 V to 5 V).

SVFC CONNECTIONS FOR NEGATIVE INPUT VOLTAGES

Voltages that are negative with respect to ground may be used as the input to the AD652 SVFC. In this case, Pin 7 is grounded and the input voltage is applied to Pin 6 (see Figure 9). In this mode, the input voltage can go as low as 4 V above $-V_S$. In this configuration, the input is a high impedance, and only the 20 nA (typical) input bias current of the op amp must be supplied by the input signal. This is contrasted with the more usual positive input voltage configuration, which has a 20 kΩ input impedance and requires 0.5 mA from the signal source.

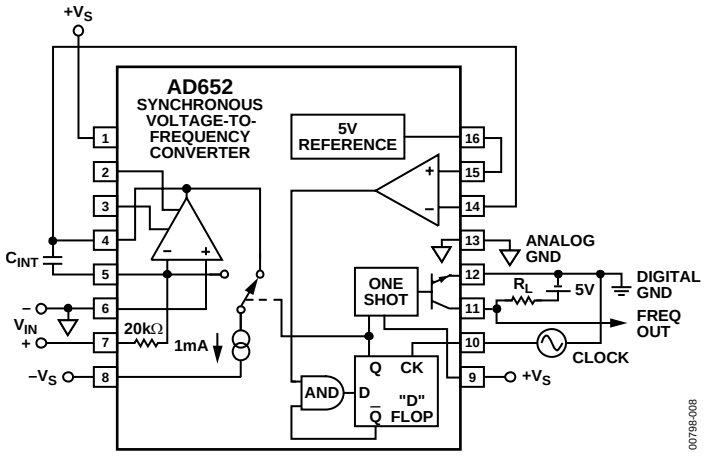


Figure 8. Standard V/F Connection for Positive Input Voltage with Dual Supply

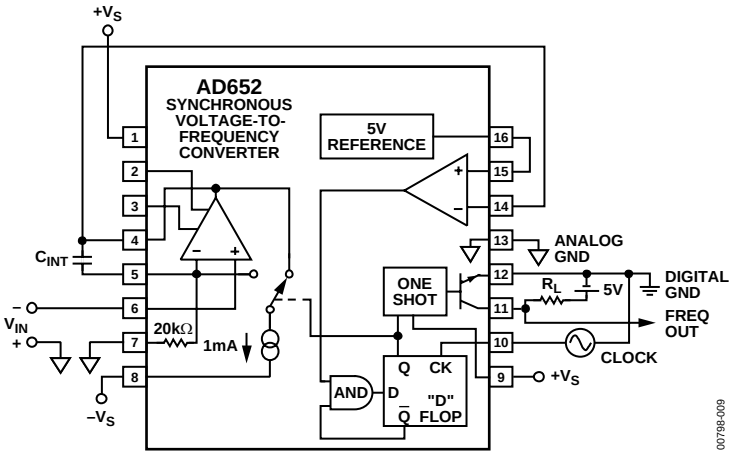


Figure 9. Negative Voltage Input

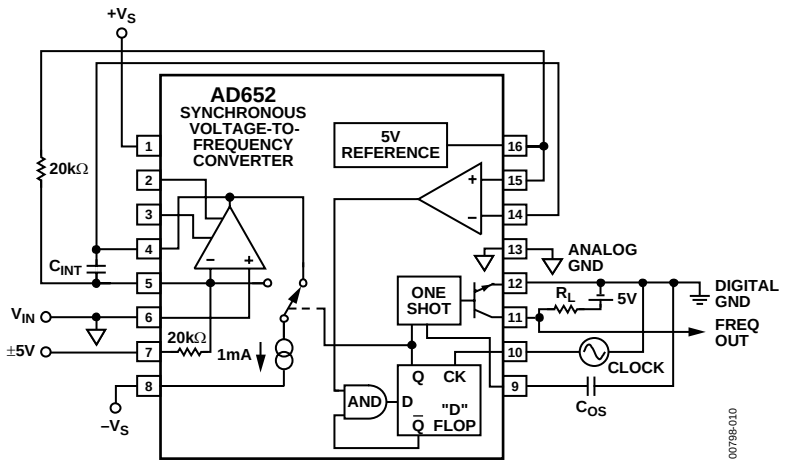


Figure 10. Bipolar Offset

SVFC CONNECTION FOR BIPOLAR INPUT VOLTAGES

A bipolar input voltage of ±5 V can be accommodated by injecting a 250 µA current into Pin 5 (see Figure 10). A −5 V signal provides a zero sum current at the integrator summing junction, which results in a zero-output frequency; a +5 V signal provides a 0.5 mA (full-scale) sum current, which results in the full-scale output frequency.

Using an external resistor to inject the offset current has some effect on the bipolar offset temperature coefficient. The ideal transfer curve with bipolar inputs is shown in Figure 11. The user actually has four options to use in injecting the bipolar offset current into the inverting input of the op amp:

1. Use an external resistor for R_{OS} and the internal 20 kΩ resistor for R_{IN} (as shown in Figure 10).
2. Use the internal 20 kΩ resistor as R_{OS} and an external R_{IN}.
3. Use two external resistors.
4. Use two internal resistors for R_{IN} and R_{OS} (available on PLCC version only).

Option 4 provides the closest to the ideal transfer function as diagrammed in Figure 11. Figure 12 shows the effects of the transfer relation on the other three options. In the first case, the slope of the transfer function is unchanged with temperature. However, V_{ZERO} (the input voltage required to produce an output frequency of 0 Hz) and F_{ZERO} (the output frequency when V_{IN} = 0 V) changes as the transfer function is displaced parallel to the voltage axis with temperature. In the second case, F_{ZERO} remains constant, but V_{ZERO} changes as the transfer function rotates about F_{ZERO} with temperature changes. In the third case, with two external resistors, the V_{ZERO} point remains invariant while the slope and offset of the transfer function change with temperature. If selecting this third option, the user should select low drift, matched resistors.

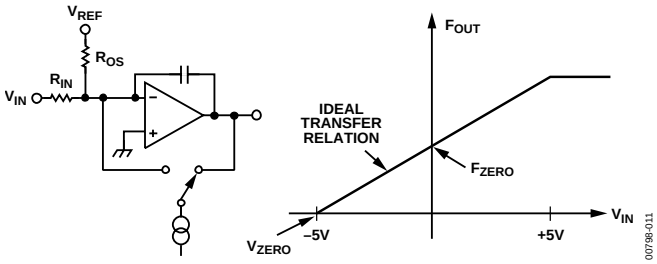


Figure 11. Ideal Bipolar Input Transfer Curve over Temperature

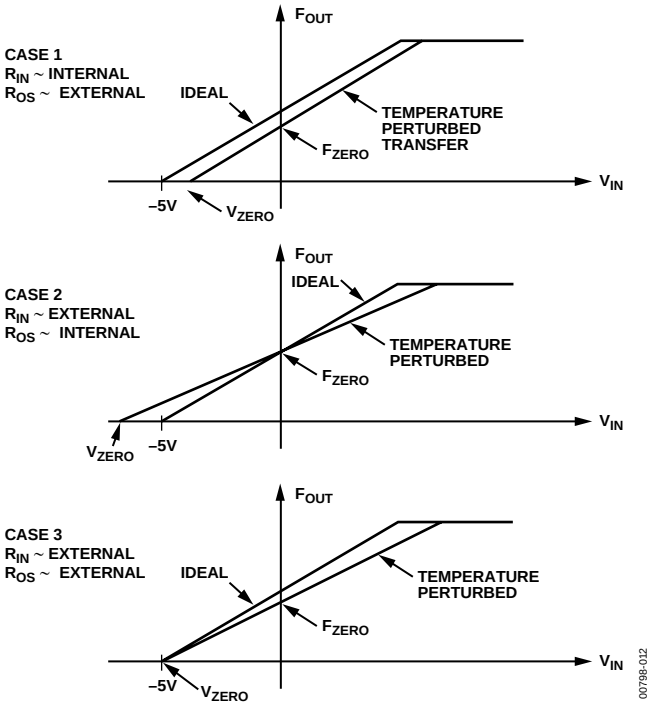


Figure 12. Actual Bipolar Input Transfer over Temperature

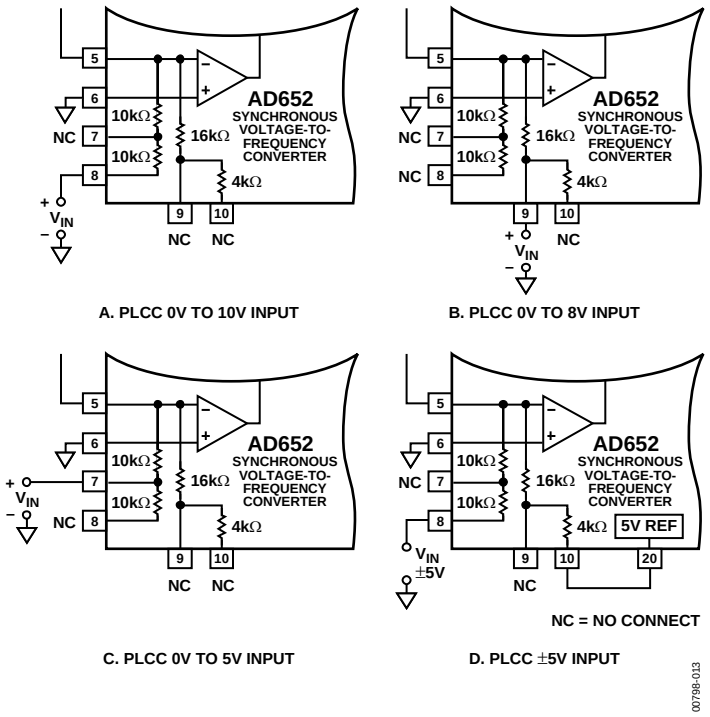


Figure 13.

PLCC CONNECTIONS

The PLCC packaged AD652 offers additional input resistors not found on the CERDIP-packaged device. These resistors provide the user with additional input voltage ranges. Besides the 10 V range available using the on-chip resistor in the CERDIP the PLCC also offers 8 V and 5 V ranges. Figure 13A to Figure 13C show the proper connections for these ranges with positive input voltages. For negative input voltages, the appropriate resistor should be tied to analog ground and the input voltage should be applied to Pin 6, the + input of the op amp.

Bipolar input voltages can be accommodated by injecting 250 μA into Pin 5 with the use of the 5 V reference and the input resistors. For the ±5 V or ±2.5 V range, the reference output, Pin 20, should be tied to Pin 10. The input signal should then be applied to Pin 8 for a ±5 V signal and to Pin 7 for a ±2.5 V signal. The input connections for a ±5 V range are shown in Figure 13D. For a ±4 V range, the input signal should be applied to Pin 9, and Pin 20 should be connected to Pin 8.

GAIN AND OFFSET CALIBRATION

The gain error of the AD652 is laser trimmed to within ±0.5%. If higher accuracy is required, the internal 20 kΩ resistor must be shunted with a 2 MΩ resistor to produce a parallel equivalent that is 1% lower in value than the nominal 20 kΩ. Full-scale adjustment is then accomplished using a 500 Ω series trimmer. See Figure 14 and Figure 15. When negative input voltages are used, this 500 Ω trimmer is tied to ground and Pin 6 is the input pin.

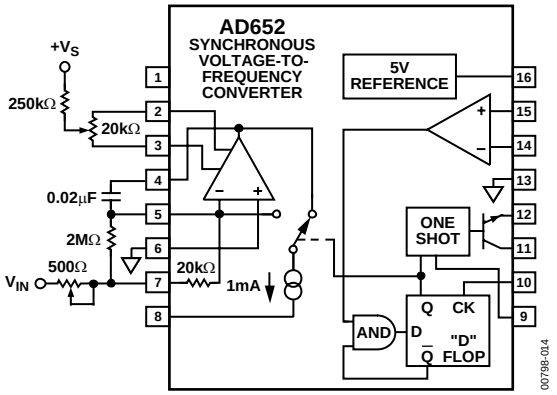


Figure 14. CERDIP Gain and Offset Trim

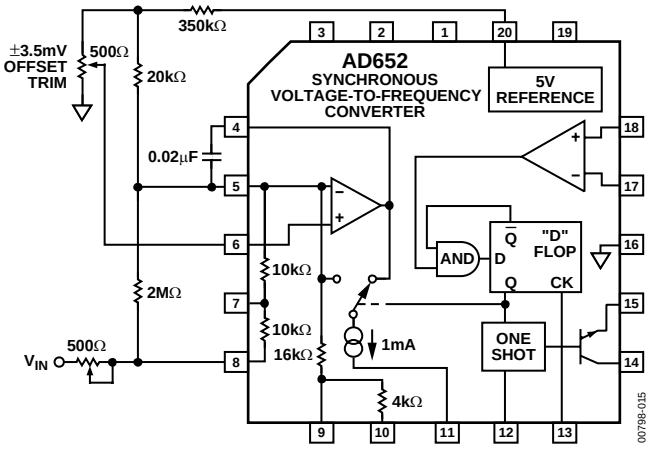


Figure 15. PLCC Gain and Offset Trim

This gain trim should be done with an input voltage of 9 V, and the output frequency should be adjusted to exactly 45% of the clock frequency. Since the device settles into a divide-by-2 mode for an input overrange condition, adjusting the gain with a 10 V input is impractical; the output frequency is exactly one-half the clock frequency if the gain is too high and does not change with adjustment until the exact proper scale factor was achieved. Thus, the gain adjustment should be done with a 9 V input.

The offset of the op amp may be trimmed to zero with the trim scheme shown in Figure 14 for the CERDIP package and Figure 15 for the PLCC package. One way of trimming the offset is by grounding Pin 7 (8) of the CERDIP (PLCC) device and observing the waveform at Pin 4. If the offset voltage of the op amp is positive, the integrator has saturated and the voltage is at the positive rail. If the offset voltage is negative, there is a small effective input current that causes the AD652 to oscillate; a sawtooth waveform is observed at Pin 4. The potentiometer should be adjusted until the downward slope of this sawtooth becomes very slow, down to a frequency of 1 Hz or less. In an analog-to-digital conversion application, an easier way to trim the offset is to apply a small input voltage, such as 0.01% of the full-scale voltage, and adjust the potentiometer until the correct digital output is reached.

GAIN PERFORMANCE

The AD652 gain error is specified as the difference in slope between the actual and the ideal transfer function over the full-scale frequency range. Figure 16 shows a plot of the typical gain error changes versus the clock input frequency, normalized to 100 kHz. Figure 16 shows the typical gain changes normalized to the original 100 kHz gain if, after using the AD652 with a full-scale clock frequency of 100 kHz, the necessary gating time is reduced by increasing the clock frequency.

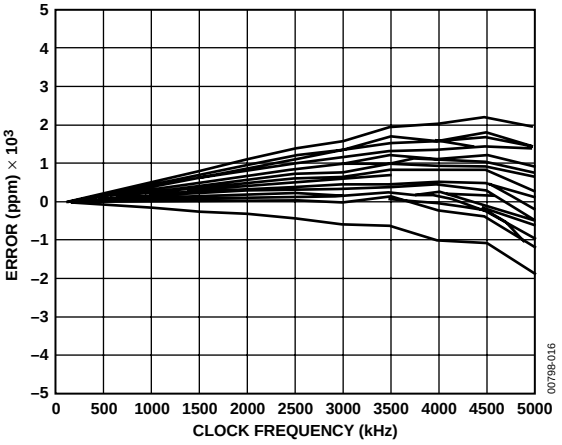


Figure 16. Gain vs. Clock Input

REFERENCE NOISE

The AD652 has an on-board, precision buffered 5 V reference available to the user. Besides being used to offset the noninverting comparator input in the voltage-to-frequency mode, this reference can be used for other applications such as offsetting the input to handle bipolar signals and providing bridge excitation. It can source 10 mA and sink 100 μA, and is short-circuit protected. Heavy loading of the reference does not change the gain of the VFC, though it does affect the external reference voltage. For example, a 10 mA load interacting with a 0.3 Ω typical output impedance changes the reference voltage by 0.06%.

DIGITAL INTERFACING CONSIDERATIONS

The AD652 clock input has a high impedance input with a threshold voltage of two diode voltages with respect to Digital Ground at Pin 12 (approximately 1.2 V at room temperature). When the clock input is low, 5 μA to 10 μA flows out of this pin. When the clock input is high, no current flows.

The frequency output is an open collector pull-down capable of sinking 10 mA with a maximum voltage of 0.4 V. This drives 6 standard TTL inputs. The open collector pull-up voltage can be as high as 36 V above digital ground.

COMPONENT SELECTION

The AD652 integrating capacitor should be 0.02 μF. If a large amount of normal mode interference is expected (more than 0.1 V) and the clock frequency is less than 500 kHz, an integrating capacitor of 0.1 μF should be used. Mylar, polypropylene, or polystyrene capacitors should be used.

The open collector pull-up resistor should be chosen to give adequately fast rise times. At low clock frequencies (100 kHz), larger resistor values (several kΩ) and slower rise times may be tolerated. However, at higher clock frequencies (1 MHz), a lower value resistor should be used. The loading of the logic input that is being driven must also be taken into consideration.

For example, if two standard TTL loads are to be driven, a 3.2 mA current must be sunk, leaving 6.8 mA for the pull-up resistor if the maximum low level voltage is to be maintained at 0.4 V. A 680 Ω resistor would therefore be selected ((5 V – 0.4 V)/6.8 mA) = 680 Ω.

The one-shot capacitor controls the pulse width of the frequency output. The pulse is initiated by the rising edge of the clock signal. The delay time between the rising edge of the clock and the falling edge of the frequency output is typically 200 ns. The width of the pulse is 5 ns/pF, and the minimum width is about 200 ns with Pin 9 floating. If the one-shot period is accidentally chosen longer than the clock period, the width of the pulse defaults to equal the clock period. The one-shot can be disabled by connecting Pin 9 to $+V_S$ (Figure 17); the output pulse width is then equal to the clock period. The one-shot is activated (Figure 18) by connecting a capacitor from Pin 9 to $+V_S$, $-V_S$, or Digital Ground ($+V_S$ is preferred).

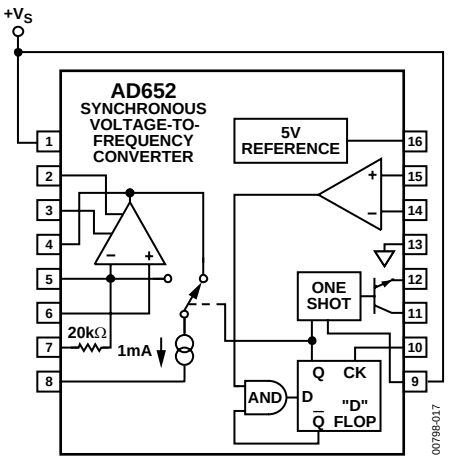


Figure 17. One-Shot Disabled

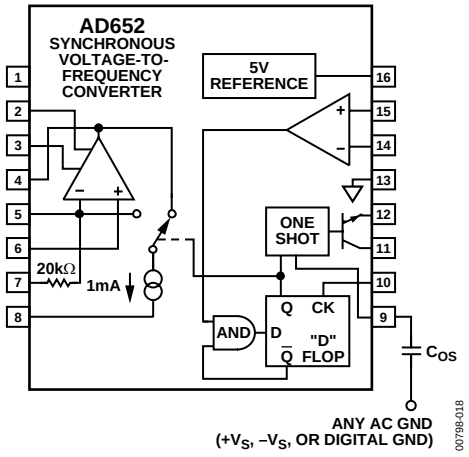


Figure 18. One-Shot Enabled

DIGITAL GROUND

Digital Ground can be at any potential between $-V_S$ and $(+V_S - 4\ V)$. This can be very useful in systems with derived grounds rather than stiff supplies. For example, in a small isolated power circuit, often only a single supply is generated and the ground is set by a divider tap. Such a ground cannot handle the large currents associated with digital signals. With the AD652 SVFC, it is possible to connect the Digital Ground to $-V_S$ for a solid logic reference, as shown in Figure 19.

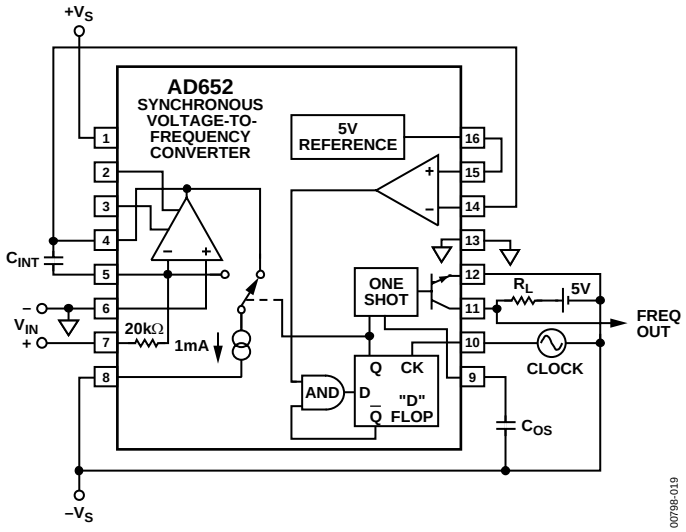


Figure 19. Digital GND at $-V_S$

SINGLE-SUPPLY OPERATION

In addition to the Digital Ground being connected to $-V_S$, it is also possible to connect Analog Ground to $-V_S$ of the AD652. Thus, the device is truly operating from a single-supply voltage that can range from 12 V to 36 V. This is shown in Figure 21 for a positive voltage input, and in Figure 20 for a negative voltage input.

In Figure 21, the comparator reference is used as a derived ground; the input voltage is referred to this point as well as to the op amp common mode (Pin 6 is tied to Pin 16). Since the input signal source must drive 0.5 mA of full-scale signal current into Pin 7, it must also draw the exact same current from the input reference potential. This current is therefore provided by the 5 V reference.

In single-supply operation, an external resistor, R_{PULLUP}, is necessary between the power supply, $+V_S$, and the 5 V reference output. This resistor should be selected such that a current of approximately 500 μA flows during operation. For example, with a power supply voltage of +15 V, a 20 kΩ resistor is selected ((15 V–5 V)/500 μA = 20 kΩ).

Figure 20 shows the negative voltage input configuration for using the AD652 in single-supply mode. In this mode, the signal source is driving the + input of the op amp, which requires only 20 nA (typical) compared to the 0.5 mA required in the positive input voltage configuration. The voltage at Pin 6 may go as low as 4 V above ground ($-V_S$ Pin 8). Since the input reference is 5.0 V above ground, this leaves a 1 V window for the input signal. To drive the integrating capacitor with a 0.5 mA full-scale current, it is necessary to provide an external 2 kΩ resistor. This results in a 2 kΩ resistor and a 1 V input range. The external 2 kΩ resistor should be a low TC metal-film type for lowest drift degradation.

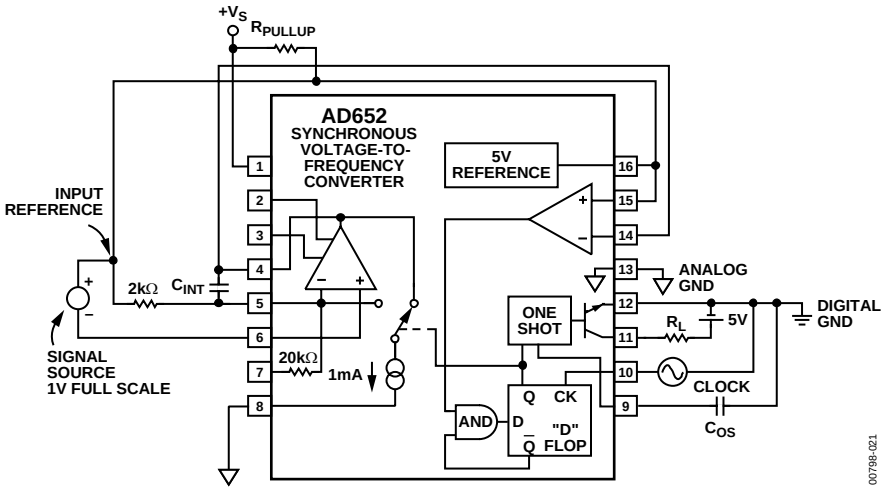


Figure 20. Single-Supply Mode Negative Voltage Input

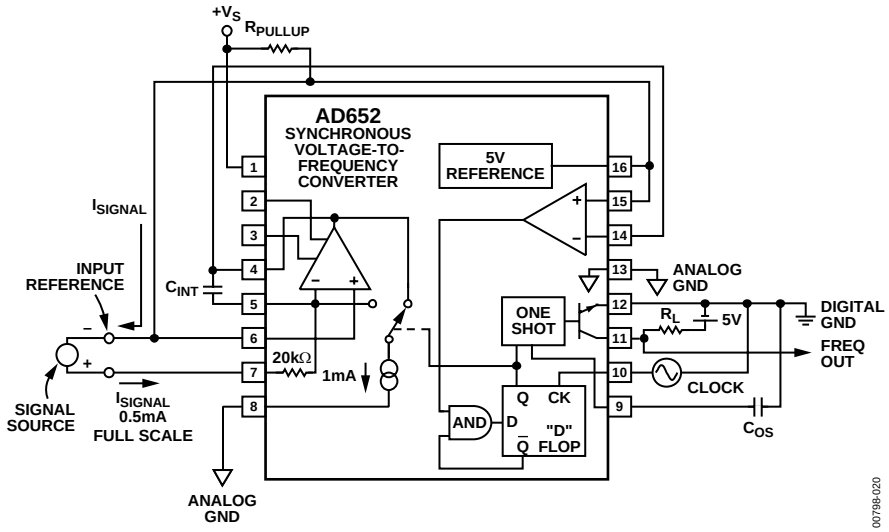


Figure 21. Single-Supply Mode Positive Voltage Input

FREQUENCY-TO-VOLTAGE CONVERTER

The AD652 SVFC also works as a frequency-to-voltage converter. Figure 22 shows the connection diagram for F/V conversion. In this case, the negative input of the comparator is fed the input pulses. Either comparator input may be used so that an input pulse of either polarity may be applied to the F/V.

In Figure 22, the + input is tied to a 1.2 V reference and low-level TTL pulses are used as the frequency input. The pulse must be low on the falling edge of the clock. On the subsequent rising edge, the 1 mA current source is switched to the integrator summing junction and ramps up the voltage at Pin 4. Due to the action of the AND gate, the 1 mA current is switched off after only one clock period. The average current delivered to the summing junction varies from 0 mA to 0.5 mA; using the internal 20 kΩ resistor, this results in a full-scale output voltage of 10 V at Pin 4.

The frequency response of the circuit is determined by the capacitor; the −3 dB frequency is simply the RC time constant. A tradeoff exists between ripple and response. If low ripple is desired, a large value capacitor must be used (1 μF); if fast response is needed, a small capacitor is used (1 nF minimum).

The op amp can drive a 5 kΩ resistor load to 10 V, using a 15 V positive power supply. If a large load capacitance (0.01 μF) must be driven, it is necessary to isolate the load with a 50 Ω resistor as shown. Because the 50 Ω resistor is 0.25% of the full scale, and the specified gain error with the 20 kΩ resistor is 0.5%, this extra resistor only increases the total gain error to 0.75% max.

The circuit shown is unipolar and only a 0 V to +10 V output is allowed. The integrator op amp is not a general-purpose op amp. Instead, it has been optimized for simplicity and high speed. The most significant difference between this amplifier and a general-purpose op amp is the lack of an integrator (or level shift) stage.

Consequently, the voltage on the output (Pin 4) must always be more positive than 1 V below the inputs (Pins 6 and 7). For example, in the F-to-V conversion mode, the noninverting input of the op amp (Pin 6) is grounded, which means the output (Pin 4) cannot go below −1 V. Normal operation of the circuit as shown never calls for a negative voltage at the output.

A second difference between this op amp and a general-purpose amplifier is that the output only sinks 1.5 mA to the negative supply. The only pull-down other than the 1 mA current used for voltage-to-frequency conversion is a 0.5 mA source. The op amp sources a great deal of current from the positive supply, and is internally protected by current limiting. The op amp output may be driven to within 4 V of the positive supply when not sourcing external current. When sourcing 10 mA, the output voltage may be driven to within 6 V of the positive supply.

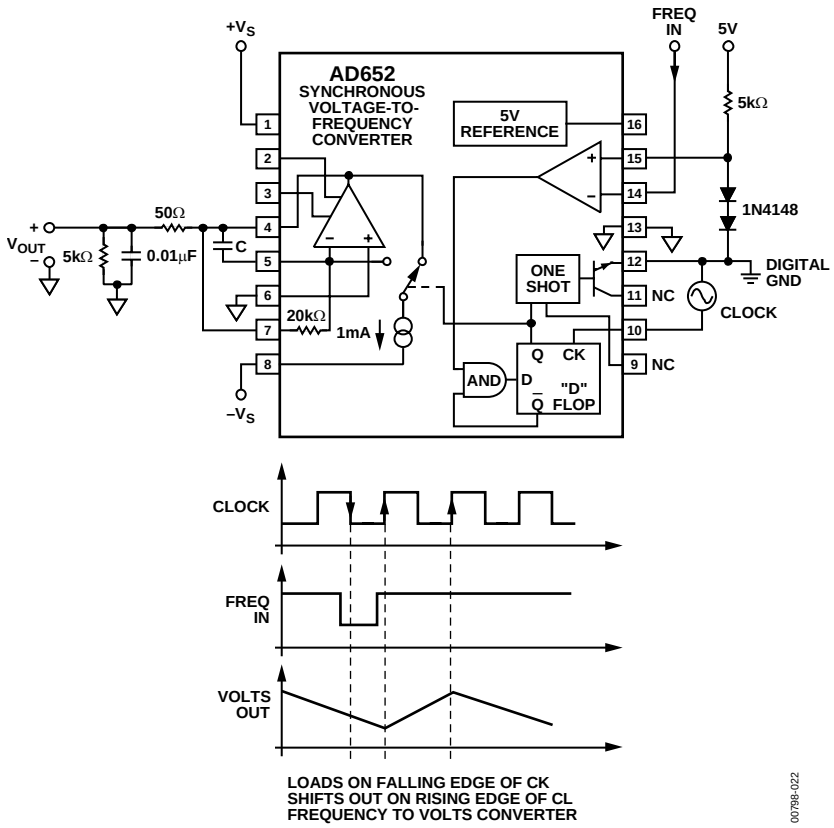


Figure 22. Frequency-to-Voltage Converter

DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins, and to insert small valued resistors (10 Ω to 100 Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1 μF to 1.0 μF should be applied between the supply voltage pins and analog signal ground for proper bypassing on the AD652.

Additionally, a larger board-level decoupling capacitor of 1 μF to 10 μF should be located relatively close to the AD652 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to exploit the full linearity and dynamic range of the AD652.

Separate digital and analog grounds are provided on the AD652. Only the emitter of the open-collector frequency output transistor and the clock input threshold are returned to the digital ground. Only the 5 V reference is connected to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. Much noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At high full-scale frequencies, it is necessary to use a pull-up resistor of about 500 Ω in order to get the rise time fast enough to provide well-defined output pulses. This means that from a 5 V logic supply, for example, the open collector output draws 10 mA. This much current being switched causes ringing on long ground runs due to the self-inductance of the wires. For instance, 20-gauge wire has an inductance of about 20 nH per inch; a current of 10 mA being switched in 50 ns at the end of 12 inches of 20-gauge wire produces a voltage spike of 50 mV. The separate digital ground of the AD652 easily handles these types of switching transients.

A problem remains from interference caused by radiation of electromagnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD652 package. A 1 μF to 10 μF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground, Pin 12. The pull-up resistor should be connected directly to the frequency output, Pin 11. The lead lengths on the bypass capacitor and the pull-up resistor should be as short as possible. The capacitor supplies (or absorbs) the current transients, and large ac signals flow in a physically small loop through the capacitor, pull-up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less inductance if the wires are short, and second, the loop does not radiate RFI efficiently.

The digital ground (Pin 12) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current. There may be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This does not cause a problem; these features greatly ease power distribution and ground manage-ment in large systems. The proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to the analog ground (Pin 6) at the package. More information on proper grounding and reduction of interference can be found in *Noise Reduction Techniques in Electronic Systems*, by H.W. Ort, (John Wiley, 1976).

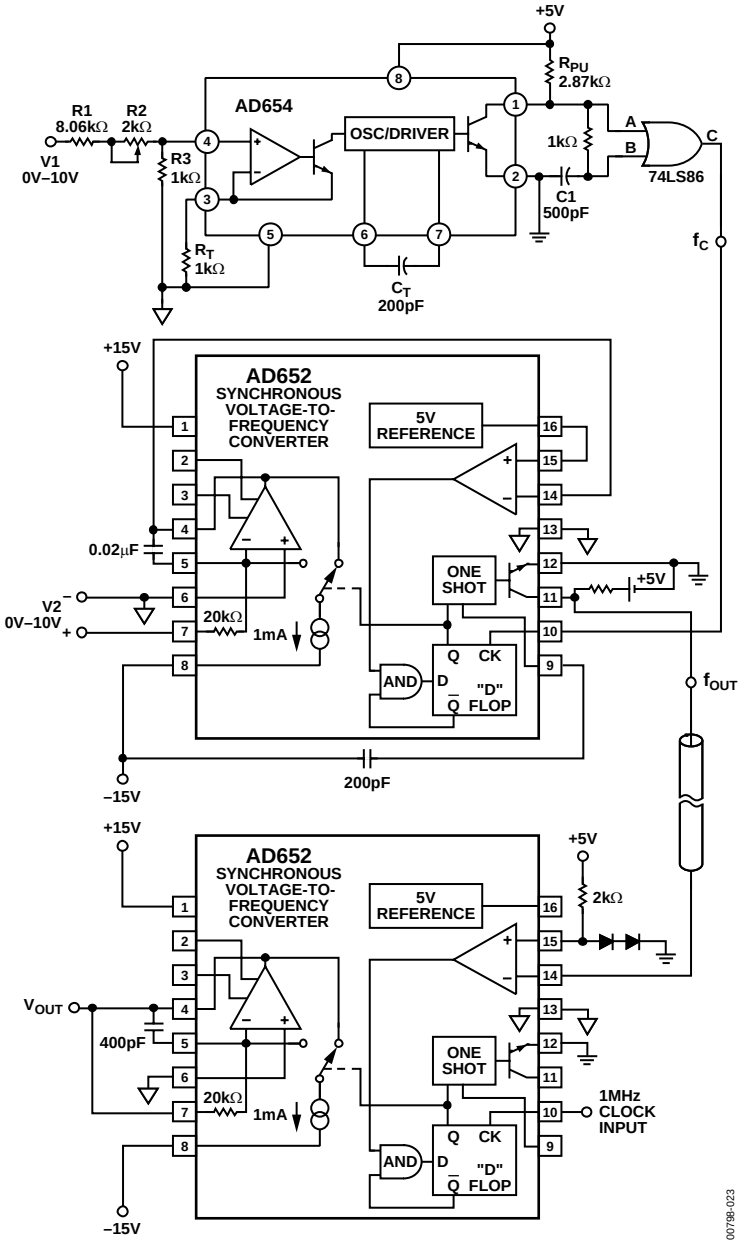


Figure 23. Frequency Output Multiplier

FREQUENCY OUTPUT MULTIPLIER

The AD652 can serve as a frequency output multiplier when used in conjunction with a standard voltage-to-frequency converter. Figure 23 shows the low cost AD654 VFC being used as the clock input to the AD652. Also shown is a second AD652 in the F/V mode. The AD654 is set up to produce an output frequency of 0 kHz to 500 kHz for an input voltage (V_1) range of 0 V to 10 V. The use of R4, C1, and the XOR gate doubles this output frequency from 0 kHz–500 kHz to 0 MHz–1 MHz.

This 1 MHz full-scale frequency is then used as the clock input to the AD652 SVFC. Because the AD652 full-scale output frequency is one-half the clock frequency, the 1 MHz FS clock frequency establishes a 500 kHz maximum output frequency for the AD652 when its input voltage (V_2) is 10 V. The user therefore has an output frequency range from 0 kHz to 500 kHz, which is proportional to the product of V_1 and V_2.

This can be shown in equation form, where f_C is the AD654 output frequency and f_{OUT} is the AD652 output frequency:

$$f_C = V_1 \frac{1\text{ MHz}}{10\text{ V}}$$

$$f_{OUT} = V_2 \left(\frac{\frac{f_C}{2}}{10\text{ V}} \right)$$

$$f_{OUT} = V_1 V_2 \left(\frac{1\text{ MHz}}{2(10\text{ V})(10\text{ V})} \right)$$

$$f_{OUT} = V_1 \times V_2 \times 5\text{ kHz}/V^2$$

The scope photo in Figure 24 shows V_1 and V_2 (top two traces) and the output of the F-V (bottom trace).

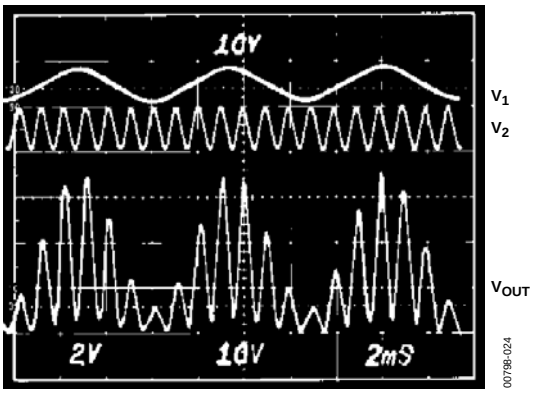


Figure 24. Multiplier Waveforms

SINGLE-LINE MULTIPLEXED DATA TRANSMISSION

It is often necessary to measure several different signals and relay the information to some remote location using a minimum amount of cable. Multiple AD652 SVFC devices may be used with a multiphase clock to combine these measurements for serial transmission and demultiplexing. Figure 25 shows a block diagram of a single-line multiplexed data transmission system with high noise immunity. Figure 26, Figure 27, and Figure 30 show the SVFC multiplexer, a representative means of data transmission, and an SVFC demultiplexer respectively.

Multiplexer

Figure 30 shows the SVFC multiplexer. The clock inputs for the several SVFC channels are generated by a TIM9904A 4-phase clock driver, and the frequency outputs are combined by strapping all the frequency output pins together (a wire OR connection). The one-shot in the AD652 sets the pulse width of the frequency output pulses to be slightly shorter than one quarter of the clock period. Synchronization is achieved by applying one of the four available phases to a fixed TTL one-shot ('121) and combining the output with external transistor.

The width of this sync pulse is shorter than the width of the frequency output pulses to facilitate decoding the signal. The RC lag network on the input of the one-shot provides a slight delay between the rising edge of the clock and the sync pulse in order to match the 150 ns delay of the AD652 between the rising edge of the clock and the output pulse.

Transmitter

The multiplex signal can be transmitted in any manner suitable to the task at hand. A pulse transformer or an opto-isolator can provide galvanic isolation; extremely high voltage isolation or transmission through severe RF environments can be accomplished with a fiber optic link; telemetry can be achieved with a radio link. The circuit shown in Figure 27 uses an EIA RS-422 standard for digital data transmission over a balanced line. Figure 24 shows the waveforms of the four clock phases and the multiplex output signal. Note that the sync pulse is present every clock cycle, but the data pulses are no more frequent than every other clock cycle since the maximum output frequency from the SVFC is half the clock frequency. The clock frequency used in this circuit is 819.2 kHz, which provides more than 16 bits of resolution if 100 ms gate time is allowed for counting pulses of the decoded output frequencies.

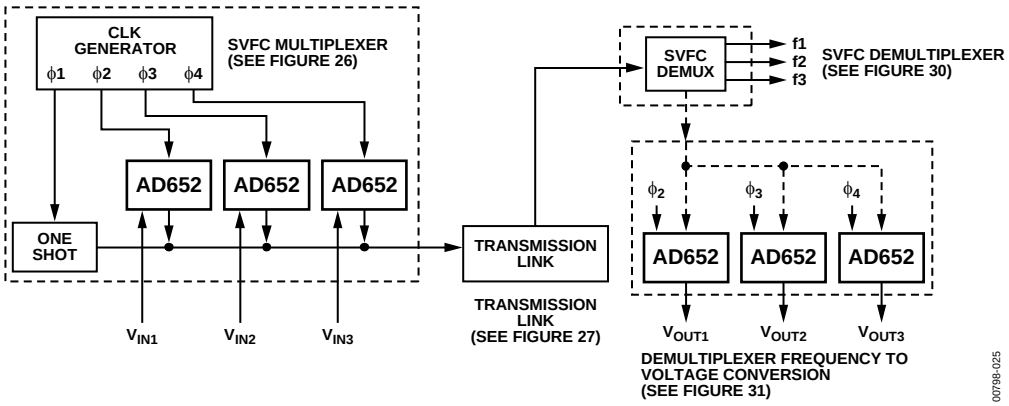


Figure 25. Single-Line Multiplexed Data Transmission Block Diagram

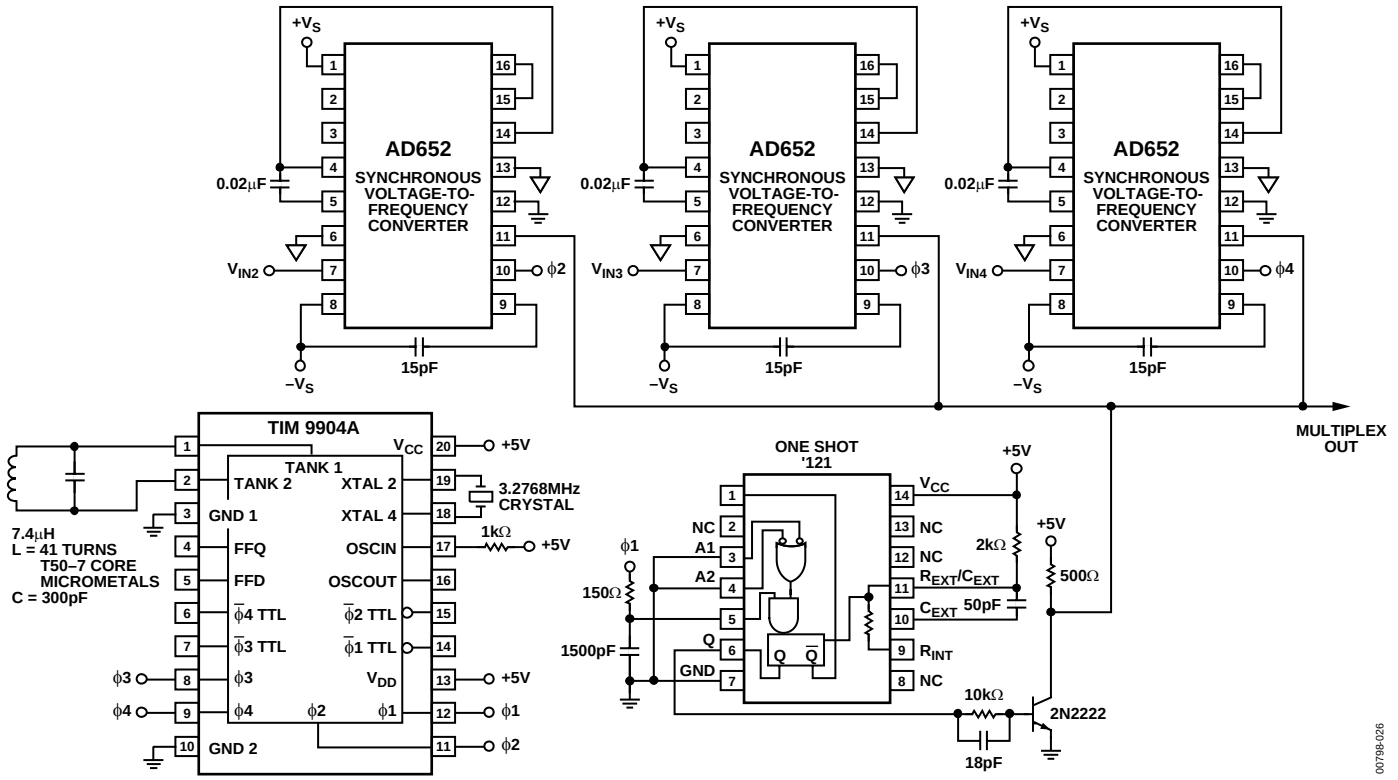


Figure 26. SVFC Multiplexer

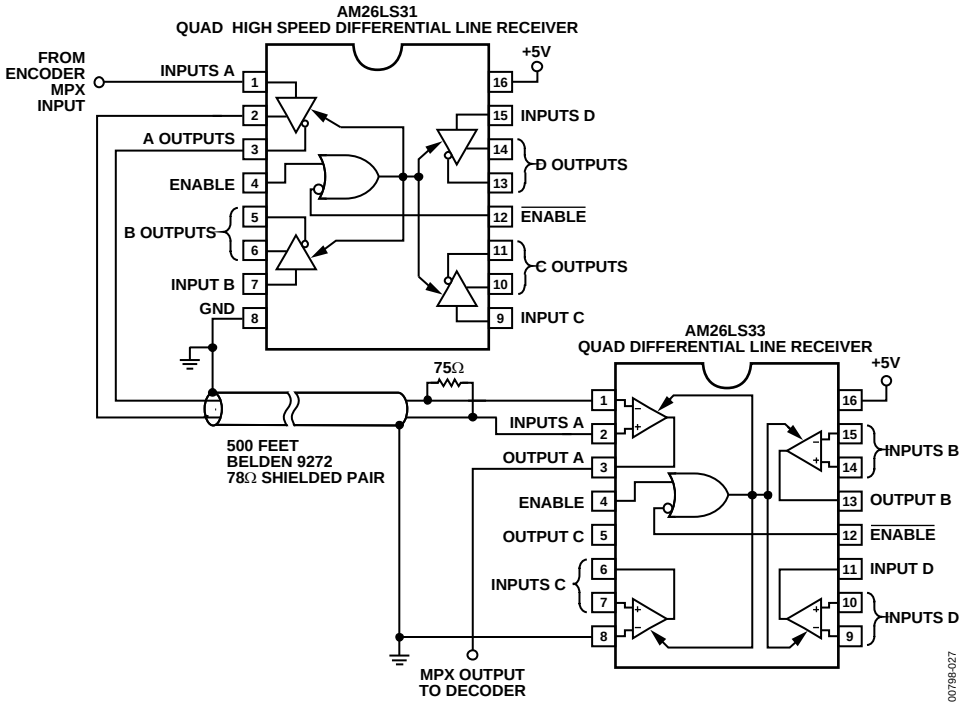


Figure 27. RS-422 Standard Data Transmission

SVFC Demultiplexer

The demultiplexer needed to separate the combined signals is shown in Figure 30. A phase-locked loop drives another 4-phase clock chip to lock onto the reconstructed clock signal. The sync pulses are distinguished from the data pulses by their shorter duration. Each falling edge on the multiplex input signal triggers the one-shot; at the end of this one-shot pulse, the multiplex input signal is sampled by a D-type flip-flop. If the signal is high, the pulse was short (a sync pulse) and the $\overline{Q}$ output of the D-flop goes low. The D-flop is cleared a short time (two gate delays) later, and the clock is reconstructed as a stream of short, low-going pulses. If the multiplex input is a data pulse, then the signal will still be low and no pulse will appear at the reconstructed clock output when the D-flop samples at the end of the one-shot period. See Figure 29.

If it is desired to recover the individual frequency signals, the multiplex input is sampled with a D-flop at the appropriate time, as determined by the rising edge of the various phases generated by the clock chip. These frequency signals can be counted as a ratio relative to the reconstructed clock, so it is not even necessary for the transmitter to be crystal-controlled as shown in Figure 30.

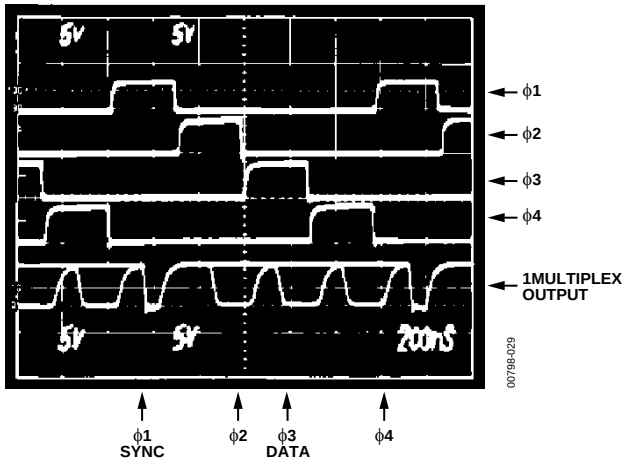


Figure 28. Multiplexer Waveforms

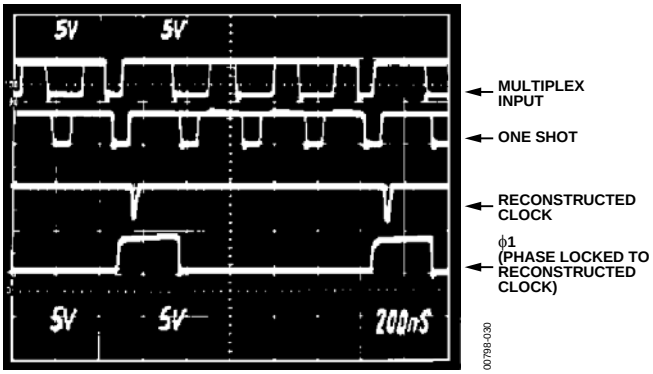


Figure 29. Demultiplexer Waveforms

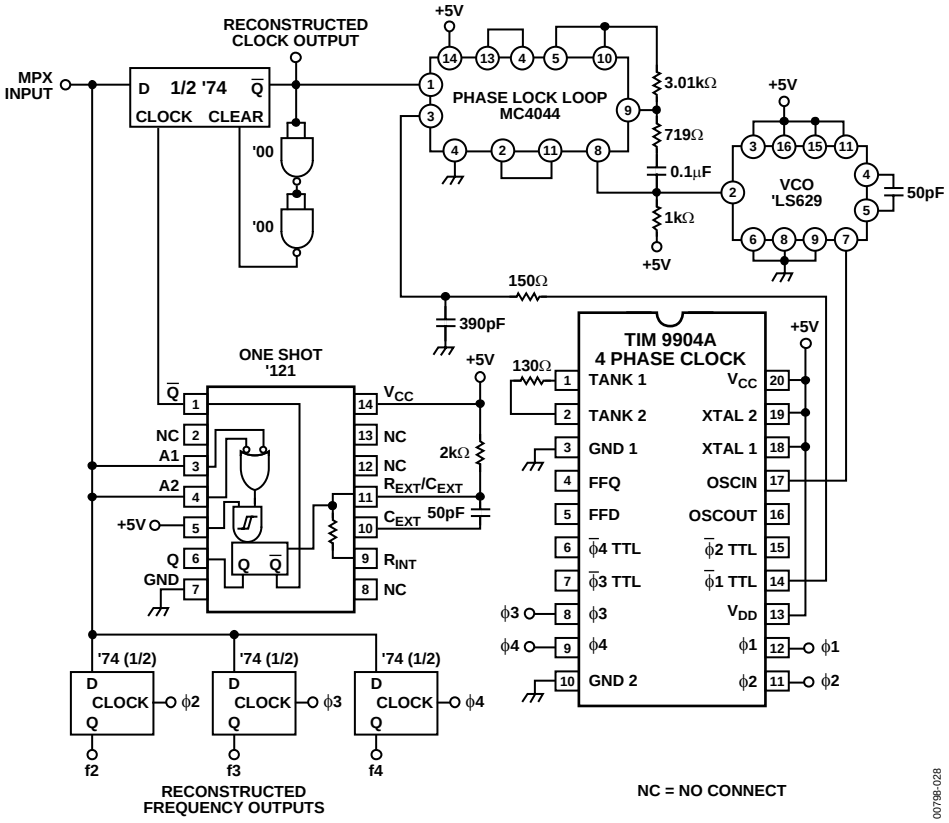


Figure 30. SVFC Demultiplexers

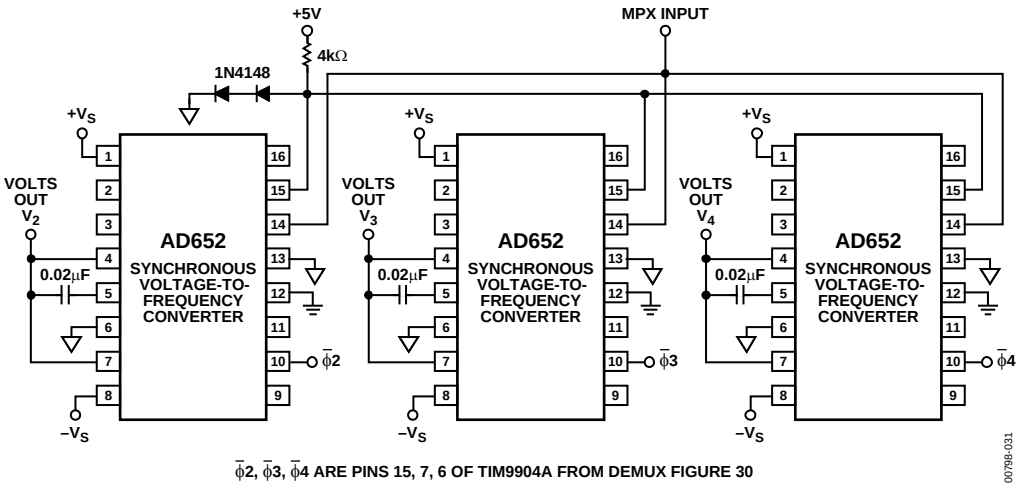


Figure 31. Demultiplexer Frequency-to-Voltage Conversion

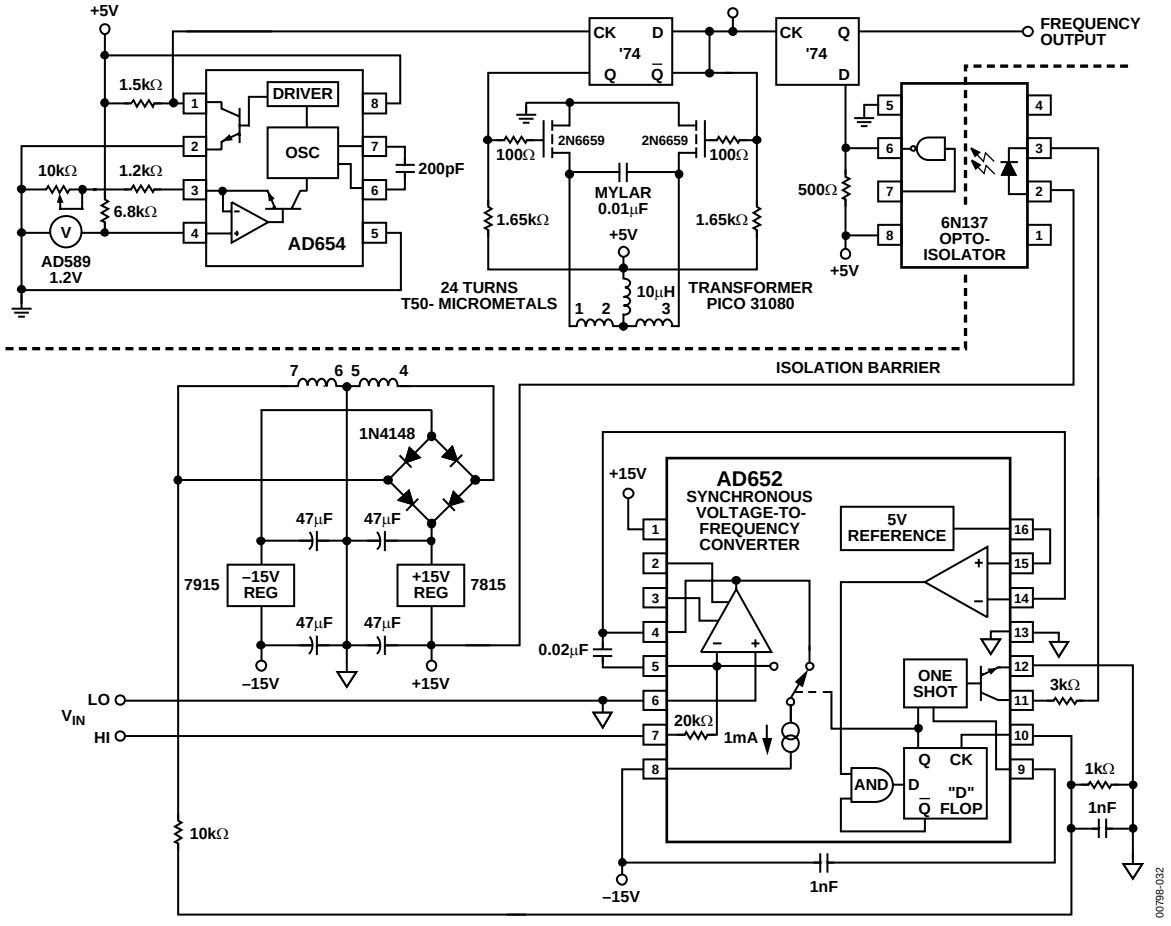


Figure 32. Isolated Synchronous VFC

Analog Signal Reconstruction

If it is desired to reconstruct the analog voltages from the multiplex signal, three more AD652 SVFC devices are used as frequency-to-voltage converters, as shown in Figure 31. The comparator inputs of all the devices are strapped together, the "+" inputs are held at a 1.2 V TTL threshold, and the "–" inputs are driven by the multiplex input. The three clock inputs are driven by the $\overline{\phi}$ outputs of the clock chip. Remember that data at the comparator input of the SVFC is loaded on the falling edge of the clock signal and shifted out on the next rising edge. Note that the frequency signals for each data channel are available at the frequency output pin of each FVC.

ISOLATED FRONT END

In some applications, it may be necessary to have complete galvanic isolation between the analog signals being measured and the digital portions of the circuit. The circuit shown in Figure 32 runs off a single 5 V power supply and provides a self-contained, completely isolated analog measurement system. The power for the AD652 SVFC is provided by a chopper and a transformer, and is regulated to 15 V.

Both the chopper frequency and the AD652 clock frequency are 125 kHz, with the clock signal being relayed to the SVFC through the transformer. The frequency output signal is relayed through an opto-isolator and latched into a D flop. The chopper frequency is generated from an AD654 VFC, and is frequency divided by two to develop differential drive for the chopper transistors, and to ensure an accurate 50% duty cycle. The pull-up resistors on the D flop outputs provide a well-defined high level voltage to the choppers to equalize the drive in each direction. The 10 μH inductor in the 5 V lead of the transformer primary is necessary to equalize any residual imbalance in the drive on each half cycle, and thus prevent saturation of the core. The capacitor across the primary resonates the system so that under light loading conditions on the secondary, the wave shape is sinusoidal and the clock frequency is relayed to the SVFC. To adjust the chopper frequency, disconnect any load on the secondary and tune the AD654 for a minimum in the supply current drawn from the 5 V supply.

A-TO-D CONVERSION

In performing an A-to-D conversion, the output pulses of a VFC are counted for a fixed-gate interval. To achieve maximum performance with the AD652, the fixed-gate interval should be generated using a multiple of the SVFC clock input. Counting in this manner eliminates any errors due to the clock (whether it be jitter, drift with time or temperature, and so on) since it is the ratio of the clock and output frequencies that is being measured.

The resolution of the A-to-D conversion measurement is determined by the clock frequency and the gate time. If, for instance, a resolution of 12 bits is desired and the clock frequency is 1 MHz (resulting in an AD652 FS frequency of 500 kHz) the gate time is:

$$\left(\frac{FS\ Freq}{N}\right)^{-1} = \left(\frac{1}{2}\frac{Clock\ Freq}{N}\right)^{-1} = \left(\frac{1\ \text{MHz}}{2(4096)}\right)^{-1}$$

$$= \frac{8192}{1\times10^{6}}\ \text{sec} = 8.192\ \text{ms}$$

Where N is the total number of codes for a given resolution.

Figure 33 shows the AD652 SVFC as an A-to-D converter in block diagram form.

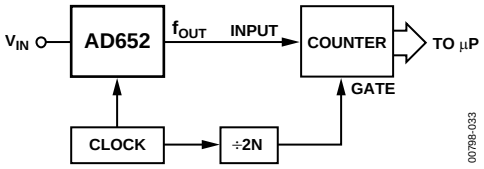


Figure 33. Block Diagram of SVFC A-to-D Converter

To provide the ÷2N block, a single-chip counter such as the 4020B can be used. The 4020B is a 14-stage binary ripple counter that has a clock and master reset for inputs, and buffered outputs from the first stage and the last 11 stages. The output of the first stage is $f_{CLOCK} \div 2^1 = f_{CLOCK}/2$, while the output of the last stage is $f_{CLOCK} \div 2^{14} = f_{CLOCK}/16384$. Therefore, using this single chip counter as the ÷2N block, 13-bit resolution can be achieved. Higher resolution can be achieved by cascading D-type flip flops or another 4020B with the counter.

Table 4 shows the relationship between clock frequency and gate time for various degrees of resolution. Note that if the variables are chosen such that the gate times are multiples of 50 Hz, 60 Hz, or 400 Hz, normal mode rejection (NMR) of those line frequencies occur.

Table 4.

Resolution	N	Clock	Conversion or Gate Time (ms)	Typical Linearity (%)	Comments
12 Bits	4096	81.92 kHz	100	0.002	50 Hz, 60 Hz,400 Hz NMR
12 Bits	4096	2 MHz	4.096	0.01	
12 Bits	4096	4 MHz	2.048	0.02	
4 Digits	10000	200 kHz	100	0.002	50 Hz, 60 Hz, 400 Hz NMR
14 Bits	16384	327.68 kHz	100	0.002	50 Hz, 60 Hz, 400 Hz NMR
14 Bits	16384	1.966 MHz	16.66	0.01	60 Hz NMR
14 Bits	16384	1.638 MHz	20	0.01	50 Hz NMR
4½ Digits	20000	400 kHz	100	0.002	50 Hz, 60 Hz, 400 Hz NMR
16 Bits	65536	655.36 kHz	200	0.002	50 Hz, 60 Hz, 400 Hz NMR
16 Bits	65536	4 MHz	32.77	0.02	

DELTA MODULATOR

The circuit of Figure 34 shows the AD652 configured as a delta modulator. A reference voltage is applied to the input of the integrator (Pin 7), which sets the steady state output frequency at one-half of the AD652 full-scale frequency (1/4 of the clock frequency). As a 0 V to 10 V input signal is applied to the comparator (Pin 15), the output of the integrator attempts to track this signal. For an input in an idling condition (dc), the output frequency is one-half full scale. For positive-going signals, the output frequency is between one-half full scale and full scale; for negative-going signals, the output frequency is between zero and one-half full scale. The output frequency corresponds to the slope of the comparator input signal.

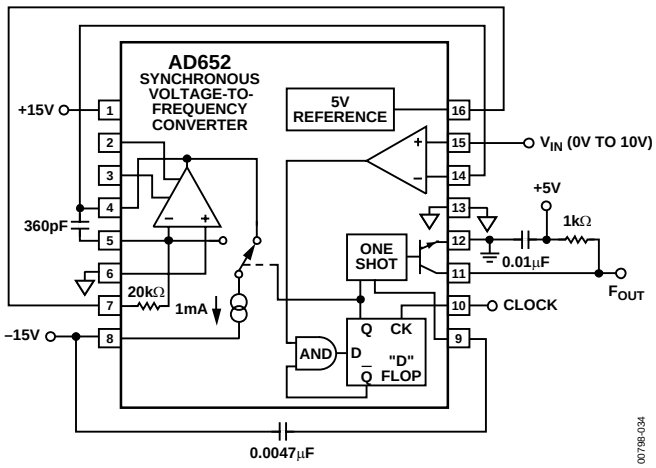


Figure 34. Delta Modulator

Since the output frequency corresponds to the slope of the input signal, the delta modulator acts as a differentiator. A delta modulator is thus a direct way of finding the derivative of a signal. This is useful in systems where, for example, a signal corresponding to velocity exists, and it is desired to determine acceleration.

Figure 35 is a scope photo showing a 20 kHz, 0 V to 10 V sine wave used as the input to the comparator and its ramp-wise approximation at the integrator output. The clock frequency used as 2 MHz and the integrating capacitor was 360 pF. Figure 36 shows the same input signal and its ramp-wise approximation, along with the output frequency corresponding to the derivative of the input signal. In this case, the clock frequency was 50 kHz.

The choice of an integrating capacitor is primarily dictated by the input signal bandwidth. Figure 37 shows this relationship. Note that as the value of C_{INT} is lowered, the ramp size of the integrator approximation becomes larger. This can be compensated for by increasing the clock frequency. The effect of the clock frequency on the ramp size is demonstrated in Figure 35 and Figure 36.

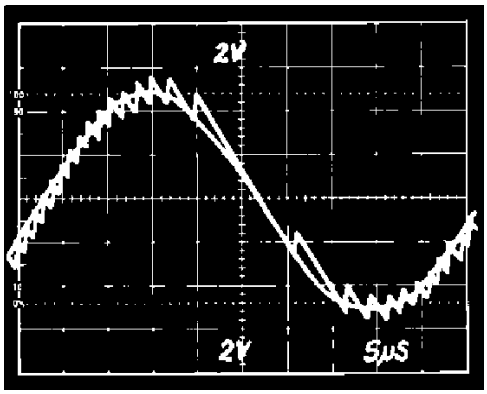


Figure 35. Delta Modulator Input Signal and Ramp-Wise Approximation

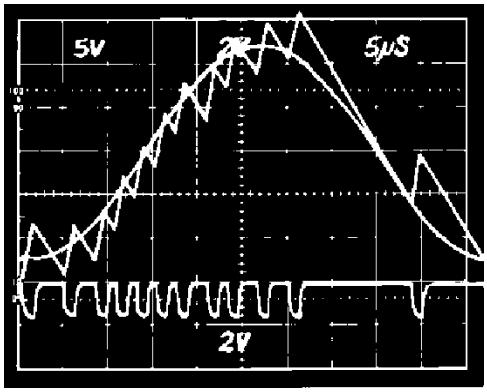


Figure 36. Delta Modulator Input Signal Ramp-Wise Approximation and Output Frequency

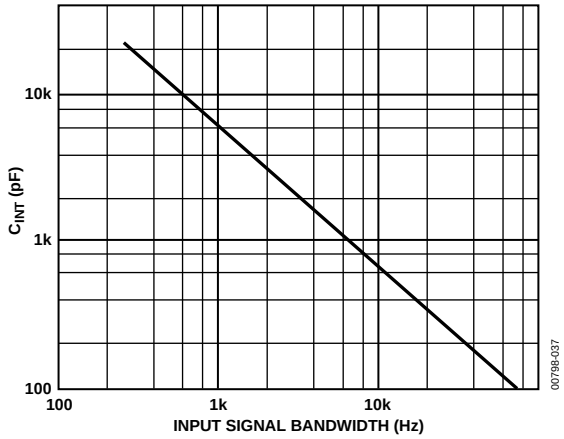


Figure 37. Maximum Integrating Cap Value vs. Input Signal Bandwidth

BRIDGE TRANSDUCER INTERFACE

The circuit of Figure 38 illustrates a simple interface between the AD652 and a bridge-type transducer. The AD652 is an ideal choice because its buffered 5 V reference can be used as the bridge excitation, thereby ratiometrically eliminating the gain drift related errors. This reference provides a minimum of 10 mA of external current, which is adequate for bridge resistance of 600 Ω and above. If, for example, the bridge resistance is 120 Ω or 350 Ω, an external pull-up resistor (R_{PU}) is required. R_{PU} and can be calculated using the following formula:

$$R_{PU}(\max) = \frac{+V_S - 5\text{ V}}{\frac{5\text{ V}}{R_{BRIDGE}} - 10\text{ mA}}$$

An instrumentation amplifier is used to condition the bridge signal before presenting it to the SVFC. With its high CMRR, the AD652 minimizes common-mode errors and can be set to arbitrary gains between 1 and 10,000 via three resistors, simplifying the scaling for the part's calibrated 10 V input range. These resistors should be selected such that the following equation holds:

$$10\text{ V} = V_{BRIDGE}\left(\frac{2R_F}{R_G} + 1\right)$$

where 10 kΩ $\leq R_F \leq$ 20 kΩ, and V_{BRIDGE} is the maximum output voltage of the bridge.

The bridge output may be unipolar, as is the case for most pressure transducers, or it may be bipolar as in some strain measurements. If the signal is unipolar, the reference input of the AD625 (Pin 7) is simply grounded. If the bridge has a bipolar output, however, the AD652 reference can be tied to Pin 7, thereby, converting a 5 V signal (after gain) into a 0 V to +10 V input for the SVFC.

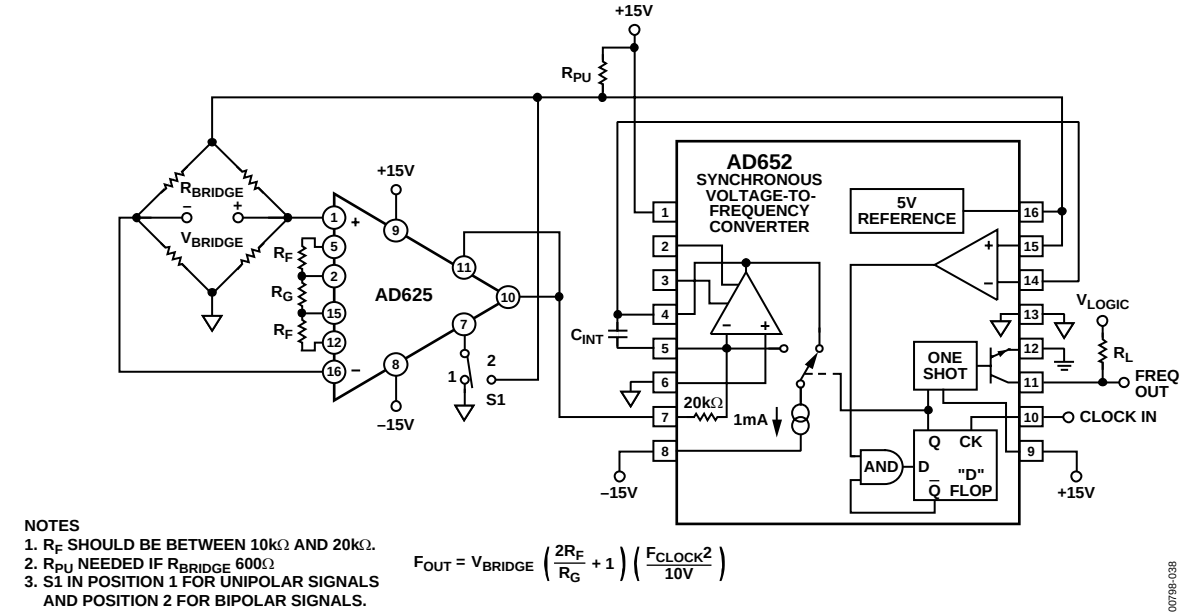
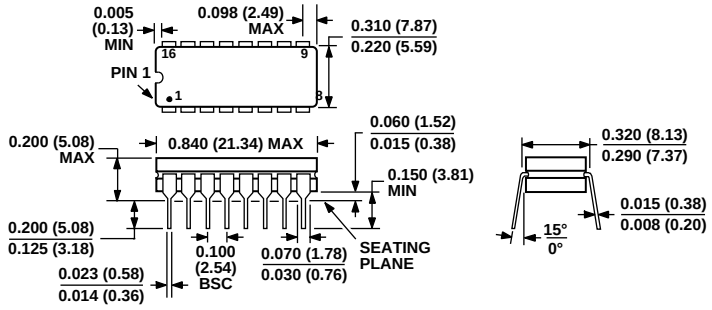


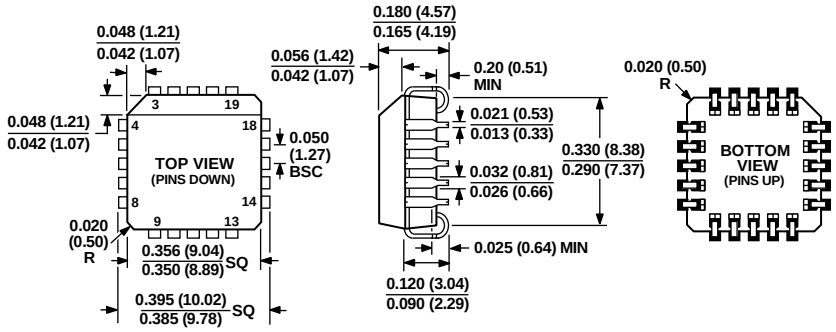
Figure 38. Bridge Transducer Interface

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 39. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-047AA
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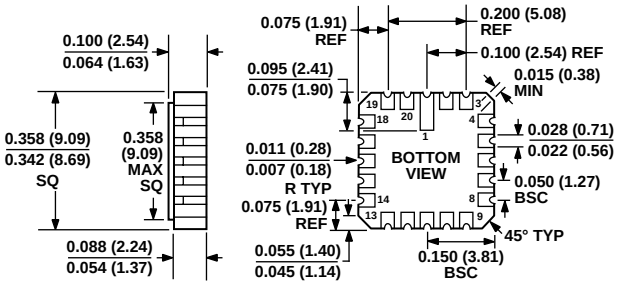
Figure 40. 20-Lead Plastic Leaded Chip Carrier [PLCC]
(P-20A)
Dimensions shown in inches and (mm)



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(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 41. 20-Terminal Leadless Chip Carrier [LCC]
(E-20A)
Dimensions shown in inches and (mm)

ORDERING GUIDE

Model	Gain Drift, 100 kHz	1 MHz Linearity (%)	Specified Temperature Range	Package Options [1]
AD652JP	50 ppm/°C max	0.02 max	0°C to +70°C	PLCC (P-20A)
AD652JP-REEL	50 ppm/°C max	0.02 max	0°C to +70°C	PLCC (P-20A)
AD652JP-REEL7	50 ppm/°C max	0.02 max	0°C to +70°C	PLCC (P-20A)
AD652KP	25 ppm/°C max	0.005 max	0°C to +70°C	PLCC (P-20A)
AD652KP-REEL	25 ppm/°C max	0.005 max	0°C to +70°C	PLCC (P-20A)
AD652AQ[2]	50 ppm/°C max	0.02 max	−40°C to +85°C	CERDIP (Q-16)
AD652BQ[2]	25 ppm/°C max	0.005 max	−40°C to +85°C	CERDIP (Q-16)
AD652SE/883B[2]	50 ppm/°C max	0.02 max	−55°C to +125°C	LCC (E-20A)
AD652SQ[2]	50 ppm/°C max	0.02 max	−55°C to +125°C	CERDIP (Q-16)
AD652SQ/883B[2]	50 ppm/°C max	0.02 max	−55°C to +125°C	CERDIP (Q-16)

[1] P = Plastic Leaded Chip Carrier; Q = CERDIP, E = Leadless Chip Carrier.
[2] For details on grade and package offerings screened in accordance with MILSTD-883, refer to the Analog Devices Military Products Databook or current AD652/883 data sheet.

NOTES

NOTES

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