THE DATASHEET OF

TPS54386PWPRG4

TPS5438x Dual 3-A Non-Synchronous Converters With Integrated High-Side MOSFET

1 Features

- 4.5-V to 28-V Input Range
- Output Voltage Range 0.8 V to 90% of Input Voltage
- Output Current Up to 3 A
- Two Fixed Switching Frequency Versions:
  - TPS54383: 300 kHz
  - TPS54386: 600 kHz
- Three Selectable Levels of Overcurrent Protection (Output 2)
- 0.8-V 1.5% Voltage Reference
- 2.1-ms Internal Soft-Start
- Dual PWM Outputs 180° Out-of-Phase
- Ratiometric or Sequential Startup Modes Selectable by a Single Pin
- 85-mΩ Internal High-Side MOSFETs
- Current Mode Control
- Internal Compensation (See Page 16)
- Pulse-by-Pulse Overcurrent Protection
- Thermal Shutdown Protection at +148°C
- 14-Pin PowerPAD™ HTSSOP package

2 Applications

- Set Top Box
- Digital TV
- Power for DSP
- Consumer Electronics

3 Description

The TPS54383 and TPS54386 are dual output, non-synchronous buck converters capable of supporting 3-A output applications that operate from a 4.5-V to 28-V input supply voltage, and require output voltages between 0.8 V and 90% of the input voltage.

With an internally-determined operating frequency, soft-start time, and control loop compensation, these converters provide many features with a minimum of external components. Channel 1 overcurrent protection is set at 4.5 A, while Channel 2 overcurrent protection level is selected by connecting a pin to ground, to BP, or left floating. The setting levels are used to allow for scaling of external components for applications that do not need the full load capability of both outputs.

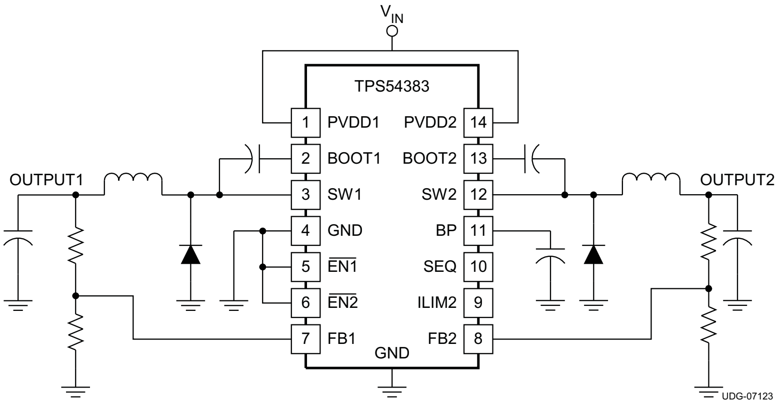
The outputs may be enabled independently, or may be configured to allow either ratio-metric or sequential startup sequencing. Additionally, the two outputs may be powered from different sources.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54383	HTSSOP (14)	4.40 mm × 5.00 mm
TPS54386		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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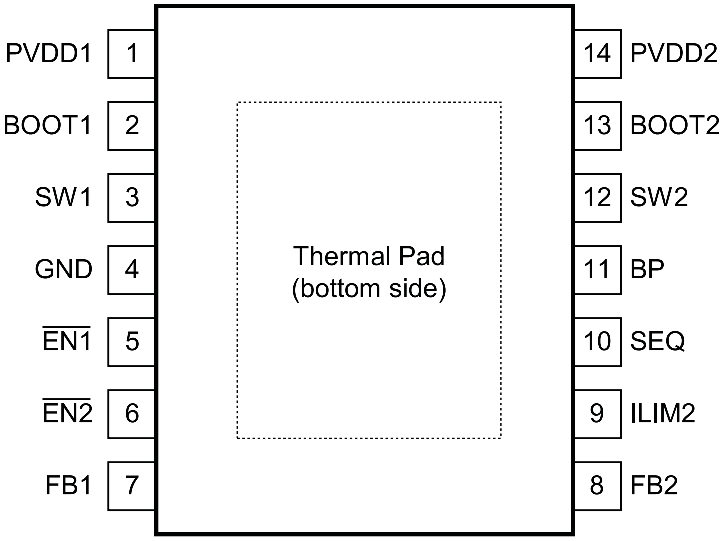
5 Revision History

Changes from Revision B (October 2007) to Revision C	**Page**
• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1

6 Pin Configuration and Functions

PWP Package
14-Pin HTSSOP
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT1	2	I	Input supply to the high side gate driver for Output 1. Connect a 22-nF to 82-nF capacitor from this pin to SW1. This capacitor is charged from the BP pin voltage through an internal switch. The switch is turned ON during the OFF time of the converter. To slow down the turn ON of the internal FET, a small resistor (1 Ω to 3 Ω) may be placed in series with the bootstrap capacitor.
BOOT2	13	I	Input supply to the high side gate driver for Output 2. Connect a 22-nF to 82-nF capacitor from this pin to SW2. This capacitor is charged from the BP pin voltage through an internal switch. The switch is turned ON during the OFF time of the converter. To slow down the turn ON of the internal FET, a small resistor (1 Ω to 3 Ω) may be placed in series with the bootstrap capacitor.
BP	11	-	Regulated voltage to charge the bootstrap capacitors. Bypass this pin to GND with a low ESR (4.7-µF to 10-µF X7R or X5R) ceramic capacitor.
$\overline{\text{EN1}}$	5	I	Active low enable input for Output 1. If the voltage on this pin is greater than 1.55 V, Output 1 is disabled (high-side switch is OFF). A voltage of less than 0.9 V enables Output 1 and allows soft-start of Output 1 to begin. An internal current source drives this pin to PVDD2 if left floating. Connect this pin to GND for "always ON" operation.
$\overline{\text{EN2}}$	6	I	Active low enable input for Output 2. If the voltage on this pin is greater than 1.55 V, Output 2 is disabled (high-side switch is OFF). A voltage of less than 0.9 V enables Output 2 and allows soft-start of Output 2 to begin. An internal current source drives this pin to PVDD2 if left floating. Connect this pin to GND for "always ON" operation.
FB1	7	I	Voltage feedback pin for Output 1. The internal transconductance error amplifier adjusts the PWM for Output 1 to regulate the voltage at this pin to the internal 0.8-V reference. A series resistor divider from Output 1 to ground, with the center connection tied to this pin, determines the value of the regulated output voltage. Compensation for the feedback loop is provided internally to the device. See *Feedback Loop and Inductor-Capacitor (L-C) Filter Selection* section for further information.
FB2	8	I	Voltage feedback pin for Output 2. The internal transconductance error amplifier adjusts the PWM for Output 2 to regulate the voltage at this pin to the internal 0.8-V reference. A series resistor divider from Output 2 to ground, with the center connection tied to this pin, determines the value of the regulated Output voltage. Compensation for the feedback loop is provided internally to the device. See *Feedback Loop and Inductor-Capacitor (L-C) Filter Selection* section for further information.
GND	4	-	Ground pin for the device. Connect directly to Thermal Pad.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	**NO.**		
ILIM2	9	I	Current limit adjust pin for Output 2 only. This function is intended to allow a user with asymmetrical load currents (Output 1 load current much greater than Output 2 load current) to optimize component scaling of the lower current output while maintaining proper component derating in a overcurrent fault condition. The discrete levels are available as shown in Table 2. Note: An internal 2-resistor divider (150-kΩ each) connects BP to ILIM2 and to GND.
PVDD1	1	I	Power input to the Output 1 high side MOSFET only. This pin should be locally bypassed to GND with a low ESR ceramic capacitor of 10-µF or greater.
PVDD2	14	I	The PVDD2 pin provides power to the device control circuitry, provides the pull-up for the $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ pins and provides power to the Output 2 high-side MOSFET. This pin should be locally bypassed to GND with a low ESR ceramic capacitor of 10-µF or greater. The UVLO function monitors PVDD2 and enables the device when PVDD2 is greater than 4.1 V.
SEQ	10	I	This pin configures the output startup mode. If the SEQ pin is connected to BP, then when Output 2 is enabled, Output 1 is allowed to start after Output 2 has reached regulation; that is, sequential startup where Output 1 is slave to Output 2. If $\overline{\text{EN2}}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present. For this sequence configuration, tie $\overline{\text{EN1}}$ to ground. If the SEQ pin is connected to GND, then when Output 1 is enabled, Output 2 is allowed to start after Output 1 has reached regulation; that is, sequential startup where Output 2 is slave to Output 1. If $\overline{\text{EN1}}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present. For this sequence configuration, tie $\overline{\text{EN2}}$ to ground. If left floating, Output 1 and Output 2 start ratio-metrically when both outputs are enabled at the same time. They will soft-start at a rate determined by their final output voltage and enter regulation at the same time. If the $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ pins are allowed to operate independently, then the two outputs also operate independently NOTE: An internal two resistor (150-kΩ each) divider connects BP to SEQ and to GND. See the *Sequence States* table.
SW1	3	O	Source (switching) output for Output 1 PWM. A snubber is recommended to reduce ringing on this node. See *SW Node Ringing* for further information.
SW2	12	O	Source (switching) output for Output 2 PWM. A snubber is recommended to reduce ringing on this node. See *SW Node Ringing* for further information.
Thermal Pad	—	—	This pad must be tied externally to a ground plane and the GND pin.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage range	PVDD1, PVDD2, $\overline{EN1}$, $\overline{EN2}$		30	V
	BOOT1, BOOT2		V_{SW}+ 7	
	SW1, SW2	–2	30	
	SW1, SW2 transient (< 50ns)	–3	31	
	BP		6.5	
	SEQ, ILIM2	–0.3	6.5	
	FB1, FB2	–0.3	3	
	SW1, SW2 output current		7	A
	BP load current		35	mA
T_J	Operating temperature	–40	+150	°C
	Soldering temperature		+260	
T_{stg}	Storage temperature	–55	165	°C

(1) Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{PVDD2}	Input voltage		4.5	28	V
T_J	Operating junction temperature		–40	+125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS54383 TPS54386	UNIT
		HTSSOP	
		14 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	48.6	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	29.4	
$R_{θJB}$	Junction-to-board thermal resistance	25.1	
$ψ_{JT}$	Junction-to-top characterization parameter	0.9	
$ψ_{JB}$	Junction-to-board characterization parameter	24.9	
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

–40°C ≤ T_J ≤ +125°C, $V_{PVDD1} = V_{PVDD2} = 12$ V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (PVDD)							
V_{PVDD1}	Input voltage range			4.5		28	V
V_{PVDD2}							
IDD_{SDN}	Shutdown		$V_{\overline{EN1}} = V_{\overline{EN2}} = V_{PVDD2}$		70	150	μA
IDD_Q	Quiescent, non-switching		$V_{FB} = 0.9$ V, Outputs off		1.8	3.0	mA
IDD_{SW}	Quiescent, while-switching		SW node unloaded; Measured as BP sink current		5		
V_{UVLO}	Minimum turn-on voltage		PVDD2 only	3.8	4.1	4.4	V
$V_{UVLO(hys)}$	Hysteresis				400		mV
t_{START} (1) (2)	Time from startup to softstart begin		$C_{BP} = 10$ μF, $\overline{EN1}$ and $\overline{EN2}$ go low simultaneously		2		ms
ENABLE ($\overline{EN}$)							
$V_{\overline{EN1}}$	Enable threshold			0.9	1.2	1.5	V
$V_{\overline{EN2}}$							
	Hysteresis				50		mV
$I_{\overline{EN1}}$	Enable pull-up current		$V_{\overline{EN1}} = V_{\overline{EN2}} = 0$ V		6	12	μA
$I_{\overline{EN2}}$							
$t_{\overline{EN}}$ (1)	Time from enable to soft-start begin		Other EN pin = GND		10		μs
BP REGULATOR (BP)							
BP	Regulator voltage		8 V < P_{VDD2} < 28 V	5	5.25	5.6	V
BP_{LDO}	Dropout voltage		$P_{VDD2} = 4.5$ V; switching, no external load on BP		400		mV
I_{BP} (1)	Regulator external load					2	mA
I_{BPS}	Regulator short circuit		4.5 V < P_{VDD2} < 28 V	10	20	30	
OSCILLATOR							
f_{SW}	Switching frequency	TPS54383		255	310	375	kHz
		TPS54386		510	630	750	
t_{DEAD} (1)	Clock dead time				140		ns
ERROR AMPLIFIER (EA) and VOLTAGE REFERENCE (REF)							
V_{FB1}	Feedback input voltage		0°C < T_J < +85°C	788	800	812	mV
V_{FB2}			–40°C < T_J < +125°C	786		812	
I_{FB1}	Feedback input bias current				3	50	nA
I_{FB2}							
g_M1 (1)	Transconductance				30		μS
g_M2 (1)							
SOFT-START (SS)							
T_{SS1}	Soft-start time			1.5	2.1	2.7	ms
T_{SS2}							
OVERCURRENT PROTECTION							
I_{CL1}	Current limit channel 1			3.6	4.5	5.6	A
I_{CL2}	Current limit channel 2		$V_{ILIM2} = V_{BP}$	3.6	4.5	5.6	
			V_{ILIM2} = (floating)	2.4	3.0	3.6	
			V_{ILIM2} = GND	1.15	1.50	1.75	
V_{UV1}	Low-level output threshold to declare a fault		Measured at feedback pin.		670		mV
V_{UV2}							
T_{HICCUP} (1)	Hiccup timeout				10		ms
$t_{ON1(oc)}$ (1)	Minimum overcurrent pulse width				90	150	ns
$t_{ON2(oc)}$ (1)							

(1) Ensured by design. Not production tested.

(2) When both outputs are started simultaneously, a 20-mA current source charges the BP capacitor. Faster times are possible with a lower BP capacitor value. More information can be found in the *Input UVLO and Startup* section.

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ +125°C, $V_{PVDD1} = V_{PVDD2}$ = 12 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOTSTRAP							
R_{BOOT1} R_{BOOT2}	Bootstrap switch resistance		From BP to BOOT1 or BP to BOOT2, I_{EXT} = 50 mA		18		Ω
OUTPUT STAGE (Channel 1 and Channel 2)							
$R_{DS(on)}$ (1)	MOSFET on resistance plus bond wire resistance		T_J = +25°C, V_{PVDD2} = 8 V		85		mΩ
			–40°C < T_J < +125°C, V_{PVDD2} = 8 V		85	165	
$t_{ON(min)}$ (1)	Minimum controllable pulse width		I_{SWx} peak current > 1 A (3)		100	200	ns
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0.9 V			0	%
D_{MAX}	Maximum Duty Cycle	TPS54383	f_{SW} = 300 kHz	90	95		%
		TPS54386	f_{SW} = 600 kHz	85	90		%
I_{SW}	Switching node leakage current (sourcing)		Outputs OFF		2	12	µA
THERMAL SHUTDOWN							
T_{SD} (1)	Shutdown temperature				148		°C
$T_{SD(hys)}$ (1)	Hysteresis				20		

(3) See Figure 14 for I_{SWx} peak current <1 A.

7.6 Typical Characteristics

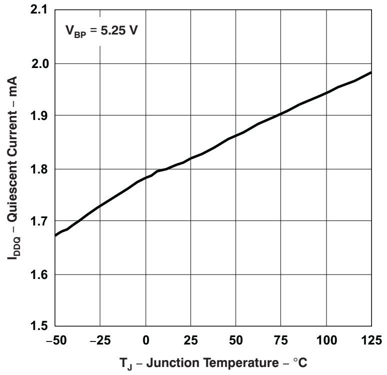


Figure 1. Quiescent Current (Non-Switching) vs Junction Temperature

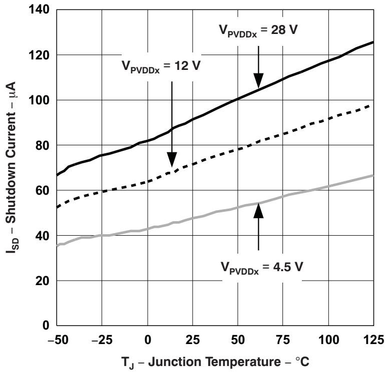


Figure 2. Shutdown Current vs Junction Temperature

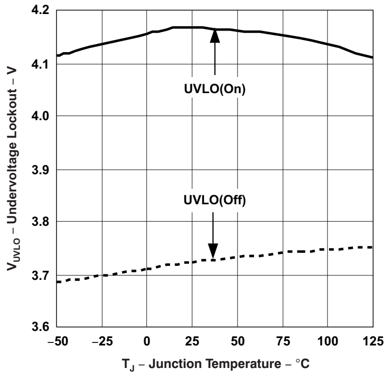


Figure 3. Undervoltage Lockout Threshold vs Junction Temperature

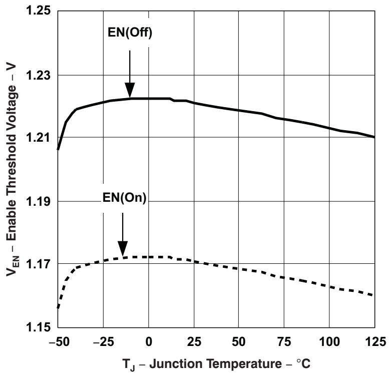


Figure 4. Enable Thresholds vs Junction Temperature

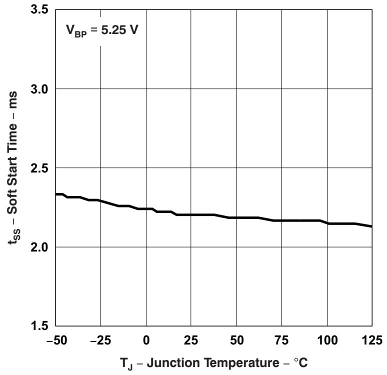


Figure 5. Soft-Start Time vs Junction Temperature

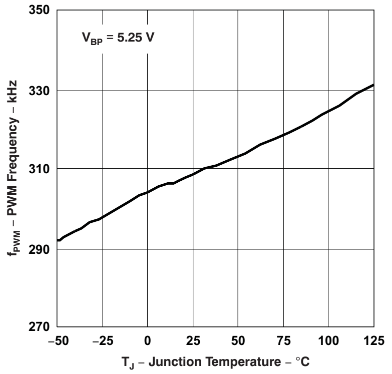


Figure 6. Switching Frequency (300 kHz) vs Junction Temperature

Typical Characteristics (continued)

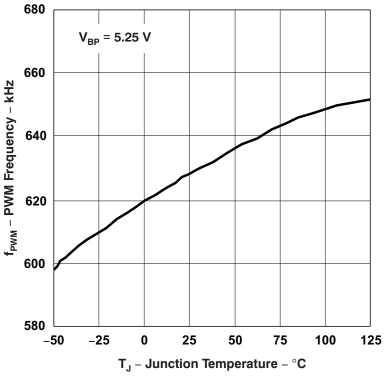


Figure 7. Switching Frequency (600 kHz) vs Junction Temperature

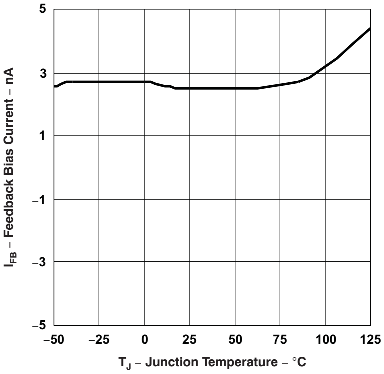


Figure 8. Feedback Bias Current vs Junction Temperature

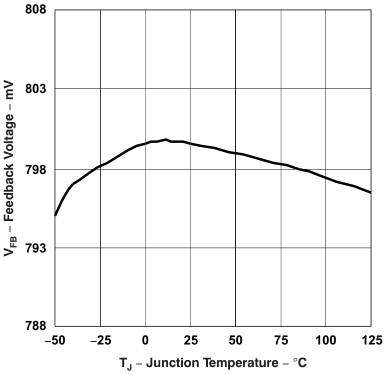


Figure 9. Feedback Voltage vs Junction Temperature

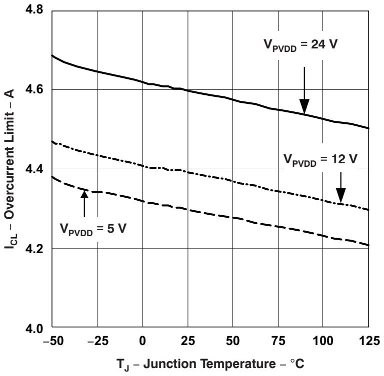


Figure 10. Overcurrent Limit (CH1, CH2 High Level) vs Junction Temperature

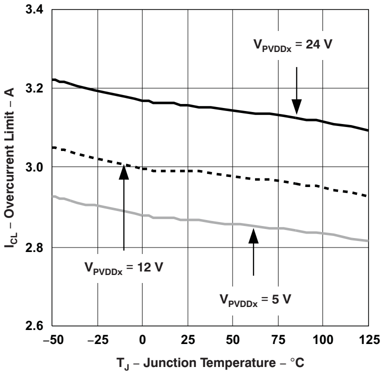


Figure 11. Overcurrent Limit (CH2 Mid Level) vs Junction Temperature

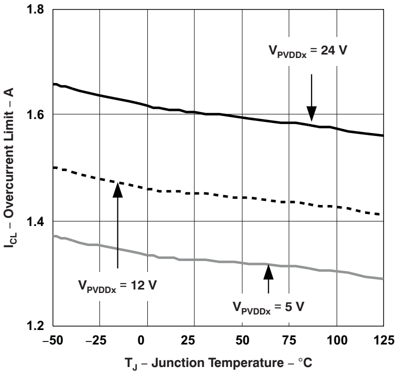


Figure 12. Overcurrent Limit (CH2 Low Level) vs Junction Temperature

Typical Characteristics (continued)

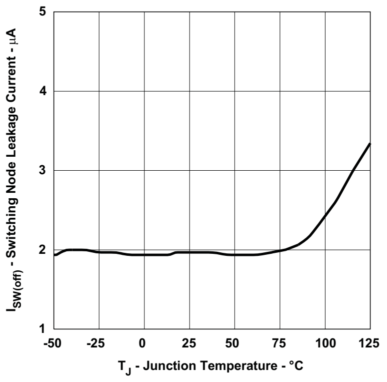


Figure 13. Switching Node Leakage Current vs Junction Temperature

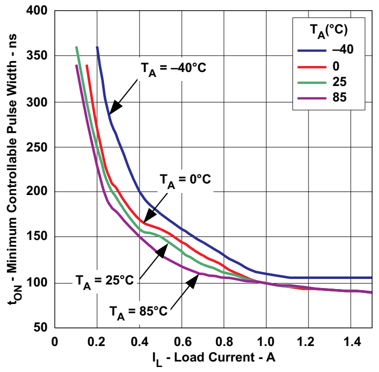


Figure 14. Minumum Controllable Pulse Width vs Load Current

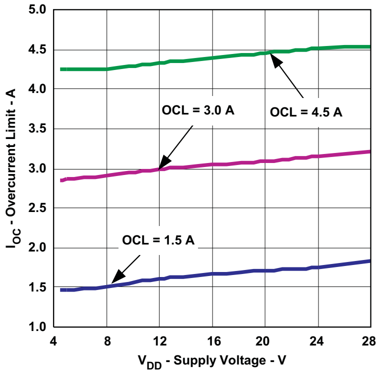


Figure 15. Overcurrent Limit vs Supply Voltage

8 Detailed Description

8.1 Overview

The TPS54383 and TPS54386 are dual output, non-synchronous step down (buck) converters. Integrated into each PWM channel is an internally-compensated error amplifier, current mode pulse width modulator (PWM), switch MOSFET, internal bootstrap switch for high-side gate drive, and fault protection circuitry. Each channel also contains an EN pin and internal fixed soft-start time. The fault protection circuitry includes cycle-by-cycle current limit, output undervoltage detection, hiccup timeout and thermal shutdown. Channel 1 has a fixed current limit and channel 2 has three selectable overcurrent levels. Common to the two channels is the internal BP voltage regulator, voltage reference, clock oscillator, and output voltage sequencing functions.

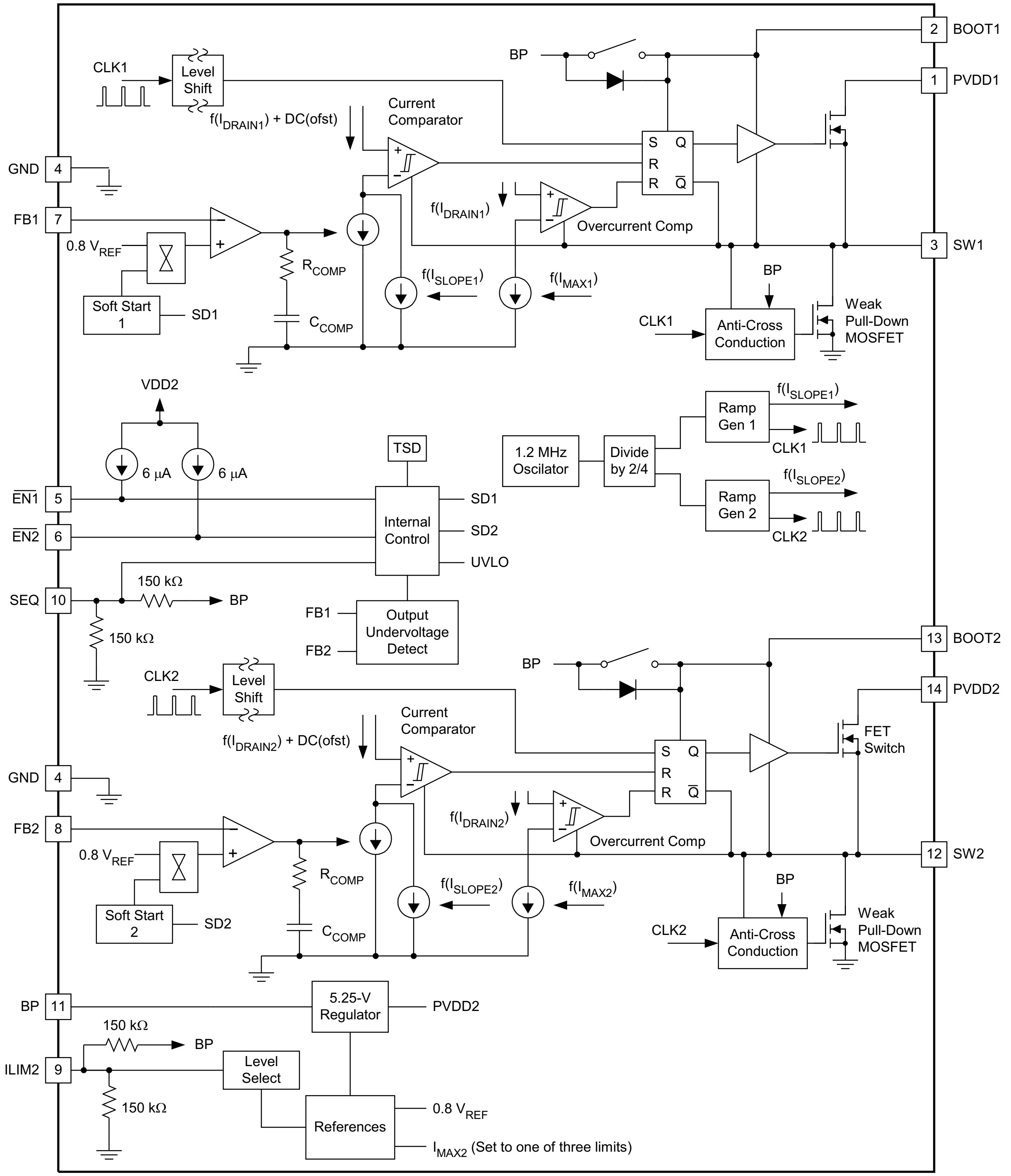
DESIGN HINT

The TPS5438x contains internal slope compensation and loop compensation components; therefore, the external L-C filter must be selected appropriately so that the resulting control loop meets criteria for stability. This approach differs from an externally-compensated controller, where the L-C filter is generally selected first, and the compensation network is found afterwards. (See *Feedback Loop and L-C Filter Selection* section.)

NOTE

Unless otherwise noted, the term *TPS5438x* applies to both the TPS54383 and TPS54386. Also, unless otherwise noted, a label with a lowercase *x* appended implies the term applies to both outputs of the two modulator channels. For example, the term *ENx* implies both EN1 and EN2. Unless otherwise noted, all parametric values given are typical. Refer to the *Electrical Characteristics* for minimum and maximum values. Calculations should be performed with tolerance values taken into consideration.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Voltage Reference

The bandgap cell common to both outputs, trimmed to 800 mV.

8.3.2 Oscillator

The oscillator frequency is internally fixed at two times the SWx node switching frequency. The two outputs are internally configured to operate on alternating switch cycles (that is, 180° out of phase).

8.3.3 Input Undervoltage Lockout (UVLO) and Startup

When the voltage at the PVDD2 pin is less than 4.1 V, a portion of the internal bias circuitry is operational, and all other functions are held OFF. All of the internal MOSFETs are also held OFF. When the PVDD2 voltage rises above the UVLO turn-on threshold, the state of the enable pins determines the remainder of the internal startup sequence. If either output is enabled ($\overline{\text{ENx}}$ pulled low), the BP regulator turns on, charging the BP capacitor with a 20-mA current. When the BP pin is greater than 4 V, PWM is enabled and soft-start begins, depending on the SEQ mode of operation and the $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ settings.

Note that the internal regulator and control circuitry are powered from PVDD2. The voltage on PVDD1 may be higher or lower than PVDD2. (See the *Dual Supply Operation* section.)

8.3.4 Enable and Timed Turn On of the Outputs

Each output has a dedicated (active low) enable pin. If left floating, an internal current source pulls the pin to PVDD2. By grounding, or by pulling the $\overline{\text{ENx}}$ pin to below approximately 1.2 V with an external circuit, the associated output is enabled and soft-start is initiated.

If both enable pins are left in the *high* state, the device operates in a shutdown mode, where the BP regulator is shut down and minimal functions are active. The total standby current from both PVDD pins is approximately 70 μA at 12-V input supply.

An R-C connected to an $\overline{\text{ENx}}$ pin may be used to delay the turn-on of the associated output after power is applied to PVDDx (see Figure 16). After power is applied to PVDD2, the voltage on the $\overline{\text{ENx}}$ pin slowly decays towards ground. Once the voltage decays to approximately 1.2 V, then the output is enabled and the startup sequence begins. If it is desired to enable the outputs of the device immediately upon the application of power to PVDD2, then omit these two components and tie the $\overline{\text{ENx}}$ pin to GND directly.

If an R-C circuit is used to delay the turn-on of the output, the resistor value must be much less than 1.2 V / 6μA or 200 kΩ. A suggested value is 51 kΩ. This resistor value allows the $\overline{\text{ENx}}$ voltage to decay below the 1.2-V threshold while the 6-μA bias current flows.

The capacitor value required to delay the startup time (after the application of PVDD2) is shown in Equation 1.

$$C = \frac{t_{DELAY}}{R \times \ell n\left(\frac{V_{IN} - 2 \times I_{ENx} \times R}{V_{TH} - I_{ENx} \times R}\right)} \text{ farads}$$

where:

- R and C are the timing components
- V_{TH} is the 1.2-V enable threshold voltage
- $I_{\overline{ENx}}$ is the 6 μA enable pin biasing current (1)

Other enable pin functionality is dictated by the state of the SEQ pin. (See the *Output Voltage Sequencing* section.)

Feature Description (continued)

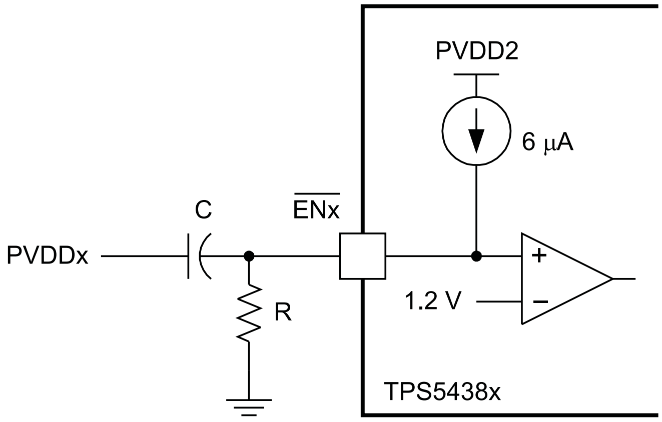


Figure 16. Startup Delay Schematic

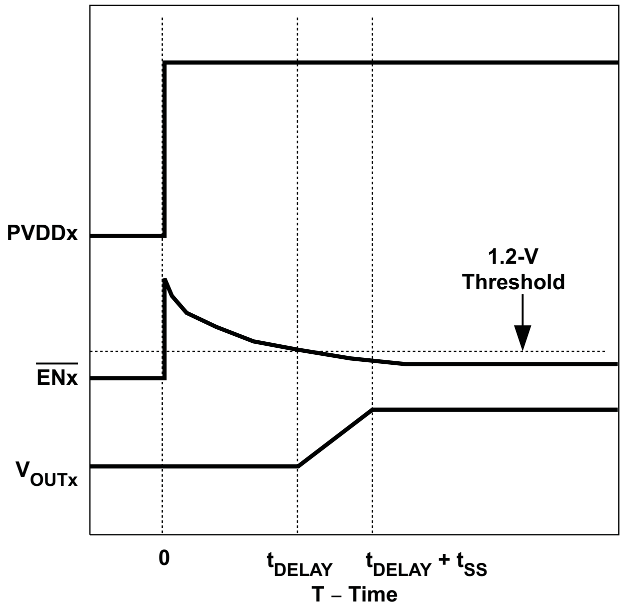


Figure 17. Startup Delay with R-C on Enable

DESIGN HINT

If delayed output voltage startup is not necessary, simply connect $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ to GND. This configuration allows the outputs to start immediately on valid application of PVDD2.

If $\overline{\text{ENx}}$ is allowed to go *high* after the Outputx has been in regulation, the upper MOSFET shuts off, and the output decays at a rate determined by the output capacitor and the load. The internal pulldown MOSFET remains in the OFF state. (See the *Bootstrap for N-Channel MOSFET* section.)

8.3.5 Output Voltage Sequencing

The TPS5438x allows single-pin programming of output voltage startup sequencing. During power-on, the state of the SEQ pin is detected. Based on whether the pin is tied to BP, to GND, or left floating, the outputs behave as described in Table 1.

Table 1. Sequence States

SEQ PIN STATE	MODE	$\overline{\text{EN1}}$	$\overline{\text{EN2}}$
BP	Sequential, Output 2 then Output 1	Ignored by the device.when $V_{\overline{EN2}}$ < enable threshold voltage	Active
		Tie $\overline{\text{EN1}}$ to < enable threshold voltage for BP to be active when $V_{\overline{EN2}}$ > enable threshold voltage	
		Tie $\overline{\text{EN1}}$ to > enable threshold voltage for low quiescent current (BP inactive) when $V_{\overline{EN2}}$ > enable threshold voltage	
GND	Sequential, Output 1 then Output 2	Active	Ignored by the device.when $V_{\overline{EN1}}$ < enable threshold voltage
			Tie $\overline{\text{EN2}}$ to < enable threshold voltage for BP to be active when $V_{\overline{EN1}}$ > enable threshold voltage
			Tie $\overline{\text{EN2}}$ to > enable threshold voltage for low quiescent current (BP inactive) when $V_{\overline{EN1}}$ > enable threshold voltage
(floating)	Independent or Ratiometric, Output 1 and Output 2	Active. $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ must be tied together for Ratio-metric startup.	Active. $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ must be tied together for Ratio-metric startup.

If the SEQ pin is connected to BP, then when Output 2 is enabled, Output 1 is allowed to start approximately 400 µs after Output 2 has reached regulation; that is, sequential startup where Output 1 is slave to Output 2. If $\overline{\text{EN2}}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present.

If the SEQ pin is connected to GND, then when Output 1 is enabled, Output 2 is allowed to start approximately 400 µs after Output 1 has reached regulation; that is, sequential startup where Output 2 is slave to Output 1. If $\overline{\text{EN1}}$ is allowed to go high after the outputs have been operating, then both outputs are disabled immediately, and the output voltages decay according to the load that is present.

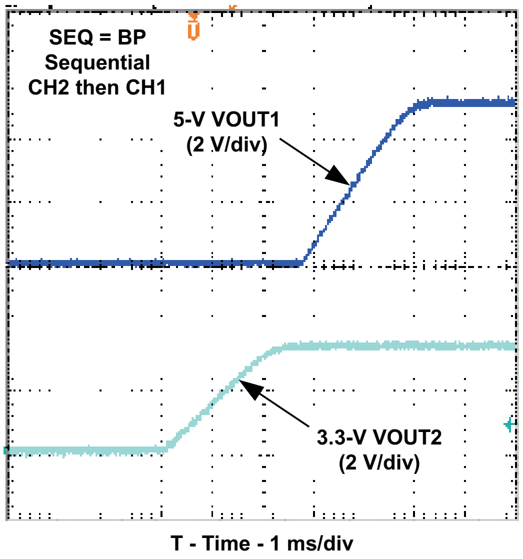


Figure 18. SEQ Pin TIed to BP

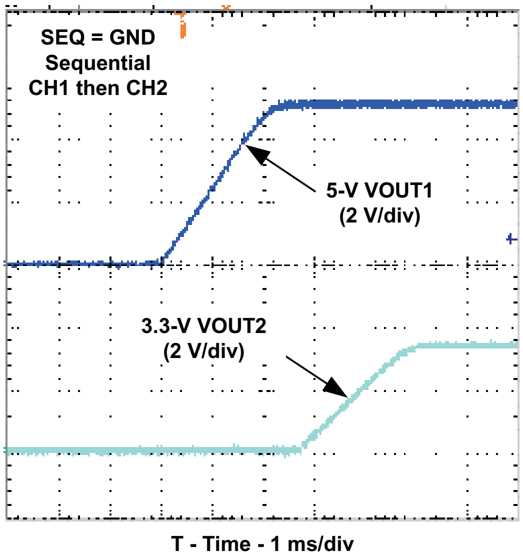


Figure 19. SEQ Pin Tied to GND

NOTE

An R-C network connected to the $\overline{\text{ENx}}$ pin may be used in addition to the SEQ pin in sequential mode to delay the startup of the first output voltage. This approach may be necessary in systems with a large number of output voltages and elaborate voltage sequencing requirements. See *Enable and Timed Turn On of the Outputs.*

If the SEQ pin is left floating, Output 1 and Output 2 each start ratiometrically when both outputs are enabled at the same time. Output 1 and Output 2 soft-start at a rate that is determined by the respective final output voltages and enter regulation at the same time. If the $\overline{\text{EN1}}$ and $\overline{\text{EN2}}$ pins are allowed to operate independently, then the two outputs also operate independently.

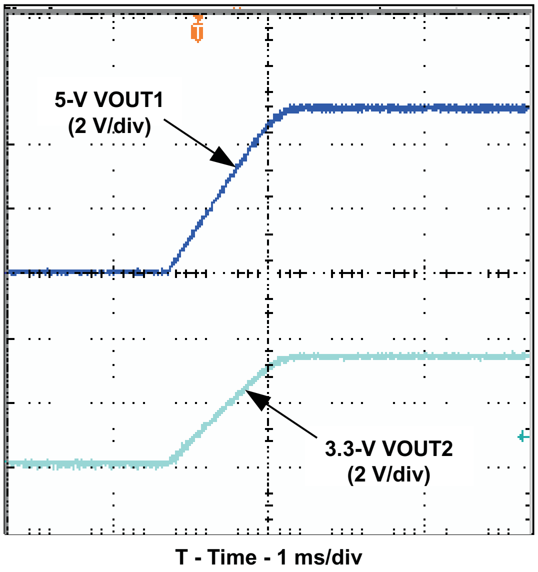


Figure 20. SEQ Pin Floating

8.3.6 Soft-Start

Each output has a dedicated soft-start circuit. The soft-start voltage is an internal digital reference ramp to one of two noninverting inputs of the error amplifier. The other input is the (internal) precision 0.8-V reference. The total ramp time for the FB voltage to charge from 0 V to 0.8 V is about 2.1 ms. During a soft-start interval, the TPS5438x output slowly increases the voltage to the noninverting input of the error amplifier. In this way, the output voltage ramps up slowly until the voltage on the noninverting input to the error amplifier reaches the internal 0.8 V reference voltage. At that time, the voltage at the noninverting input to the error amplifier remains at the reference voltage.

NOTE

To avoid a disturbance in the output voltage during the stepping of the digital soft -tart, a minimum output capacitance of 50µF is recommended. See *Feedback Loop and Inductor-Capacitor (L-C) Filter Selection* Once the filter and compensation components have been established, laboratory measurements of the physical design should be performed to confirm converter stability.

During the soft-start interval, pulse-by-pulse current limiting is in effect. If an overcurrent pulse is detected, six PWM pulses are skipped to allow the inductor current to decay before another PWM pulse is applied. (See the *Output Overload Protection* section.) There is no pulse skipping if a current limit pulse is not detected.

DESIGN HINT

If the rate of rise of the input voltage (PVDDx) is such that the input voltage is too low to support the desired regulation voltage by the time Soft-Start has completed, then the output UV circuit may trip and cause a *hiccup* in the output voltage. In this case, use a timed delay startup from the ENx pin to delay the startup of the output until the PVDDx voltage has the capability of supporting the desired regulation voltage. See *Operating Near Maximum Duty Cycle* and *Maximum Output Capacitance* for related information.

8.3.7 Output Voltage Regulation

Each output has a dedicated feedback loop comprised of a voltage setting divider, an error amplifier, a pulse width modulator, and a switching MOSFET. The regulation output voltage is determined by a resistor divider connecting the output node, the FBx pin, and GND (see Figure 21). Assuming the value of the upper voltage setting divider is known, the value of the lower divider resistor for a desired output voltage is calculated by Equation 2.

$$R2 = R1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}} \right) \tag{2}$$

where

- V_{REF} is the internal 0.8-V reference voltage

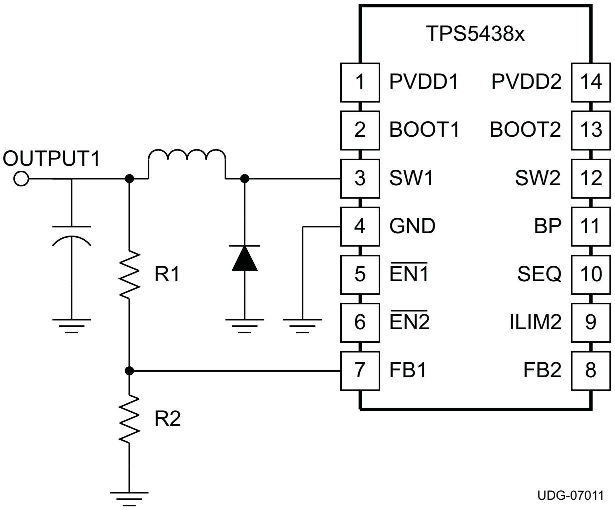


Figure 21. Feedback Network for Channel 1

DESIGN HINT

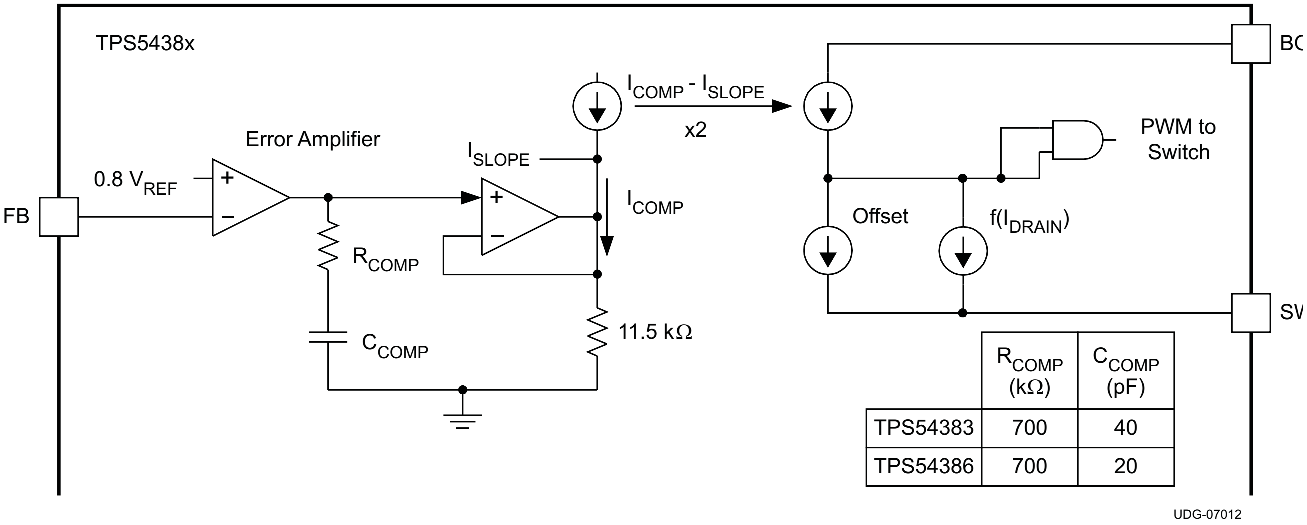
There is a leakage current of up to 12 µA out of the SW pin when a single output of the TPS5438x is disabled. Keeping the series impedance of R1 + R2 less than 50 kΩ prevents the output from floating above the reference voltage while the controller output is in the OFF state.

8.3.8 Feedback Loop and Inductor-Capacitor (L-C) Filter Selection

In the feedback signal path, the output voltage setting divider is followed by an internal g_M-type error amplifier with a typical transconductance of 30 µS. An internal series connected R-C circuit from the g_M amplifier output to ground serves as the compensation network for the converter. The signal from the error amplifier output is then buffered and combined with a slope compensation signal before it is mirrored to be referenced to the SW node. Here, it is compared with the current feedback signal to create a pulse-width-modulated (PWM) signal-fed to drive the upper MOSFET switch. A simplified equivalent circuit of the signal control path is depicted in Figure 22.

NOTE

Noise coupling from the SWx node to internal circuitry of BOOTx may impact narrow pulse width operation, especially at load currents less than 1 A. See *SW Node Ringing* for further information on reducing noise on the SWx node.



	R_{COMP} (kΩ)	C_{COMP} (pF)
TPS54383	700	40
TPS54386	700	20

Figure 22. Feedback Loop Equivalent Circuit

A more conventional small signal equivalent block diagram is shown in Figure 23. Here, the full closed loop signal path is shown. Because the TPS5438x contains internal slope compensation and loop compensation components, the external L-C filter must be selected appropriately so that the resulting control loop meets criteria for stability. This approach differs from an externally-compensated controller, where the L-C filter is generally selected first, and the compensation network is found afterwards. To find the appropriate L and C filter combination, the Output-to-Vc signal path plots (see the next section) of gain and phase are used along with other design criterial to aid in finding the combinations that best results in a stable feedback loop.

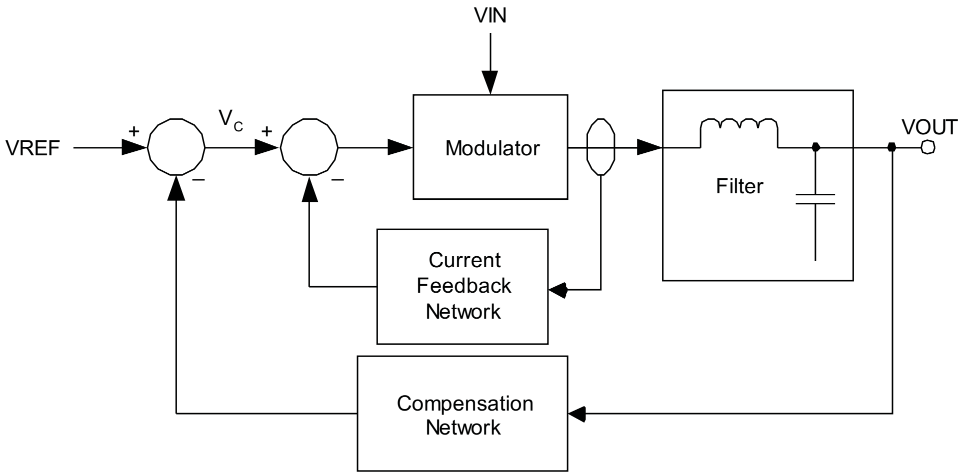


Figure 23. Small Signal Equivalent Block Diagram

8.3.9 Inductor-Capacitor (L-C) Selection

The following figures plot the TPS5438x Output-to-Vc gain and phase versus frequency for various duty cycles (10%, 30%, 50%, 70%, 90%) at three (200 mA, 400 mA, 600 mA) peak-to-peak ripple current levels. The loop response curve selected to compensate the loop is based on the duty cycle of the application and the ripple current in the inductor. Once the curve has been selected and the inductor value has been calculated, the output capacitor is found by calculating the L-C resonant frequency required to compensate the feedback loop. A brief example follows the curves.

Note that the internal error amplifier compensation is optimized for output capacitors with an ESR zero frequency between 20 kHz and 60 kHz. See the following sections for further details.

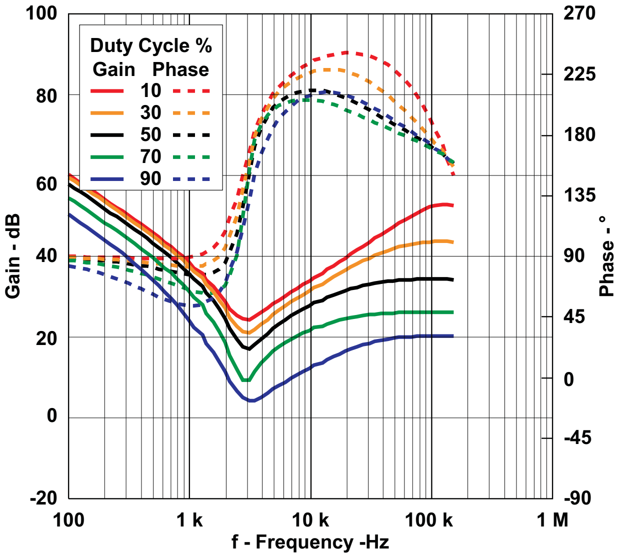


Figure 24. Gain and Phase vs Frequency. TPS54383 at 200-mApp Ripple Current

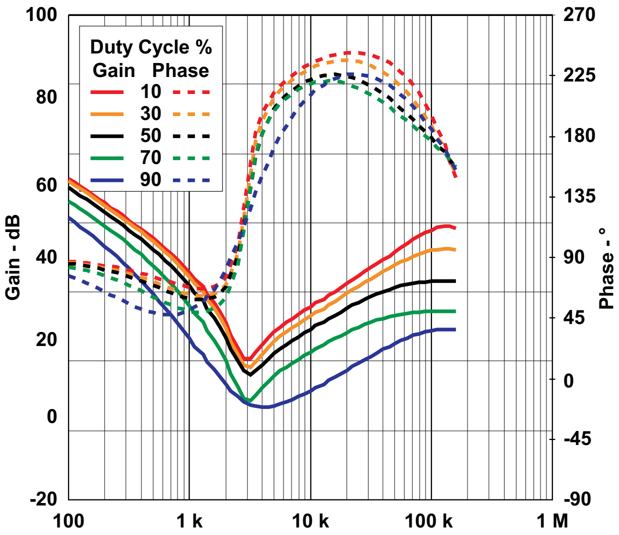


Figure 25. Gain and Phase vs Frequency. TPS54383 at 400-mApp Ripple Current

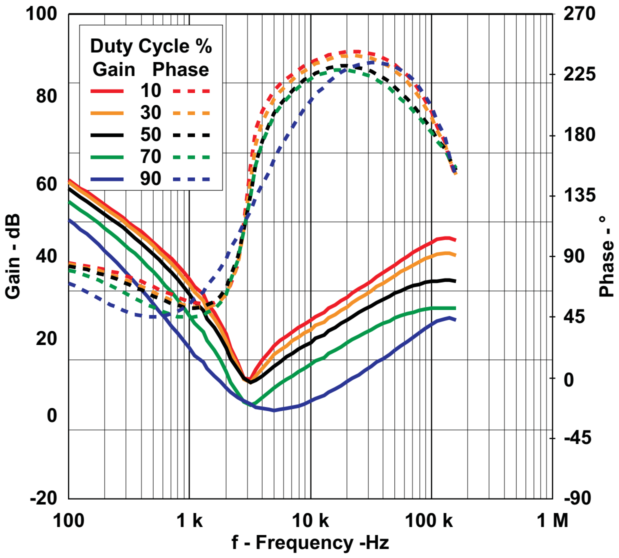


Figure 26. Gain and Phase vs Frequency. TPS54383 at 600-mApp Ripple Current

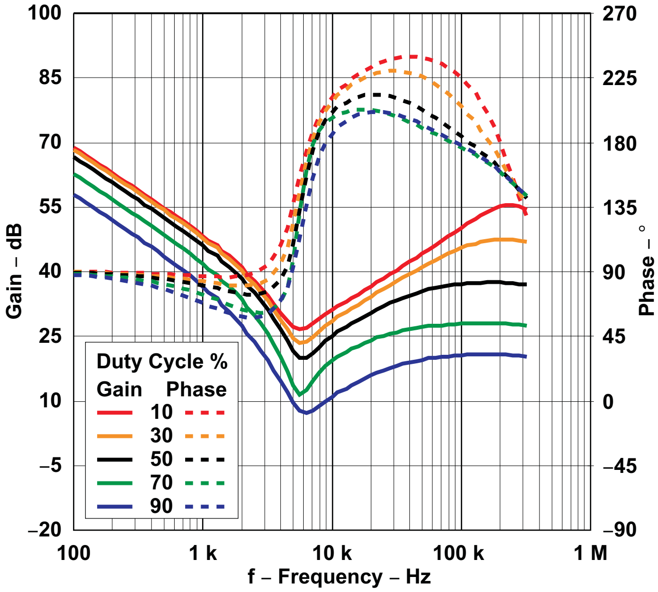


Figure 27. Gain and Phase vs Frequency. TPS54386 at 200-mApp Ripple Current

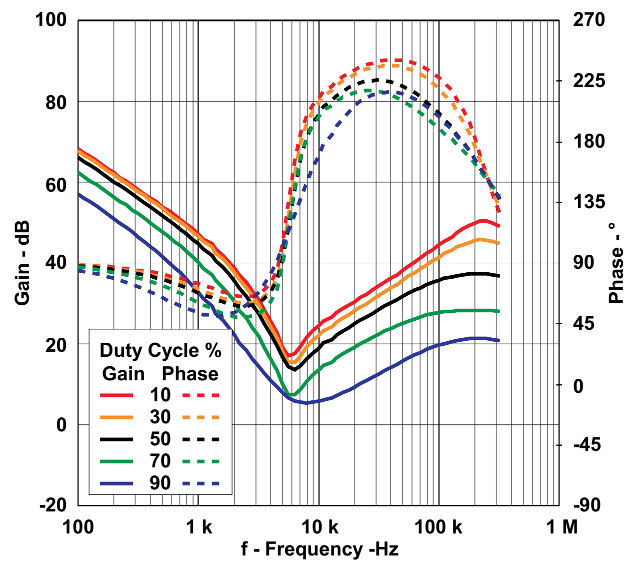


Figure 28. Gain and Phase vs Frequency. TPS54386 at 400-mApp Ripple Current

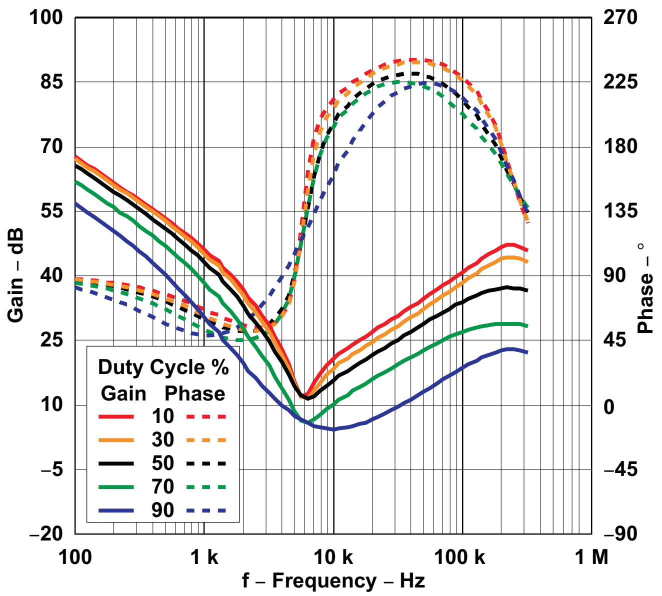


Figure 29. Gain and Phase vs Frequency. TPS54386 at 600-mApp Ripple Current

8.3.10 Maximum Output Capacitance

With internal pulse-by-pulse current limiting and a fixed soft-start time, there is a maximum output capacitance which may be used before startup problems begin to occur. If the output capacitance is large enough so that the device enters a current limit protection mode during startup, then there is a possibility that the output will never reach regulation. Instead, the TPS5438x simply shuts down and attempts a restart as if the output were short-circuited to ground. The maximum output capacitance (including bypass capacitance distributed at the load) is given by Equation 3:

$$C_{OUTmax} = \frac{t_{SS}}{V_{REF}}\left[I_{CLx} - V_{REF}\left(1+\frac{R1}{R2}\right)\left(1 - \frac{V_{REF}\left(1+\frac{R1}{R2}\right)\times T_S}{2\times V_{IN}\times L} + \frac{1}{R_{LOAD}}\right)\right] \qquad (3)$$

8.3.11 Minimum Output Capacitance

Ensure the value of capacitance selected for closed loop stability is compatible with the requirements of *Soft-Start* .

8.3.12 Modifying The Feedback Loop

Within the limits of the internal compensation, there is flexibility in the selection of the inductor and output capacitor values. A smaller inductor increases ripple current, and raises the resonant frequency, thereby incerasing the required amount of output capacitance. A smaller capacitor could also be used, increasing the resonant frequency, and increasing the overall loop bandwidth—perhaps at the expense of adequate phase margin.

The internal compensation of the TPS54x8x is designed for capacitors with an ESR zero frequency between 20kHz and 60kHz. It is possible, with additional feedback compensation components, to use capacitors with higher or lower ESR zero frequencies. For either case, the components C1 and R3 (ref.Figure 30) are added to re-compensate the feedback loop for stability. In this configuration a low frequency pole is followed by a higher frequency zero. The placement of this pole-zero pair is dependent on the type of output capacitor used, and the desired closed loop frequency response.

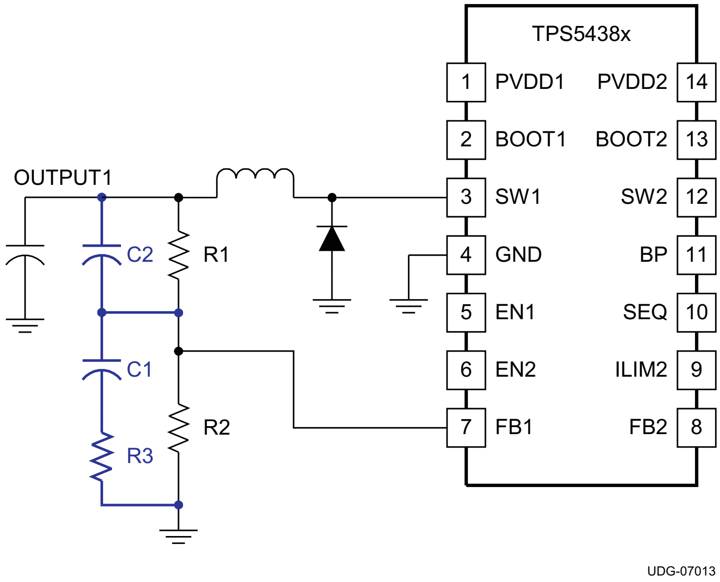


Figure 30. Optional Loop Compensation Components

NOTE

Once the filter and compensation components have been established, laboratory measurements of the physical design should be performed to confirm converter stability.

8.3.12.1 Using High-ESR Output Capacitors

If a high-ESR capacitor is used in the output filter, a zero appears in the loop response that could lead to instability. To compensate, a small R-C series connected network is placed in parallel with the lower voltage setting divider resistor (see Figure 30). The values of the components are determined such that a pole is placed at the same frequency as the ESR zero and a new zero is placed at a frequency location conducive to good loop stability.

The value of the resistor is calculated using a ratio of impedances to match the ratio of ESR zero frequency to the desired zero frequency.

$$R3 = \frac{R2}{\left(\left(\frac{f_{ZERO(desired)}}{f_{ESR(zero)}}\right) - 1\right)}$$

where:

- $f_{ESR(zero)}$ is the ESR zero frequency of the output capacitor.
- $f_{ZERO(desired)}$ is the desired frequency of the zero added to the feedback. This frequency should be placed between 20 kHz and 60 kHz to ensure good loop stability. (4)

The value of the capacitor is calculated in Equation 5.

$$C1 = \frac{1}{2\pi \times R_{EQ} \times f_{ESR(zero)}}$$

where:

- R_{EQ} is an equivalent impedance created by the parallel combination of the voltage setting divider resistors (R1 and R2) in series with R3. (5)

$$R_{EQ} = R3 + \frac{1}{\left(\left(\frac{1}{R1}\right) + \left(\frac{1}{R2}\right)\right)} \tag{6}$$

8.3.12.2 Using All Ceramic Output Capacitors

With low ESR ceramic capacitors, there may not be enough phase margin at the crossover frequency. In this case, (see Figure 30) resistor R3 is set equal to 1/2 R2. This lowers the gain by 6 dB, reduce the crossover frequency, and improve phase margin.

The value of C1 is found by determining the frequency to place the low frequency pole. The minimum frequency to place the pole is 1 kHz. Any lower, and the time constant will be too slow and interfere with the internal soft-start (see *Soft-Start*). The upper bound for the pole frequency is determined by the operating frequency of the converter. It is 3 kHz for the TPS54x83, and 6 kHz for the TPS54x86. C1 is then found from Equation 7. Keep component tolerances in mind when selecting the desired pole frequency.

$$C1 = \frac{1}{2\pi \times R_{EQ} \times f_{POLE(desired)}}$$

where:

- $f_{POLE(desired)}$ is the desired pole frequency between 1 kHz and 3 kHz (TPS54x83) or 1 kHz and 6 kHz (TPS54x86).
- R_{EQ} is an equivalent impedance created by the parallel combination of the voltage setting divider resistors (R1 and R2) in series with R3. (7)

$$R_{EQ} = R3 + \frac{1}{\left(\left(\frac{1}{R1}\right) + \left(\frac{1}{R2}\right)\right)} \tag{8}$$

If it is necessary to increase phase margin, place a capacitor in parallel with the upper voltage setting divider resistor (Ref. C2 in Equation 9).

$$C2 = \frac{1}{2\pi \times f_C \times R1} \times \sqrt{1 + \frac{R1}{\left(\frac{(R2 \times R3)}{(R2 + R3)}\right)}}$$

where

- f_C is the unity gain crossover frequency, (approximately 50 kHz for most designs following these guidelines) (9)

8.3.13 Example: TPS54386 Buck Converter Operating at 12-V Input, 3.3-V Output and 400-mA$_{(P-P)}$ Ripple Current

First, the steady state duty cycle is calculated. Assuming the rectifier diode has a voltage drop of 0.5 V, the duty cycle is approximated using Equation 10.

$$\delta = \frac{V_{OUT} + V_{DIODE}}{V_{IN} + V_{DIODE}} = \frac{3.3 + 0.5}{12 + 0.5} = 30\% \tag{10}$$

The filter inductor is then calculated; see Equation 11.

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_L} \times \delta \times T_S = \frac{12 - 3.3}{0.4} \times 0.3 \times \frac{1}{600000} = 10.9\,\mu H \tag{11}$$

A custom-designed inductor may be used for the application, or a standard value close to the calculated value may be used. For this example, a standard 10-µH inductor is used. Using Figure 28, find the 30% duty cycle curve. The 30% duty cycle curve has a down slope from low frequency and rises at approximately 6 kHz. This curve is the resonant frequency that must be compensated. Any frequency wthin an octave of the peak may be used in calculating the capacitor value. In this example, 6 kHz is used.

$$C = \frac{1}{L \times (2 \times \pi \times f_{RES})^2} = \frac{1}{10 \times 10^{-6} \times (2 \times 3.14 \times 6000)^2} = 70\,\mu F \tag{12}$$

A 68-µF capacitor should be used as a bulk capacitor, with up to 10 µF of ceramic bypass capacitance. To ensure the ESR zero does not significantly impact the loop response, the ESR of the bulk capacitor should be placed a decade above the resonant frequency.

$$R_{ESR} < \frac{1}{2 \times \pi \times 10 \times f_{RES} \times C} = \frac{1}{2 \times 3.14 \times 10 \times 6000 \times 68 \times (10)^{-6}} \approx 40\ m\Omega \tag{13}$$

The resulting loop gain and phase are shown in Figure 31. Based on measurement, loop crossover is 45 kHz with a phase margin of 60 degrees.

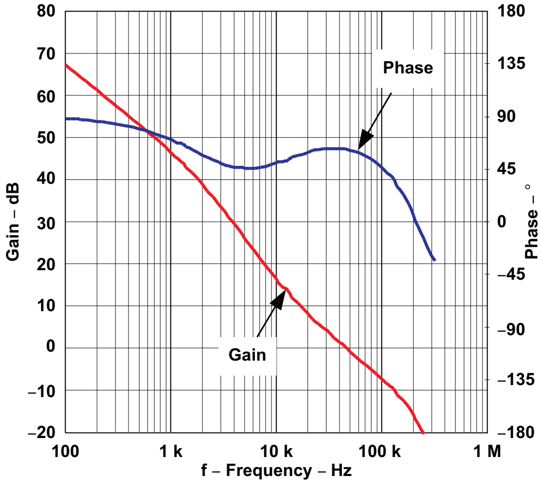


Figure 31. Gain and Phase vs Frequency. Example Loop Result

8.3.14 Bootstrap for the N-Channel MOSFET

A bootstrap circuit provides a voltage source higher than the input voltage and of sufficient energy to fully enhance the switching MOSFET each switching cycle. The PWM duty cycle is limited to a maximum of 90%, allowing an external bootstrap capacitor to charge through an internal synchronous switch (between BP and BOOTx) during every cycle. When the PWM switch is commanded to turn ON, the energy used to drive the MOSFET gate is derived from the voltage on this capacitor.

To allow the bootstrap capacitor to charge each switching cycle, an internal pulldown MOSFET (from SW to GND) is turned ON for approximately 140 ns at the beginning of each switching cycle. In this way, if, during light load operation, there is insufficient energy for the SW node to drive to ground naturally, this MOSFET forces the SW node toward ground and allow the bootstrap capacitor to charge.

Because this is a charge transfer circuit, care must be taken in selecting the value of the bootstrap capacitor. It must be sized such that the energy stored in the capacitor on a per cycle basis is greater than the gate charge requirement of the MOSFET being used.

DESIGN HINT

For the bootstrap capacitor, use a ceramic capacitor with a value between 22 nF and 82 nF.

NOTE

For 5-V input applications, connect PVDDx to BP directly. This connection bypasses the internal control circuit regulator and provides maximum voltage to the gate drive circuitry. In this configuration, shutdown mode IDD_{SDN} will be the same as quiescent IDD_Q.

8.3.15 Light Load Operation

There is no special circuitry for pulse skipping at light loads. The normal characteristic of a nonsynchronous converter is to operate in the *discontinuous conduction mode* (DCM) at an average load current less than one-half of the inductor peak-to-peak ripple current. Note that the amplitude of the ripple current is a function of input voltage, output voltage, inductor value, and operating frequency, as shown in Equation 14.

$$I_{DCM} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times \delta \times T_S \tag{14}$$

Further, during discontinuous mode operation the commanded pulse width may become narrower than the capability of the converter to resolve. To maintain the output voltage within regulation, skipping switching pulses at light load conditions is a natural by-product of that mode. This condition may occur if the output capacitor is charged to a value greater than the output regulation voltage, and there is insufficient load to discharge the capacitor. A by-product of pulse skipping is an increase in the peak-to-peak output ripple voltage.

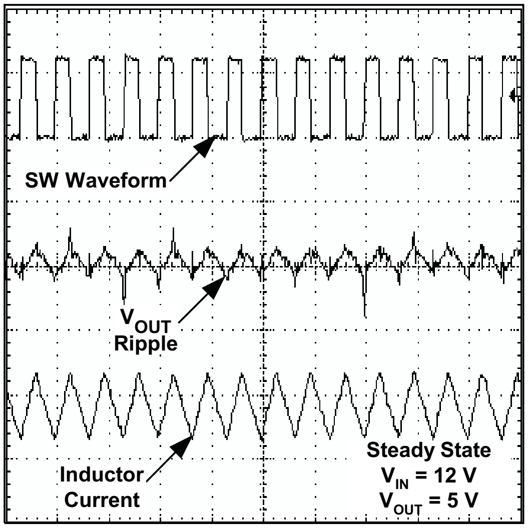


Figure 32. Steady State

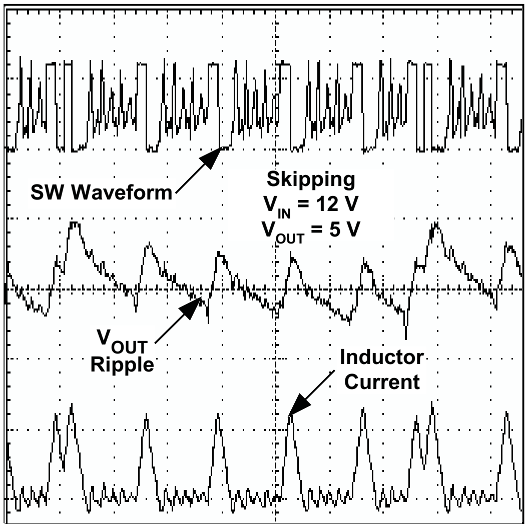


Figure 33. Skipping

DESIGN HINT

If additional output capacitance is required to reduce the output voltage ripple during DCM operation, be sure to recheck *Feedback Loop and Inductor-Capacitor (L-C) Filter Selection* and *Maximum Output Capacitance* sections.

8.3.16 SW Node Ringing

A portion of the control circuitry is referenced to the SW node. To ensure jitter-free operation, it is necessary to decrease the voltage waveform ringing at the SW node to less than 5 volts peak and of a duration of less than 30-ns. In addition to following good printed circuit board (PCB) layout practices, there are a couple of design techniques for reducing ringing and noise.

8.3.16.1 SW Node Snubber

Voltage ringing observable at the SW node is caused by fast switching edges and parasitic inductance and capacitance. If the ringing results in excessive voltage on the SW node, or erratic operation of the converter, an R-C snubber may be used to dampen the ringing and ensure proper operation over the full load range.

DESIGN HINT

A series-connected R-C snubber (C = between 330 pF and 1 nF, R = 10 Ω) connected from SW to GND reduces the ringing on the SW node.

8.3.16.2 Bootstrap Resistor

A small resistor in series with the bootstrap capacitor reduces the turn-on time of the internal MOSFET, thereby reducing the rising edge ringing of the SW node.

DESIGN HINT

A resistor with a value between 1Ω and 3Ω may be placed in series with the bootstrap capacitor to reduce ringing on the SW node.

DESIGN HINT

Placeholders for these components should be placed on the initial prototype PCBs in case they are needed.

8.3.17 Output Overload Protection

In the event of an overcurrent during soft-start on either output (such as starting into an output short), pulse-by-pulse current limiting and PWM frequency division are in effect for that output until the internal soft-start timer ends. At the end of the soft-start time, a UV condition is declared and a fault is declared. During this fault condition, both PWM outputs are disabled and the small pulldown MOSFETs (from SWx to GND) are turned ON. This process ensures that both outputs discharge to GND in the event that overcurrent is on one output while the other is not loaded. The converter then enters a *hiccup* mode timeout before attempting to restart. "Frequency Division" means if an overcurrent pulse is detected, six clock cycles are skipped before a next PWM pulse is initiated, effectively dividing the operating frequency by six and preventing excessive current build up in the inductor.

In the event of an overcurrent on either output after the output reaches regulation, pulse-by-pulse current limit is in effect for that output. In addition, an output undervoltage (UV) comparator monitors the FBx voltage (that follows the output voltage) to declare a fault if the output drops below 85% of regulation. During this fault condition, both PWM outputs are disabled and the small pulldown MOSFETs (from SWx to GND) are turned ON. This design ensures that both outputs discharge to GND, in the event that overcurrent is on one output while the other is not loaded. The converter then enters a *hiccup* mode timeout before attempting to restart.

The overcurrent threshold for Output 1 is set nominally at 4.5 A. The overcurrent level of Output 2 is determined by the state of the ILIM2 pin. The ILIM setting of Output 2 is not latched in place and may be changed during operation of the converter.

Table 2. Current Limit Threshold Adjustment for Output 2

ILIM2 Connection	OCP Threshold for Output 2
BP	4.5 A nominal setting
(floating)	3.0 A nominal setting
GND	1.5 A nominal setting

DESIGN HINT

The OCP threshold refers to the peak current in the internal switch. Be sure to add one-half of the peak inductor ripple current to the dc load current in determining how close the actual operating point is to the OCP threshold

8.3.18 Operating Near Maximum Duty Cycle

If the TPS5438x operates at maximum duty cycle, and if the input voltage is insufficient to support the output voltage (at full load or during a load current transient), then there is a possibility that the output voltage will fall from regulation and trip the output UV comparator. If this should occur, the TPS5438x protection circuitry will declare a fault and enter a shut down-and-restart cycle.

DESIGN HINT

Ensure that under ALL conditions of line and load regulation, there is sufficient duty cycle to maintain output voltage regulation.

To calculate the operating duty cycle, use Equation 15.

$$\delta = \frac{V_{OUT} + V_{DIODE}}{V_{IN} + V_{DIODE}}$$

where

- V_{DIODE} is the voltage drop of the rectifier diode (15)

8.3.19 Dual Supply Operation

It is possible to operate a TPS5438x from two supply voltages. If this application is desired, then the sequencing of the supplies must be such that PVDD2 is above the UVLO voltage before PVDD1 begins to rise. This level requirement ensures that the internal regulator and the control circuitry are in operation before PVDD1 supplies energy to the output. In addition, Output 1 must be held in the disabled state ($\overline{\text{EN1}}$ high) until there is sufficient voltage on PVDD1 to support Output 1 in regulation. (See the *Operating Near Maximum Duty Cycle* section.)

The preferred sequence of events is:

1. PVDD2 rises above the input UVLO voltage
2. PVDD1 rises with Output 1 disabled until PVDD1 rises above level to support Output 1 regulation.

   With these two conditions satisfied, there is no restriction on PVDD2 to be greater than, or less than PVDD1.

DESIGN HINT

An R-C delay on $\overline{\text{EN1}}$ may be used to delay the startup of Output1 for a long enough period of time to ensure that PVDD1 can support Output 1 load.

8.3.20 Cascading Supply Operation

It is possible to source PVDD1 from Output 2 as depicted in Figure 34 and Figure 35. This configuration may be preferred if the input voltage is high, relative to the voltage on Output 1.

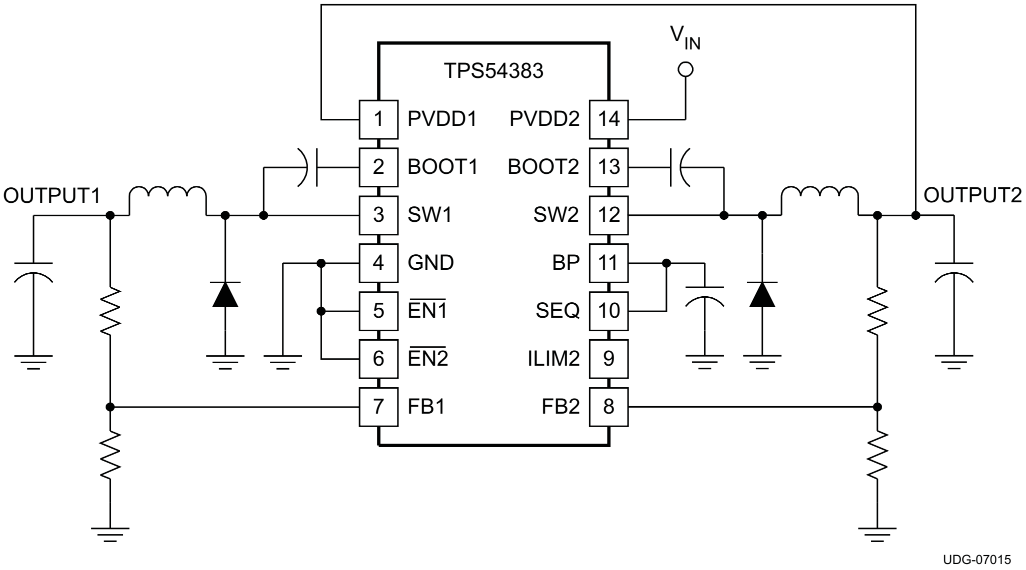


Figure 34. Schematic Showing Cascading PVDD1 from Output 2

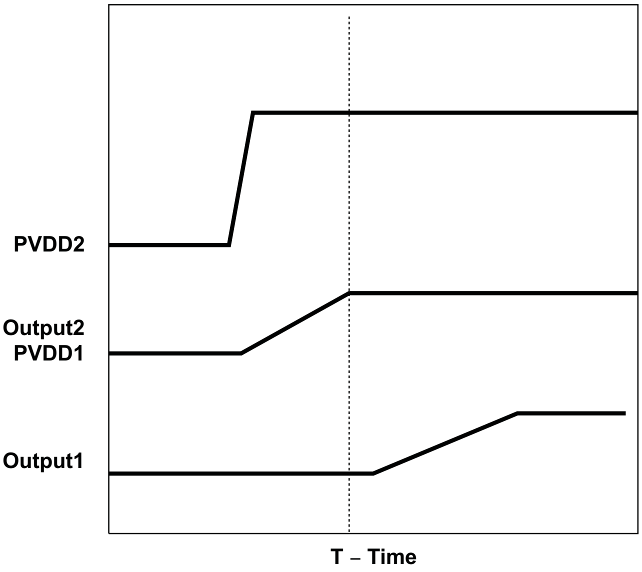


Figure 35. Waveforms Resulting from Cascading PVDD1 from Output 2

In this configuration, the following conditions must be maintained:

1. Output 2 must be of a voltage high enough to maintain regulation of Output 1 under all load conditions.
2. The sum of the current drawn by Output 2 load plus the current into PVDD1 must be less than the overload protection current level of Output 2.
3. The method of output sequencing must be such that the voltage on Output 2 is sufficient to support Output 1 before Output 1 is enabled. This requrement may be accomplished by:
   (a) a delay of the enable function
   (b) selecting sequential sequencing of Output 1 starting after Output 2 is in regulation

8.3.21 Multiphase Operation

The TPS5438x is not designed to operate as a two-channel multiphase converter. See http://www.power.ti.com for appropriate device selection.

8.3.22 Bypass and FIltering

As with any integrated circuit, supply bypassing is important for jitter-free operation. To improve the noise immunity of the converter, ceramic bypass capacitors must be placed as close to the package as possible.

1. PVDD1 to GND: Use a 10-μF ceramic capacitor
2. PVDD2 to GND: Use a 10-μF ceramic capacitor
3. BP to GND: Use a 4.7-μF to 10-μF ceramic capacitor

8.3.23 Overtemperature Protection and Junction Temperature Rise

The overtemperature thermal protection limits the maximum power to be dissipated at a given operating ambient temperature. In other words, at a given device power dissipation, the maximum ambient operating temperature is limited by the maximum allowable junction operating temperature. The device junction temperature is a function of power dissipation, and the thermal impedance from the junction to the ambient. If the internal die temperature should reach the thermal shutdown level, the TPS5438x shuts off both PWMs and remains in this state until the die temperature drops below the hysteresis value, at which time the device restarts.

The first step to determine the device junction temperature is to calculate the power dissipation. The power dissipation is dominated by the two switching MOSFETs and the BP internal regulator. The power dissipated by each MOSFET is composed of conduction losses and output (switching) losses incurred while driving the external rectifier diode. To find the conduction loss, first find the RMS current through the upper switch MOSFET.

$$I_{RMS(outputx)} = \sqrt{D \times \left(\left(I_{OUTPUTx}\right)^2 + \left(\frac{\left(\Delta I_{OUTPUTx}\right)^2}{12} \right) \right)}$$

where

- D is the duty cycle
- $I_{OUTPUTx}$ is the dc output current
- $\Delta I_{OUTPUTx}$ is the peak ripple current in the inductor for Outputx (16)

Notice the impact of the operating duty cycle on the result.

Multiplying the result by the $R_{DS(on)}$ of the MOSFET gives the conduction loss.

$$P_{D(cond)} = I_{RMS(outputx)}^{\ 2} \times R_{DS(on)} \tag{17}$$

The switching loss is approximated by:

$$P_{D(SW)} = \left[\frac{\left(V_{IN}\right)^2 \times C_J \times f_S}{2} \right]$$

where

- where C_J is the prallel capacitance of the rectifier diode and snubber (if any)
- f_S is the switching frequency (18)

The total power dissipation is found by summing the power loss for both MOSFETs plus the loss in the internal regulator.

$$P_D = P_{D(cond)output1} + P_{D(SW)output1} + P_{D(cond)output2} + P_{D(SW)output2} + V_{IN} \times Iq \tag{19}$$

The temperature rise of the device junction depends on the thermal impedance from junction to the mounting pad (See the *Thermal Information* table for performance on the standard test board), plus the thermal impedance from the thermal pad to ambient. The thermal impedance from the thermal pad to ambient depends on the PCB layout (PowerPAD interface to the PCB, the exposed pad area) and airflow (if any). See the *Layout Guidelines* section.

The operating junction temperature is shown in Equation 20.

$$T_J = T_A + P_D \times \left(\theta_{TH(pkg)} + \theta_{TH(pad-amb)}\right) \tag{20}$$

8.3.24 Power Derating

The TPS5438x delivers full current at ambient temperatures up to +85°C if the thermal impedance from the thermal pad maintains the junction temperature below the thermal shutdown level. At higher ambient temperatures, the device power dissipation must be reduced to maintain the junction temperature at or below the thermal shutdown level. Figure 36 illustrates the power derating for elevated ambient temperature under various airflow conditions. Note that these curves assume that the PowerPAD is properly soldered to the recommended thermal pad. (See the *Related Documentation* section for further information.)

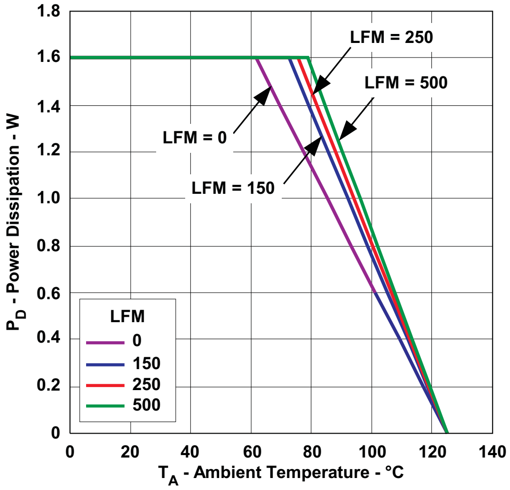


Figure 36. Power Dissipation vs Ambient Temperature. Power Derating Curves

8.4 Device Functional Modes

8.4.1 Minimum Input Voltage

The TPS5438x is recommended to operate with input voltages above 4.5 V. The typical UVLO threshold is 4.1 V at PVDD2 and the device may operate at PVDD2 voltages down to the UVLO voltage. PVDD2 is used for input voltage UVLO protection because it is the power supply for the BP regulator. The device will operate with PVDD1 voltages even lower as long as PVDD2 is above its UVLO threshold. With V_{PVDD2} below the UVLO voltage threshold the device will not switch. If either ENx pins is pulled below 0.9 V, when V_{PVDD2} passes the UVLO threshold the BP regulator turns on and begins charging the BP capacitor. After V_{BP} is greater than 4 V, depending on the state of the SEQ pin, the channel corresponding to the low ENx pin will become active. When a channel becomes active switching is enabled and the soft-start sequence is initiated. The TPS5438x starts linearly ramping up an internal soft-start reference voltage of the active channel from 0 V to its final value over the internal soft-start time period. The designer should make sure the input voltage is sufficient to support the output voltage of the active channels.

8.4.2 ENx Control

The enable start threshold voltage is 1.2 V typical. With ENx held above the 1.2 V threshold voltage the correspondeng cahnnel of the TPS548x is disabled and switching is inhibited even if PVDD2 is above its UVLO threshold. The quiescent current is reduced in this state. When the first ENx pin voltage is decreased below the threshold while $V_{(PVDD2)}$ is above the UVLO threshold the BP regulator turns on and begins charging the BP capacitor. After V_{BP} is greater than 4 V, depending on the state of the SEQ pin, the channel corresponding to the low ENx pin will become active. If the second ENx pin voltage is decreased below the threshold after V_{BP} is greater than 4 V, again depending on the state of the SEQ pin, the corresponding channel will become active immediately. When a channel becomes active switching is enabled and the slow-start sequence is initiated. The TPS548x starts linearly ramping up the internal soft-start reference voltage of the active channel from 0 V to its final value over the internal slow-start time period. If both channels are active the start-up sequence is deteremined by the stat of the SEQ pin. The designer should make sure the input voltage is sufficient to support the output voltageof the active channels.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS5438x is a dual 28-V, 3-A, step down regulator with an integrated high-side MOSFETs. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A on each channel. Example applications are: High Density Point-of-Load Regulators for Set-top Box, Digital TV, Power for DSP and other Consumer Electronics.

9.2 Typical Applications

9.2.1 12-V to 5-V and 3.3-V Converter

The following example illustrates a design process and component selection for a 12-V to 5-V and 3.3-V dual non-synchronous buck regulator using the TPS54383 converter.

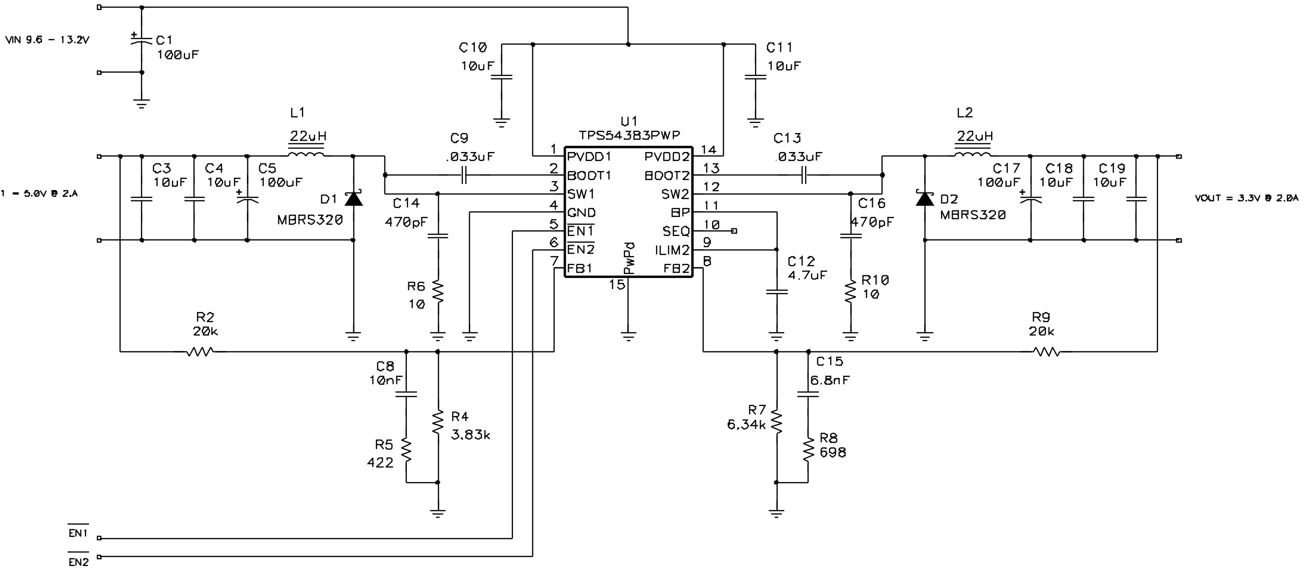


Figure 37. Design Example Schematic

9.2.1.1 *Design Requirements*

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		6.9	12.0	13.2	V
I_{IN}	Input current	V_{IN} = nom, I_{OUT} = max		1.6	2.0	A
	No load input current	V_{IN} = nom, I_{OUT} = 0 A		12	20	mA
OUTPUT CHARACTERISTICS						
V_{OUT1}	Output voltage 1	V_{IN} = nom, I_{OUT} = nom	4.8	5.0	5.2	V
V_{OUT2}	Output voltage 2	V_{IN} = nom, I_{OUT} = nom	3.2	3.3	3.4	
	Line regulation	V_{IN} = min to max			1%	
	Load regulation	I_{OUT} = min to max			1%	

Typical Applications (continued)

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
$V_{OUT(ripple)}$	Output voltage ripple	V_{IN} = nom, I_{OUT} = max			50	mV_{PP}
I_{OUT1}	Output current 1	V_{IN} = min to max	0		2.0	A
I_{OUT2}	Output current 2	V_{IN} = min to max	0		2.0	
I_{OCP1}	Output overcurrent channel 1	V_{IN} = nom, V_{OUT} = V_{OUT1} = 5%	2.4	3	3.5	
I_{OCP2}	Output overcurrent channel 2	V_{IN} = nom, V_{OUT} = V_{OUT2} = 5%	2.4	3	3.5	
	Transient response ΔV_{OUT} from load transient	ΔI_{OUT} = 1 A @ 3 A/µs		200		mV
	Transient response settling time			1		ms
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency		250	310	370	kHz
η	Full load efficiency			85%		
T_J	Operating temperature range		0	25	60	°C

Table 3. Design Example List of Materials

QTY	REFERENCE DESIGNATOR	VALUE	DESCRIPTION	SIZE	PART NUMBER	MANUFACTURER
1	C1	100 µF	Capacitor, Aluminum, 25V, 20%	E-can	EEEFC1E101P	Panasonic
2	C10, C11	10 µF	Capacitor, Ceramic, 25V, X5R 20%	1210	C3216X5R1E106M	TDK
1	C12	4.7 µF	Capacitor, Ceramic, 10V, X5R 20%	0805	Std	Std
2	C14, C16	470 pF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
1	C15	6.8 nF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
1	C17, C5	100 µF	Capacitor, Aluminum, 10V, 20%, FC Series	F-can	EEEFC1A101P	Panasonic
4	C3, C4, C18, C19	10 µF	Capacitor, Ceramic, 6.3V, X5R 20%	0805	C2012X5R0J106M	TDK
1	C8	10 nF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
2	C9, C13	0.033 µF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
2	D1, D2	MBRS320	Diode, Schottky, 3-A, 30-V	SMC	MBRS330T3	On Semi
2	L1, L2	22 µH	Inductor, Power, 6.8A, 0.038 Ω	0.484 x 0.484	MSS1278-153ML	Coilcraft
2	R2, R9	20 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	422 Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R6, R10	10 Ω	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R8	698 Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	3.83 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	6.34 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1		TPS54383 DC-DC Switching Converter w/ FET	HTSSOP -14	TPS54383PWP	TI

9.2.1.2 Detailed Design Procedure

Use the following design procedure to select component values for the TPS5438x.

9.2.1.2.1 Duty Cycle Estimation

The first step is to estimate the duty cycle of each switching FET.

$$D_{max} \approx \frac{V_{OUT} + V_{FD}}{V_{IN(min)} + V_{FD}} \tag{21}$$

$$D_{min} \approx \frac{V_{OUT} + V_{FD}}{V_{IN(max)} + V_{FD}} \tag{22}$$

Using an assumed forward drop of 0.5 V for a schottky rectifier diode, the Channel 1 duty cycle is approximately 40.1% (minimum) to 48.7% (maximum) while the Channel 2 duty cycle is approximately 27.7% (minimum) to 32.2% (maximum).

9.2.1.2.2 Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current. This places the peak current far enough from the minimum overcurrent trip level to ensure reliable operation.

For both Channel 1 and Channel 2, the maximum inductor ripple current is 600 mA. The inductor size is estimated in Equation 23.

$$L_{min} \approx \frac{V_{IN(max)} - V_{OUT}}{I_{LRIP(max)}} \times D_{min} \times \frac{1}{f_{SW}} \tag{23}$$

The inductor values are

- L1 = 18.3 μH
- L2 = 15.3 μH

The next higher standard inductor value of 22 μH is used for both inductors.

The resulting ripple currents are :

$$I_{RIPPLE} \approx \frac{V_{IN(max)} - V_{OUT}}{L} \times D_{min} \times \frac{1}{f_{SW}} \tag{24}$$

Peak-to-peak ripple currents of 0.498 A and 0.416 A are estimated for Channel 1 and Channel 2 respectively.

The RMS current through an inductor is approximated by Equation 25.

$$I_{L(rms)} = \sqrt{\left(I_{L(avg)}\right)^2 + \frac{1}{12}\left(I_{RIPPLE}\right)^2} \tag{25}$$

and is approximately 2.0 A for both channels.

The peak inductor current is found using:

$$I_{L(peak)} \approx I_{OUT(max)} + \frac{1}{2} I_{RIPPLE} \tag{26}$$

An inductor with a minimum RMS current rating of 2.0 A and minimum saturation current rating of 2.25 A is required. A Coilcraft MSS1278-223ML 22-μH, 6.8-A inductor is selected.

9.2.1.2.3 Rectifier Diode Selection

A schottky diode is selected as a rectifier diode for its low forward voltage drop. Allowing 20% over VIN for ringing on the switch node, the required minimum reverse break-down voltage of the rectifier diode is:

$$V_{(BR)R(min)} \geq 1.2 \times V_{IN} \tag{27}$$

The diode must have reverse breakdown voltage greater than 15.8 V, therefore a 20-V device is used.

The average current in the rectifier diode is estimated by Equation 28.

$$I_{D(avg)} \approx I_{OUT(max)} \times (1 - D) \tag{28}$$

For this design, 1.2-A (average) and 2.25 A (peak) is estimated for Channel 1 and 1.5-A (average) and 2.21-A (peak) for Channel 2.

An MBRS320, 20-V, 3-A diode in an SMC package is selected for both channels. This diode has a forward voltage drop of 0.4 V at 2 A.

The power dissipation in the diode is estimated by Equation 29.

$$P_{D(max)} \approx V_{FM} \times I_{D(avg)} \tag{29}$$

For this design, the full load power dissipation is estimated to be 480 mW in D1, and 580 mW in D2.

9.2.1.2.4 Output Capacitor Selection

The TPS54383's internal compensation limits the selection of the output capacitors. From Figure 25, the internal compensation has a double zero resonance at about 3 kHz. The output capacitor is selected by Equation 30.

$$C_{OUT} = \frac{1}{4 \times \pi^2 \times (f_{RES})^2 \times L} \tag{30}$$

Solving for C_{OUT} using

- f_{RES} = 3 kHz
- L = 22 µH

The resulting is C_{OUT} = 128 µF. The output ripple voltage of the converter is composed of the ripple voltage across the output capacitance and the ripple voltage across the ESR of the output capacitor. To find the maximum ESR allowable to meet the output ripple requirements the total ripple is partitioned, and the equation manipulated to find the ESR.

$$ESR_{(max)} = \frac{V_{RIPPLE(tot)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(tot)}}{I_{RIPPLE}} - \frac{D}{f_S \times C_{OUT}} \tag{31}$$

Based on 128 µF of capacitance, 300-kHz switching frequency and 50-mV ripple voltage plus rounding up the ripple current to 0.5 A, and the duty cycle to 50%, the capacitive portion of the ripple voltage is 6.5 mV, leaving a maximum allowable ESR of 87 mΩ.

To meet the ripple voltage requirements, a low-cost 100-µF electrolytic capacitor with 400 mΩ ESR (C5, C17) and two 10-µF ceramic capacitors (C3 and C4; and C18 and C19) with 2.5-mΩ ESR are selected. From the datasheets for the ceramic capacitors, the parallel combination provides an impedance of 28 mΩ @ 300 kHz for 14 mV of ripple.

9.2.1.2.5 Voltage Setting

The primary feedback divider resistors (R2, R9) from VOUT to FB should be between 10 kΩ and 50 kΩ to maintain a balance between power dissipation and noise sensitivity. For this design, 20 kΩ is selected.

The lower resistors, R4 and R7 are found using the following equations.

$$R4 = \frac{V_{FB} \times R2}{V_{OUT1} - V_{FB}} \tag{32}$$

$$R7 = \frac{V_{FB} \times R9}{V_{OUT2} - V_{FB}} \tag{33}$$

- R2 = R9 = 20 kΩ
- V_{FB} = 0.80 V
- R4= 3.80 kΩ (3.83 kΩ standard value is used)
- R7= 6.40 kΩ (6.34 kΩ standard value is used)

9.2.1.2.6 Compensation Capacitors

Checking the ESR zero of the output capacitors:

$$f_{ESR(zero)} = \frac{1}{2 \times \pi \times C \times ESR}$$

- C = 100 µF
- ESR = 400 mΩ
- ESR(zero) = 3980 Hz (34)

Since the ESR zero of the main output capacitor is less than 20 kHz, an R-C filter is added in parallel with R4 and R7 to compensate for the electrolytic capacitors' ESR and add a zero approximately 40 kHz.

$$R5 = \frac{R4}{\left(\left(\frac{f_{ZERO(desired)}}{f_{ESR(zero)}}\right) - 1\right)}$$

- $f_{ESR(zero)}$ = 4 kHz
- $f_{ESR(desired)}$ = 40 kHz
- R4 = 3.83 kΩ
- R5 = 424Ω (422Ω selected)
- R7 = 6.34 kΩ
- R8 = 702Ω (698Ω selected) (35)

$$R_{EQ} = R5 + \frac{1}{\left(\left(\frac{1}{R2}\right) + \left(\frac{1}{R4}\right)\right)}$$

- R2 = R9 = 20 kΩ
- R_{EQ1} = 3.63 kΩ
- R_{EQ2} = 5.51 kΩ (36)

$$C8 = \frac{1}{2 \times \pi \times R_{EQ} \times f_{ESR(zero)}}$$

- C8 = 10.9 nF (10 nF selected)
- C15 = 7.22 nF (6800 pF selected) (37)

9.2.1.2.7 Input Capacitor Selection

The TPS54383 datasheet recommends a minimum 10-µF ceramic input capacitor on each PVDD pin. These capacitor must be capable of handling the RMS ripple current of the converter. The RMS current in the input capacitors is estimated by Equation 38.

$$I_{RMS(outputx)} = \sqrt{D \times \left(\left(I_{OUTPUTx}\right)^2 + \left(\frac{\left(\Delta I_{OUTPUTx}\right)^2}{12}\right)\right)} \quad (38)$$

- $I_{RMS(CIN)}$ = 0.43 A

One 1210 10-µF, 25 V, X5R ceramic capacitor with 2-mΩ ESR and a 2-A RMS current rating are selected for each PVDD input. Higher voltage capacitors are selected to minimize capacitance loss at the DC bias voltage to ensure the capacitors maintain sufficient capacitance at the working voltage.

9.2.1.2.8 Boot Strap Capacitor

To ensure proper charging of the high-side FET gate and limit the ripple voltage on the boost capacitor, a 33-nF boot strap capacitor is used.

9.2.1.2.9 ILIM

Current limit must be set above the peak inductor current $I_{L(peak)}$. Comparing $I_{L(peak)}$ to the available minimum current limits, ILIM is connected to BP for the highest current limit level.

9.2.1.2.10 SEQ

The SEQ pin is left floating, leaving the enable pins to function independently. If the enable pins are tied together, the two supplies start-up ratiometrically. Alternatively, SEQ could be connected to BP or GND to provide sequential start-up.

9.2.1.2.11 Power Dissipation

The power dissipation in the TPS54383 is composed of FET conduction losses, switching losses and internal regulator losses. The RMS FET current is found using Equation 39.

$$I_{RMS(outputx)} = \sqrt{D \times \left(\left(I_{OUTPUTx}\right)^2 + \left(\frac{\left(\Delta I_{OUTPUTx}\right)^2}{12} \right) \right)} \quad (39)$$

This results in 1.05-A RMS for Channel 1 and 0.87-A RMS for Channel 2.

Conduction losses are estimated by:

$$P_{CON} = R_{DS(on)} \times \left(I_{QSW(rms)}\right)^2 \quad (40)$$

Conduction losses of 198 mW and 136 mW are estimated for Channel 1 and Channel 2 respectively.

The switching losses are estimated in Equation 41.

$$P_{SW} \approx \frac{\left(V_{IN(max)}\right)^2 \times \left(C_{DJ} + C_{OSS}\right) \times f_{SW}}{2} \quad (41)$$

From the data sheet of the MBRS320, the junction capacitance is 658 pF. Since this is large compared to the output capacitance of the TPS54x8x the FET capacitance is neglected, leaving switching losses of 17 mW for each channel.

The regulator losses are estimated in Equation 42.

$$P_{REG} \approx I_{DD} \times V_{IN(max)} + I_{BP} \times \left(V_{IN(max)} - V_{BP}\right) \quad (42)$$

With no external load on BP (I_{BP}=0) the regulator power dissipation is 66 mW.

Total power dissipation in the device is the sum of conduction and switching for both channels plus regulator losses.

The total power dissipation is P_{DISS}=0.198+0.136+0.017+0.017+.066 = 434 mW.

9.2.1.3 Application Curves

The following results are from the TPS54383-001 EVM.

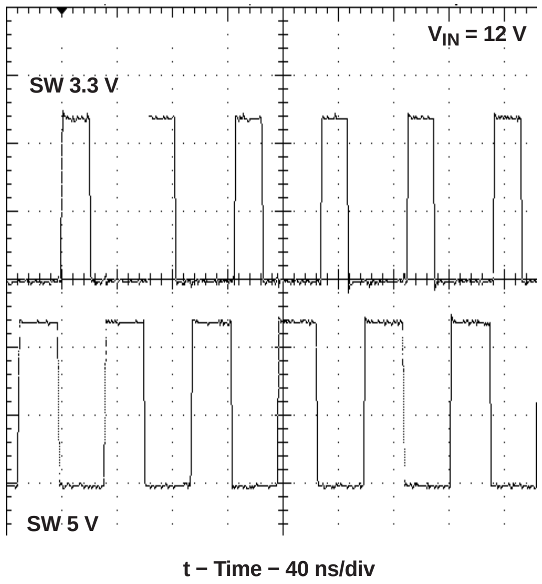


Figure 38. Switching Node Waveforms

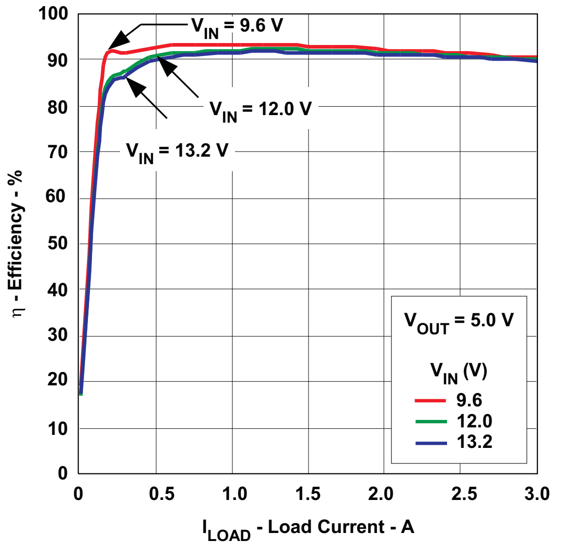


Figure 39. 5.0-V Output Efficiency vs. Load Current

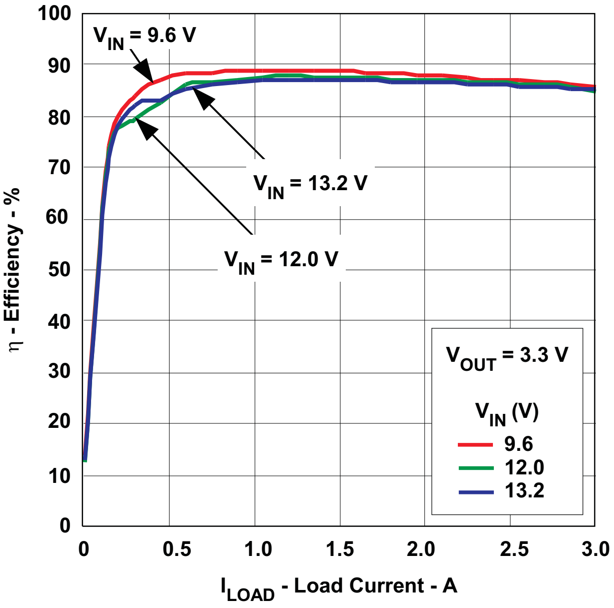


Figure 40. 3.3-V Output Efficiency vs. Load Current

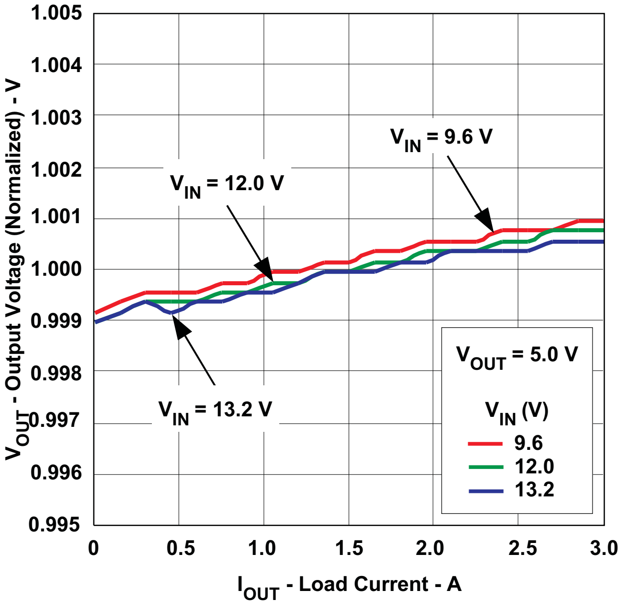


Figure 41. 5.0-V Output Voltage vs. Load Current

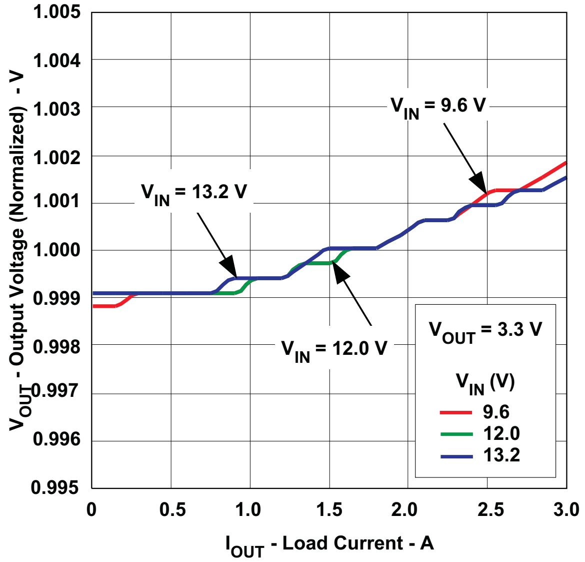


Figure 42. 3.3-V Output Voltage vs. Load Current

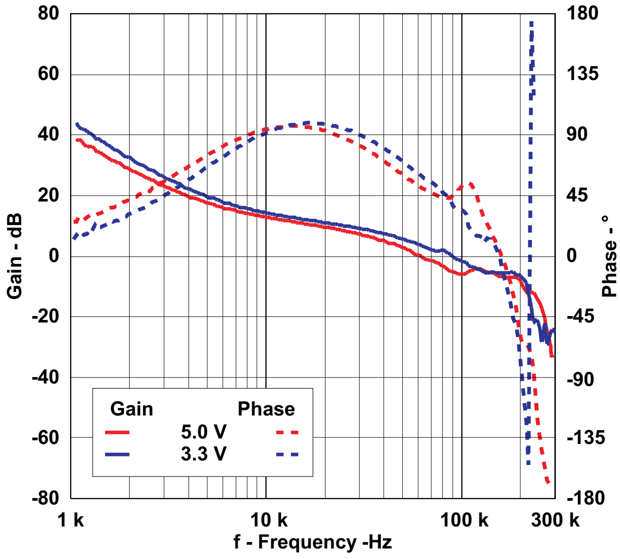


Figure 43. Example 1 Loop Response

9.2.2 24-V to 12-V and 24-V to 5-V

For a higher input voltage, both a snubber and bootstrap resistors are added to reduce ringing on the switch node and a 30 V schottky diode is selected. A higher resistance feedback network is chosen for the 12 V output to reduce the feedback current.

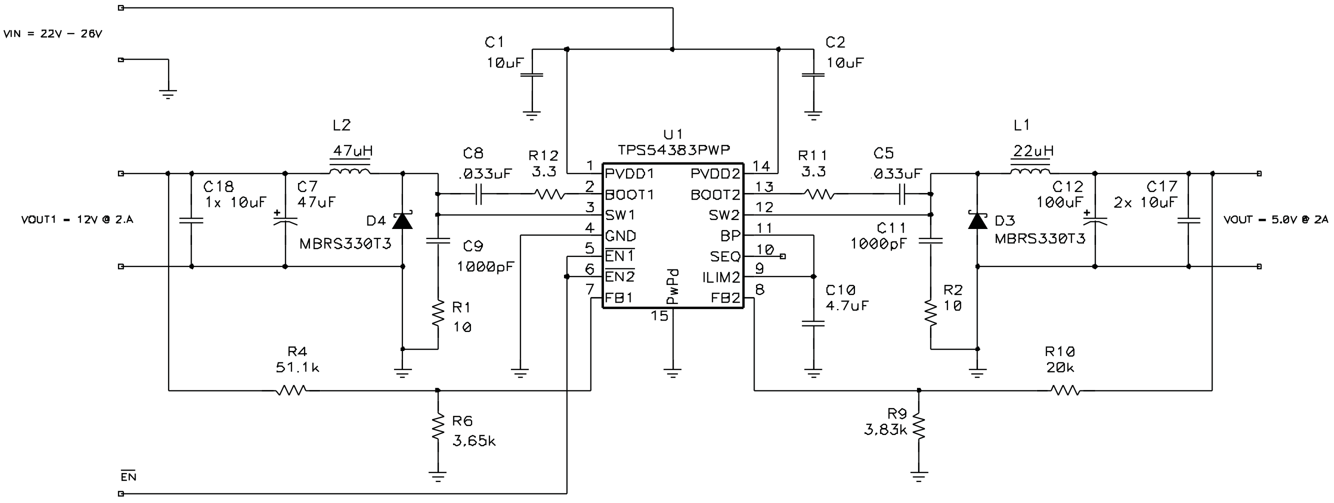


Figure 44. 24-V to 12-V and 24-V to 5-V Using the TPS54383

9.2.2.1 Design Requirements

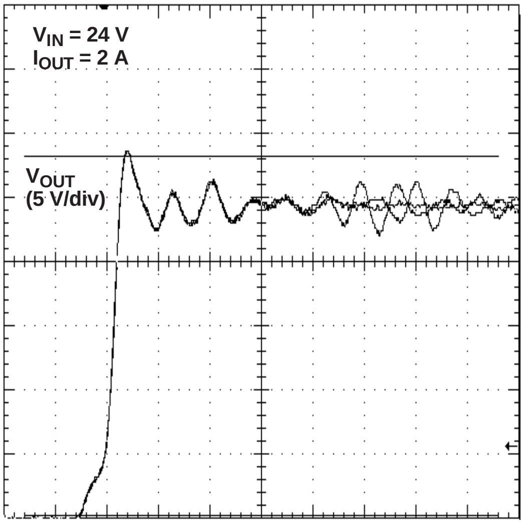
PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		22	24	26	V
OUTPUT CHARACTERISTICS						
V_{OUT1}	Output voltage 1	V_{IN} = nom, I_{OUT} = nom		12.0		V
V_{OUT2}	Output voltage 2	V_{IN} = nom, I_{OUT} = nom		5.0		

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
I_{OUT1}	Output current 1	V_{IN} = min to max	0		2.0	A
I_{OUT2}	Output current 2	V_{IN} = min to max	0		2.0	
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency		250	310	370	kHz

9.2.2.2 Detailed Design Procedure

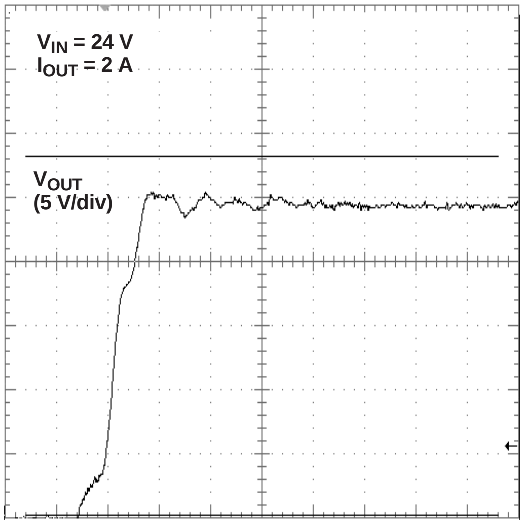
See the previous *Detailed Design Procedure*.

9.2.2.3 Application Curves



T – Time – 10 ns / div

Figure 45. Switch Node Ringing Without Snubber and Boost Resistor



T – Time – 10 ns / div

Figure 46. Switch Node Ringeing With Snubber and Boost Resistor

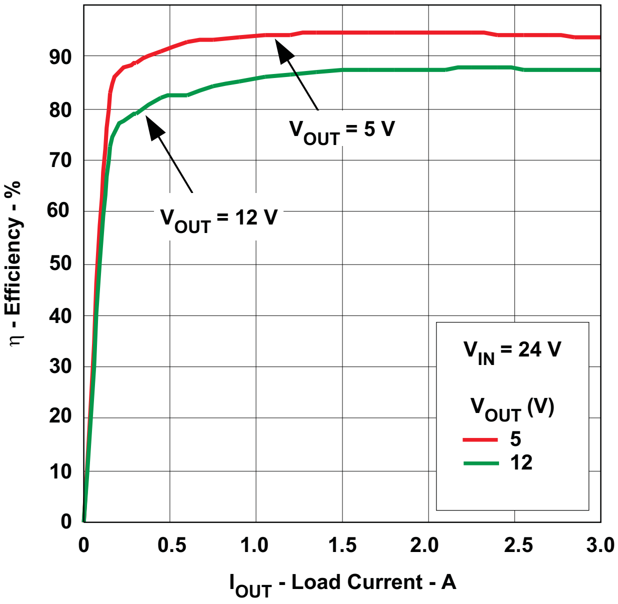


Figure 47. Efficiency vs. Load Current

9.2.3 5-V to 3.3V and 5-V to 1.2 V

For a low input voltage application, the TPS54386 is selected for reduced size and all ceramic output capacitors are used. 22-μF input capacitors are selected to reduce input ripple and lead capacitors are placed in the feedback to boost phase margin.

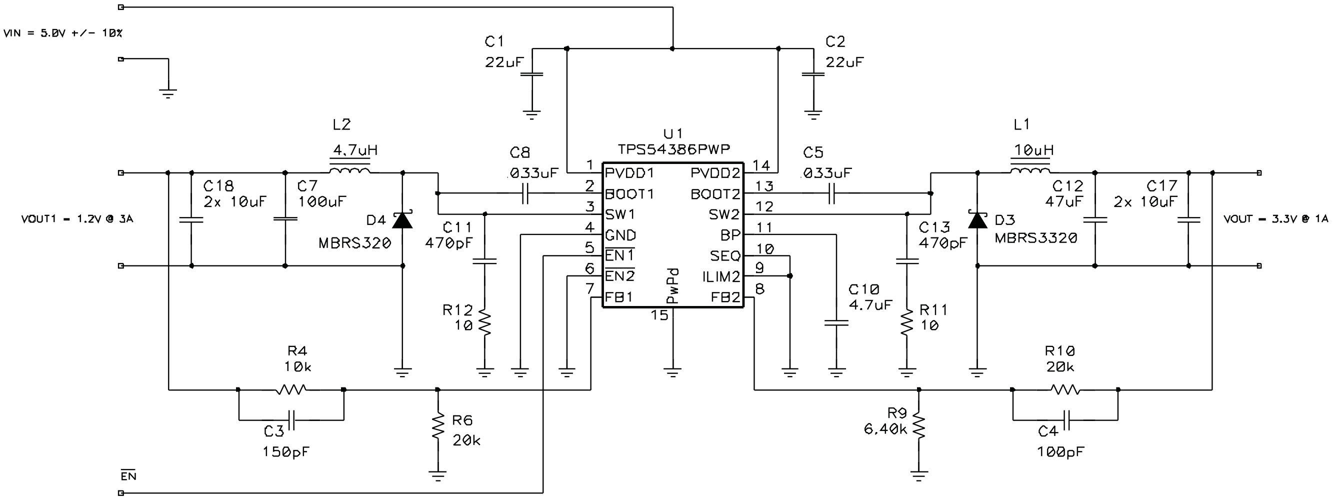


Figure 48. 5-V to 3.3V and 5-V to 1.2 V

9.2.3.1 Design Requirements

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		4.75	5	5.25	V
OUTPUT CHARACTERISTICS						
V_{OUT1}	Output voltage 1	V_{IN} = nom, I_{OUT} = nom		1,2		V
V_{OUT2}	Output voltage 2	V_{IN} = nom, I_{OUT} = nom		3.3		
I_{OUT1}	Output current 1	V_{IN} = min to max	0		3	A
I_{OUT2}	Output current 2	V_{IN} = min to max	0		1	
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency		510	630	750	kHz

9.2.3.2 Detailed Design Procedure

See the pervious *Detailed Design Procedure* and *Using All Ceramic Output Capacitors*.

9.2.3.3 Application Curves

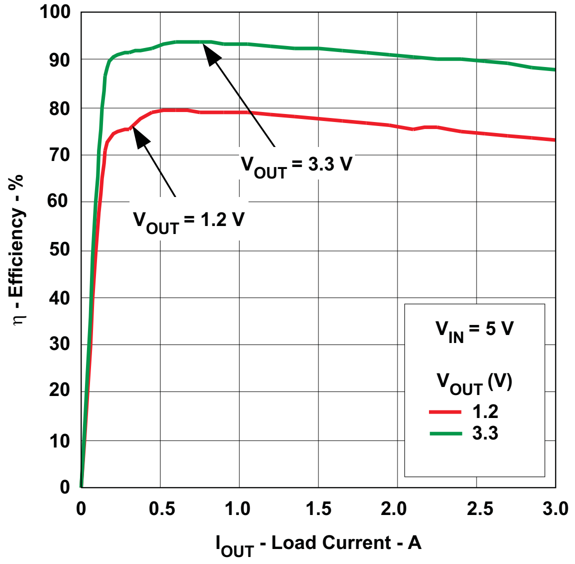


Figure 49. Efficiency vs. Load Current

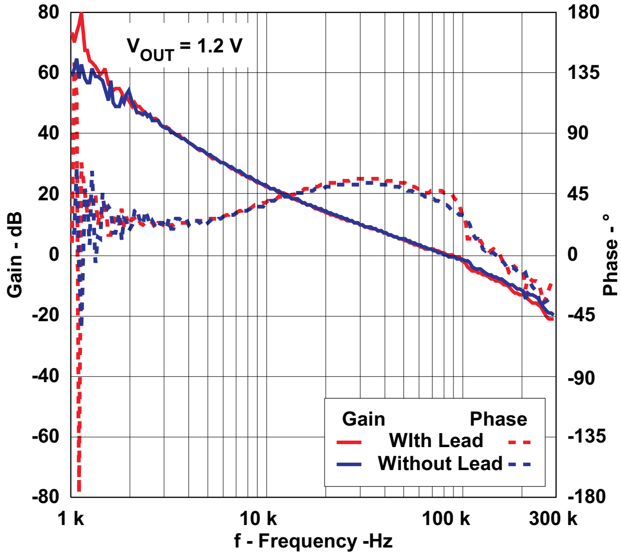


Figure 50. Example 3 Loop Response

10 Power Supply Recommendations

The TPS5438x is designed to operate from an input voltage supply range between 4.5 V and 28 V. This input supply should remain within the input voltage supply range. If the input supply is located more than a few inches from the TPS5438x converter bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

The layout guidelines presented here are illustrated in the PCB layout examples given in Figure 51 and Figure 52.

- The PowerPAD must be connected to a low current (signal) ground plane having a large copper surface area to dissipate heat. Extend the copper surface well beyond the IC package area to maximize thermal transfer of heat away from the IC.
- Connect the GND pin to the PowerPAD through a 10-mil (.010 in, or 0.0254 mm) wide trace.
- Place the ceramic input capacitors close to PVDD1 and PVDD2; connect using short, wide traces.
- Maintain a tight loop of wide traces from SW1 or SW2 through the switch node, inductor, output capacitor and rectifier diode. Avoid using vias in this loop.
- Use a wide ground connection from the input capacitor to the rectifier diode, placed as close to the power path as possible. Placement directly under the diode and the switch node is recommended.
- Locate the bootstrap capacitor close to the BOOT pin to minimize the gate drive loop.
- Locate voltage setting resistors and any feedback components over the ground plane and away from the switch node and the rectifier diode to input capacitor ground connection.
- Locate snubber components (if used) close to the rectifier diode with minimal loop area.
- Locate the BP bypass capacitor very close to the IC; a minimal loop area is recommended.
- Locate the output ceramic capacitor close to the inductor output terminal between the inductor and any electrolytic capacitors, if used.

11.2 Layout Example

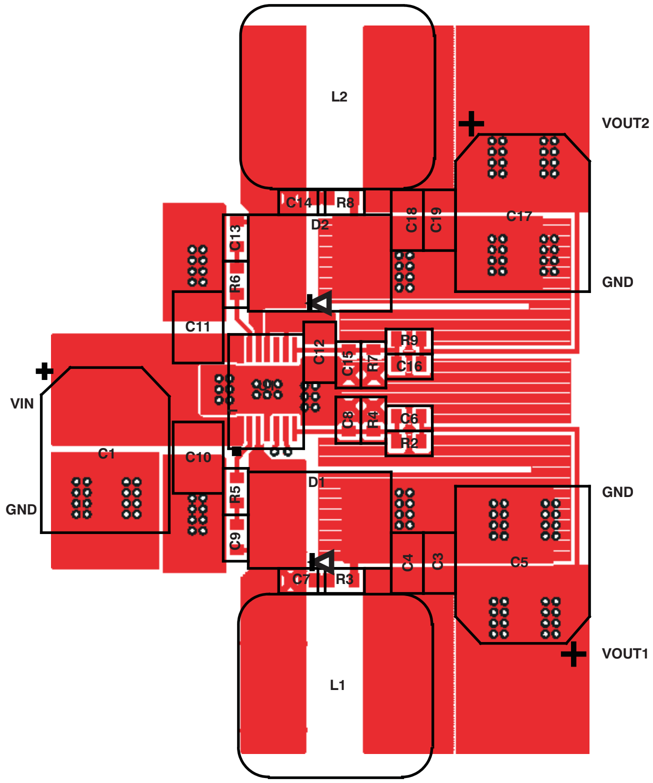


Figure 51. Top Layer Copper Layout and Component Placement

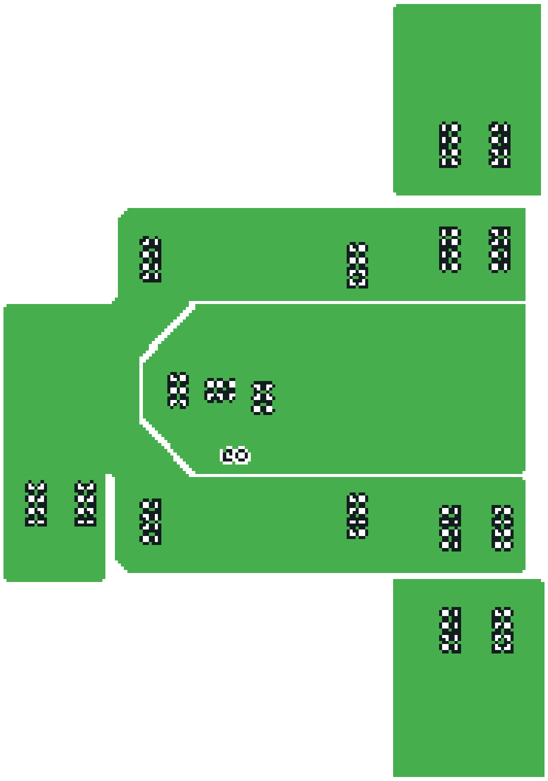


Figure 52. Bottom Layer Copper Layout

11.3 PowerPAD Package

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD package. Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) work well when 1-oz. copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. (See the *Related Documentation* section.)

12 Device and Documentation Support

12.1 Device Support

The following parts have characteristics similar to the TPS54383/6 and may be of interest.

Table 4. Devices Related to the TPS54383 and TPS54386

TI LITERATURE NUMBER	DEVICE	DESCRIPTION
SLUS642	TPS40222	5-V Input, 1.6-A Non-Synchronous Buck Converter
SLUS749	TPS54283 / TPS54286	2-A Dual Non-Synchronous Converter with Integrated High-Side MOSFET

12.1.1 Definition of Symbols

C_{DJ}	Average junction capacitance of the rectifier diode from 0V to VIN(max)
C_{OSS}	Average output capacitance of the switching MOSFET from 0V to VIN(max)
C_{OUT}	Output Capacitor
$D_{(max)}$	Maximum steady state operating duty cycle
$D_{(min)}$	Minimum steady state operating duty cycle
$ESR_{(max)}$	Maximum allowable output capacitor ESR
f_{SW}	Switching frequency
I_{BP}	Output Current of BP regulator due to external loads
I_{DD}	Switching quiescent current with no load on BP
$I_{D(avg)}$	Average diode conduction current
$I_{D(peak)}$	Peak diode conduction current
$I_{IN(avg)}$	Average input current
$I_{IN(rms)}$	Root mean squared (RMS) input current
$I_{L(avg)}$	Average inductor current
$I_{L(rms)}$	Root mean squared (RMS) inductor current
$I_{L(peak)}$	Peak current in inductor
$I_{LRIP(max)}$	Maximum allowable inductor ripple current
$L_{(min)}$	Minimum inductor value to maintain desired ripple current
$I_{OUT(max)}$	Maximum designed output current
$I_{RMS(cin)}$	Root mean squared (RMS) current through the input capacitor
I_{RIPPLE}	Inductor peak to peak ripple current
$I_{QSW(rms)}$	Root mean squared current through the switching MOSFET
P_{CON}	Power loss due to conduction through switching MOSFET
$P_{D(max)}$	Maximum power dissipation in diode
$R_{DS(on)}$	Drain to source resistance of the switching MOSFET when “ON”
P_{SW}	Power loss due to switching
P_{REG}	Power loss due to the internal regulator
V_{BP}	Output Voltage of BP regulator
$V_{(BR)R(min)}$	Minimum reverse breakdown voltage rating for rectifier diode
V_{FB}	Regulated feedback voltage
V_{FD}	Forward voltage drop across rectifier diode
V_{IN}	Power stage input voltage
V_{OUT}	Regulated output voltage
$V_{RIPPLE(cap)}$	Peak-to-Peak ripple voltage due to ideal capacitor (ESR = 0M)
$V_{RIPPLE(tot)}$	Maximum allowable peak-to-peak output ripple voltage

12.2 Documentation Support

12.2.1 Related Documentation

These references, design tools and links to additional references, including design software, may be found at http:www.power.ti.com

- PowerPAD Thermally Enhanced Package Application Report, SLMA002
- PowerPAD™ Made Easy, SLMA004
- Under The Hood Of Low Voltage DC/DC Converters. SEM1500 Topic 5, 2002 Seminar Series, SLUP206
- Understanding Buck Power Stages in Switchmode Power Supplies, SLVA057
- Designing Stable Control Loops. SEM 1400, 2001 Seminar Series, SLUP173

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS54383	Click here	Click here	Click here	Click here	Click here
TPS54386	Click here	Click here	Click here	Click here	Click here

12.4 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54383PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54383	Samples
TPS54383PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54383	Samples
TPS54386PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54386	Samples
TPS54386PWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54386	Samples
TPS54386PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54386	Samples
TPS54386PWPRG4	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54386	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54386 :

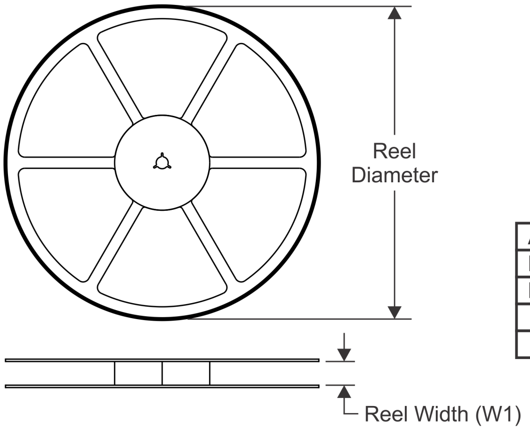
- Automotive: TPS54386-Q1

NOTE: Qualified Version Definitions:

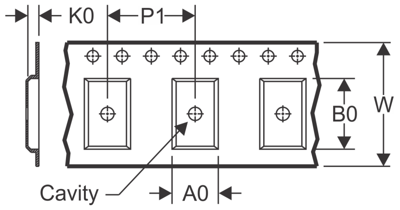
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

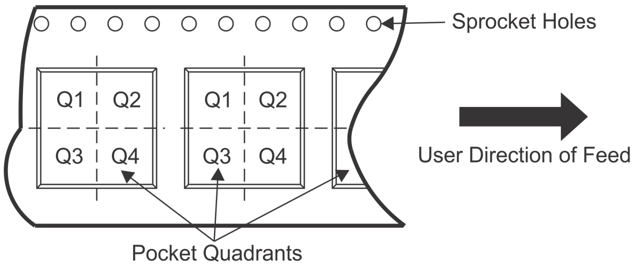


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

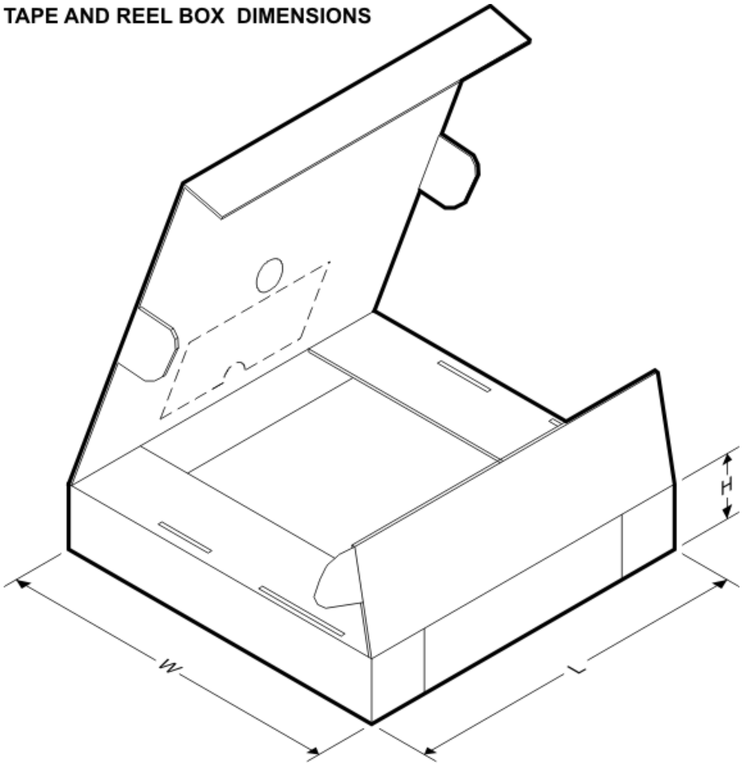
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54383PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54386PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

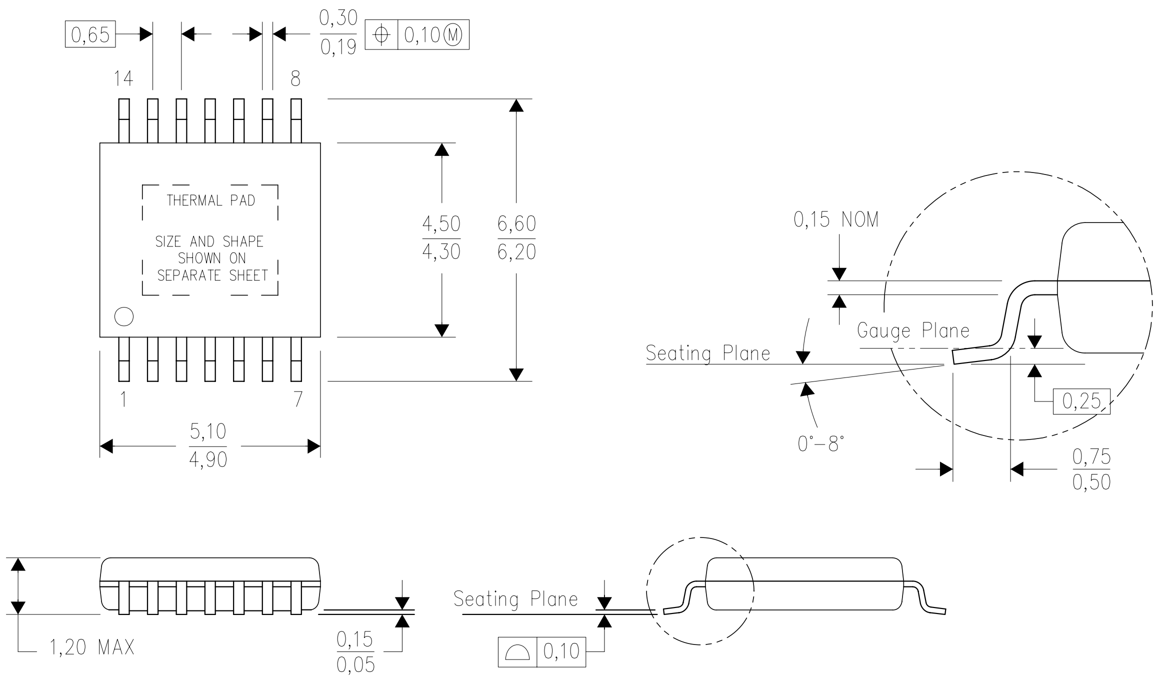
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54383PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS54386PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



4073225–2/I 05/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

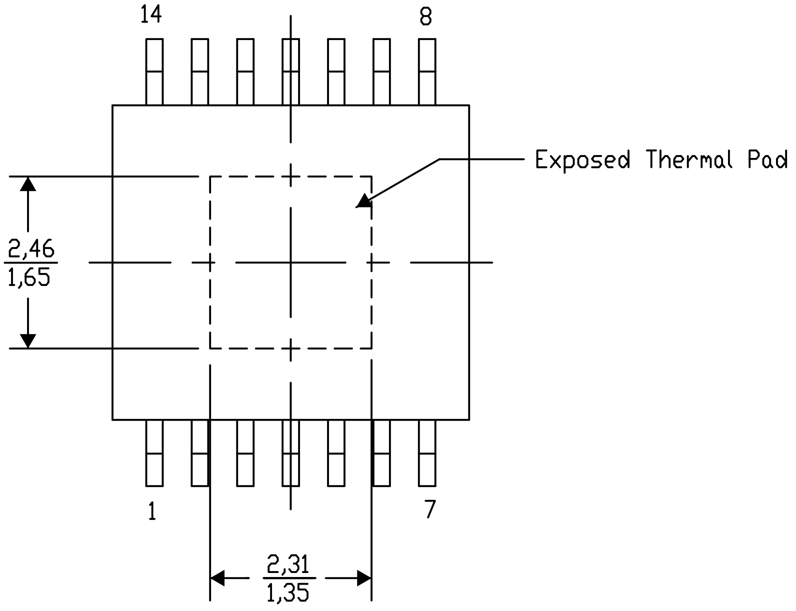
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

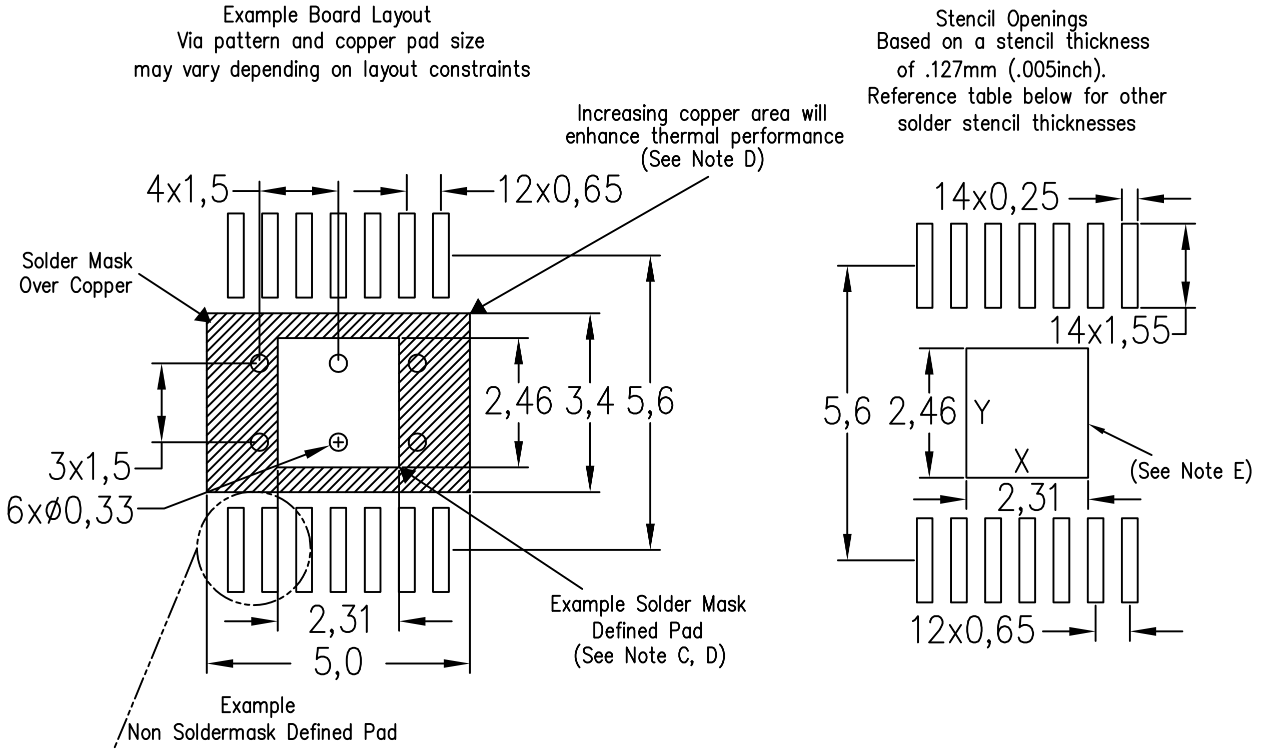
Exposed Thermal Pad Dimensions

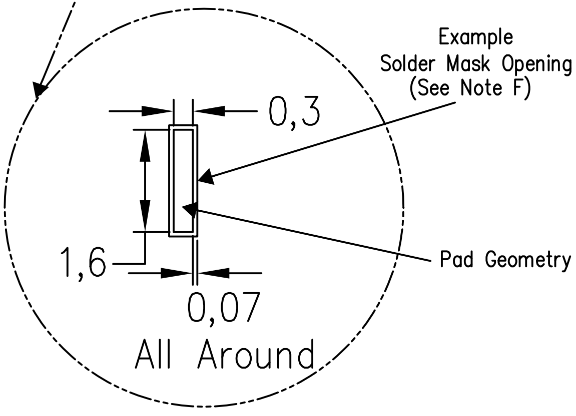
4206332-2/A0 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC–7351 is recommended for alternate designs.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

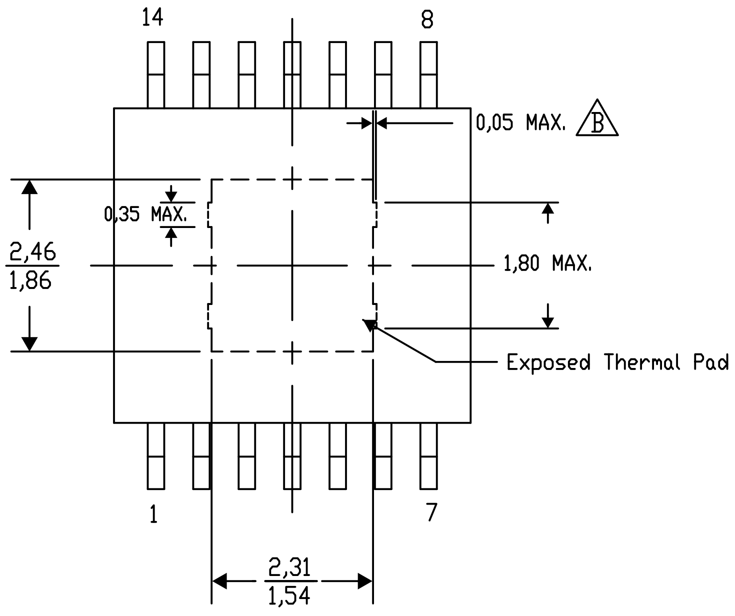
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

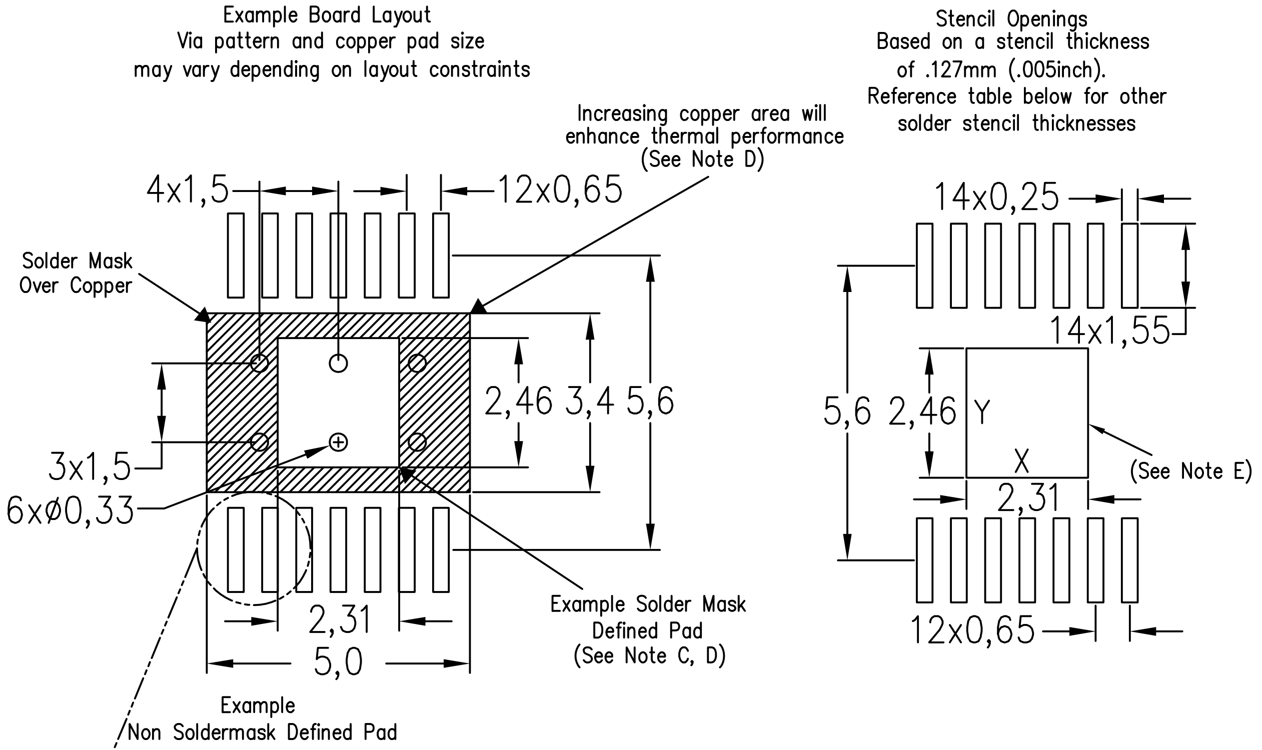
4206332-44/A0 01/16

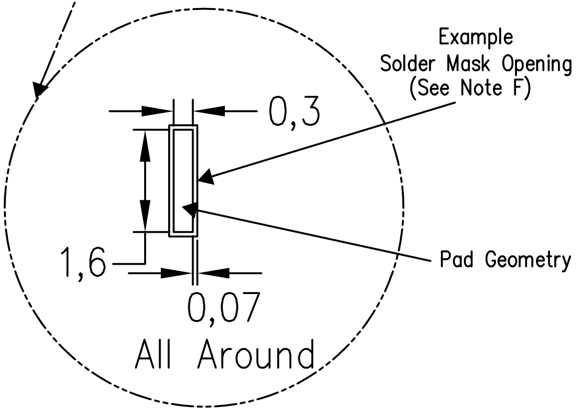
NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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