



**THE DATASHEET OF
S9S08LG16J0VLF**



MC9S08LG32 Series with Addendum Covers: MC9S08LG32 and MC9S08LG16

Rev. 10 of the MC9S08LG32 Series data sheet (covering MC9S08LG32 and MC9S08LG16) has two parts:

- The addendum to revision 9 of the data sheet, immediately following this cover page.
- Revision 9 of the data sheet, following the addendum. The changes described in the addendum have not been implemented in the specified pages.

Addendum to Rev. 9 of the MC9S08LG32 Series Covers: MC9S08LG32 and MC9S08LG16

This addendum identifies changes to Rev. 9 of the MC9S08LG32 Series data sheet (covering MC9S08LG32 and MC9S08LG16). The changes described in this addendum have not been implemented in the specified pages.

1 Add min values for I_{IC} (DC injection current)

Location: [Table 8. DC Characteristics, Page 14](#)

In Table 8, “DC Characteristics,” add min values for I_{IC} (row number 14) as follows:

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit	
14	D	DC injection current ^{5, 6, 7} $V_{IN} < V_{SS}$ (min) $V_{IN} > V_{DD}$ (max)	Single pin limit	I_{IC}	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	mA

2 Change the max value of t_{LPO} (low power oscillator period)

Location: [Table 14. Control Timing, Page 29](#)

In Table 14, “Control Timing,” change the max value of t_{LPO} (row number 2) from 1300 to 1500 μ s.

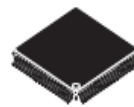


MC9S08LG32 Series

Covers: MC9S08LG32 and MC9S08LG16

Features

- 8-bit HCS08 Central Processor Unit (CPU)
 - Up to 40 MHz CPU at 5.5 V to 2.7 V across temperature range of -40°C to 85°C and -40°C to 105°C
 - HCS08 instruction set with added BGND instruction
 - Support for up to 32 interrupt/reset sources
 - On-Chip Memory
 - 32 KB or 18 KB dual array flash; read/program/erase over full operating voltage and temperature
 - 1984 byte random access memory (RAM)
 - Security circuitry to prevent unauthorized access to RAM and flash contents
 - Power-Saving Modes
 - Two low-power stop modes (stop2 and stop3)
 - Reduced-power wait mode
 - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
 - Low power On-Chip crystal oscillator (XOSC) that can be used in low-power modes to provide accurate clock source to real time counter and LCD controller
 - 100 μs typical wakeup time from stop3 mode
 - Clock Source Options
 - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
 - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 20 MHz.
 - System Protection
 - COP reset with option to run from dedicated 1 kHz internal clock or bus clock
 - Low-voltage warning with interrupt
 - Low-voltage detection with reset
 - Illegal opcode detection with reset
 - Illegal address detection with reset
 - Flash and RAM protection
 - Development Support
 - Single-wire background debug interface
 - Breakpoint capability to allow single breakpoint setting during in-circuit debugging and plus two more breakpoints in On-Chip debug module
-
- On-Chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes; eight deep FIFO for storing change-of-flow addresses and event-only data; debug module supports both tag and force breakpoints
 - Peripherals
 - **LCD** — Up to 4×41 or 8×37 LCD driver with internal charge pump.
 - **ADC** — Up to 16-channel, 12-bit resolution, 2.5 μs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel, runs in stop3 and can wake up the system, fully functional from 5.5 V to 2.7 V
 - **SCI** — Full duplex non-return to zero (NRZ), LIN master extended break generation, LIN slave extended break detection, wakeup on active edge
 - **SPI** — Full-duplex or single-wire bidirectional, double-buffered transmit and receive, master or slave mode, MSB-first or LSB-first shifting
 - **IIC** — With up to 100 kbps with maximum bus loading, multi-master operation, programmable slave address, interrupt driven byte-by-byte data transfer, supports broadcast mode and 10-bit addressing
 - **TPMx** — One 6 channel and one 2 channel, selectable input capture, output compare, or buffered edge or center-aligned PWM on each channel
 - **MTIM** — 8-bit counter with match register, four clock sources with prescaler dividers, can be used for periodic wakeup
 - **RTC** — 8-bit modulus counter with binary or decimal based prescaler, three clock sources including one external source, can be used for time base, calendar, or task scheduling functions
 - **KBI** — One keyboard control module capable of supporting 8×8 keyboard matrix
 - **IRQ** — External pin for wakeup from low-power modes
 - Input/Output
 - 39, 53, or 69 GPIOs
 - 8 KBI and 1 IRQ interrupt with selectable polarity
 - Hysteresis and configurable pullup device on all input pins, configurable slew rate and drive strength on all output pins.
 - Package Options
 - 48-pin LQFP, 64-pin LQFP, and 80-pin LQFP



80-LQFP
Case 917A
14 mm \times 14 mm



64-LQFP
Case 840F
10 mm \times 10 mm



48-LQFP
Case 932
7 mm \times 7 mm

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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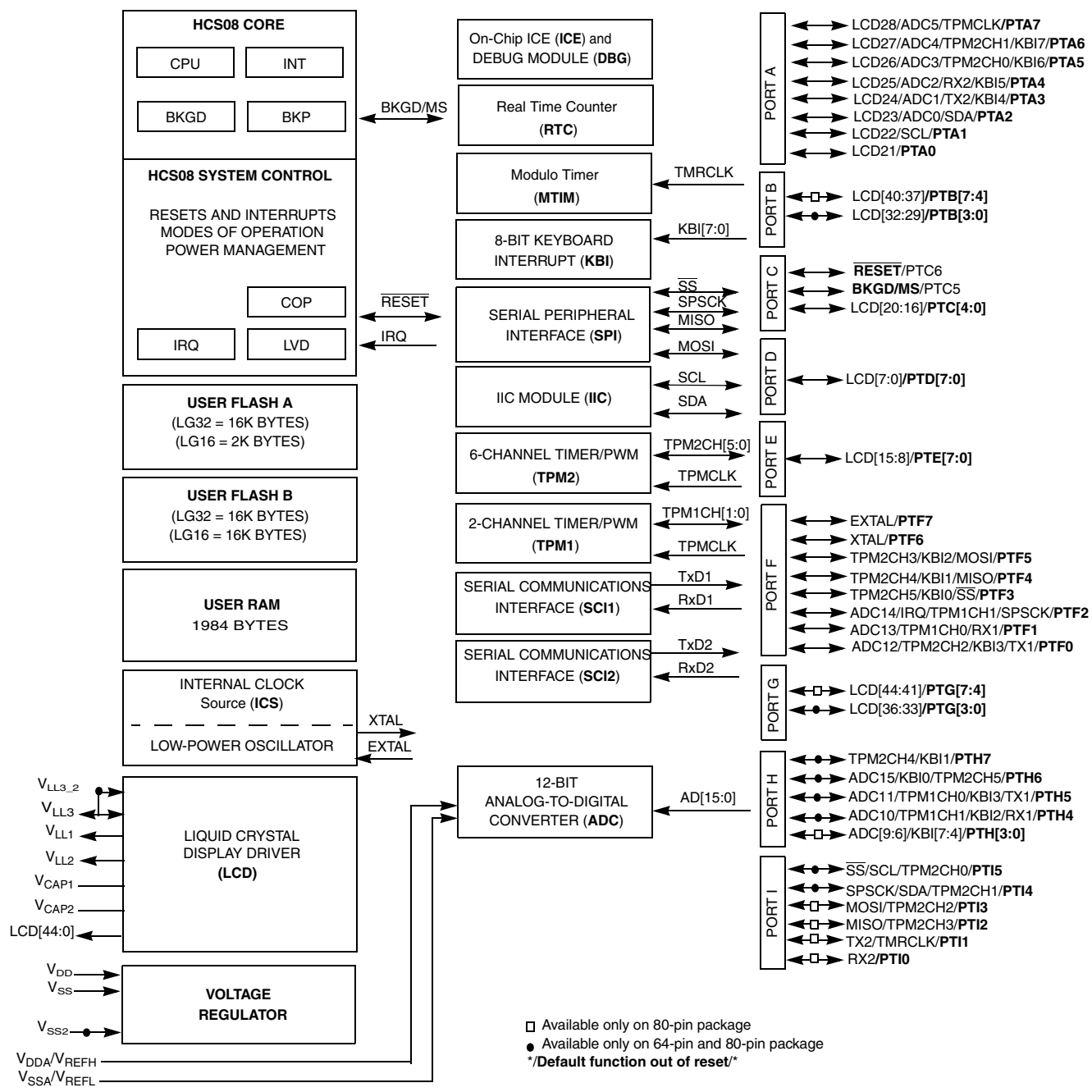


Figure 1. MC9S08LG32 Series Block Diagram

Table 1. MC9S08LG32 Series Features by MCU and Package

Feature	MC9S08LG32			MC9S08LG16	
	Flash size (bytes)	32,768			18,432
RAM size (bytes)	1984				
Pin quantity	80	64	48	64	48
ADC	16 ch	12 ch	9 ch	12 ch	9 ch
LCD	8 x 37 4 x 41	8 x 29 4 x 33	8 x 21 4 x 25	8 x 29 4 x 33	8 x 21 4 x 25
ICE + DBG	yes				
ICS	yes				
IIC	yes				
IRQ	yes				
KBI	8 pin				
GPIOs	69	53	39	53	39
RTC	yes				
MTIM	yes				
SCI1	yes				
SCI2	yes				
SPI	yes				
TPM1 channels	2				
TPM2 channels	6				
XOSC	yes				

1 Pin Assignments

This section shows the pin assignments for the MC9S08LG32 series devices. The priority of functions on a pin is in ascending order from left to right and bottom to top. Another view of pinouts and function priority is given in [Table 2](#).

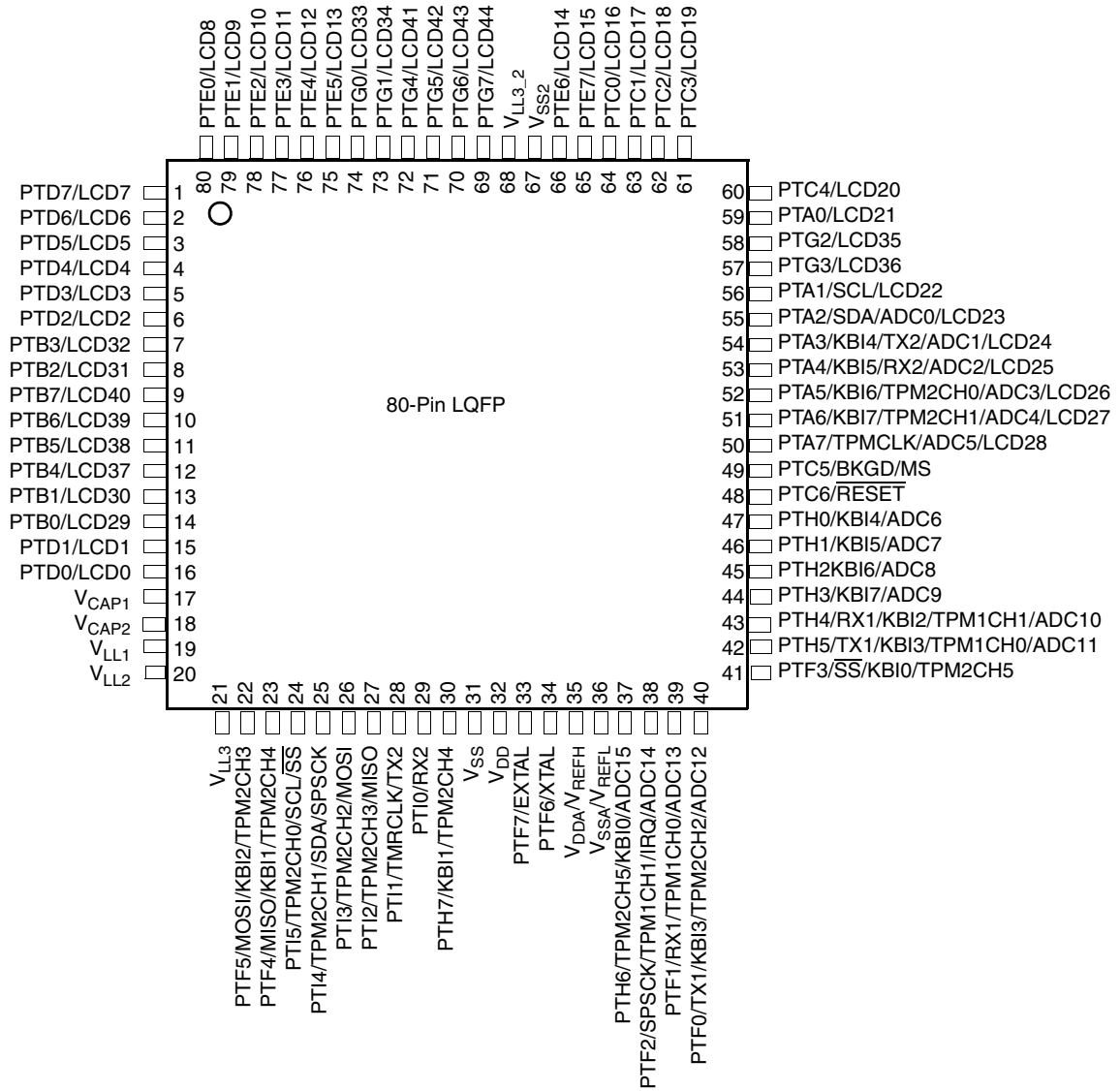


Figure 2. 80-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

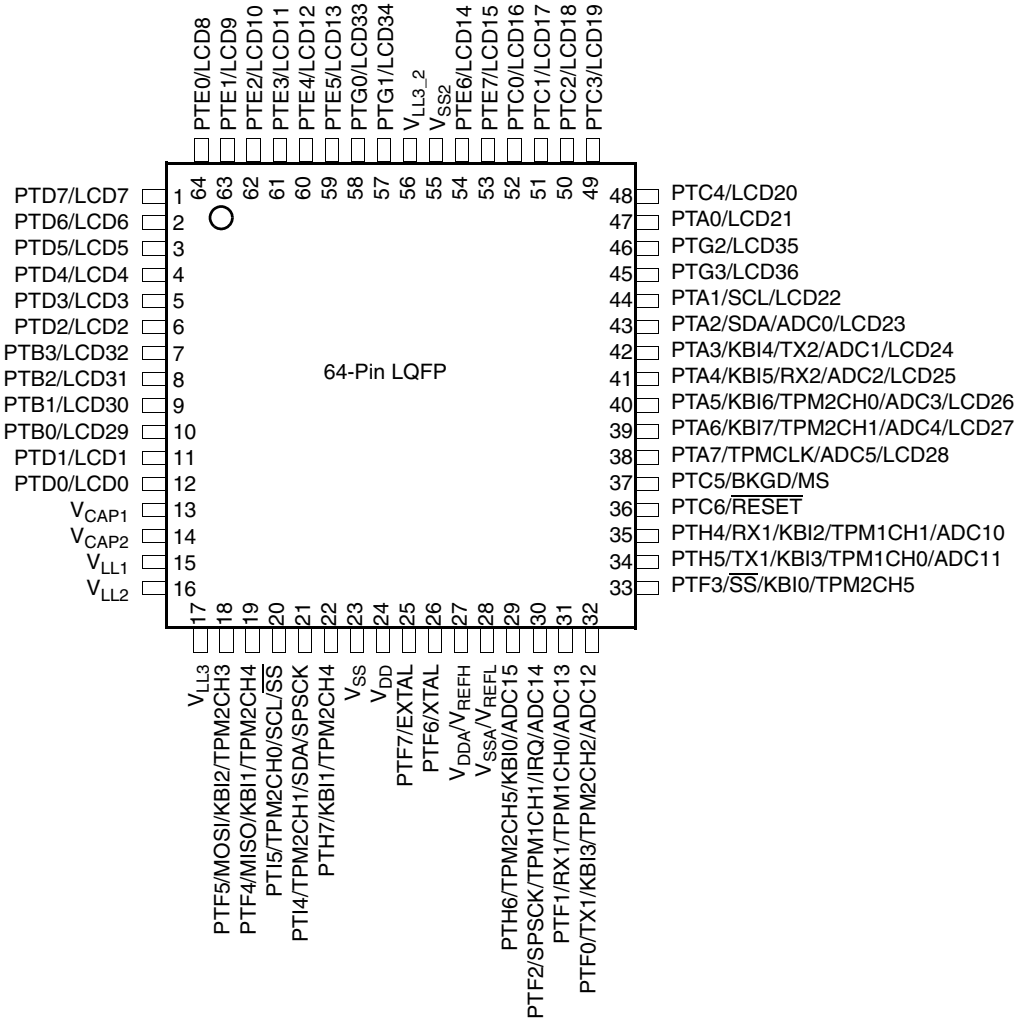


Figure 3. 64-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

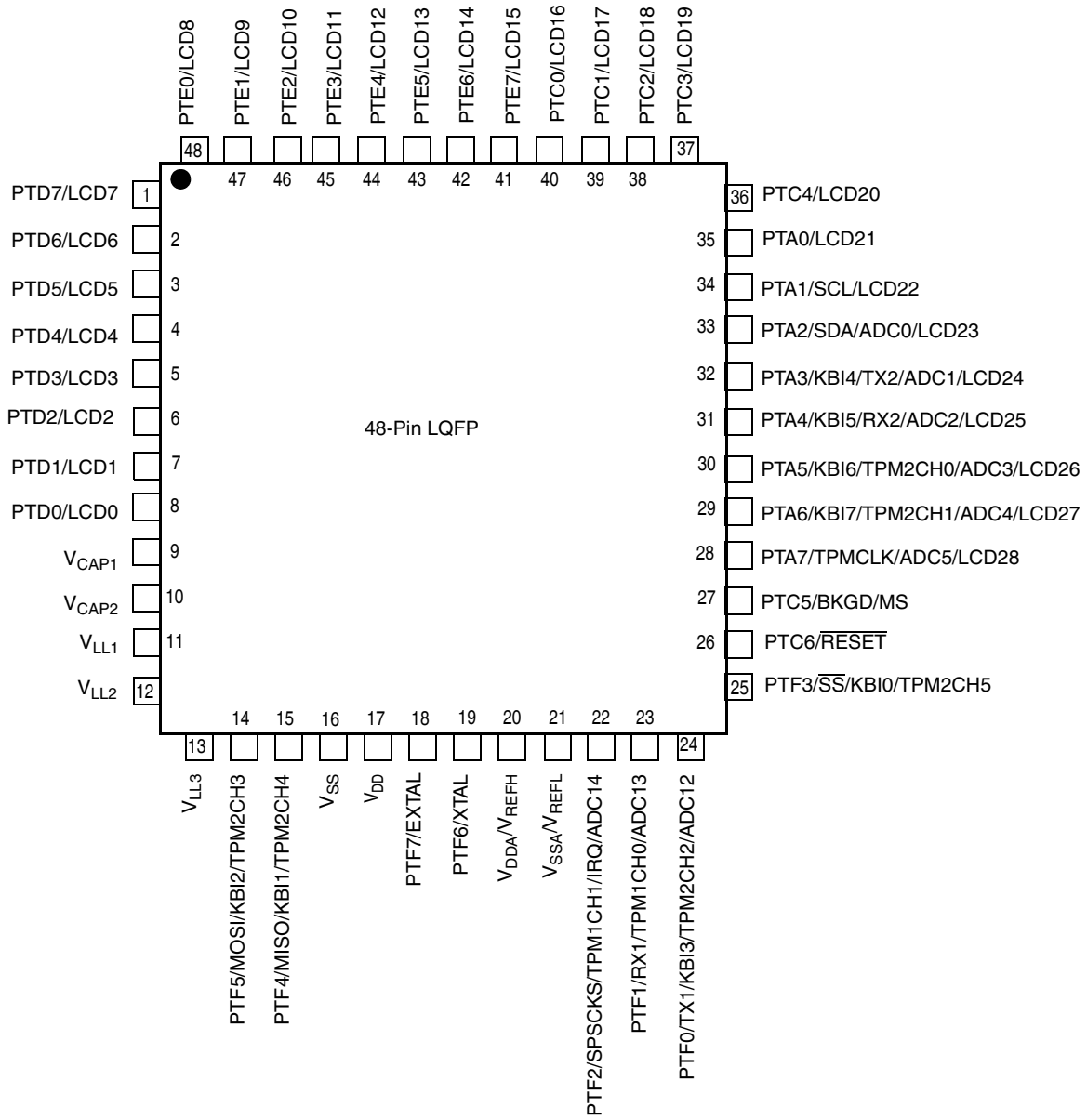


Figure 4. 48-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Table 2. Pin Availability by Package Pin-Count

Packages			<-- Lowest Priority --> Highest				
80	64	48	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	PTD7	LCD7	—	—	—
2	2	2	PTD6	LCD6	—	—	—
3	3	3	PTD5	LCD5	—	—	—
4	4	4	PTD4	LCD4	—	—	—
5	5	5	PTD3	LCD3	—	—	—
6	6	6	PTD2	LCD2	—	—	—
7	7	—	PTB3	LCD32	—	—	—
8	8	—	PTB2	LCD31	—	—	—
9	—	—	PTB7	LCD40	—	—	—
10	—	—	PTB6	LCD39	—	—	—
11	—	—	PTB5	LCD38	—	—	—
12	—	—	PTB4	LCD37	—	—	—
13	9	—	PTB1	LCD30	—	—	—
14	10	—	PTB0	LCD29	—	—	—
15	11	7	PTD1	LCD1	—	—	—
16	12	8	PTD0	LCD0	—	—	—
17	13	9	V _{CAP1}	—	—	—	—
18	14	10	V _{CAP2}	—	—	—	—
19	15	11	V _{LL1}	—	—	—	—
20	16	12	V _{LL2}	—	—	—	—
21	17	13	V _{LL3}	—	—	—	—
22	18	14	PTF5	MOSI	KBI2	TPM2CH3	—
23	19	15	PTF4	MISO	KBI1	TPM2CH4	—
24	20	—	PTI5	TPM2CH0	SCL	\overline{SS}	—
25	21	—	PTI4	TPM2CH1	SDA	SPSCK	—
26	—	—	PTI3	TPM2CH2	MOSI	—	—
27	—	—	PTI2	TPM2CH3	MISO	—	—
28	—	—	PTI1	TMRCLK	TX2	—	—
29	—	—	PTI0	RX2	—	—	—
30	22	—	PTH7	KBI1	TPM2CH4	—	—
31	23	16	V _{SS}	—	—	—	—
32	24	17	V _{DD}	—	—	—	—
33	25	18	PTF7	EXTAL	—	—	—
34	26	19	PTF6	XTAL	—	—	—
35	27	20	V _{DDA}	V _{REFH}	—	—	—
36	28	21	V _{SSA}	V _{REFL}	—	—	—
37	29	—	PTH6	TPM2CH5	KBI0	ADC15	—
38	30	22	PTF2	SPSCK	TPM1CH1	IRQ	ADC14

Table 2. Pin Availability by Package Pin-Count (continued)

Packages			<-- Lowest Priority --> Highest				
80	64	48	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
39	31	23	PTF1	RX1	TPM1CH0	ADC13	—
40	32	24	PTF0	TX1	KBI3	TPM2CH2	ADC12
41	33	25	PTF3	SS	KBI0	TPM2CH5	—
42	34	—	PTH5	TX1	KBI3	TPM1CH0	ADC11
43	35	—	PTH4	RX1	KBI2	TPM1CH1	ADC10
44	—	—	PTH3	KBI7	ADC9	—	—
45	—	—	PTH2	KBI6	ADC8	—	—
46	—	—	PTH1	KBI5	ADC7	—	—
47	—	—	PTH0	KBI4	ADC6	—	—
48	36	26	PTC6	RESET	—	—	—
49	37	27	PTC5	BKGD/MS	—	—	—
50	38	28	PTA7	TPMCLK	ADC5	LCD28	—
51	39	29	PTA6	KBI7	TPM2CH1	ADC4	LCD27
52	40	30	PTA5	KBI6	TPM2CH0	ADC3	LCD26
53	41	31	PTA4	KBI5	RX2	ADC2	LCD25
54	42	32	PTA3	KBI4	TX2	ADC1	LCD24
55	43	33	PTA2	SDA	ADC0	LCD23	—
56	44	34	PTA1	SCL	LCD22	—	—
57	45	—	PTG3	LCD36	—	—	—
58	46	—	PTG2	LCD35	—	—	—
59	47	35	PTA0	LCD21	—	—	—
60	48	36	PTC4	LCD20	—	—	—
61	49	37	PTC3	LCD19	—	—	—
62	50	38	PTC2	LCD18	—	—	—
63	51	39	PTC1	LCD17	—	—	—
64	52	40	PTC0	LCD16	—	—	—
65	53	41	PTE7	LCD15	—	—	—
66	54	42	PTE6	LCD14	—	—	—
67	55	—	V _{SS2}	—	—	—	—
68	56	—	V _{LL3_2}	—	—	—	—
69	—	—	PTG7	LCD44	—	—	—
70	—	—	PTG6	LCD43	—	—	—
71	—	—	PTG5	LCD42	—	—	—
72	—	—	PTG4	LCD41	—	—	—
73	57	—	PTG1	LCD34	—	—	—
74	58	—	PTG0	LCD33	—	—	—
75	59	43	PTE5	LCD13	—	—	—
76	60	44	PTE4	LCD12	—	—	—

Table 2. Pin Availability by Package Pin-Count (continued)

Packages			<-- Lowest Priority --> Highest				
80	64	48	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
77	61	45	PTE3	LCD11	—	—	—
78	62	46	PTE2	LCD10	—	—	—
79	63	47	PTE1	LCD9	—	—	—
80	64	48	PTE0	LCD8	—	—	—

2 Electrical Characteristics

2.1 Introduction

This section contains electrical and timing specifications for the MC9S08LG32 series of microcontrollers available at the time of publication.

2.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 4](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry that protects against damage due to high static voltage or electrical fields. However, it is advised that normal precautions should be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	± 25 ± 2	mA
Storage temperature range	T_{stg}	-55 to 150	°C

- ¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages and use the largest of the two resistance values.
- ² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .
- ³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in an external power supply going out of regulation. Ensure that the external V_{DD} load will shunt current greater than maximum injection current, this will be of greater risk when the MCU is not consuming power. For instance, if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

2.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in On-Chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to +105	°C
Maximum junction temperature	T_J	125	°C
Thermal resistance Single-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	61 71 80	°C/W
Thermal resistance Four-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	48 52 56	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

Electrical Characteristics

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273 \text{ °C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273 \text{ °C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

2.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for automotive grade integrated circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-Up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating ¹	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	2500	—	V
2	Charge device model (CDM)	V_{CDM}	750	—	V
3	Latch-up current at $T_A = 85\text{ }^\circ\text{C}$	I_{LAT}	± 100	—	mA

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit
1	—	Operating Voltage	—	2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = -2\text{ mA}$ 3 V, $I_{Load} = -0.6\text{ mA}$	V_{OH}	$V_{DD} - 0.8$ $V_{DD} - 0.8$	— —	— —	V
		Output high voltage — High Drive (PTxDSn = 1) V 5 V, $I_{Load} = -10\text{ mA}$ 3 V, $I_{Load} = -3\text{ mA}$		$V_{DD} - 0.8$ $V_{DD} - 0.8$	— —	— —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = 2\text{ mA}$ 3 V, $I_{Load} = 0.6\text{ mA}$	V_{OL}	—	— —	0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = 10\text{ mA}$ 3 V, $I_{Load} = 3\text{ mA}$		— —	0.8 0.8		
4	P	Output high current — Max total I_{OH} for all ports 5 V 3 V	I_{OHT}	—	—	100 60	mA
5	C	Output high current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	—	—	100 60	mA
6	P	Bandgap voltage reference	V_{BG}	—	1.225	—	V
7	P	Input high voltage; all digital inputs	V_{IH}	$0.65 \times V_{DD}$	—	—	V
8	P	Input low voltage; all digital inputs	V_{IL}	—	—	$0.35 \times V_{DD}$	V
9	P	Input hysteresis; all digital inputs	V_{hys}	$0.06 \times V_{DD}$	—	—	mV
10	P	Input leakage current; input only pins ² $V_{In} = V_{DD}$ or V_{SS}	$ I_{In} $	—	0.1	1	μA
11	P	High impedance (off-state) leakage current $V_{In} = V_{DD}$ or V_{SS}	$ I_{OZ} $	—	0.1	1	μA
12	P	Internal pullup resistors ³	R_{PU}	20	45	65	k Ω
13	P	Internal pulldown resistors ⁴	R_{PD}	20	45	65	k Ω

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit	
14	D	DC injection current ^{5, 6, 7} $V_{IN} < V_{SS}, V_{IN} > V_{DD}$	Single pin limit	I_{IC}	—	—	2	mA
		Total MCU limit, includes sum of all stressed pins	—		—	25	mA	
15	C	Input Capacitance, all non-supply pins	C_{In}	—	—	8	pF	
16	C	RAM retention voltage	V_{RAM}	2	—	—	V	
17	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V	
18	D	POR rearm time	t_{POR}	10	—	—	μs	
19	P	Low-voltage detection threshold — high range	V_{LVD1}	V_{DD} falling	3.9	4.0	4.1	V
				V_{DD} rising	4.0	4.1	4.2	
20	P	Low-voltage detection threshold — low range	V_{LVD0}	V_{DD} falling	2.48	2.56	2.64	V
				V_{DD} rising	2.54	2.62	2.70	
21	P	Low-voltage warning threshold — high range 1	V_{LVW3}	V_{DD} falling	4.5	4.6	4.7	V
				V_{DD} rising	4.6	4.7	4.8	
22	P	Low-voltage warning threshold — high range 0	V_{LVW2}	V_{DD} falling	4.2	4.3	4.4	V
				V_{DD} rising	4.3	4.4	4.5	
23	P	Low-voltage warning threshold — low range 1	V_{LVW1}	V_{DD} falling	2.84	2.92	3.00	V
				V_{DD} rising	2.90	2.98	3.06	
24	P	Low-voltage warning threshold — low range 0	V_{LVW0}	V_{DD} falling	2.66	2.74	2.82	V
				V_{DD} rising	2.72	2.80	2.88	
25	P	Low-voltage inhibit reset/recover hysteresis	V_{hys}	5 V	—	100	mV	
				3 V	—	60		

¹ Typical values are measured at 25 °C. Characterized, not tested

² Measured with $V_{In} = V_{DD}$ or V_{SS} .

³ Measured with $V_{In} = V_{SS}$.

⁴ Measured with $V_{In} = V_{DD}$.

⁵ All functional non-supply pins, except for PTC6 are internally clamped to V_{SS} and V_{DD} .

⁶ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁷ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. For instance, if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

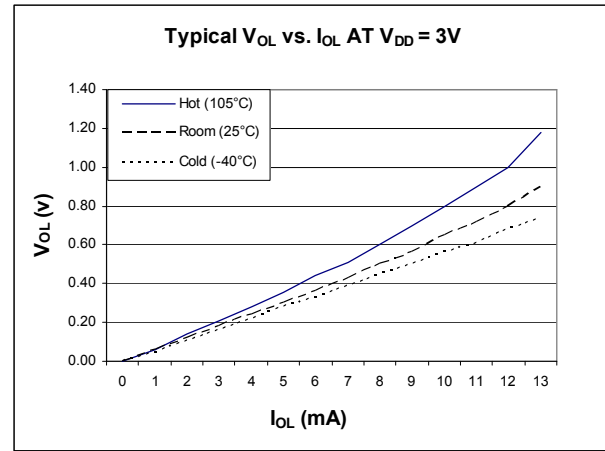
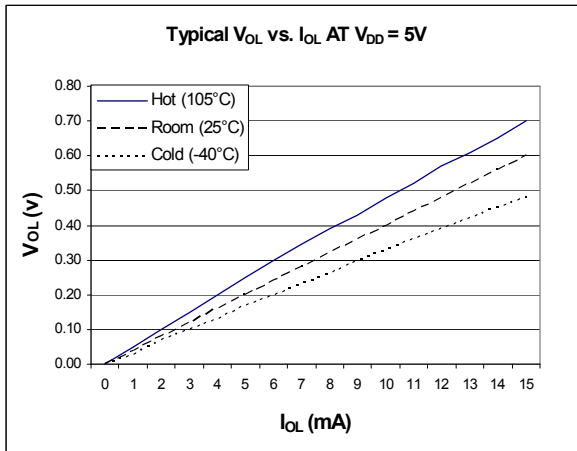


Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)

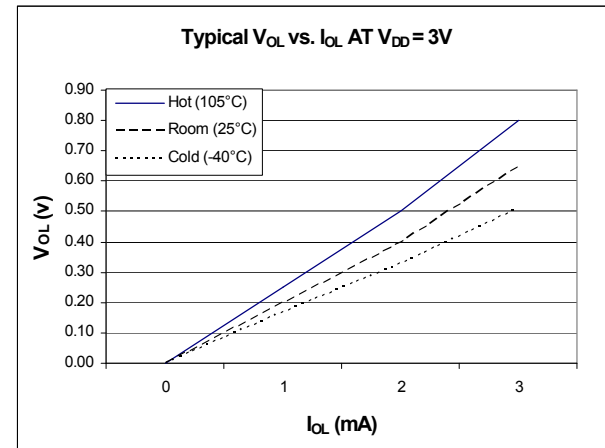
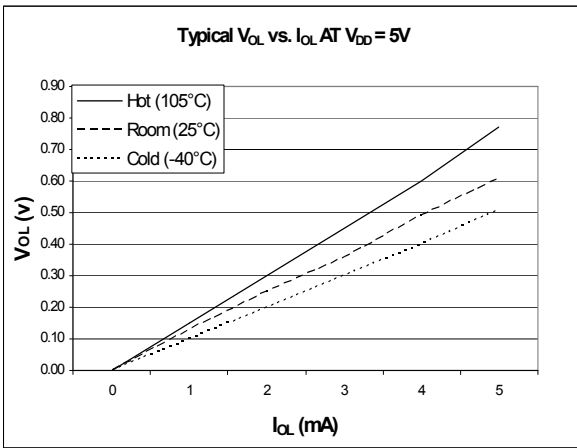


Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)

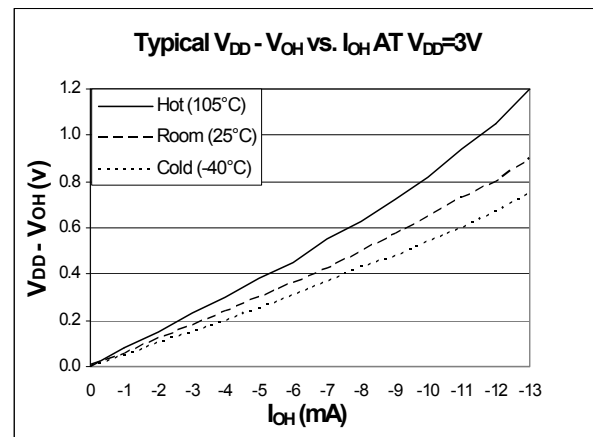
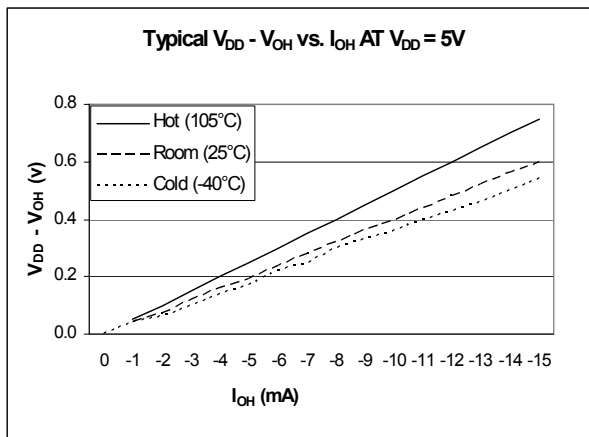


Figure 7. Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)

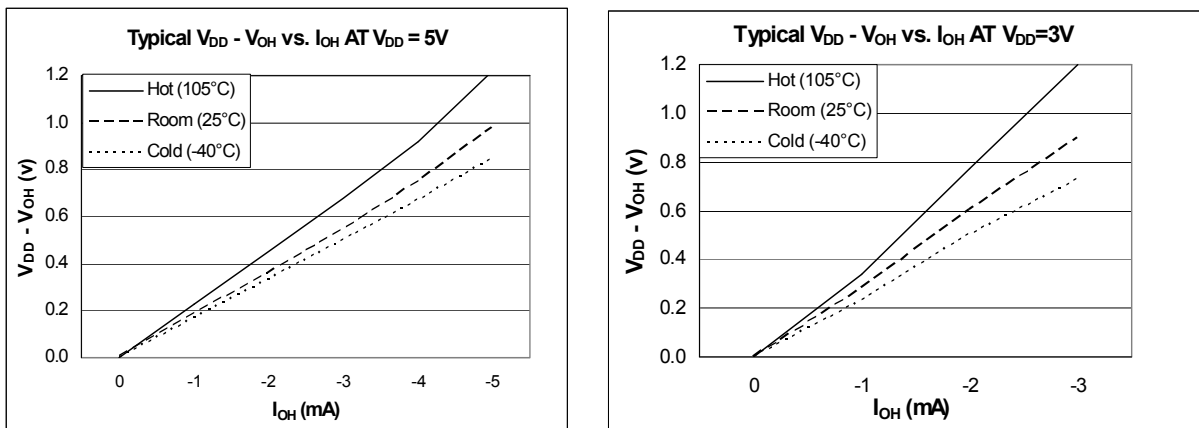


Figure 8. Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)

2.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typ ¹	Max	Unit	Temp (°C)	
1	C	Run supply current FEI mode, all modules on	RI _{DD}	20 MHz	3	16.38	27.85	mA	-40 °C to 85 °C	
	C						28.05		-40 °C to 105 °C	
	C					1 MHz	1.67		2.84	-40 °C to 85 °C
	C								2.87	-40 °C to 105 °C
	P			20 MHz	5	16.55	28.14	mA	-40 °C to 85 °C	
	P						28.35		-40 °C to 105 °C	
	C					1 MHz	1.77		3.01	-40 °C to 85 °C
	C								3.05	-40 °C to 105 °C
2	T	Run supply current FEI mode, all modules off	RI _{DD}	20 MHz	3	11.9	20.25	mA	-40 °C to 85 °C	
	T						21.72		-40 °C to 105 °C	
	T					1 MHz	1.16		1.95	-40 °C to 85 °C
	T								1.98	-40 °C to 105 °C
	T			20 MHz	5	12.68	21.56	mA	-40 °C to 85 °C	
	T						23.12		-40 °C to 105 °C	
	T					1 MHz	1.4		2.39	-40 °C to 85 °C
	T								2.41	-40 °C to 105 °C
3	T	Wait mode supply current FEI mode, all modules off	WI _{DD}	20 MHz	3	7.9	13.42	mA	-40 °C to 85 °C	
	T						13.59		-40 °C to 105 °C	
	T					1 MHz	0.88		1.49	-40 °C to 85 °C
	T								1.51	-40 °C to 105 °C
	P			20 MHz	5	8.13	13.81	mA	-40 °C to 85 °C	
	P						13.98		-40 °C to 105 °C	
	T					1 MHz	1.12		1.91	-40 °C to 85 °C
	T								1.94	-40 °C to 105 °C
4	C	Stop2 mode supply current	S2I _{DD}	n/a	3	1.1	16.0	μA	-40 °C to 85 °C	
	C						39.0		-40 °C to 105 °C	
	P					5	1.2	18.7	μA	-40 °C to 85 °C
	P							46.1		-40 °C to 105 °C
5	C	Stop3 mode supply current No clocks active	S3I _{DD}	n/a	3	1.2	22.4	μA	-40 °C to 85 °C	
	C						56.2		-40 °C to 105 °C	
	P				5	1.32	25.5	μA	-40 °C to 85 °C	
	P						63.9		-40 °C to 105 °C	

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typ ¹	Max	Unit	Temp (°C)	
6	T	Stop2 adders:	RTC using LPO	—	n/a	3	210	—	nA	-40 °C to 105 °C
			RTC using low power crystal oscillator				4.25	—	μA	
			LCD ² with rbias (Low Gain)				1.2 ³	—		
			LCD ² with rbias (High Gain)				18 ⁴	—		
			LCD ² with Cpump				4.05 ³	—		
			RTC using LPO			5	210	—	nA	-40 °C to 105 °C
			RTC using low power crystal oscillator				4.22	—	μA	
			LCD ² with rbias (Low Gain)				1.5 ³	—		
			LCD ² with rbias (High Gain)				32 ⁴	—		
			LCD ² with Cpump				7.12 ³	—		
7	T	Stop3 adders:	RTC using LPO	—	n/a	3	210	—	nA	-40 °C to 105 °C
			RTC using low power crystal oscillator				4.75	—	μA	
			LCD ² with rbias (Low Gain)				1.2 ³	—		
			LCD ² with rbias (High Gain)				18 ⁴	—		
			LCD ² with Cpump				4.35 ³	—		
			RTC using LPO			5	230	—	nA	-40 °C to 105 °C
			RTC using low power crystal oscillator				4.74	—	μA	
			LCD ² with rbias (Low Gain)				1.5 ³	—		
			LCD ² with rbias (High Gain)				32 ⁴	—		
			LCD ² with Cpump				7.49 ³	—		

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typ ¹	Max	Unit	Temp (°C)	
8	T	Stop3 adders:	EREFSTEN = 1	—	n/a	3	4.58	—	μA	-40 °C to 105 °C
			IREFSTEN = 1				71.7	—		
			LVD				94.35	—		
			EREFSTEN = 1			5	4.61	—	μA	
			IREFSTEN = 1				71.69	—		
			LVD				107.34	—		

- ¹ Typical values are measured at 25 °C. Characterized, not tested.
- ² LCD configured for Charge Pump Enabled V_{LL3} connected to V_{DD}.
- ³ This does not include current required for 32 kHz oscillator.
- ⁴ This is the maximum current when all LCD inputs/outputs are used.

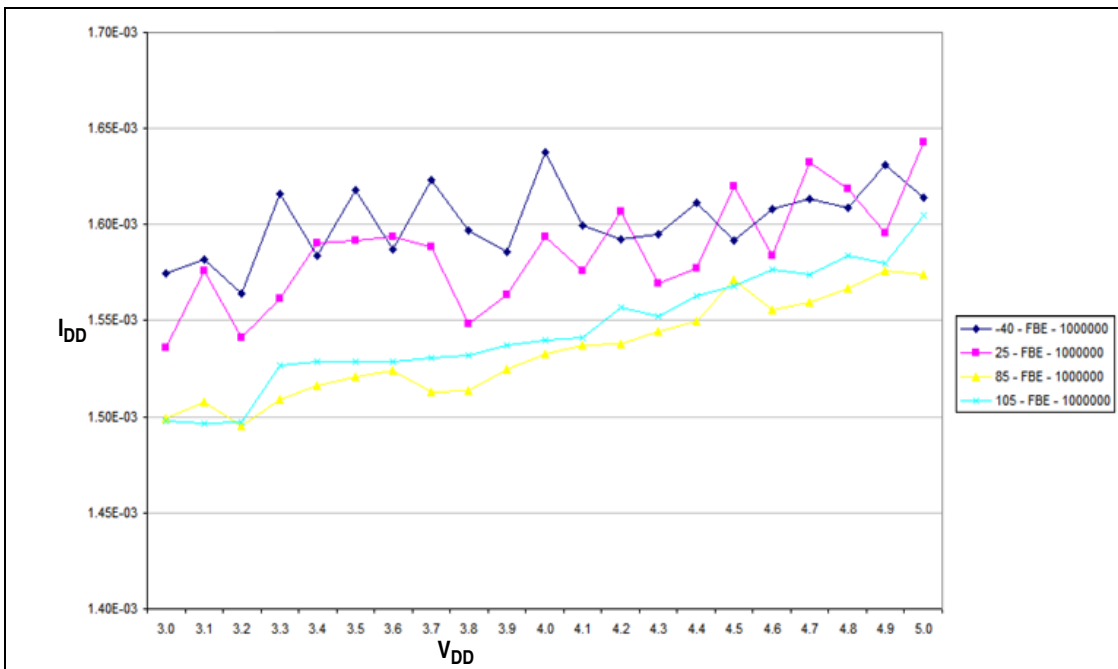


Figure 9. Typical Run I_{DD} for FBE Mode at 1 MHz

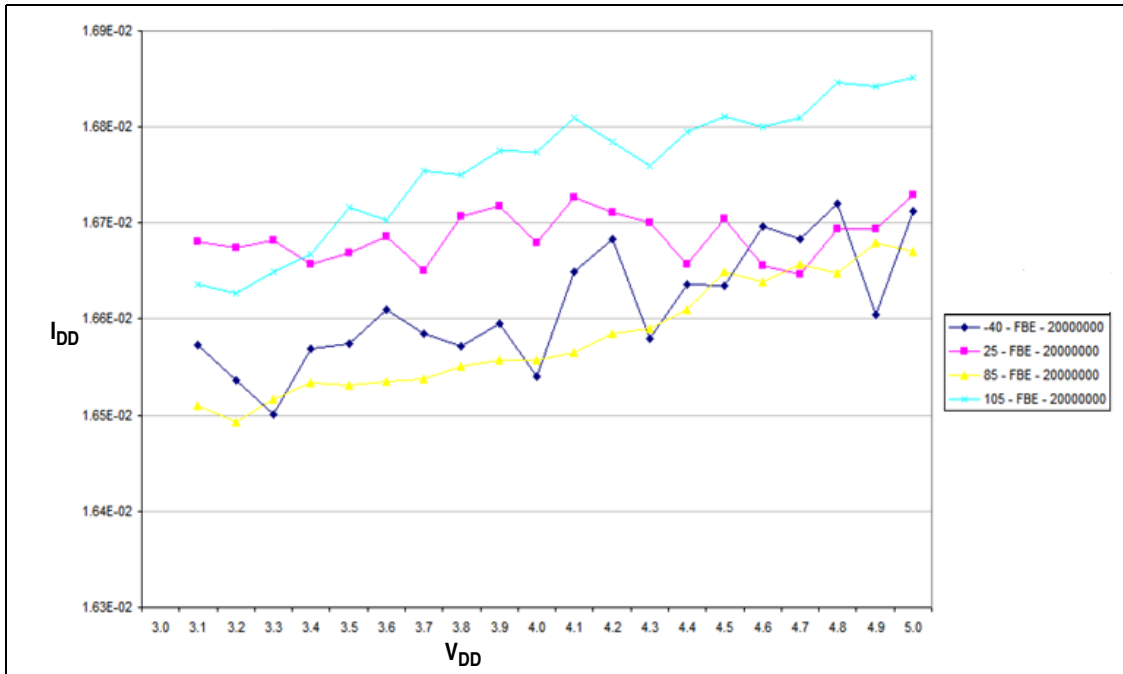


Figure 10. Typical Run I_{DD} for FBE Mode at 20 MHz

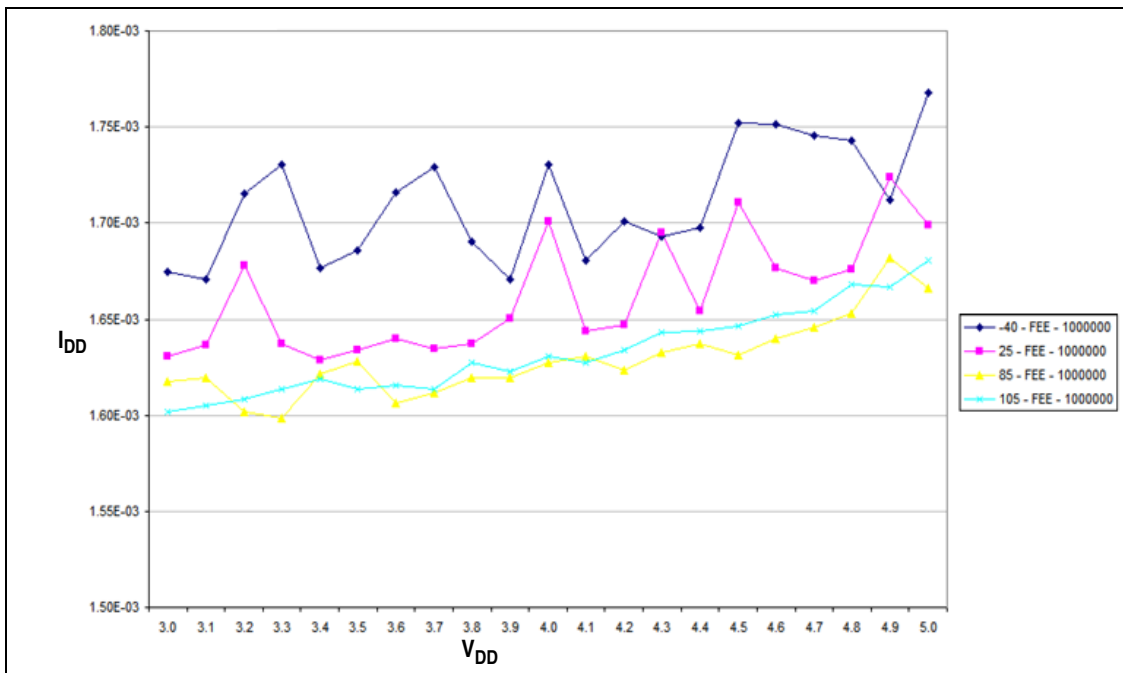


Figure 11. Typical Run I_{DD} for FEE Mode at 1 MHz

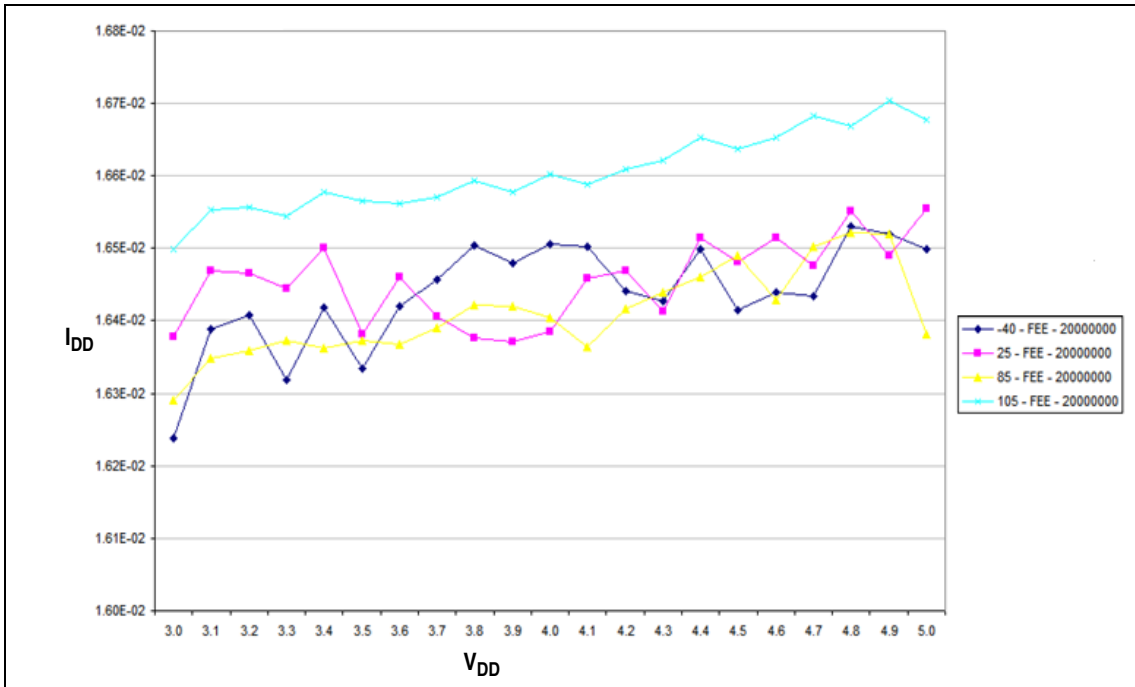


Figure 12. Typical Run I_{DD} for FEE Mode at 20 MHz

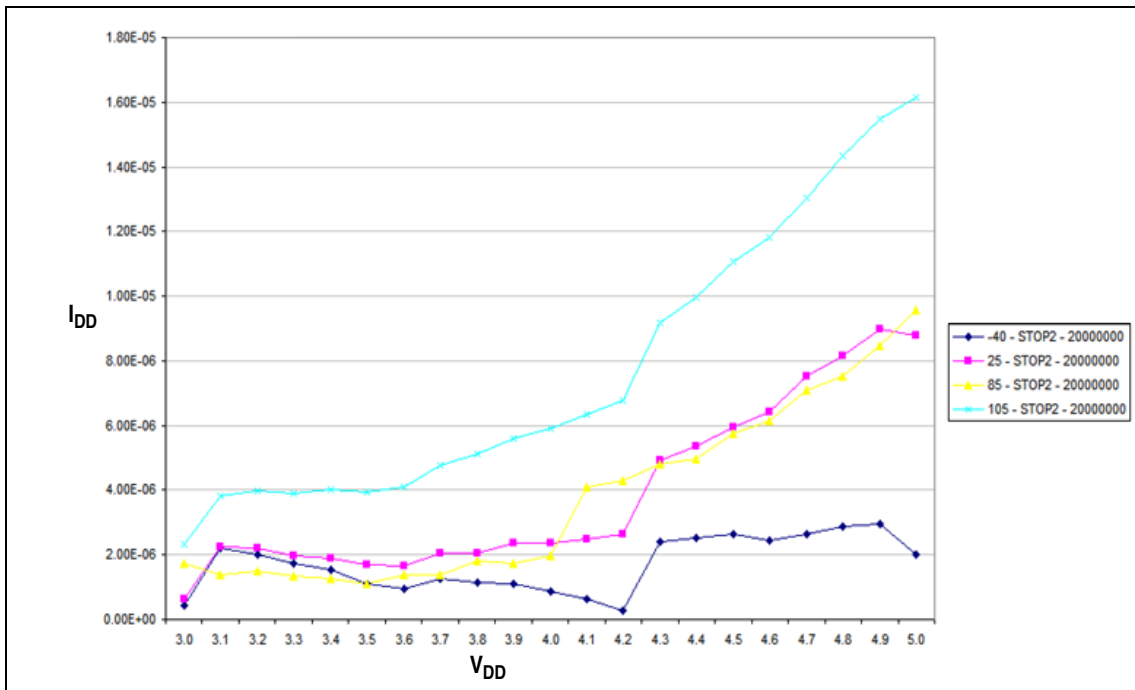


Figure 13. Typical Stop2 I_{DD}

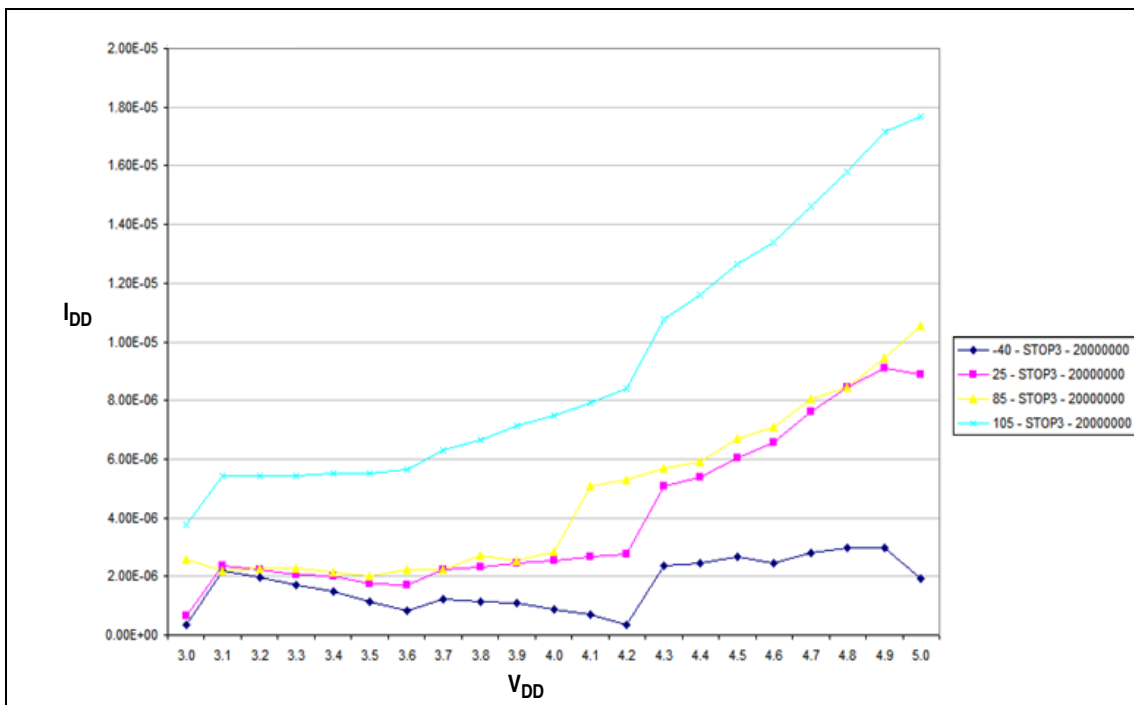


Figure 14. Typical Stop3 I_{DD}

2.8 External Oscillator (XOSC) Characteristics

Table 10. Oscillator Electrical Specifications (Temperature Range = -40 °C to 105 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit	
1	D	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) <ul style="list-style-type: none"> • Low range (RANGE = 0) • High range (RANGE = 1) FEE or FBE mode² • High range (RANGE = 1, HGO = 1) BLPE mode • High range (RANGE = 1, HGO = 0) BLPE mode 	f _{lo} f _{hi} f _{hi-hgo} f _{hi-lp}	32 1 1 1	— — — —	38.4 5 16 8	kHz MHz MHz MHz	
2	D	Load capacitors	C ₁ C ₂	See crystal or resonator manufacturer's recommendation.				

Table 10. Oscillator Electrical Specifications (Temperature Range = -40 °C to 105 °C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit
3	D	Feedback resistor • Low range (32 kHz to 100 kHz) • High range (1 MHz to 16 MHz)	R_F	— —	10 1	— —	$M\Omega$
4	D	Series resistor • Low range, low gain (RANGE = 0, HGO = 0) • Low range, high gain (RANGE = 0, HGO = 1)	R_S		0 100		$k\Omega$
5	D	Series resistor • High range, low gain (RANGE = 1, HGO = 0) • High range, high gain (RANGE = 1, HGO = 1)	R_S				$k\Omega$
		≥8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
6	T	Crystal start-up time ^{3, 4} • Low range (HGO = 0) • Low range (HGO = 1) • High range (HGO = 0) ⁵ • High range (HGO = 1) ⁵	$t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	— — — —	500 3570 4 4	— — — —	ms
7	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) • FEE or FBE mode ² • BLPE mode	f_{extal}	0.03125 0	— —	5 40	MHz

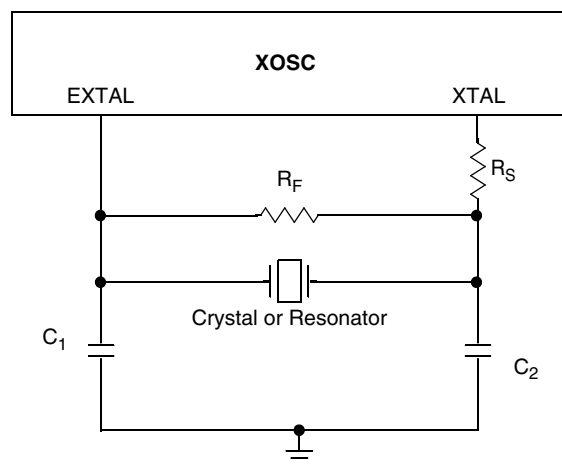
¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

³ This parameter is characterized and not tested on each device.

⁴ Proper PC board layout procedures must be followed to achieve specifications.

⁵ 4 MHz crystal


Figure 15. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

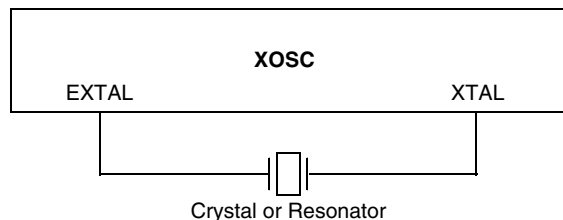


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

2.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = -40 °C to 105 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit	
1	P	Average internal reference frequency — factory trimmed at VDD = 5.0 V and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz	
2	C	Average internal reference frequency — user trimmed	f_{int_t}	31.25	—	39.0625	kHz	
3	C	Internal reference start-up time	t_{IRST}	—	60	100	μs	
4	P	DCO output frequency range — trimmed ²	f_{dco_t}	Low range (DRS = 00)	16	—	20	MHz
	P			Mid range (DRS = 01)	32	—	40	
5	P	DCO output frequency ² Reference = 32768 Hz and DMX32 = 1	f_{dco_DMX32}	Low range (DRS = 00)	—	19.92	—	MHz
	P			Mid range (DRS = 01)	—	39.85	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM) ³	$\Delta f_{dco_res_t}$	—	±0.1	±0.2	% f_{dco}	
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM) ³	$\Delta f_{dco_res_t}$	—	±0.2	±0.4	% f_{dco}	
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	-1.0 to +0.5	±2	% f_{dco}	
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C ³	Δf_{dco_t}	—	±0.5	±1	% f_{dco}	
10	C	FLL acquisition time ^{3, 4}	$t_{Acquire}$	—	—	1	mS	
11	C	Long term jitter of DCO output clock (averaged over 2 ms interval) ⁵	C_{Jitter}	—	0.02	0.2	% f_{dco}	

¹ Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

² The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

³ This parameter is characterized and not tested on each device.

⁴ This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁵ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

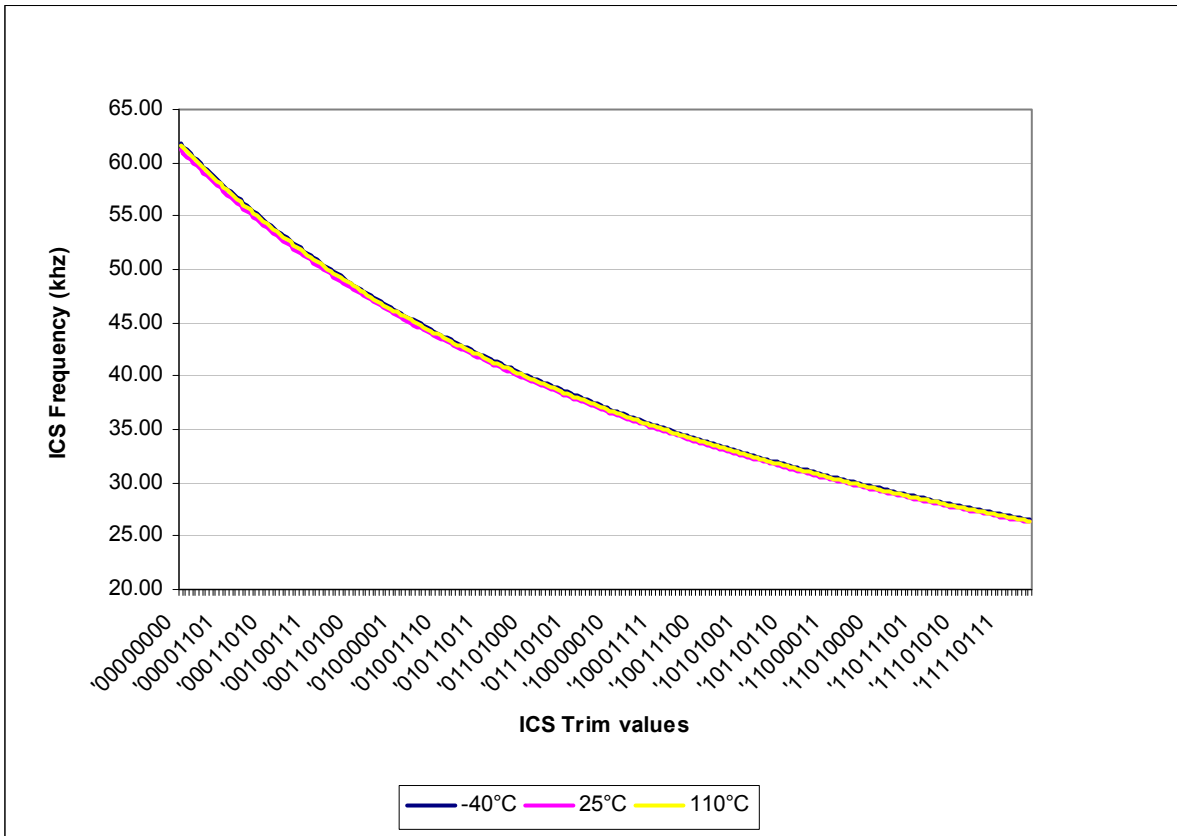


Figure 17. Internal Oscillator Deviation from Trimmed Frequency

2.10 ADC Characteristics

Table 12. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V	—
	Delta to V_{DD} $(V_{DD} - V_{DDAD})^2$	ΔV_{DDAD}	-100	0	+100	mV	—
Ground voltage	Delta to V_{SS} $(V_{SS} - V_{SSAD})^2$	ΔV_{SSAD}	-100	0	+100	mV	—
Ref Voltage High	—	V_{REFH}	—	—	—	V	V_{REFH} shorted to V_{DDAD}
Ref Voltage Low	—	V_{REFL}	—	—	—	V	V_{REFL} shorted to V_{SSAD}
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—

Table 13. 12-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

Num	C	Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
1	T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	195	—	μA	—
2	T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	347	—	μA	—
3	T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	407	—	μA	—
4	P	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	0.755	1	mA	—
5	—	Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.011	1	μA	—
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
			Low Power (ADLPC=1)		1.25	2	3.3		
7	C	Conversion Time (Including sample time)	Short sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See ADC chapter in the LG32 Reference Manual for conversion time variances
			Long sample (ADLSMP=1)		—	40	—		
8	C	Sample Time	Short sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long sample (ADLSMP=1)		—	23.5	—		
9	T	Total Unadjusted Error	12-bit mode	E_{TUE}	—	± 3.0	—	LSB ²	Includes quantization
	P		10-bit mode		—	± 1	± 2.5		
	T		8-bit mode		—	± 0.5	± 1		
10	T	Differential Non-Linearity	12-bit mode	DNL	—	± 1.75	—	LSB ²	
	P		10-bit mode ³		—	± 0.5	± 1.0		
	T		8-bit mode ³		—	± 0.3	± 0.5		
11	T	Integral Non-Linearity	12-bit mode	INL	—	± 1.5	—	LSB ²	
	P		10-bit mode		—	± 0.5	± 1		
	T		8-bit mode		—	± 0.3	± 0.5		
12	T	Zero-Scale Error	12-bit mode	E_{ZS}	—	± 1.5	—	LSB ²	$V_{ADIN} = V_{SSAD}$
	P		10-bit mode		—	± 0.5	± 1.5		
	T		8-bit mode		—	± 0.5	± 0.5		

Table 13. 12-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
13	T	Full-Scale Error	12-bit mode	E_{FS}	—	± 1	—	LSB ²	$V_{ADIN} = V_{DDAD}$
	P		10-bit mode		—	± 0.5	± 1		
	T		8-bit mode		—	± 0.5	± 0.5		
14	D	Quantization Error	12-bit mode	E_Q	—	-1 to 0	—	LSB ²	—
			10-bit mode		—	—	± 0.5		
			8-bit mode		—	—	± 0.5		
15	D	Input Leakage Error	12-bit mode	E_{IL}	—	± 1	—	LSB ²	Pad leakage ^{4*} R_{AS}
			10-bit mode		—	± 0.2	± 2.5		
			8-bit mode		—	± 0.1	± 1		
16	C	Temp Sensor Slope	-40 °C to 25 °C	m	—	1.646	—	mV/°C	—
			25 °C to 125 °C		—	1.769	—		
17	C	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	—

¹ Typical values assume $V_{DDAD} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$

³ Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes

⁴ Based on input pad leakage current. Refer to pad electricals.

2.11 AC Characteristics

This section describes timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 14. Control Timing

Num	C	Rating	Symbol	Min	Typ ¹	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μ s
3	D	External reset pulse width ²	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$66 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ³	t_{MSH}	100	—	—	μ s
7	D	IRQ pulse width Asynchronous path ² Synchronous path ⁴	t_{LIH} t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path ² Synchronous path ⁴	t_{LIH} t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns
9	C	Port rise and fall time — (load = 50 pF) ^{5, 6} Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise} t_{Fall}	— —	3 30	— —	ns

¹ Typical values are based on characterization data at $V_{DD} = 5.0$ V, 25 °C unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

³ To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .

⁴ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

⁵ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

⁶ Except for LCD pins in Open Drain mode.

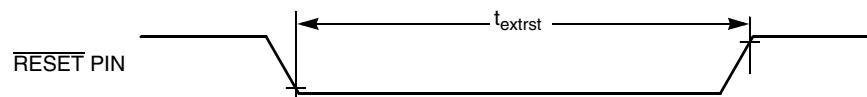


Figure 19. Reset Timing

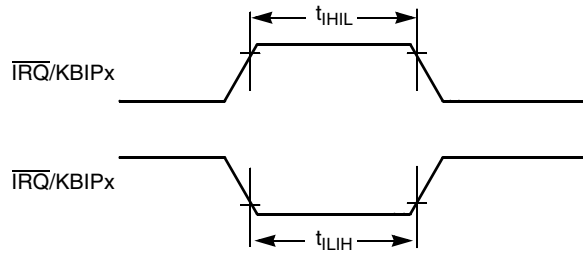


Figure 20. $\overline{\text{IRQ/KBIPx}}$ Timing

2.11.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 15. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{\text{Bus}}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

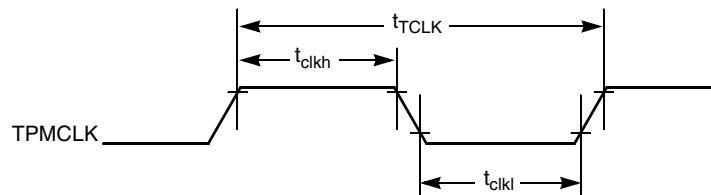


Figure 21. Timer External Clock

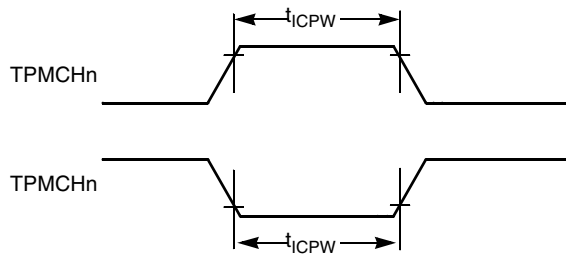


Figure 22. Timer Input Capture Pulse

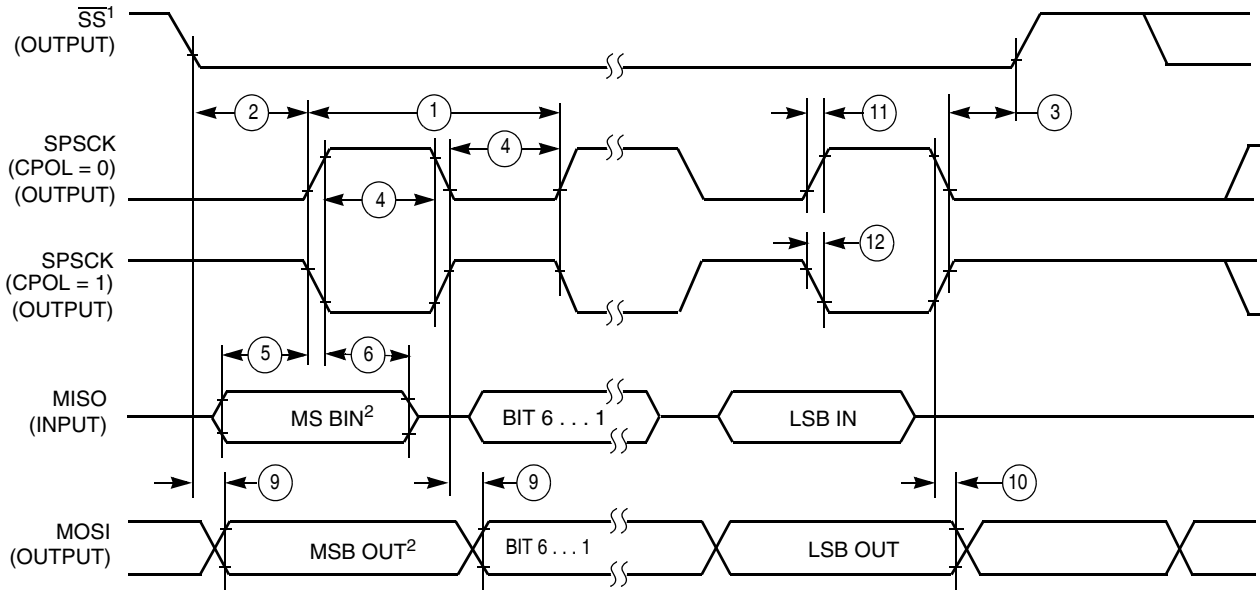
2.11.3 SPI Timing

Table 16 and Figure 23 through Figure 26 describe the timing requirements for the SPI system.

Table 16. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	$1024 t_{cyc}$ —	ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
⑩	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
⑪	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
⑫	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns

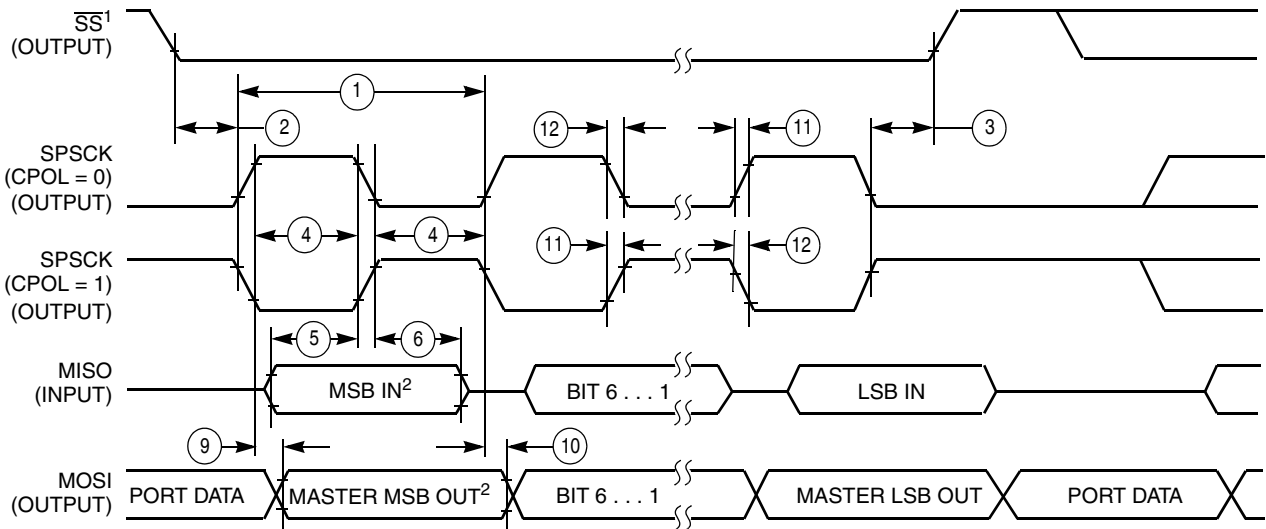
Electrical Characteristics



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

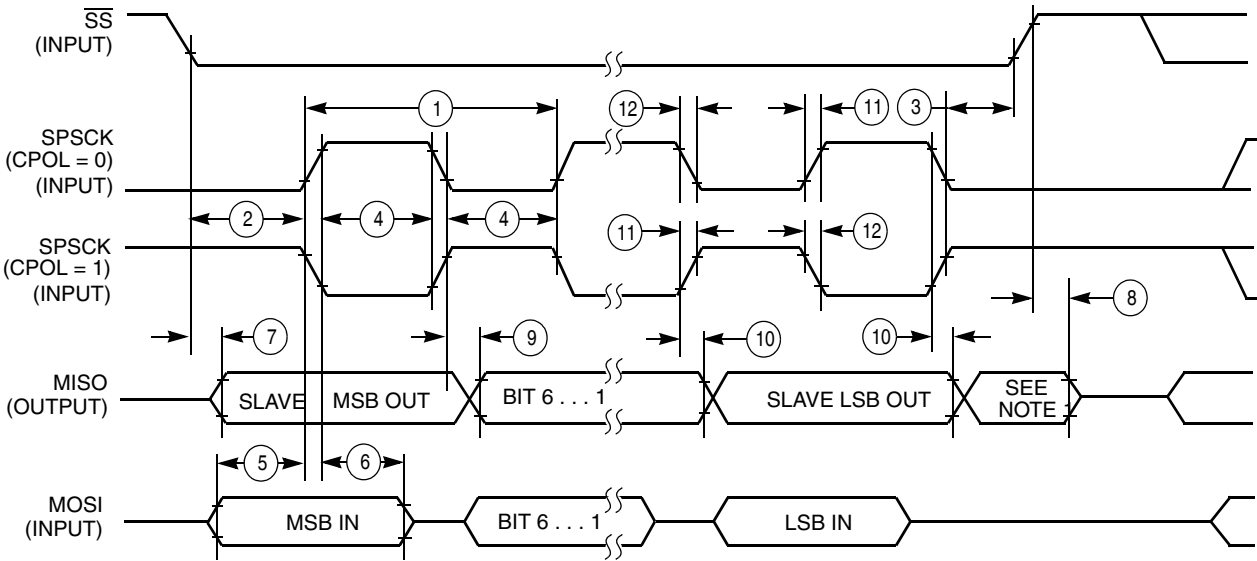
Figure 23. SPI Master Timing (CPHA = 0)



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

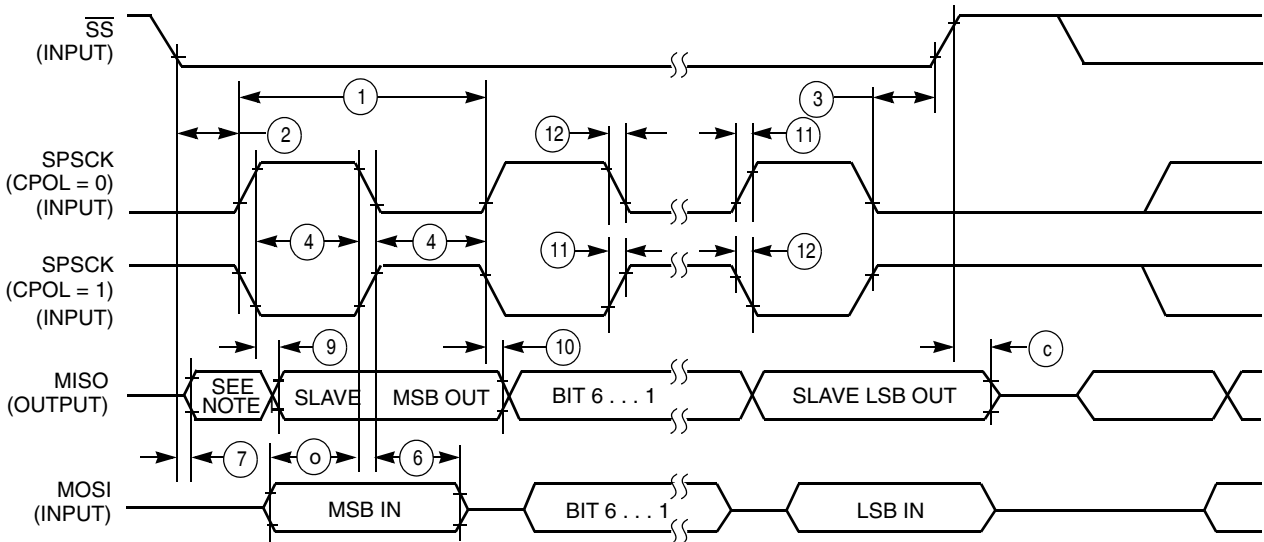
Figure 24. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received.

Figure 25. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 26. SPI Slave Timing (CPHA = 1)

2.12 LCD Specifications

Table 17. LCD Electricals, 3 V Glass

C	Characteristic	Symbol	Min	Typ	Max	Units
D	VLL3 Supply Voltage	VLL3	2.7	—	5.5	V
D	LCD Frame Frequency	f _{Frame}	28	30	64	Hz
D	LCD Charge Pump Capacitance	C _{LCD}	—	100	100	pF
D	LCD Bypass Capacitance	C _{BYLCD}	—	100	100	
D	LCD Glass Capacitance	C _{glass}	—	2000	8000	

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 18. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	V _{prog/erase}	2.7		5.5	V
D	Supply voltage for read operation	V _{Read}	2.7		5.5	V
D	Internal FCLK frequency ¹	f _{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t _{Fcyc}	5		6.67	μs
C	Byte program time (random location) ²	t _{prog}		9		t _{Fcyc}
C	Byte program time (burst mode) ²	t _{Burst}		4		t _{Fcyc}
C	Page erase time ²	t _{Page}		4000		t _{Fcyc}
C	Mass erase time ²	t _{Mass}		20,000		t _{Fcyc}
D	Byte program current ³	R _{IDDBP}	—	4	—	mA
D	Page erase current ³	R _{IDDPE}	—	6	—	mA
C	Program/erase endurance ⁴ T _L to T _H = –40 °C to + 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention ⁵	t _{D_ret}	15	100	—	years

¹ The frequency of this clock is controlled by a software setting.

² These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

³ The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 5.0 V, bus frequency = 4.0 MHz.

⁴ **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to *Engineering Bulletin EB619, Typical Endurance for Nonvolatile Memory*.

⁵ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to *Engineering Bulletin EB618, Typical Data Retention for Nonvolatile Memory*.

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 19. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{osc}/f_{BUS}	Level ¹ (Max)	Unit	
Radiated emissions, electric field	V_{RE_TEM}	$V_{DD} = 5.5$ $T_A = +25\text{ }^\circ\text{C}$ Package type = 80 LQFP	0.15 – 50 MHz	4 MHz crystal 16 MHz bus	10	dB μ V	
			50 – 150 MHz		14		
			150 – 500 MHz		8		
			500 – 1000 MHz		5		
			IEC Level		L		—
			SAE Level		2		—

¹ Data based on qualification test results.

2.14.2 Conducted Transient Susceptibility

Microcontroller transient conducted susceptibility is measured in accordance with an internal Freescale test method. The measurement is performed with the microcontroller installed on a custom EMC evaluation board and running specialized EMC test software designed in compliance with the test method. The conducted susceptibility is determined by injecting the transient susceptibility signal on each pin of the microcontroller. The transient waveform and injection methodology is based on IEC 61000-4-4 (EFT/B). The transient voltage required to cause performance degradation on any pin in the tested configuration is greater than or equal to the reported levels unless otherwise indicated by footnotes below [Table 20](#).

Table 20. Conducted Susceptibility, EFT/B

Parameter	Symbol	Conditions	f_{osc}/f_{BUS}	Result	Amplitude ¹ (Min)	Unit
Conducted susceptibility, electrical fast transient/burst (EFT/B)	V_{CS_EFT}	$V_{DD} = 5.5$ $T_A = +25\text{ }^\circ\text{C}$ Package type = 80-pin LQFP	4 kHz crystal 4 MHz bus	A B C D	>4.0 ² >4.0 ³ >4.0 ⁴ >4.0	kV

¹ Data based on qualification test results. Not tested in production.

² Exceptions as covered in footnotes 3 and 4.

Electrical Characteristics

- ³ Except pins PHT1, PTH2, PTH3, PTH4, PTH5. See figures below for values.
- ⁴ Except pins PTF3, PTH5, PTH4, PHT0, Reset, and BKGD. See figures below for values.

Individual performance of each pin is shown in [Figure 27](#), [Figure 28](#), [Figure 29](#), and [Figure 30](#).

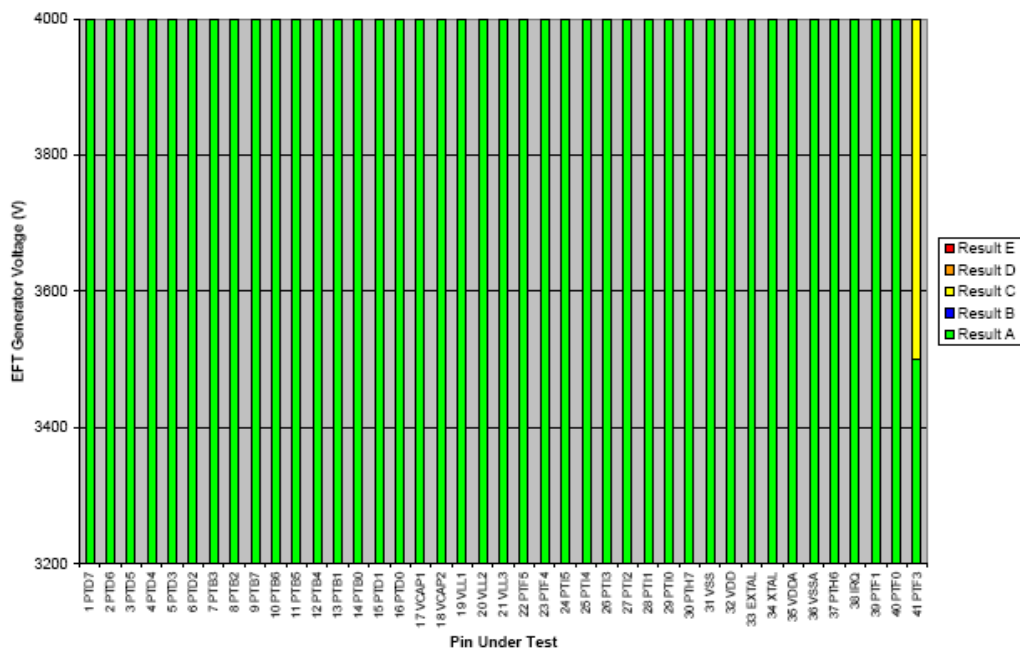
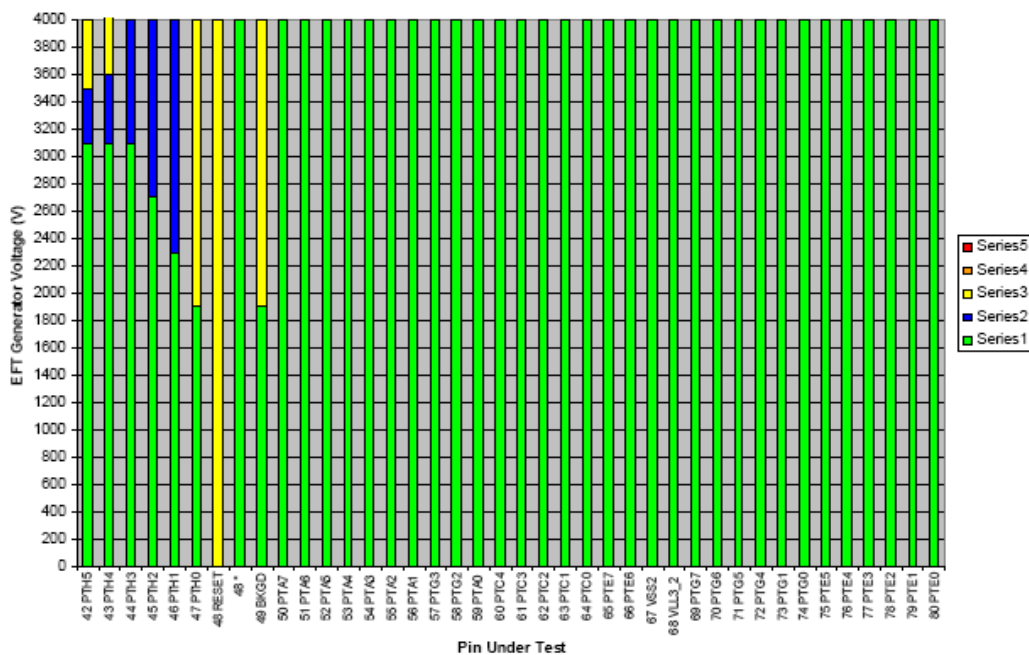


Figure 27. 4 MHz, Positive Polarity Pins 1 – 41



Note:

RESET retested with 0.1 μF capacitor from pin to ground is Class A compliant as shown by 48*.

Figure 28. 4 MHz, Positive Polarity Pins 42 – 80

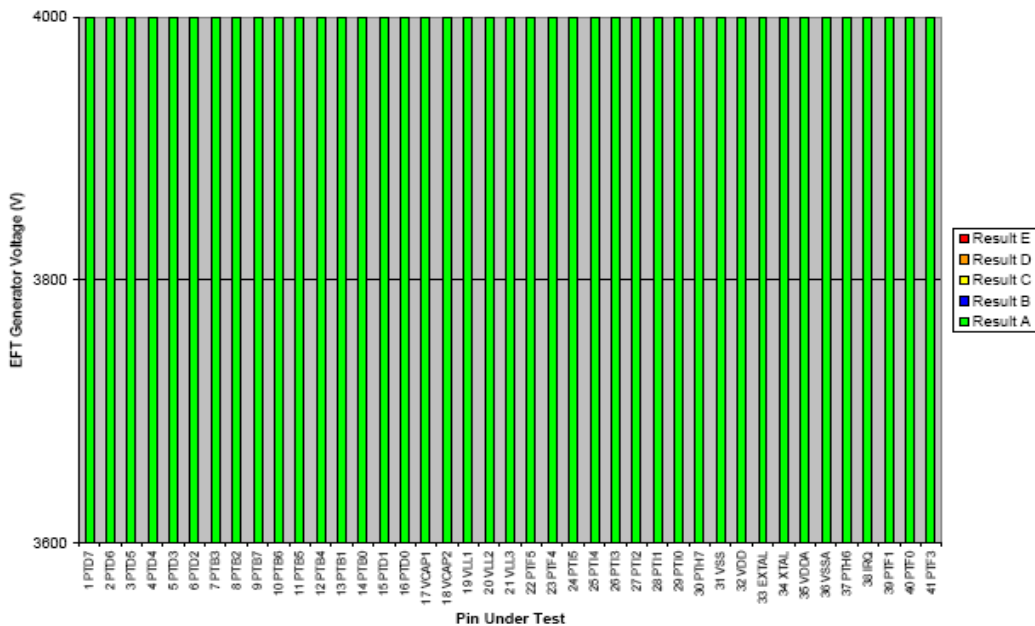
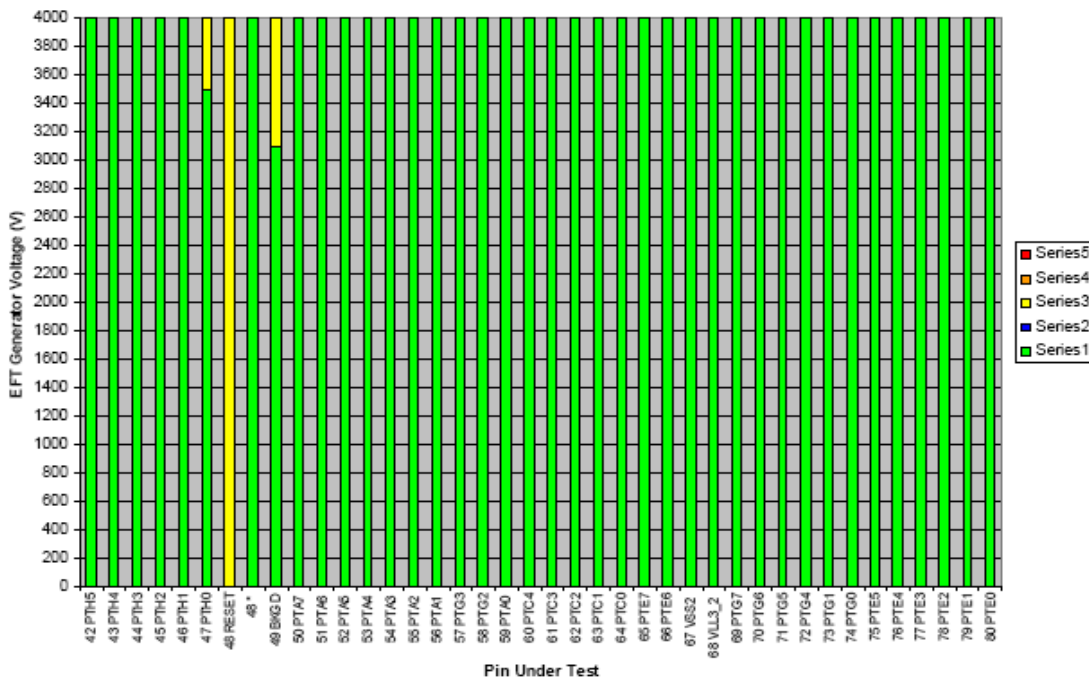


Figure 29. 4 MHz, Negative Polarity Pins 1 – 41



Note:

RESET retested with 0.1 μF capacitor from pin to ground is Class A compliant as shown by 48*.

Figure 30. 4 MHz, Negative Polarity Pins 42 – 80

Ordering Information

The susceptibility performance classification is described in [Table 21](#).

Table 21. Susceptibility Performance Classification

Result	Performance Criteria	
A	No failure	The MCU performs as designed during and after exposure.
B	Self-recovering failure	The MCU does not perform as designed during exposure. The MCU returns automatically to normal operation after exposure is removed.
C	Soft failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the RESET pin is asserted.
D	Hard failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the power to the MCU is cycled.
E	Damage	The MCU does not perform as designed during and after exposure. The MCU cannot be returned to proper operation due to physical damage or other permanent performance degradation.

3 Ordering Information

This section contains ordering information for MC9S08LG32 and MC9S08LG16 devices.

Table 22. Device Numbering System

Device Number ¹	Memory		Temperature Range (°C)	LCD Mode Operation	Available Packages ²
	FLASH	RAM			
Auto					
S9S08LG32J0CLK	32 KB	1984	-40 °C to +85 °C	Charge Pump	80-pin LQFP
S9S08LG32J0CLH					64-pin LQFP
S9S08LG32J0CLF					48-pin LQFP
S9S08LG32J0VLK	32 KB	1984	-40 °C to +105 °C	Register Bias	80-pin LQFP
S9S08LG32J0VLH					64-pin LQFP
S9S08LG32J0VLF					48-pin LQFP
S9S08LG16J0VLH	18 KB	1984			64-pin LQFP
S9S08LG16J0VLF					48-pin LQFP
IMM					
MC9S08LG32CLK	32 KB	1984	-40 °C to + 85 °C	Charge Pump	80-pin LQFP
MC9S08LG32CLH					64-pin LQFP
MC9S08LG32CLF					48-pin LQFP
MC9S08LG16CLH	18 KB	1984			64-pin LQFP
MC9S08LG16CLF					48-pin LQFP

¹ See the *MC9S08LG32 Reference Manual* (document MC9S08LG32RM), for a complete description of modules included on each device.

² See [Table 23](#) for package information.

3.1 Device Numbering System

Example of the device numbering system:

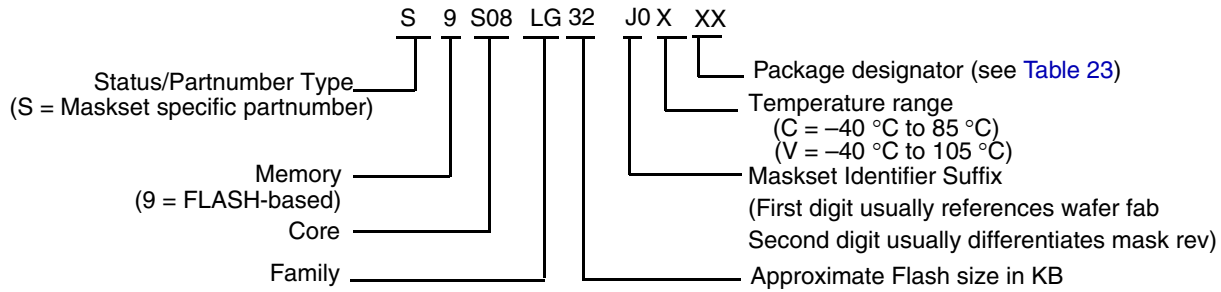


Figure 31. Device Number Example for Auto Parts

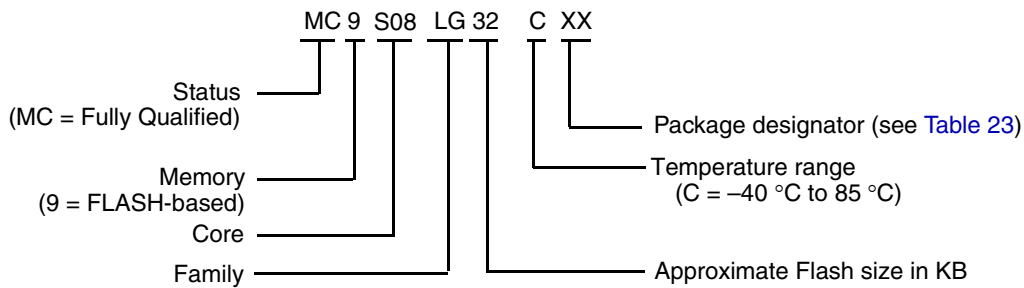


Figure 32. Device Number Example for IMM Parts

4 Package Information

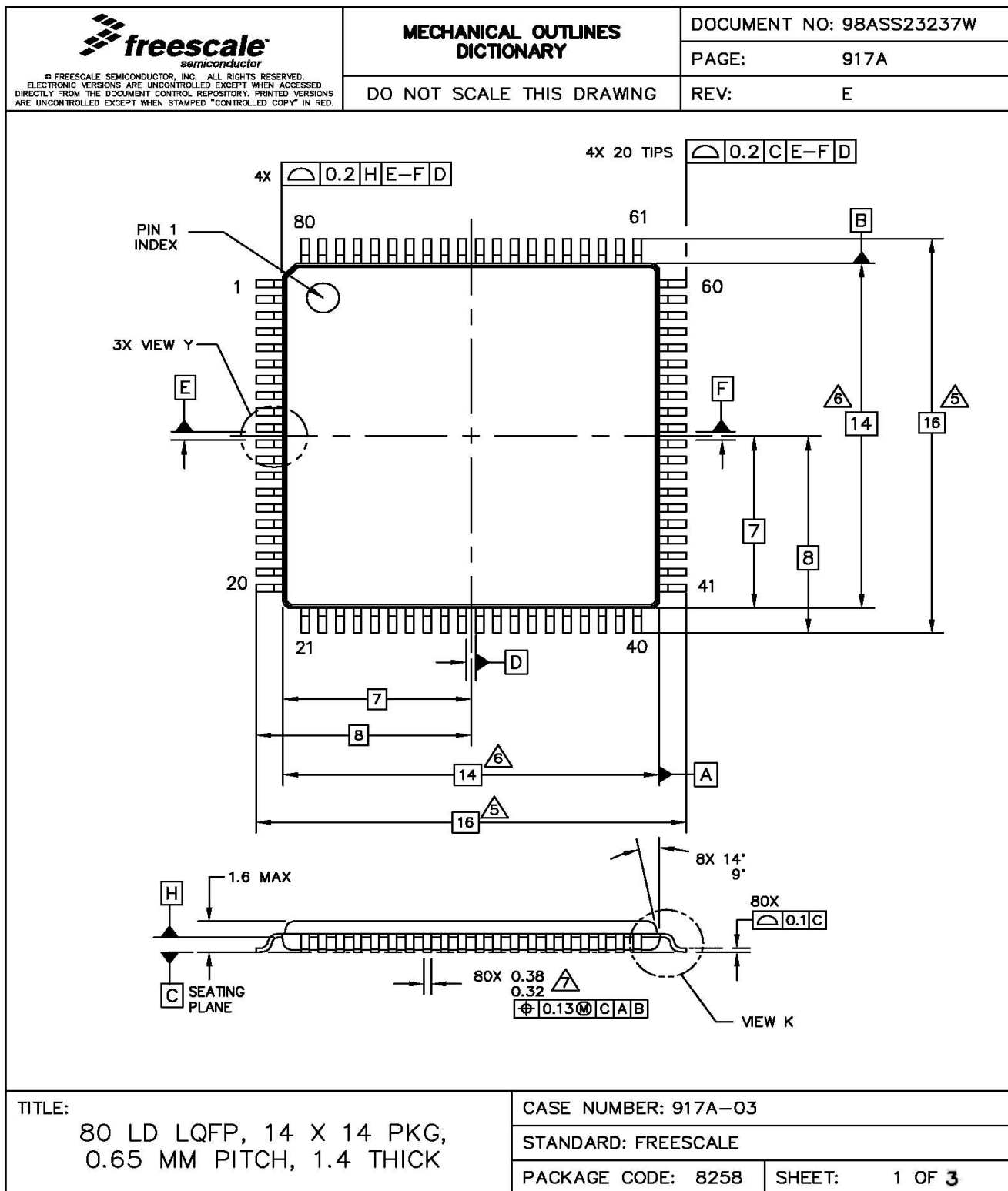
Table 23. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Low Quad Flat Package	LQFP	LF	932	98ASH00962A

4.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 23. For the latest available drawings please visit our web site (<http://www.freescale.com>) and enter the package’s document number into the keyword search box.

4.1.1 80-pin LQFP



TITLE:
80 LD LQFP, 14 X 14 PKG,
0.65 MM PITCH, 1.4 THICK

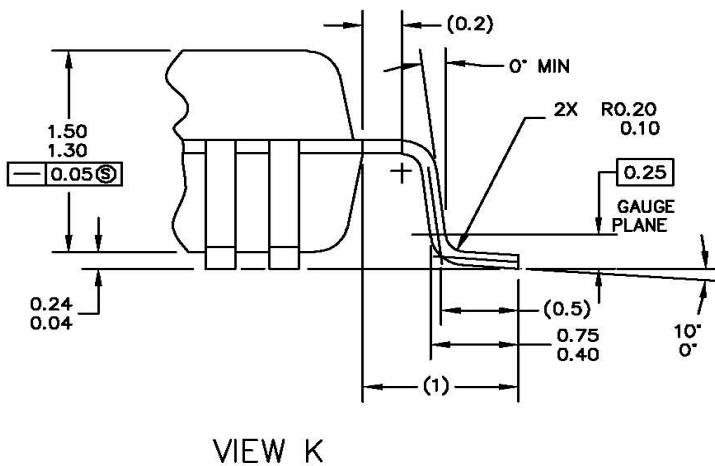
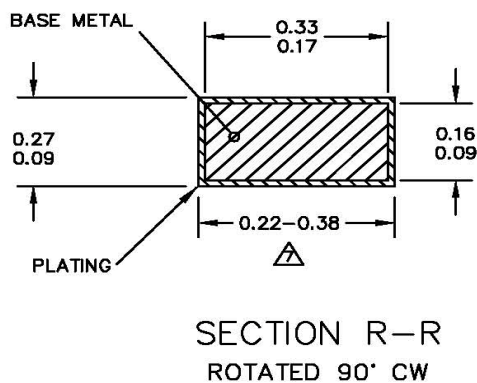
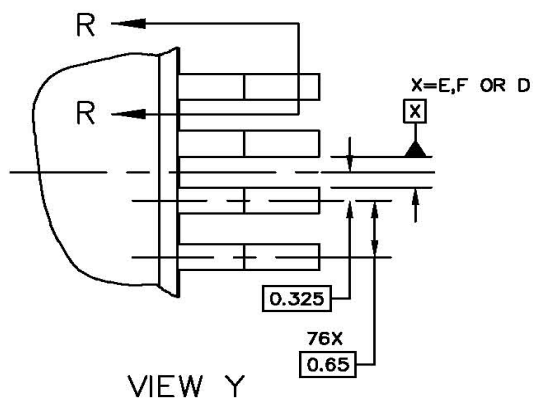
CASE NUMBER: 917A-03

STANDARD: FREESCALE

PACKAGE CODE: 8258

SHEET: 1 OF 3

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	DO NOT SCALE THIS DRAWING	PAGE: 917A
		REV: E

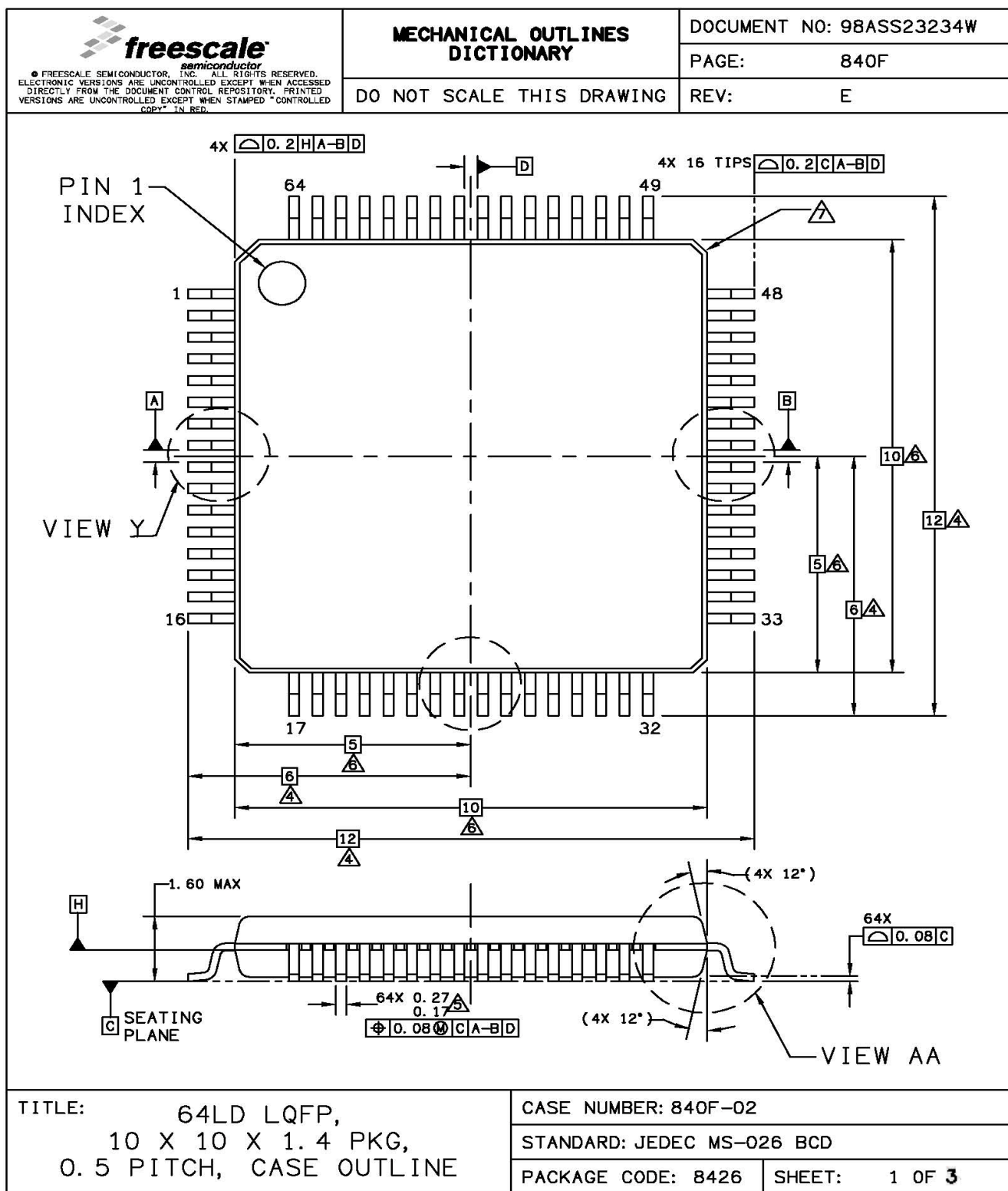


TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A-03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 2 OF 3

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		PAGE:	917A
		REV:	E
<p>NOTES:</p> <ol style="list-style-type: none"> DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. CONTROLLING DIMENSION : MILIMETER. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H. <p>⚠ DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.</p> <p>⚠ DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.</p> <p>⚠ DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.</p>			
<p>TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK</p>		CASE NUMBER: 917A-03	
		STANDARD: FREESCALE	
		PACKAGE CODE: 8258	SHEET: 3 OF 3

Figure 33. 80-pin LQFP Package Drawing (Case 917A, Doc #98ASS23237W)

4.1.2 64-pin LQFP



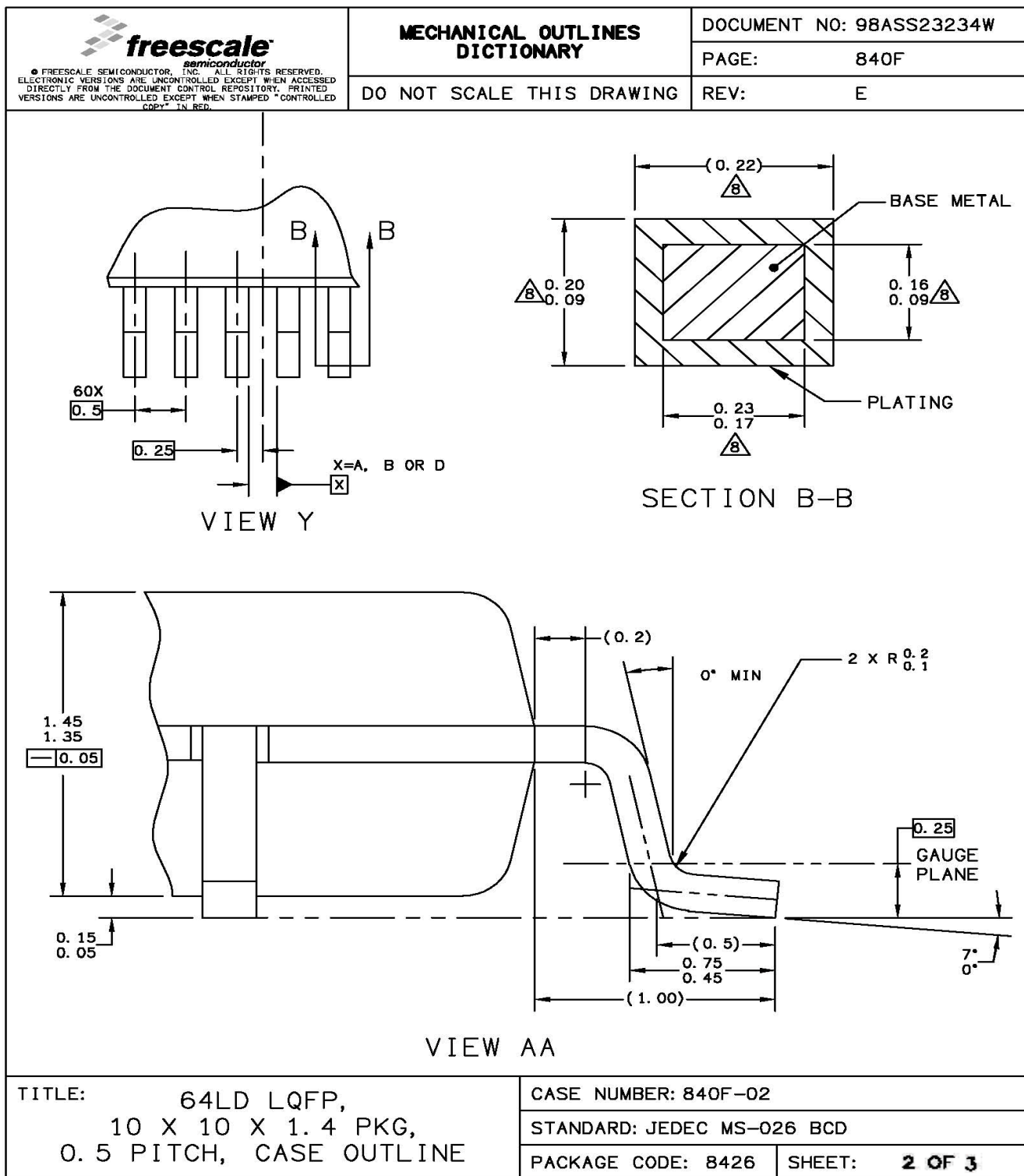
TITLE: 64LD LQFP,
10 X 10 X 1.4 PKG,
0.5 PITCH, CASE OUTLINE

CASE NUMBER: 840F-02

STANDARD: JEDEC MS-026 BCD

PACKAGE CODE: 8426

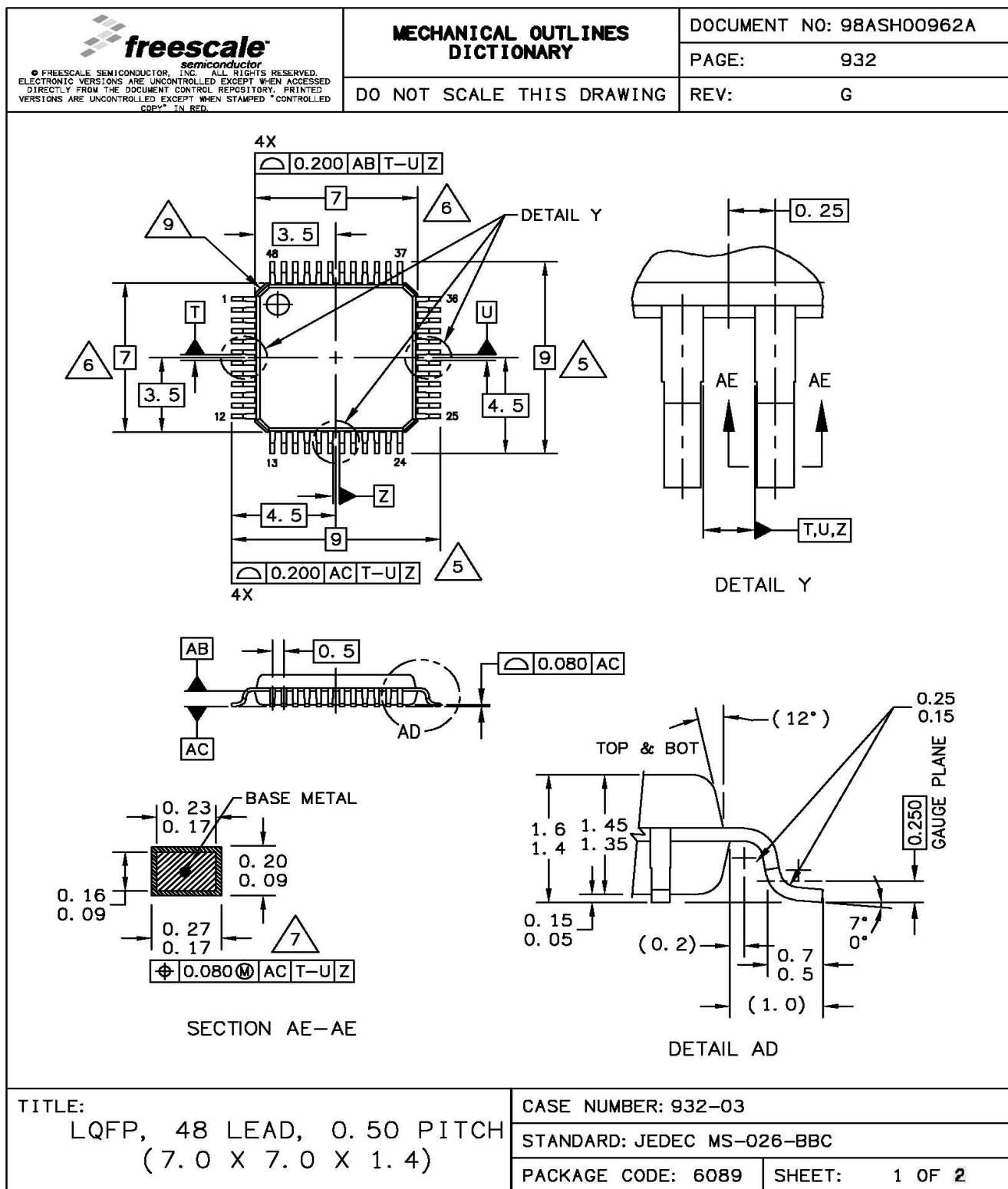
SHEET: 1 OF 3



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		PAGE:	840F
DO NOT SCALE THIS DRAWING		REV:	E
<p>NOTES:</p> <ol style="list-style-type: none"> 1. DIMENSIONS ARE IN MILLIMETERS. 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. 3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H. 4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C. 5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm. 6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH. 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL. 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP. 			
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE		CASE NUMBER: 840F-02	
		STANDARD: JEDEC MS-026 BCD	
		PACKAGE CODE: 8426	SHEET: 3 OF 3

Figure 34. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W)

4.1.3 48-pin LQFP



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	DO NOT SCALE THIS DRAWING	PAGE:	932
		REV:	G
<p>NOTES:</p> <ol style="list-style-type: none"> 1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE. 4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB. 5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC. 6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB. 7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350. 8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076. 9. EXACT SHAPE OF EACH CORNER IS OPTIONAL. 			
TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)		CASE NUMBER: 932-03	
		STANDARD: JEDEC MS-026-BBC	
		PACKAGE CODE: 6089	SHEET: 2 OF 2

Figure 35. 48-pin LQFP Package Drawing (Case 932, Doc #98ASH00962A)

5 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://www.freescale.com>

The following revision history table summarizes changes contained in this document.

Table 24. Revision History

Revision	Date	Description of Changes
1	8/2008	First Initial release.
2	9/2008	Second Initial Release.
3	11/2008	Alpha Customer Release.
4	2/2009	Launch Release.
5	4/2009	Added EMC Radiated Emission and Transient Susceptibility data in Table 19 and Table 20 .
6	4/2009	Updated EMC performance data.
7	8/2009	Updated auto part numbers, changed TCLK, T0CH0, T0CH1, T1CH0, T1CH1, T1CH2, T1CH3, T1CH3, T1CH4, and T1CH5 to TPMCLK, TPM0CH0, TPM0CH1, TPM1CH0, TPM1CH1, TPM1CH2, TPM1CH3, TPM1CH4, and TPM1CH5, and changed the maximum LCD frame frequency to 64 Hz.
8	8/2011	Updated Table "ICS Frequency Specifications (Temperature Range = -40 xC to 105 xC Ambient)". Changed the value of row 8 column C from C to P.
9	9/2011	Updated Table "ICS Frequency Specifications (Temperature Range = -40 xC to 105 xC Ambient)". Removed Footnote from Row 8. Updated the Revision History

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Document Number: MC9S08LG32
Rev. 10
04/2015

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