



**THE DATASHEET OF  
CD74FCT245MG4**

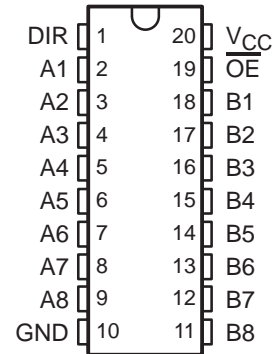


# CD74FCT245 BiCMOS OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCBS721 – JULY 2000

- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Noninverted Outputs
- Input/Output Isolation From  $V_{CC}$
- Controlled Output Edge Rates
- 64-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- Package Options Include Plastic Small-Outline (M) and Shrink Small-Outline (SM) Packages and Standard Plastic (E) DIP

E, M, OR SM PACKAGE  
(TOP VIEW)



## description

The CD74FCT245 is an octal bus transceiver with 3-state outputs using a small-geometry BiCMOS technology. The output stages are a combination of bipolar and CMOS transistors that limit the output high level to two diode drops below  $V_{CC}$ . This resultant lowering of output swing (0 V to 3.7 V) reduces the power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes  $V_{CC}$  bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 mA.

The CD74FCT245 allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CD74FCT245 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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**TEXAS  
INSTRUMENTS**

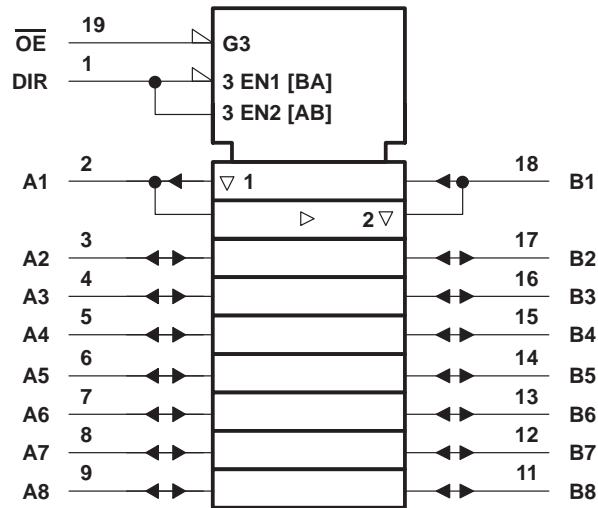
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# CD74FCT245 BiCMOS OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

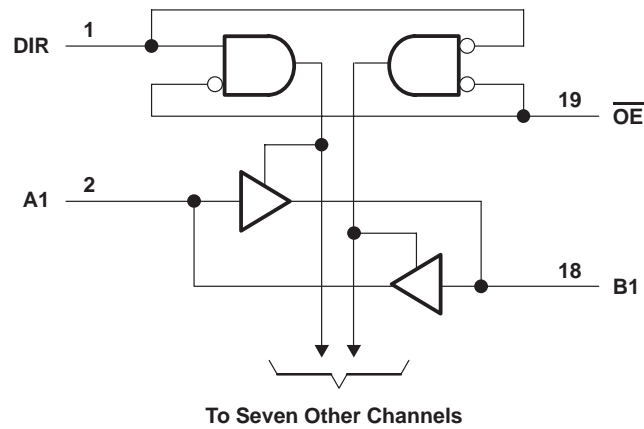
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



**CD74FCT245**  
**BiCMOS OCTAL BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCBS721 – JULY 2000

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

DC supply voltage range, $V_{CC}$ .....	-0.5 V to 6 V
DC input clamp current, $I_{IK}$ ( $V_I < -0.5$ V) .....	-20 mA
DC output clamp current, $I_{OK}$ ( $V_O < -0.5$ V) .....	-50 mA
DC output sink current per output pin, $I_{OL}$ .....	70 mA
DC output source current per output pin, $I_{OH}$ .....	-30 mA
Continuous current through $V_{CC}$ , $I_{CC}$ .....	140 mA
Continuous current through GND) .....	528 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): E package) .....	69°C/W
M package) .....	58°C/W
SM package) .....	70°C/W
Storage temperature range, $T_{stg}$ ) .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions (see Note 2)**

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5.25	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		-15	mA
$I_{OL}$ Low-level output current		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0	10	ns/V
$T_A$ Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
$V_{IK}$	$I_I = -18$ mA	4.75 V		-1.2		-1.2	V
$V_{OH}$	$I_{OH} = -15$ mA	4.75 V	2.4		2.4		V
$V_{OL}$	$I_{OL} = 64$ mA	4.75 V		0.55		0.55	V
$I_I$	$V_I = V_{CC}$ or GND	5.25 V		$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.25 V		$\pm 0.5$		$\pm 10$	$\mu\text{A}$
$I_{OS}^\ddagger$	$V_I = V_{CC}$ or GND, $V_O = 0$	5.25 V		-60		-60	mA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.25 V		8		80	$\mu\text{A}$
$\Delta I_{CC}^\S$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.25 V		1.6		1.6	mA
$C_i$	$V_I = V_{CC}$ or GND			10		10	pF
$C_o$	$V_O = V_{CC}$ or GND			15		15	pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

§ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .



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SCBS721 – JULY 2000

switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C		UNIT
			MIN	MAX	
t <sub>pd</sub>	A or B	B or A	5	7	ns
t <sub>en</sub>	$\overline{OE}$	A or B	6	9.5	ns
t <sub>dis</sub>	$\overline{OE}$	A or B	6	7.5	ns

noise characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

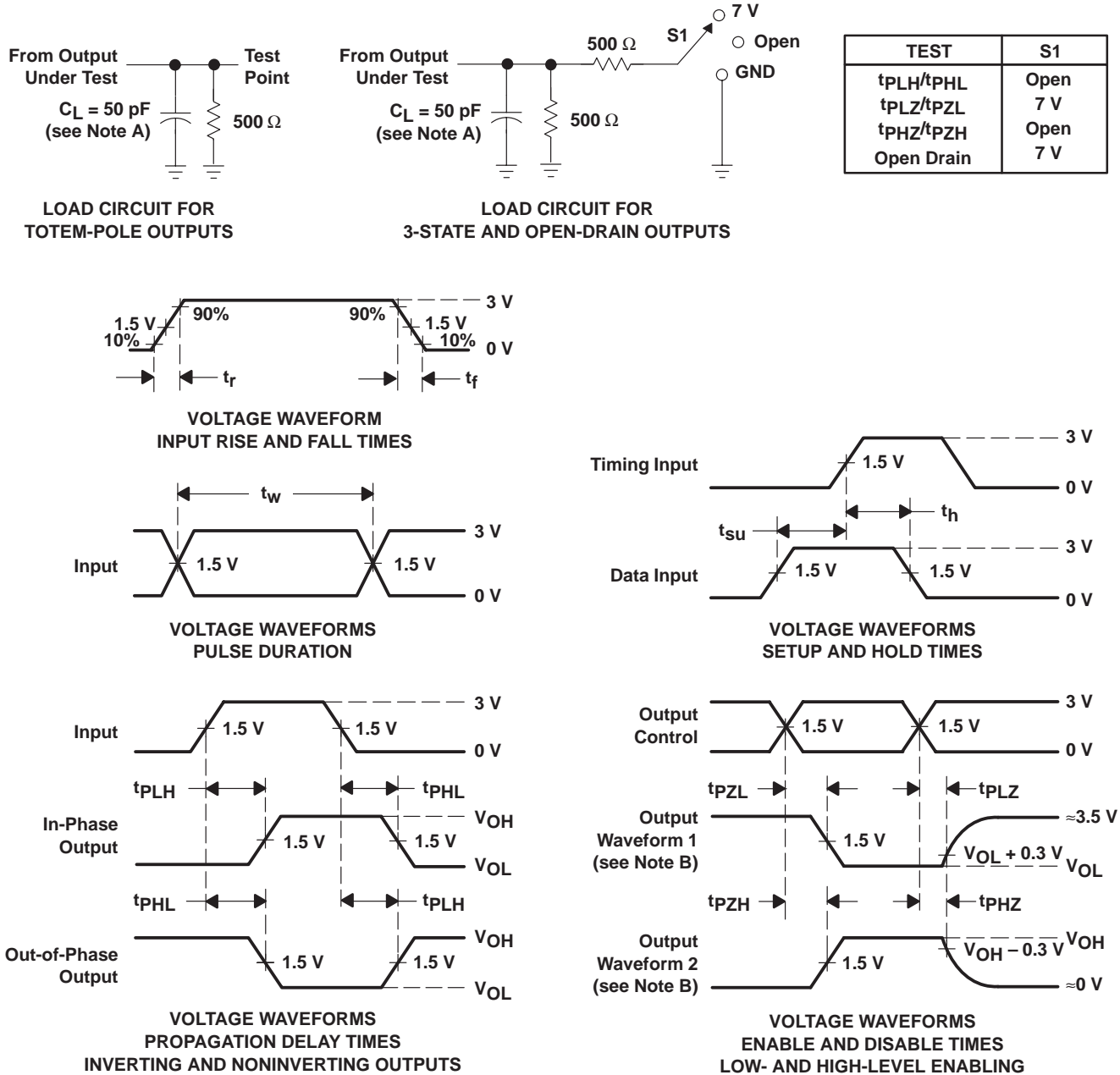
PARAMETER	MIN	TYP	MAX	UNIT
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>		1		V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>		0.5		V
V <sub>IH(D)</sub> High-level dynamic input voltage	2			V
V <sub>IL(D)</sub> Low-level dynamic input voltage			0.8	V

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load, f = 1 MHz	49	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> and t<sub>f</sub> = 2.5 ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.  
 F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.  
 G. t<sub>PHL</sub> and t<sub>PLH</sub> are the same as t<sub>pd</sub>.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74FCT245E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	CD74FCT245E	<a href="#">Samples</a>
CD74FCT245M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT245M	<a href="#">Samples</a>
CD74FCT245M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT245M	<a href="#">Samples</a>
CD74FCT245MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74FCT245M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74FCT245M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74FCT245M96	SOIC	DW	20	2000	367.0	367.0	45.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

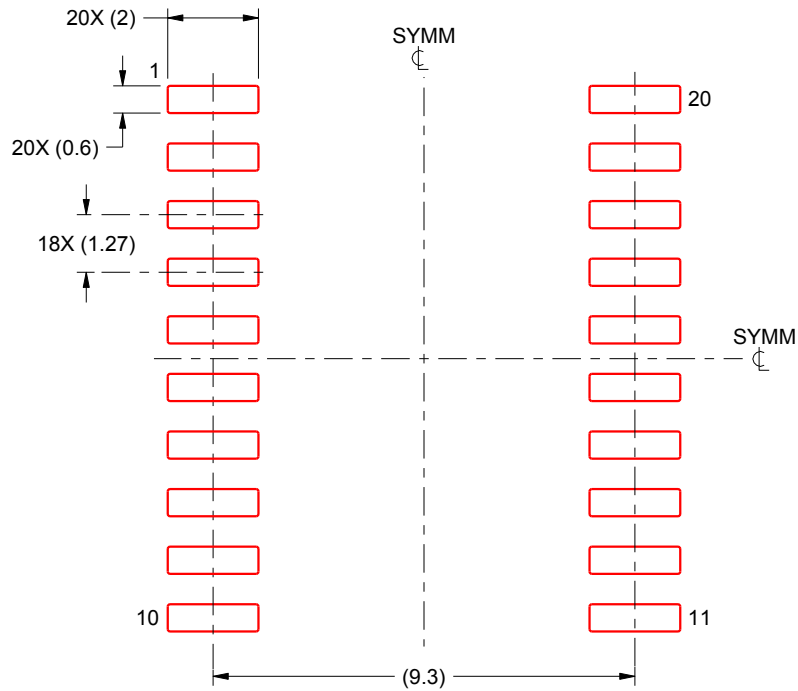
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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