THE DATASHEET OF

ADP1050ACPZ-RL

Digital Controller for Isolated Power Supply with PMBus Interface

Data Sheet

ADP1050

FEATURES

- Versatile digital voltage mode controller
- High speed input voltage feedforward control
- 4 pulse-width modulation (PWM) logic outputs with 625 ps resolution
- Switching frequency: 49 kHz to 625 kHz
- Frequency synchronization as slave device
- Pulse skipping power saving mode
- Prebias startup
- Conditional overvoltage protection
- Extensive fault detection and protection
- PMBus compliant
- Graphical user interface (GUI) for ease of programming
- On-board EEPROM for programming and data storage
- Available in a 20-lead, 4 mm × 4 mm LFCSP
- –40°C to +125°C operating temperature

APPLICATIONS

- High density, isolated dc-to-dc power supplies
  - Intermediate bus converters
  - High availability parallel power systems
- Server, storage, industrial, networking, and communications infrastructure

GENERAL DESCRIPTION

The ADP1050 is an advanced digital controller with a PMBus™ interface targeting high density, high efficiency dc-to-dc power conversion. This controller implements voltage mode control with high speed, input voltage feedforward operation for enhanced transient and noise performance. The ADP1050 has four programmable pulse-width modulation (PWM) outputs capable of controlling most high efficiency power supply topologies, with the added control of synchronous rectification (SR).

The ADP1050 implements several features to enable a robust system of parallel and redundant operation for customers who require high availability. The device provides synchronization, prebias startup, and conditional overvoltage techniques to identify and safely shut down an erroneous power supply in parallel operation mode.

The ADP1050 is based on flexible state machine architecture and is programmed using an intuitive graphical user interface (GUI). The easy to use GUI reduces design cycle time and results in a robust, hardware coded system loaded into the built-in EEPROM. The small size (4 mm × 4 mm) of the LFCSP package makes the ADP1050 ideal for ultracompact, isolated dc-to-dc power module or embedded power designs.

TYPICAL APPLICATIONS CIRCUIT

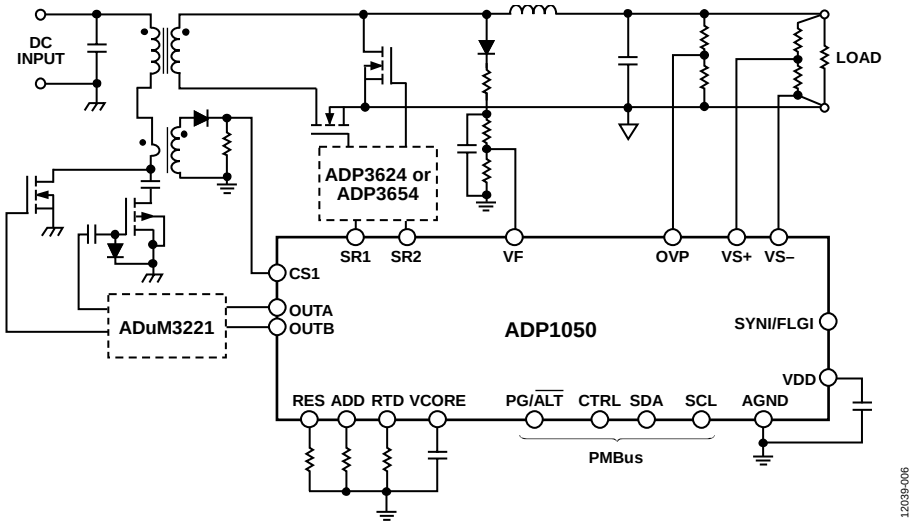

Figure 1.

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

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1/14—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V, T_J = −40°C to +125°C, unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	2.2 µF capacitor connected to AGND
Supply Current	I_{DD}		28.5	33	mA	Normal operation; PWM pins unloaded
			I_{DD} + 6		mA	During EEPROM programming
			50	100	µA	Shutdown; V_{DD} below undervoltage lockout (UVLO) threshold
POWER-ON RESET						
Power-On Reset				3.0	V	V_{DD} rising
UVLO Threshold		2.75	2.85	2.97	V	V_{DD} falling
UVLO Hysteresis			35		mV	
OVLO Threshold		3.7	3.9	4.1	V	
OVLO Debounce			2		µs	VDD_OV flag debounce set to 2 µs
			500		µs	VDD_OV flag debounce set to 500 µs
VCORE PIN						
Output Voltage	V_{CORE}	2.45	2.6	2.75	V	330 nF capacitor connected to AGND
OSCILLATOR AND PLL						
PLL Frequency		190	200	210	MHz	RES input = 10 kΩ (±0.1%)
Digital PWM Resolution			625		ps	
OUTA, OUTB, SR1, SR2 PINS						
Output Low Voltage	V_{OL}			0.4	V	I_{OH} = 10 mA
Output High Voltage	V_{OH}	V_{DD} − 0.4			V	I_{OL} = −10 mA
Rise Time	t_R		3.5		ns	C_{LOAD} = 50 pF
Fall Time	t_F		1.5		ns	C_{LOAD} = 50 pF
Output Source Current	I_{OL}	−10			mA	
Output Sink Current	I_{OH}			10	mA	
VS+, VS− VOLTAGE SENSE PINS						
Input Voltage Range	V_{IN}	0	1	1.6	V	Differential voltage from VS+ to VS−
Leakage Current				1.0	µA	
VS Accurate ADC						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			10		ms	
Measurement Resolution			12		Bits	
Measurement Accuracy						Factory trimmed at 1.0 V
		−5		+5	% FSR	0% to 100% of input voltage range
		−80		+80	mV	
		−2		+2	% FSR	10% to 90% of input voltage range
		−32		+32	mV	
		−1.0		+1.0	% FSR	900 mV to 1.1 V
		−16		+16	mV	
Temperature Coefficient				70	ppm/°C	
Voltage Differential from VS− to AGND		−200		+200	mV	
VS High Speed ADC						
Equivalent Sampling Frequency	f_{SAMP}		f_{SW}		kHz	
Equivalent Resolution			6		Bits	f_{SW} = 390.5 kHz
Dynamic Range			±25		mV	Regulation voltage = 0 mV to 1.6 V
VS UVP Digital Comparator						Triggers VOUT_UV_FAULT flag
Threshold Accuracy		−2		+2	% FSR	10% to 90% of input voltage range
Comparator Update Speed			82		µs	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OVP PIN						Triggers VOUT_OV_FAULT flag
Leakage Current				1.0	µA	
OVP Comparator						
Voltage Range		0.75		1.5	V	Differential voltage from OVP to VS−
Threshold Accuracy		−1.6	+1	+1.6	%	0.75 V to 1.5 V voltage range
Propagation Delay (Latency)			61	85	ns	Debounce time not included
VF VOLTAGE SENSE PIN						
Input Voltage Range	V_{IN}	0	1	1.6	V	Voltage from VF to AGND
Leakage Current				1.0	µA	
General ADC						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			1.31		ms	
Measurement Resolution			11		Bits	
Measurement Accuracy		−2		+2	% FSR	10% to 90% of input voltage range
		−32		+32	mV	
		−5		+5	% FSR	0% to 100% of input voltage range
		−80		+80	mV	
VF UVP Digital Comparator						Triggers VIN_LOW or VIN_UV_FAULT flag
Threshold Accuracy						Based on VF general ADC parameter values
Comparator Update Speed			1.31		ms	
Feedforward ADC						
Input Voltage Range	V_{IN}	0.5	1	1.6	V	
Resolution			11		Bits	
Sampling Period			10		µs	
CS1 CURRENT SENSE PIN						
Input Voltage Range	V_{IN}	0	1	1.6	V	Voltage from CS1 to AGND
Source Current		−1.2		−0.35	µA	
CS1 ADC						
Valid Input Voltage Range		0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			10		ms	
Measurement Resolution			12		Bits	
Measurement Accuracy		−2		+2	% FSR	10% to 90% of input voltage range
		−32		+32	mV	
		−5		+5	% FSR	0% to 100% of input voltage range
		−80		+80	mV	
CS1 OCP Comparator						Triggers internal CS1_OCP flag
Reference Accuracy		1.185	1.2	1.215	V	When set to 1.2 V
		0.235	0.25	0.265	V	When set to 0.25 V
Propagation Delay (Latency)			65	105	ns	Debounce/blanking time not included
CS3[1] Measurement and Digital Comparator						Triggers CS3_OC_FAULT flag
Register Update Rate			10		ms	
Comparator Speed			10		ms	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RTD TEMPERATURE SENSE PIN						
Input Voltage Range	V_{IN}	0		1.6	V	Voltage from RTD to AGND
Source Current						Factory default setting
Register 0xFE2D = 0xE6		44.6	46	47.3	µA	
Register 0xFE2D = 0xB0		38.6	40	42	µA	
Register 0xFE2D = 0x80		28.6	30	31.8	µA	
Register 0xFE2D = 0x40		18.6	20	21.6	µA	
Register 0xFE2D = 0x00		9.1	10	11	µA	
RTD ADC						
Valid Input Voltage Range	V_{IN}	0		1.6	V	
ADC Clock Frequency			1.56		MHz	
Register Update Rate			10		ms	
Measurement Resolution			12		Bits	
Measurement Accuracy		−0.3		+0.45	% FSR	2% to 20% of the input voltage range
		−4.8		+7.2	mV	
		−2		+2	% FSR	0% to 100% of the input voltage range
		−80		+80	mV	
OTP Digital Comparator						Triggers OT_FAULT flag
Threshold Accuracy		−0.9		+0.25	% FSR	T = 85°C with 100 kΩ||16.5 kΩ
		−14.4		+4	mV	
		−0.5		+1.1	% FSR	T = 100°C with 100 kΩ||16.5 kΩ
		−8		+17.6	mV	
Comparator Update Speed			10		ms	
Temperature Readings According to Internal Linearization Scheme						Source current is set to 46 µA (Register 0xFE2D = 0xE6); NTC R25 = 100 kΩ (1%); beta = 4250 (1%); R_{EXT} = 16.5 kΩ (1%)
				7	°C	25°C to 100°C
				5	°C	100°C to 125°C
PG/$\overline{\text{ALT}}$ (OPEN-DRAIN) PIN						
Output Low Level	V_{OL}			0.4	V	Sink current = 10 mA
CTRL PIN						
Input Low Level	V_{IL}			0.4	V	
Input High Level	V_{IH}	V_{DD} − 0.8			V	
Leakage Current				1.0	µA	
SYNI/FLGI PIN						
Input Low Level	V_{IL}			0.4	V	
Input High Level	V_{IH}	V_{DD} − 0.8			V	
Synchronization Range % of Internal Clock Period	t_{SYNC}	90		110	%	
SYNI Positive Pulse Width		360			ns	External clock applied on the SYNI/FLGI pin
SYNI Negative Pulse Width		360			ns	External clock applied on the SYNI/FLGI pin
SYNI Period Drift				280	ns	Period drift between two consecutive external clocks
Leakage Current				1.0	µA	
SDA AND SCL PINS						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	V_{DD} − 0.8			V	
Output Low Voltage	V_{OL}			0.4	V	Sink current = 3 mA
Leakage Current		−5		+5	µA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL BUS TIMING						See Figure 2
Clock Operating Frequency		10	100	400	kHz	
Glitch Immunity				50	ns	
Bus Free Time	t_{BUF}	1.3			µs	Between stop and start conditions
Start Setup Time	$t_{SU;STA}$	0.6			µs	Repeated start condition setup time
Start Hold Time	$t_{HD;STA}$	0.6			µs	Hold time after repeated start condition; after this period, the first clock is generated
Stop Setup Time	$t_{SU;STO}$	0.6			µs	
SDA Setup Time	$t_{SU;DAT}$	100			ns	
SDA Hold Time	$t_{HD;DAT}$	125			ns	For readback
		300			ns	For write
SCL Low Timeout	$t_{TIMEOUT}$	25		35	ms	
SCL Low Time	t_{LOW}	0.6			µs	
SCL High Time	t_{HIGH}	0.6			µs	
SCL Low Extended Time	$t_{LOW;SEXT}$			25	ms	
SCL, SDA Rise Time	t_R	20		300	ns	
SCL, SDA Fall Time	t_F	20		300	ns	
EEPROM						
EEPROM Update Time				40	ms	Time from the update command to completion of the EEPROM update
Reliability						
Endurance[2]		10,000			Cycles	T_J = 85°C
		1000			Cycles	T_J = 125°C
Data Retention[3]		20			Years	T_J = 85°C
		15			Years	T_J = 125°C

[1] CS3 is an alternative output current reading that is calculated by the CS1 reading (representing input current), duty cycle, and the main transformer turns ratio.
[2] Endurance is qualified as per JEDEC Standard 22, Method A117, and is measured at −40°C, +25°C, +85°C, and +125°C.
[3] Retention lifetime equivalent at junction temperature as per JEDEC Standard 22, Method A117.

TIMING DIAGRAM

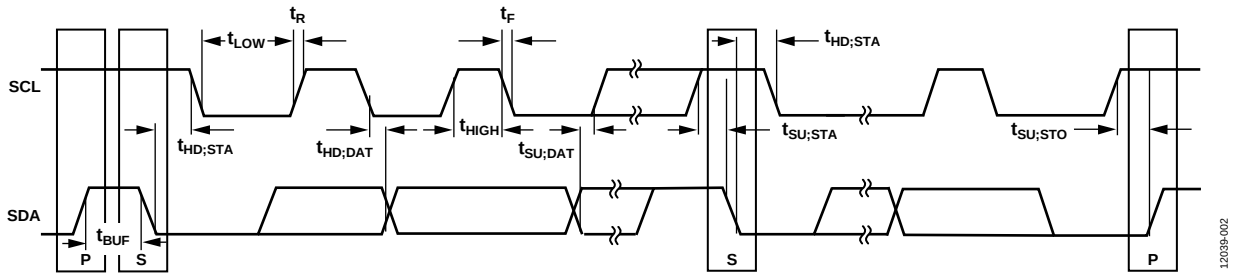


Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous) V_{DD}	4.2 V
Digital Pins (OUTA, OUTB, SR1, SR2, PG/$\overline{ALT}$, SDA, SCL) to AGND	−0.3 V to V_{DD} + 0.3 V
VS−, VS+, VF, OVP, RTD, ADD, CS1 to AGND	−0.3 V to V_{DD} + 0.3 V
SYNI/FLGI, CTRL	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (T_A)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD Charged Device Model	1.25 kV
ESD Human Body Model	5.0 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead LFCSP	37.05	1.53	°C/W

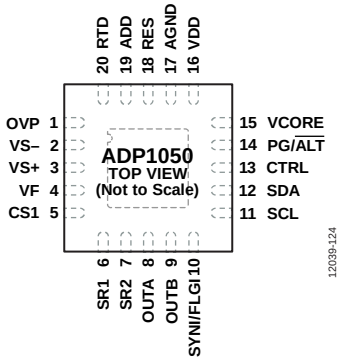
SOLDERING

It is important to follow the correct guidelines when laying out the printed circuit board (PCB) footprint for the ADP1050 and for soldering the device onto the PCB. For detailed information about these guidelines, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE ADP1050 HAS AN EXPOSED THERMAL PAD ON THE UNDERSIDE OF THE PACKAGE. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE EXPOSED PAD BE SOLDERED TO THE PCB AGND PLANE.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OVP	Overvoltage Protection. This signal is used as redundant overvoltage protection. This signal is referred to AGND.
2	VS–	Inverting Voltage Sense Input. This pin is the connection for the ground line of the power rail. Provide a low ohmic connection to AGND. To allow trimming, it is recommended that the resistor divider on this input have a tolerance specification of ≤0.5%.
3	VS+	Noninverting Voltage Sense Input. This signal is referred to VS–. To allow trimming, it is recommended that the resistor divider on this input have a tolerance specification of ≤0.5%.
4	VF	Voltage Feedforward. Three optional functions can be implemented with this pin: feedforward, primary side input voltage sensing, and input voltage UVLO protection. The pin is connected upstream of the output inductor through a resistor divider network. The nominal voltage at this pin is 1 V. This signal is referred to AGND.
5	CS1	Primary Side Current Sense Input. This pin is connected to the primary side current sensing ADC and to the cycle-by-cycle current-limit comparator. This signal is referred to AGND. To allow trimming, it is recommended that the resistors on this input have a tolerance specification of ≤0.5%. If this pin is not used, connect it to AGND.
6	SR1	PWM Logic Output Drive. This pin can be disabled when not in use. This signal is referred to AGND.
7	SR2	PWM Logic Output Drive. This pin can be disabled when not in use. This signal is referred to AGND.
8	OUTA	PWM Logic Output Drive. This pin can be disabled when not in use. This signal is referred to AGND.
9	OUTB	PWM Logic Output Drive. This pin can be disabled when not in use. This signal is referred to AGND.
10	SYNI/FLGI	Synchronization Signal Input (SYNI)/External Signal Input to Generate a Flag Condition (FLGI). If this pin is not used, connect it to AGND.
11	SCL	I²C/PMBus Serial Clock Input and Output (Open Drain). This signal is referred to AGND.
12	SDA	I²C/PMBus Serial Data Input and Output (Open Drain). This signal is referred to AGND.
13	CTRL	PMBus Control Signal. It is recommended that a 1 nF capacitor be connected from the CTRL pin to AGND for noise debounce and decoupling. This signal is referred to AGND.
14	PG/$\overline{\text{ALT}}$	Power-Good Output (Open Drain)(PG)/Active Low SMBus $\overline{\text{ALERT}}$ Signal ($\overline{\text{ALT}}$). Connect this pin to VDD using a pull-up resistor (typically 2.2 kΩ). The power-good signal is referred to AGND. For information about the SMBus specification, see the PMBus Features section.
15	VCORE	Output of the 2.6 V Regulator. Connect a decoupling capacitor of at least 330 nF from this pin to AGND, as close as possible to the ADP1050 to minimize the PCB trace length. It is recommended that this pin not be used as a reference or to generate other logic levels using resistive dividers.
16	VDD	Positive Supply Input. Voltage of 3.0 V to 3.6 V. This signal is referred to AGND. Connect a 2.2 µF decoupling capacitor from this pin to AGND, as close as possible to the ADP1050 to minimize the PCB trace length.
17	AGND	Common Analog Ground. The internal analog circuitry ground and the digital circuitry ground are star connected to this pin through bonding wires.
18	RES	Resistor Input. This pin sets the internal reference for the internal PLL frequency. Connect a 10 kΩ resistor (±0.1%) from this pin to AGND. This signal is referred to AGND.
19	ADD	Address Select Input. This pin is used to program the I²C/PMBus address. Connect a resistor from ADD to AGND. This signal is referred to AGND.

Pin No.	Mnemonic	Description
20	RTD	Thermistor Input. Place a thermistor (R25 = 100 kΩ (1%), beta = 4250 (1%)) in parallel with a 16.5 kΩ (1%) resistor and a 1 nF filtering capacitor. This pin is referred to AGND. If this pin is not used, connect it to AGND.
	EP	Exposed Pad. The ADP1050 has an exposed thermal pad on the underside of the package. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad be soldered to the PCB AGND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

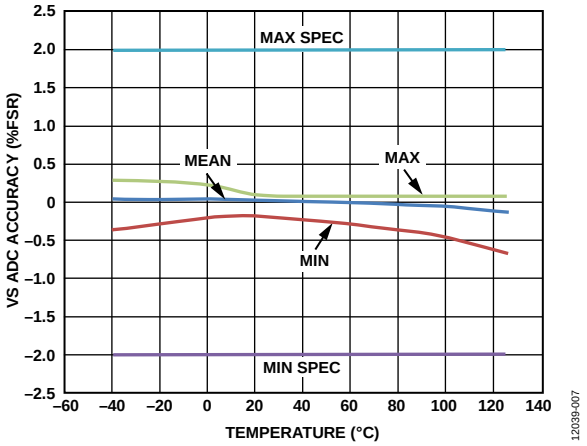


Figure 4. VS ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

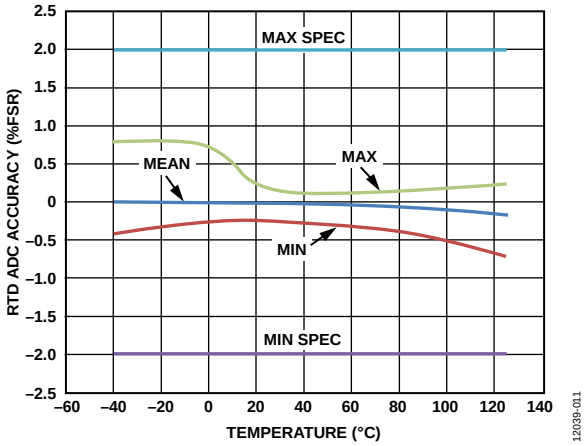


Figure 7. RTD ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

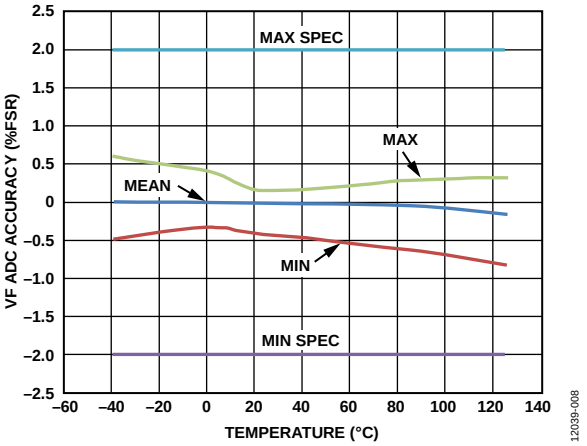


Figure 5. VF ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

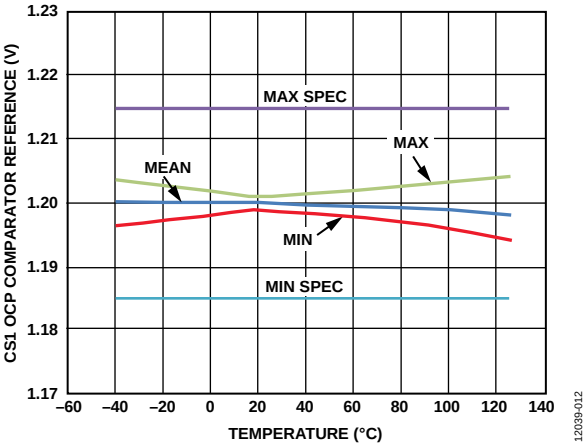


Figure 8. CS1 OCP Comparator Reference vs. Temperature (1.2 V Reference)

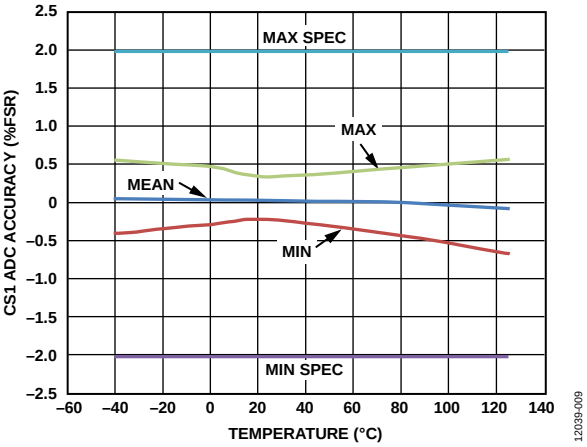


Figure 6. CS1 ADC Accuracy vs. Temperature (From 10% to 90% of FSR)

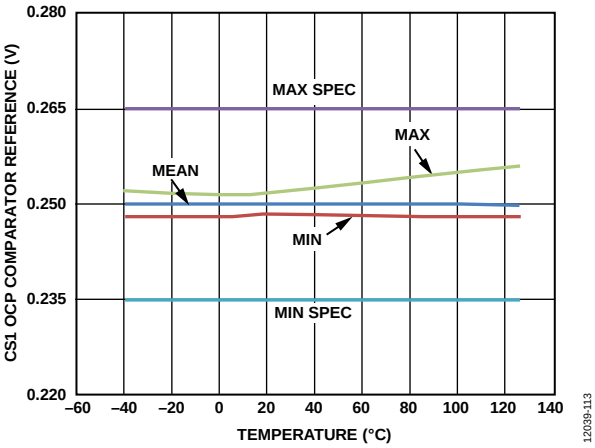


Figure 9. CS1 OCP Comparator Reference vs. Temperature (0.25 V Reference)

THEORY OF OPERATION

The ADP1050 is designed as a flexible, easy to use, digital power supply controller. The ADP1050 integrates the typical functions that are needed to control a power supply, such as

- Output voltage sense and feedback
- Voltage feedforward control
- Digital loop filter compensation
- PWM generation
- Current, voltage, and temperature sense
- Housekeeping and I²C/PMBus interface
- Calibration and trimming

The main function of controlling the output voltage is performed by the feedback ADCs, the digital loop compensator, and the digital PWM engine.

The feedback ADCs feature a patented multipath architecture, with a high speed, low resolution (fast and coarse) ADC and a low speed, high resolution (slow and accurate) ADC. The ADC outputs are combined to form a high speed and high resolution feedback path. Loop compensation is implemented using the digital compensator. This proportional, integral, derivative (PID) compensator is implemented in the digital domain to allow easy programming of filter characteristics, which is of great value in customizing and debugging designs. The PWM engine generates up to four programmable PWM outputs for control of primary side FET drivers and synchronous rectification FET drivers. This programmability allows many generic and specific switching power supply topologies to be realized.

Conventional power supply housekeeping features, such as input voltage sense, output voltage sense, primary side current sense, and secondary side current sense, are included. An extensive set of protections is included, such as overvoltage protection (OVP), overcurrent protection (OCP), overtemperature protection (OTP), and undervoltage protection (UVP).

These features are programmable through the I²C/PMBus digital bus interface. This interface is also used for calibrations. Other information, such as input current, output current, and fault flags, is also available through this digital bus interface.

The internal EEPROM can store all programmed values and allows standalone control without a microcontroller. A free, downloadable GUI is available that provides all the necessary software to program the ADP1050. To obtain the latest GUI software and a user guide, visit http://www.analog.com/digitalpower.

The ADP1050 operates from a single 3.3 V power supply and is specified from −40°C to +125°C.

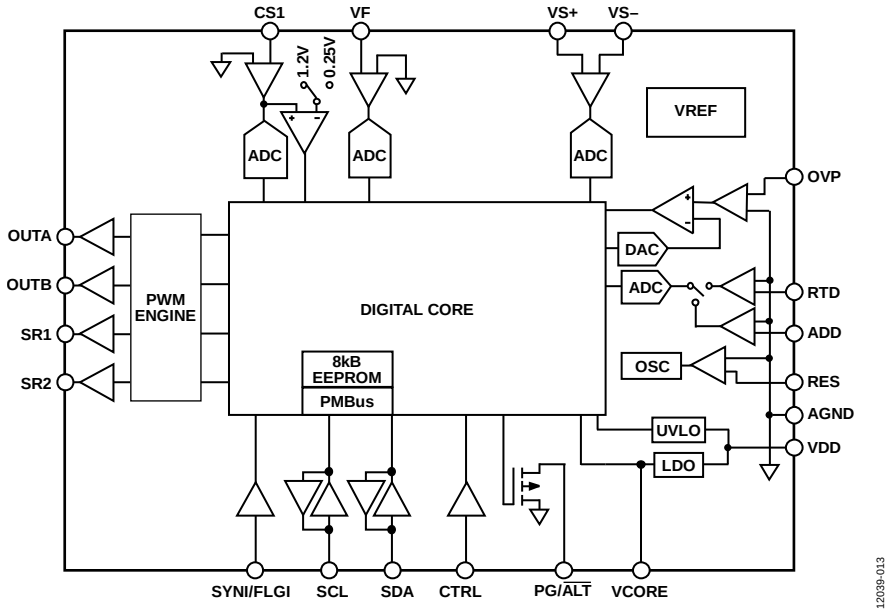


Figure 10. Functional Block Diagram

PWM OUTPUTS (OUTA, OUTB, SR1, AND SR2)

The PWM outputs are used for control of the primary side drivers and the synchronous rectifier drivers. They can be used for several topologies, including hard-switched full bridge, half bridge, push pull, two-switch forward, active clamp forward, and interleaved buck. Delays between rising and falling edges can be individually programmed. Special care must be taken to avoid shoothrough and cross conduction. It is recommended that the ADP1050 GUI software be used to program these outputs.

Figure 11 shows an example configuration to drive an active clamp forward topology with synchronous rectification. The QA, QB, QSR1, and QSR2 switches are driven separately by the PWM outputs (OUTA, OUTB, SR1, and SR2). Figure 12 shows an example of the PWM settings in the GUI for the power stage shown in Figure 11.

The PWM outputs are all synchronized with each other. Therefore, when reprogramming more than one of these outputs, it is important to first update all of the registers and then latch the information into the shadow registers at one time. During the reprogramming operation, the outputs are temporarily disabled. To ensure that the new PWM timings and the switching frequency setting are programmed simultaneously, a special instruction is sent to the ADP1050 by setting Register 0xFE61[2:1] (the go commands). It is recommended that the PWM outputs not in use be disabled via Register 0xFE53[5:4] and Register 0xFE53[1:0].

See the PWM Outputs Timing Registers section for additional information about the PWM timings.

SYNCHRONOUS RECTIFICATION

SR1 and SR2 are recommended for use as the PWM control signals when synchronous rectification is in use. These PWM signals can be configured much like the other PWM outputs.

An optional soft start can be applied to the synchronous rectifier (SR) PWM outputs. The SR soft start can be programmed using Register 0xFE08[4:0].

- When the SR soft start is disabled (Register 0xFE08[1:0] = 00), the SR signals are immediately turned on to their modulated PWM duty cycle values.
- When the SR soft start is enabled (Register 0xFE08[1:0] = 11), the SR1 and SR2 rising edges move left from the t_{RX} + t_{MODU_LIMIT} position to the t_{RX} + $t_{MODULATION}$ position in steps that are set in Register 0xFE08[3:2]. t_{RX} represents the rising edge timing of SR1 (t_{R5}) and the rising edge timing of SR2 (t_{R6}) (see Figure 58); t_{MODU_LIMIT} represents the modulation limit defined in Register 0xFE3C (see Figure 57); $t_{MODULATION}$ represents the real-time modulation value.
- The SR soft start is still applicable even if the SR1 and SR2 outputs are not programmed to be modulated. When the SR soft start is enabled, the SR1 and SR2 rising edges move left from the t_{RX} + t_{MODU_LIMIT} position to the t_{RX} position in steps that are set in Register 0xFE08[3:2].

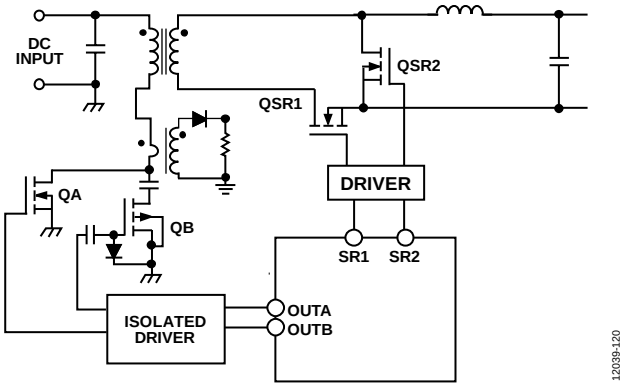


Figure 11. PWM Assignment for Active Clamp Forward Topology with Synchronous Rectification

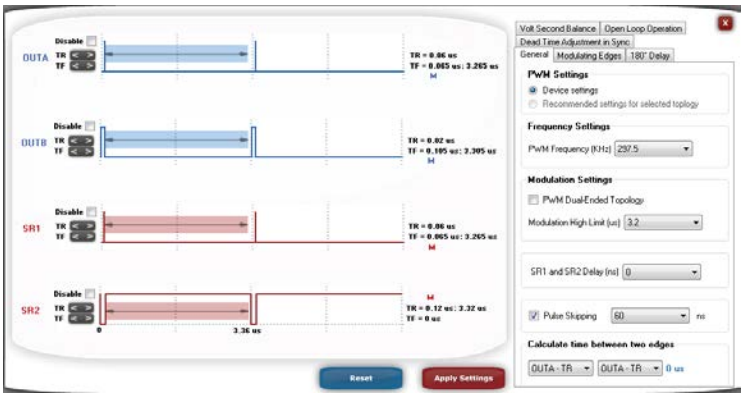


Figure 12. PWM Settings for Active Clamp Forward Topology with Synchronous Rectification Using the ADP1050 GUI

The advantage of the SR soft start is that it minimizes the output voltage undershoot that occurs when the SR FETs are turned on without a soft start. The advantage of turning the SRx signals completely on immediately is that they can help minimize the voltage transient caused during a load step.

Using Register 0xFE08[4], the SR soft start can be programmed to occur only once (the first time that the SRx signals are enabled) or every time that the SRx signals are enabled.

When programming the ADP1050 to use the SR soft start, ensure the correct operation of this function by setting the falling edge of SR1 (t_{F5}) to a lower value than the rising edge of SR1 (t_{R5}) and setting the falling edge of SR2 (t_{F6}) to a lower value than the rising edge of SR2 (t_{R6}). During the SR soft start, the rising edges of SRx move gradually from the right side (the t_{RX} + t_{MODU_LIMIT} position) to the left side to increase the duty cycle.

The ADP1050 is well suited for dc-to-dc converters in isolated topologies. Every time a PWM signal crosses the isolation barrier, a propagation delay is added because of the isolating components. Using Register 0xFE3A[5:0], an adjustable delay (0 ns to 315 ns in steps of 5 ns) can be programmed to move both SR1 and SR2 later in time to compensate for the added propagation delay. In this way, all the PWM edges can be aligned (see Figure 58).

PWM MODULATION LIMIT AND 180° PHASE SHIFT

The modulation limit register (Register 0xFE3C) can be programmed to apply a maximum modulation limit to any PWM signal, thus limiting the modulation range of any PWM output. If modulation is enabled, the maximum modulation limit is applied to all PWM outputs collectively. This limit, t_{MODU_LIMIT}, is the maximum time variation for the modulated edges from the default timing, following the configured modulation direction (see Figure 13). There is no setting for the minimum duty cycle limit. Therefore, the user must set the rising edges and falling edges based on the case with the least modulation.

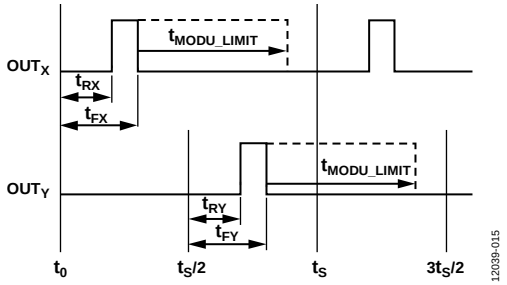


Figure 13. Setting Modulation Limits

Each least significant bit (LSB) in Register 0xFE3C corresponds to a different time step size, depending on the switching frequency (see Table 137). If the ADP1050 is to control a dual-ended topology (such as full bridge, half bridge, or push pull), enable the dual-ended topology mode using Register 0xFE13[6]. When dual-ended topology mode is enabled, the modulation limit in each half cycle is half of the modulation value programmed by Register 0xFE3C.

The modulated edges cannot go beyond one switching cycle. To extend the modulation range for some applications, the 180° phase shift can be enabled, using Register 0xFE3B[5:4] and Register 0xFE3B[1:0]. When the 180° phase shift is disabled, the rising edge timing and the falling edge timing are referred to the start of the switching cycle (see t_{RX} and t_{FX} in Figure 13). When the 180° phase shift is enabled, the rising edge timing and the falling edge timing are referred to half of the switching cycle (see t_{RY} and t_{FY} in Figure 13, which are referred to $t_S/2$). Therefore, when the 180° phase shift is disabled, the edges are always located between t_0 and t_S. When the 180° phase shift is enabled, the edges are located between $t_S/2$ and $3t_S/2$.

The 180° phase shift function can be used to extend the maximum duty cycle in a multiphase, interleaved converter. Figure 14 shows a dual phase, interleaved buck converter. The OUTB and SR1 PWM outputs can be programmed with a 180° phase shift with the OUTA and SR2 PWM outputs.

The ADP1050 GUI is recommended for evaluating this feature.

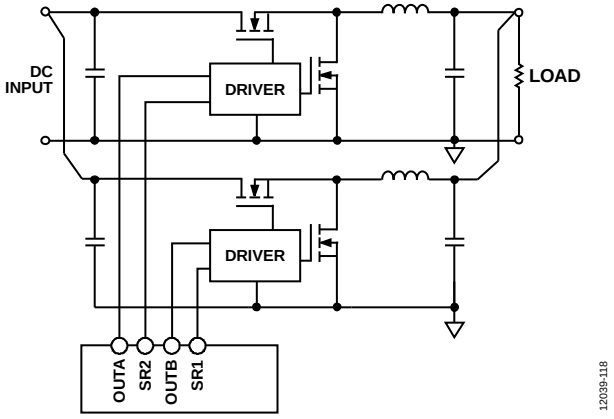


Figure 14. Dual Phase, Interleaved Buck Converter Controlled by the ADP1050

FREQUENCY SYNCHRONIZATION

The ADP1050 can be programmed as a slave device to use the SYNI/FLGI pin signal as the reference to synchronize the internal programmed PWM clock with an external clock.

The period of the external clock that is applied at the SYNI/FLGI pin must be in the range of 90% to 110% of the period of the internal programmed PWM clock. The minimum pulse width of the SYNI signal is 360 ns. From the rising edge of the SYNI signal to the start of the internal clock cycle, there is a 760 ns propagation delay. To realize interleaving control with different controllers, additional delay time can be programmed using Register 0xFE11.

To achieve a smooth synchronization transition between asynchronous operation and synchronous operation, there is a phase capture range bit for synchronization in Register 0xFE12[6] for capturing the phase of the external clock signal. The ADP1050 detects the phase shift between the external clock signal and the internal clock signal when synchronization is enabled. When the phase shift falls within the phase capture range, synchronization begins.

The ADP1050 synchronizes to the external clock frequency as follows:

1. After the synchronization function is enabled by Register 0xFE12[3] and Register 0xFE12[0], the ADP1050 starts to detect the period of the external clock signal applied at the SYNI/FLGI pin.
2. If all periods of the most recent 64 consecutive cycles of the external clocks fall within 90% to 110% of the internal switching clock period, the ADP1050 uses the latest current cycle as the synchronization reference, and the period of the external clock is identified. This interval is t_2 or t_4, as shown in Figure 15. Otherwise, the ADP1050 discards this cycle and looks for the next cycle (frequency capture mode).
3. After the external clock period is determined, the ADP1050 detects the phase shift between the external clock (plus the delay time set by Register 0xFE11) and the internal PWM signal. If the phase shift is within the phase capture range, the internal and external clocks are synchronized (phase capture mode).
4. The PWM clock is synchronized with the external clock. Cycle-by-cycle synchronization starts.
5. If the external clock signal is lost at any time, or if the period exceeds the minimum limit (89% of the internal programmed frequency) or the maximum limit (114% of the internal programmed frequency), the ADP1050 takes the last valid external clock signal as the synchronization reference source. At the same time, the phase shift between the synchronization reference and the internal clock is detected. When the phase shift falls within the phase capture range, the PWM clock returns to the internal clock set by the internal oscillator. This interval is t_1 or t_3, as shown in Figure 15.
   This is the first synchronization unlock condition, called Synchronization Unlocked Mode 1, in which the switching frequency is out of range (range is 89% to approximately 114% of the internal programmed frequency).
6. If the period of the external SYNI signal changes significantly (for example, if the period difference between contiguous cycles exceeds 280 ns), the ADP1050 takes the last valid external clock signal as the synchronization reference source. At the same time, the phase shift between the synchronization reference and the internal clock is detected. When the phase shift falls within the phase capture range, the PWM clock returns to the internal clock set by the internal oscillator.
   This is the second synchronization unlock condition, called Synchronization Unlocked Mode 2, in which the phase shift exceeds 280 ns.

Figure 15 shows the synchronization operation diagram. The internal frequency, f_{SW_INT}, is the internal free-running frequency of the ADP1050. Before the synchronization is locked, the ADP1050 runs at f_{SW_INT}. The external frequency, f_{SW_EXT}, is the frequency of the external clock to which the ADP1050 must synchronize. After synchronization is locked, the ADP1050 runs at f_{SW_EXT}.

The ADP1050 does not allow the switching frequency to cross the boundaries of 97.5 kHz, 195.5 kHz, or 390.5 kHz on-the-fly. Ensure that the external clock does not cross these boundaries. Otherwise, the internal switching frequency cannot be set within ±10% of these boundaries.

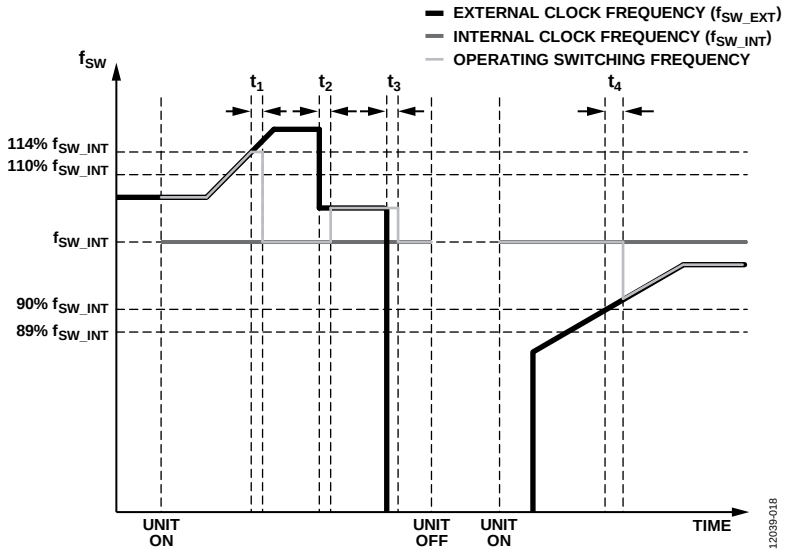


Figure 15. Synchronization Operation

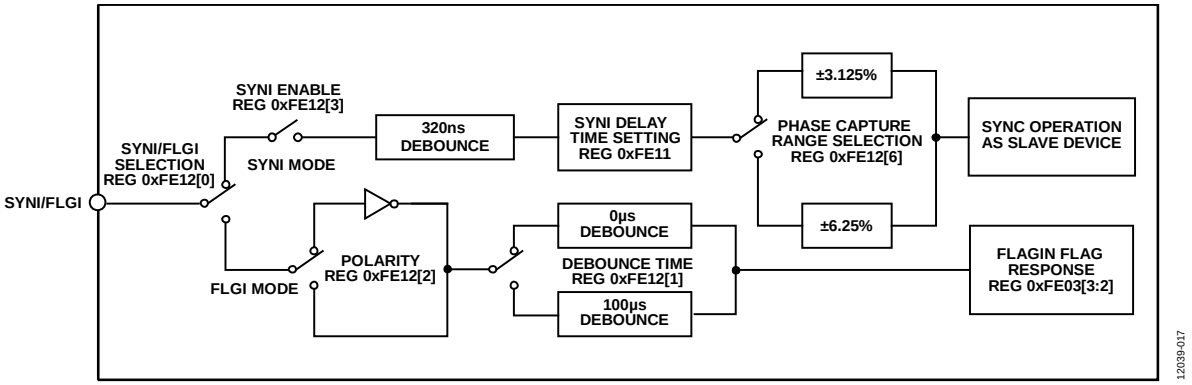


Figure 16. Synchronization Configuration

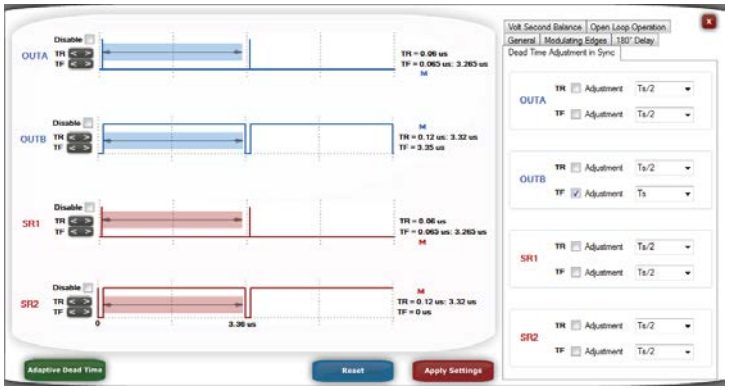


Figure 17. Edge Adjustment Reference During Synchronization

To ensure a constant dead time before and after synchronization, Register 0xFE6D and Register 0xFE6F can be set for edge adjustment referred to $t_S/2$ or t_S. For example, the falling edge of OUTA (t_{F1}) is referred to the ½ × t_S position, which means that the time difference between t_{F1} and ½ × t_S is a constant during the synchronization transition. Figure 17 shows an example of the edge adjustment reference settings in a full bridge topology.

OUTPUT VOLTAGE SENSE AND ADJUSTMENT

The output voltage sense and adjustment function is used for control, monitoring, and undervoltage protection of the remote output voltage. VS– (Pin 2) and VS+ (Pin 3) are fully differential inputs. The voltage sense point can be calibrated digitally to remove any errors due to external components. This calibration can be performed in the production environment, and the settings can be stored in the EEPROM of the ADP1050 (see the Power Supply Calibration and Trim section for more information).

For voltage monitoring, the READ_VOUT output voltage command (Register 0x8B) is updated every 10 ms. The ADP1050 stores every ADC sample for 10 ms and then calculates the average value at the end of the 10 ms period. Therefore, if Register 0x8B is read at least every 10 ms, a true average value is obtained. The voltage information is available through the I²C/PMBus interface.

The control loop of the ADP1050 features a patented multipath architecture. The output voltage is converted simultaneously by two ADCs: a high accuracy ADC and a high speed ADC. The complete signal is reconstructed and processed in the digital compensator to provide a high performance and cost competitive solution.

Voltage Feedback Sensing (VS+ and VS– Pins)

The voltage sense point on the power rail requires an external resistor divider (R1 and R2 in Figure 18) to bring the nominal differential mode signal to 1 V between the VS+ and VS– pins (see Figure 18). This external resistor divider is necessary because the VS ADC input range of the ADP1050 is 0 V to 1.6 V. When R1 and R2 are known, the VOUT_SCALE_LOOP parameter can be calculated using the following equation:

$$VOUT\_SCALE\_LOOP = R2/(R1 + R2)$$

In a 12 V system with resistor dividers of 11 kΩ and 1 kΩ, VOUT_SCALE_LOOP can be calculated as follows:

$$VOUT\_SCALE\_LOOP = 1\ k\Omega/(11\ k\Omega + 1\ k\Omega) = 0.08333$$

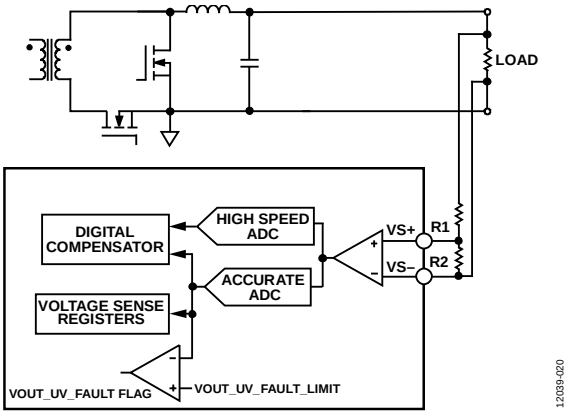


Figure 18. Voltage Sense Configuration

Voltage Sense ADCs

Two kinds of Σ-Δ ADCs are used in the ADP1050 feedback loop, as follows:

- Low frequency (LF) ADC, running at 1.56 MHz
- High frequency (HF) ADC, running at 25 MHz

The Σ-Δ ADCs have a resolution of one bit and operate differently from traditional flash ADCs. The equivalent resolution that is obtained depends on how long the output bit stream of the Σ-Δ ADC is filtered.

The Σ-Δ ADCs also differ from Nyquist rate ADCs in that the quantization noise is not uniform across the frequency spectrum. At lower frequencies, the noise decreases. At higher frequencies, the noise increases (see Figure 19).

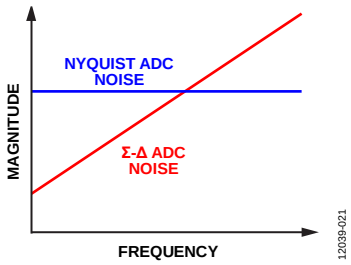


Figure 19. ADC Noise Performance

The low frequency ADC runs at approximately 1.56 MHz. For a specified bandwidth, the equivalent resolution is calculated as

$$\ln(1.56\text{ MHz}/BW)/\ln(2) = N\text{ bits}$$

For example, at a bandwidth of 95 Hz, the equivalent resolution/noise is

$$\ln(1.56\text{ MHz}/95\text{ Hz})/\ln(2) = 14\text{ bits}$$

At a bandwidth of 1.5 kHz, the equivalent resolution/noise is

$$\ln(1.56\text{ MHz}/1.5\text{ kHz})/\ln(2) = 10\text{ bits}$$

The high frequency ADC has a 25 MHz clock. It is comb filtered and outputs at the switching frequency into the digital compensator. See Table 5 for equivalent resolutions at selected sampling frequencies.

Table 5. Equivalent Resolutions for High Frequency ADC at Selected Switching Frequencies

f_{SW} (kHz)	High Frequency ADC Resolution (Bits)
49 to 87	9
97.5 to 184	8
195.5 to 379	7
390.5 to 625	6

The high frequency ADC has a range of ±25 mV. Using a base switching frequency of 97.5 kHz at an 8-bit HF ADC resolution, the quantization noise is 0.195 mV (1 LSB = 2 × 25 mV/2^8 = 0.195 mV). When the switching frequency increases to 195.5 kHz at a 7-bit HF ADC resolution, the quantization noise is 0.391 mV (1 LSB = 2 × 25 mV/2^7 = 0.391 mV). Increasing the switching frequency to 390.5 kHz increases the quantization noise to 0.781 mV (1 LSB = 2 × 25 mV/2^6 = 0.781 mV).

Output Voltage Adjustment Commands

In the ADP1050, the voltage data for commanding or reading the output voltage or related parameters is in linear data format. The linear format exponent is fixed at −10 decimal (see the VOUT_MODE command, Register 0x20, in Table 21).

The following three basic commands are used for setting the output voltage:

- VOUT_COMMAND command (Register 0x21, Table 22)
- VOUT_MARGIN_HIGH command (Register 0x25, Table 26)
- VOUT_MARGIN_LOW command (Register 0x26, Table 27)

One of these three values is selected by the OPERATION command (Register 0x01, Table 13).

The VOUT_MAX command (Register 0x24, Table 25) sets an upper limit on the output voltage that the ADP1050 can command, regardless of any other commands or combinations.

During output voltage adjustment, use the VOUT_TRANSITION_RATE command (Register 0x27, Table 28) to set the rate (in mV/µs) at which the VS± pins change voltage.

DIGITAL COMPENSATOR

Use the internal programmable digital compensator to change the control loop of the power supply. A Type III digital compensator architecture has been implemented. This Type III compensator is reconstructed by a low frequency filter, with input from the low frequency ADC, and a high frequency filter, with input from the high frequency ADC. From the voltage sense ADC outputs to the digital compensator output, the transfer function of the digital compensator in z-domain is as follows:

$$H(z) = \frac{d}{204.8 \times m} \times \frac{z}{z-1} + \frac{c}{12.8} \times \frac{z-b}{z-a}$$

where:
a = HF filter pole register value/256 (Register 0xFE32/256).
b = HF filter zero registers value/256 (Register 0xFE31/256).
c = HF filter gain register value (Register 0xFE33).
d = LF filter gain register value (Register 0xFE30).
m is the scale factor, as follows:

m = 1 when 49 kHz ≤ f_{SW} < 97.5 kHz
m = 2 when 97.5 kHz ≤ f_{SW} < 195.5 kHz
m = 4 when 195.5 kHz ≤ f_{SW} < 390.5 kHz
m = 8 when 390.5 kHz ≤ f_{SW}

To tailor the loop response to the specific application, the low frequency gain (represented by d), the zero location of the HF filter (represented by b), the pole location of the HF filter (represented by a), and the high frequency gain (represented by c) can all be set up individually (see the Digital Compensator and Modulation Setting Registers section).

It is recommended that the ADP1050 GUI be used to program the compensator. The GUI displays the filter response, using a Bode plot in the s-domain, and calculates all stability criteria for the power supply.

To transfer the z-domain value to the s-domain, plug the following bilinear transformation equation into the H(z) equation:

$$z(s) = \frac{2f_{SW} + s}{2f_{SW} - s}$$

where s is the s-domain value.

The filter introduces an extra phase delay element into the control loop. The digital compensator circuit sends the information about the duty cycle to the digital PWM engine at the beginning of each switching cycle (unlike an analog controller, which makes decisions on the duty cycle information continuously). There is an additional delay for ADC sampling and decimation filtering. This extra phase delay for phase margin (Φ) is expressed as follows:

$$\Phi = 360 \times f_C/f_{SW}$$

where
f_C is the crossover frequency.
f_{SW} is the switching frequency.

At one-tenth the switching frequency, the phase delay is 36°. The GUI incorporates this phase delay into its calculations. Note that the ADP1050 GUI does not account for other delays, such as gate driver and propagation delay.

The main compensator, called the normal mode compensator, is programmed using Register 0xFE30 to Register 0xFE33. In addition, a dedicated filter is used during soft start. The filter is disabled at the end of the soft start routine, after which the voltage loop digital compensator is used. The soft start filter gain is a programmable value of 1, 2, 4, or 8, using Register 0xFE3D[1:0].

CLOSED-LOOP INPUT VOLTAGE FEEDFORWARD CONTROL AND VF SENSE

The ADP1050 supports closed-loop input voltage feedforward control to improve input transient performance. The VF value is sensed by the feedforward ADC and is used to divide the output of the digital compensator. The result is fed into the digital PWM engine. The input voltage signal can be sensed at the center tap in the secondary windings of the isolation transformer and must be filtered by a residual current device (RCD) circuit network to eliminate the voltage spike at the switching node. Alternatively, the input voltage signal can be sensed from a winding of the auxiliary power transformer.

The VF pin (Pin 4) voltage must be set to 1 V when the nominal input voltage is applied. The feedforward ADC sampling period is 10 µs. Therefore, the decision to modify the PWM outputs, based on the input voltage, is performed at this rate.

As shown in Figure 20, the feedforward scheme modifies the modulation value, based on the VF voltage. When the VF input is 1 V, the line voltage feedforward has no effect. For example, if the digital compensator output remains unchanged and the VF voltage changes to 50% of its original value (still greater than 0.5 V), the modulation of the OUTx edges that are configured for modulation doubles.

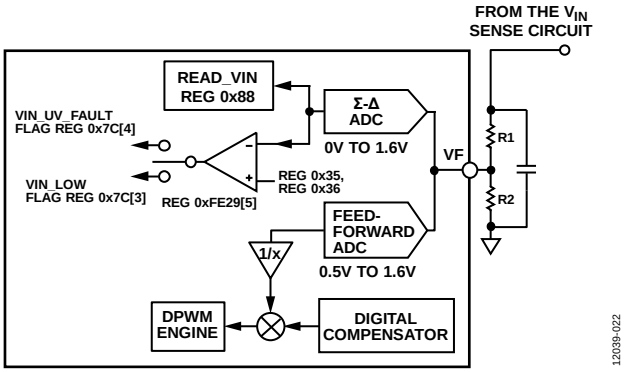


Figure 20. Closed-Loop Input Voltage Feedforward Configuration

If the digital compensator output remains unchanged and the VF voltage changes to 200% of its original value (still less than 1.6 V), the modulation of the OUTx edges that are configured for modulation is divided by 2 (see Figure 21). Register 0xFE3D[3:2] is used to program the optional input voltage feedforward function.

The VF pin also has a low speed, high resolution Σ-Δ ADC. The ADC has an update rate of 800 Hz with 11-bit resolution. The ADC output value is stored in Register 0xFEAC and converted to the READ_VIN command (Register 0x88). This value provides information for the input voltage monitoring and flag functions.

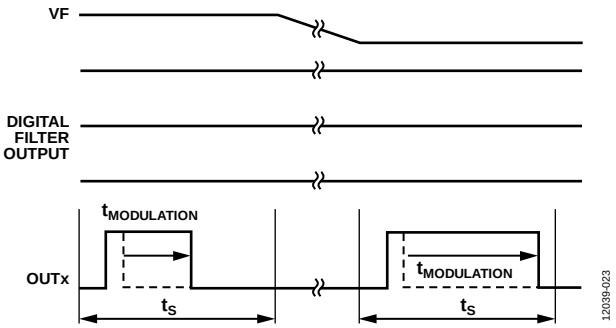


Figure 21. Closed-Loop Input Voltage Feedforward Changes Modulation Values

OPEN-LOOP INPUT VOLTAGE FEEDFORWARD OPERATION

The ADP1050 can run in open-loop input voltage feedforward operation mode. In this mode, the input voltage is sensed as the feedforward signal for the generation of the PWM outputs.

As shown in Figure 22, the digital compensator output is modified by a programmable modulation reference. The VF value, which represents the input voltage, is fed into the feedforward ADC to divide the modulation reference. The result of this division is then fed into the PWM engine. The duty cycle value is in inverse proportion to the input voltage.

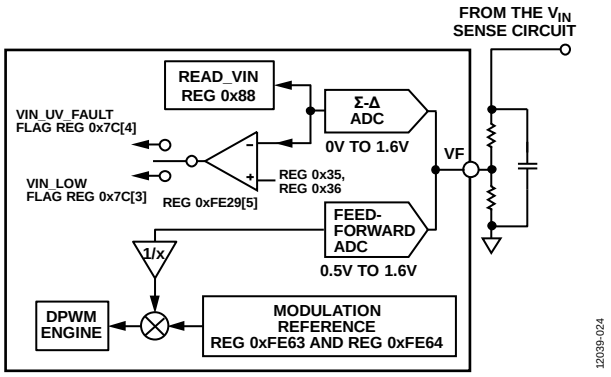


Figure 22. Open-Loop Feedforward Operation

Use the following equations to derive the output voltage equation:

$$D = \frac{V_{IN\_NOM}}{V_{IN}} \times (t_{REF} \times f_{SW})$$

and

$$V_{OUT} = \frac{V_{IN} \times D}{n}$$

The output voltage can then be derived by

$$V_{OUT} = \frac{V_{IN\_NOM} \times (t_{REF} \times f_{SW})}{n}$$

where:
D is the duty cycle value.
V_{IN_NOM} is the nominal input voltage.
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
n is the turns ratio of the main transformer.
t_{REF} is the modulation reference, which is set by Register 0xFE63 and Register 0xFE64.
f_{SW} is the switching frequency.

In the equation to derive V_{OUT}, the input voltage, V_{IN}, is cancelled out. Therefore, the output voltage does not change when the input voltage changes.

Register 0xFE63 and Register 0xFE64 set the modulation reference, based on the target output voltage and the nominal input voltage at which the VF pin voltage is 1 V (see Figure 22).

The PWM settings for open-loop input voltage feedforward operation are similar to those of general closed-loop operation. The falling edge timings, rising edge timings, and modulation are set in the same manner as for closed-loop operation, by using Register 0xFE3E to Register 0xFE52. Register 0xFE09[4:3] sets the soft start speed of the modulation edges. Register 0xFE3D[6] enables open-loop feedforward operation. Register 0xFE3D[7] is used to enable the soft start procedure for open-loop feedforward operation.

The flag settings for open-loop feedforward operation are also similar to those of general closed-loop operation.

Because the output voltage is not regulated in the same manner as in closed-loop operation, some settings, such as the V_{OUT} setting, the digital compensator settings, and the constant current mode setting, are not functional. Other settings can be programmed in a manner that is similar to general closed-loop operation.

OPEN-LOOP OPERATION

The ADP1050 can also run in open-loop operation mode. In this mode, the rising edges and falling edges of the PWM outputs are fixed during normal operation. Therefore, the output voltage varies with the input voltage. The topologies include full bridge, half bridge, and push pull converters.

The PWM settings for open-loop operation are different from those of general closed-loop operation.

1. Set the rising edge timings and falling edge timings using Register 0xFE3E to Register 0xFE4F. Typically, a duty cycle setting of ~50% is recommended for ease of zero voltage switching operation. A phase shift function of 180° is recommended to guarantee balanced PWM outputs.
2. Program Register 0xFE3C to a value of 0x00, which sets the modulation limit to 0 µs.
3. For soft start, apply negative modulation to the falling edges of the OUTA and OUTB outputs. The soft start of SR1 and SR2 is not recommended.
4. Write 111111 to Register 0xFE67[5:4] and Register 0xFE67[1:0] to set all PWM channels to follow open-loop operation. Set Register 0xFE09[7] to enable the soft start procedure. The soft start speed is specified by Register 0xFE09[4:3].
5. Always set Register 0xFE09[2] = 1. The soft start ramp time is determined by $t_{F2} - t_{R2}$.

Because the output voltage is not regulated, some of the settings, such as the V_{OUT} setting, digital compensator settings, and constant current control, are not functional. Other settings can be programmed to be similar to those of general closed-loop operation.

CS1 CURRENT SENSE (CS1 PIN)

The CS1 current sense input (Pin 5) senses, protects, and controls the primary side input. CS1 can be calibrated to reduce errors due to the external components.

Current Sense 1 (CS1) is typically used for the monitoring and protection of the primary side current, which is commonly sensed using a current transformer (CT). The input signal at the CS1 pin is fed into an ADC for current monitoring. The range of the ADC is 0 V to 1.60 V. The input signal is also fed into an analog comparator for cycle-by-cycle current limiting and I_{IN} overcurrent fast protection, with a reference of 0.25 V or 1.2 V set by Register 0xFE1B[6]. The typical configuration for the CS1 current sense is shown in Figure 23.

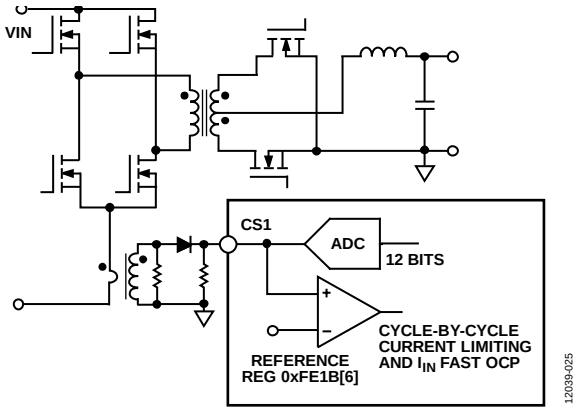


Figure 23. Current Sense 1 (CS1) Operation

The CS1 ADC is used to measure the average value of the primary side current. The ADC samples at a frequency of 1.56 MHz and reports a CS1 reading (12 bits) in the READ_IIN command (Register 0x89), with an asynchronously averaged rate of 10 ms, 52 ms, 105 ms, or 210 ms set by Register 0xFE65[1:0].

Various I_{IN} overcurrent fast fault limits and response actions can be set for CS1. These are described in the Current Sense and Limit Setting Registers section.

SOFT START AND SHUTDOWN

On/Off Control

The OPERATION command (Register 0x01) and the ON_OFF_CONFIG command (Register 0x02) control the power-on and power-off behavior of the ADP1050. The OPERATION command turns the ADP1050 on and off in conjunction with input from the CTRL pin (Pin 13). The combination of the CTRL pin input and the serial bus commands required to turn the ADP1050 on and off is configured by the ON_OFF_CONFIG command. When the ADP1050 is commanded to turn on, the power supply on (PSON) signal is enabled, and the ADP1050 follows the soft start procedure to begin the power conversion.

Soft Start

After VDD power-up and initialization, the PSON signal is enabled when the ADP1050 is commanded to turn on. The controller waits for a user specified turn-on delay (TON_DELAY, Register 0x60) before initiating output voltage soft start ramp. The soft start is then performed by actively regulating the output voltage and digitally ramping up the target voltage to the commanded voltage setpoint. The rise time of the voltage ramp is programmed, using the TON_RISE command (Register 0x61) to minimize the inrush currents associated with the start-up voltage ramp. A nonzero prebiased voltage results in a longer turn-on delay and shorter rise time.

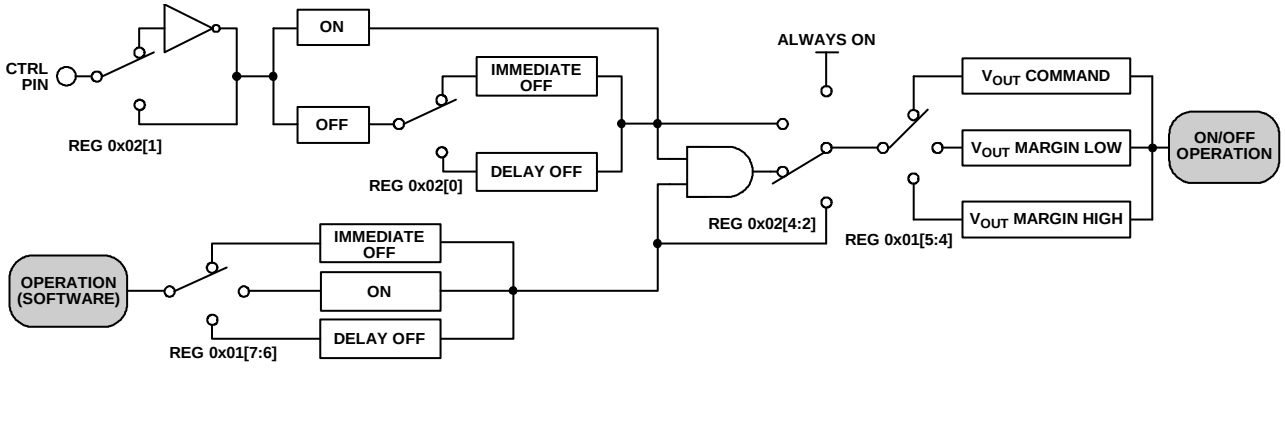


Figure 24. On/Off Control Diagram

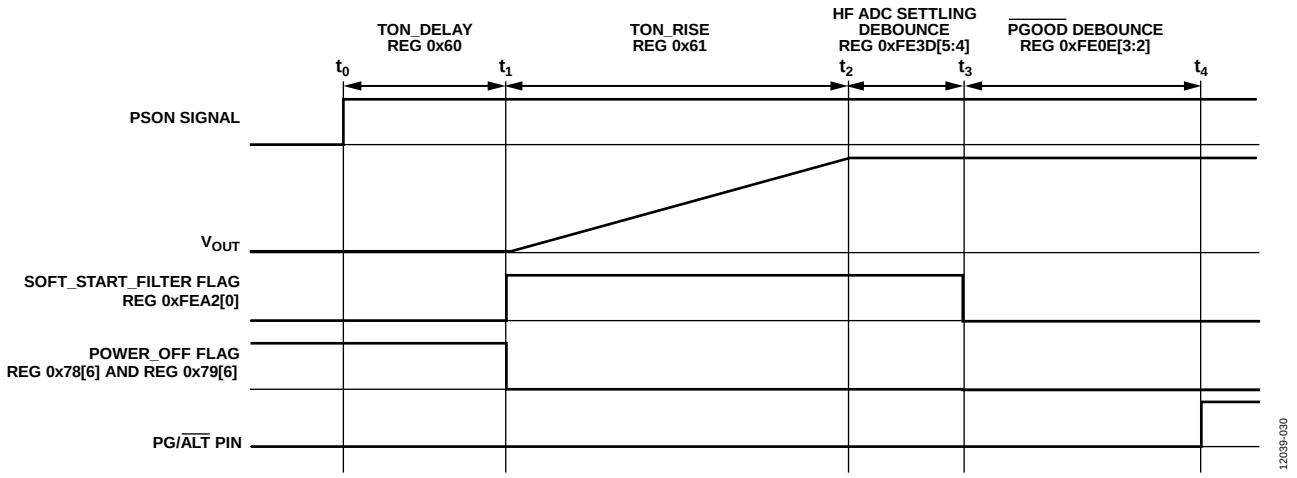


Figure 25. Soft Start Timing Diagram

When the user turns on the power supply, the following soft start procedure is initiated (see Figure 25):

1. At t_0, the PSON signal is enabled by using the OPERATION command, the ON_OFF_CONFIG command, and/or the CTRL pin. The ADP1050 verifies that the initial flags indicate no abnormalities.
2. The ADP1050 waits for the programmed TON_DELAY time to ramp up the power stage voltage at t_1. The soft start filter gain (set by Register 0xFE3D[1:0]) is used for closed-loop control.
3. The soft start begins to ramp up the internal reference. The soft start ramp time is programmed using the TON_RISE command.
4. At t_2, the soft start ramp reaches the output voltage setpoint. The high frequency ADC starts to settle.
5. Additional high frequency ADC settling debounce time can be programmed using Register 0xFE3D[5:4]. If the debounce time is used, the high frequency ADC is activated at t_3. The period between t_2 and t_3 is the high frequency ADC settling debounce time. At t_3, the control loop is switched from the soft start filter to the normal filter.

If no faults are present, the $\overline{\text{PGOOD}}$ signal waits for the programmed clearing debounce time (Register 0xFE0E[3:2]) before the PG/$\overline{\text{ALT}}$ pin is pulled high at t_4.

If a fault condition occurs during the soft start ramp (the time set by the TON_RISE command, t_1 to t_2), the ADP1050 responds as programmed, unless the flag is blanked during soft start. The user can program which flags are active during the soft start. All flags are active at the end of the soft start ramp (t_2). See the Flag Blanking During Soft Start section for more information.

The SR1 and SR2 outputs and the volt-second balance functions can also be disabled during the soft start ramp. For more information, see the Synchronous Rectification section and the Volt-Second Balance Control section, respectively.

Digital Filters During Soft Start

A dedicated soft start filter is used during soft start. The soft start filter is a pure low frequency filter with a programmable gain. The filter is disabled at the end of the soft start routine (t_2), and then the general digital compensator is used. The soft start filter gain is programmed using Register 0xFE3D[1:0]. The soft start filter is used during the ramp time of the voltage reference, until the VS high frequency ADC is settled. The user can program (using Register 0xFE3D[4]) whether a high frequency ADC debounce time is added. The high frequency ADC debounce time is the interval from when the high frequency ADC is settled to when the frequency filter takes action. The debounce time can be programmed at 5 ms or 10 ms using Register 0xFE3D[5]. During the time when the soft start filter is in use, the SOFT_START_FILTER flag is set. It is recommended that a high frequency ADC debounce time not be used if the fast load transient occurs during soft start.

Software Reset

The software reset command allows the user to perform a software reset of the ADP1050. When a 1 is written to Register 0xFE06[0], the power supply is immediately turned off and then restarted with a soft start following a restart delay. The restart delay time can be programmed as 0 ms, 500 ms, 1 sec, or 2 sec (Register 0xFE07[1:0]). If both TON_DELAY and the restart delay are programmed with 0 ms, a write to Register 0xFE06[0] does nothing.

Shutdown

When the ADP1050 is commanded to turn off, the PSON signal is cleared. Depending on the setting of the OPERATION command, the ADP1050 shuts down immediately or waits for a user specified turn-off delay (TOFF_DELAY) prior to the shutdown action.

If the ADP1050 is turned off because a fault condition occurs, the shutdown actions are programmed by the specific fault flag responses. See the Power Monitoring, Flags, and Fault Responses section for more information. The $\overline{\text{PGOOD}}$ flag setting debounce time can be programmed in Register 0xFE0E[1:0]). This debounce time is from when the $\overline{\text{PGOOD}}$ setting condition is met to when the $\overline{\text{PGOOD}}$ flag is set and the PG/$\overline{\text{ALT}}$ pin is pulled low.

Power-Good Signals

The ADP1050 has an open-drain, power-good pin, PG (PG/$\overline{\text{ALT}}$, Pin 14). When the pin is logic high, the power is good. The ADP1050 also has a power-good flag, $\overline{\text{PGOOD}}$, which is a negation of power good. When this flag is set, it indicates that the power is not good. The PG/$\overline{\text{ALT}}$ pin and the $\overline{\text{PGOOD}}$ flag can be programmed to respond to the flags from the following list:

- VIN_UV_FAULT
- IIN_OC_FAST_FAULT
- VOUT_OV_FAULT
- VOUT_UV_FAULT
- OT_FAULT
- OT_WARNING

Register 0xFE0D is used to program the masking of these flags, which prevents them from setting the $\overline{\text{PGOOD}}$ flag and driving the PG/$\overline{\text{ALT}}$ pin low. Register 0xFE0E[1:0] is used to set the debounce time to drive the PG/$\overline{\text{ALT}}$ pin low and set the $\overline{\text{PGOOD}}$ flag (see Figure 26).

The POWER_GOOD_ON command (Register 0x5E) sets the voltage limit that the output voltage must exceed before the $\overline{\text{POWER\_GOOD}}$ flag (Register 0x79[11]) can be cleared. Similarly, the output voltage must fall below the POWER_GOOD_OFF limit (Register 0x5F) for the $\overline{\text{POWER\_GOOD}}$ flag to be set.

The PG/$\overline{\text{ALT}}$ pin is always driven low and the $\overline{\text{PGOOD}}$ flag is always set when one of the POWER_OFF, SOFT_START_FILTER, CRC_FAULT, or $\overline{\text{POWER\_GOOD}}$ flags is set.

The debounce timings for setting and clearing the $\overline{\text{PGOOD}}$ flag can be programmed to 0 ms, 200 ms, 320 ms, or 600 ms in Register 0xFE0E[3:0].

VOLT-SECOND BALANCE CONTROL

The ADP1050 has a dedicated circuit to maintain volt-second balance in the main transformer when operating in full bridge topology. This circuit eliminates the need for a dc blocking capacitor. In interleaved topologies, volt-second balance can also be used for current balancing to ensure that each interleaved phase contributes equal power.

The circuit monitors the current flowing in both legs of the full bridge topology and stores this information. It compensates the selected PWM signals to ensure equal current flow in the two legs of the full bridge topology. The CS1 pin is used as the input for this function.

Several switching cycles are required for the circuit to operate effectively. The maximum amount of modulation applied to each edge of the selected PWM outputs is programmable to ±80 ns or ±160 ns, using Register 0xFE54[2]. The balance control gains are programmable via Register 0xFE54[1:0].

The compensation of the PWM drive signals is performed on the edges of two selected outputs, using Register 0xFE55 and Register 0xFE57. The direction of the modulation is also programmable in these registers.

The volt-second balance control can be disabled during soft start using Register 0xFE0C[1].

There are also leading edge blanking functions at the sensed CS1 signal for more accurate control results. The blanking time follows the CS1 cycle-by-cycle current-limit blanking time (see the CS1 Current Sense section).

To avoid the wrong compensation in light load condition, there is a CS1 threshold in Register 0xFE38 to enable volt-second balance. Below this threshold, volt-second balance is not enabled.

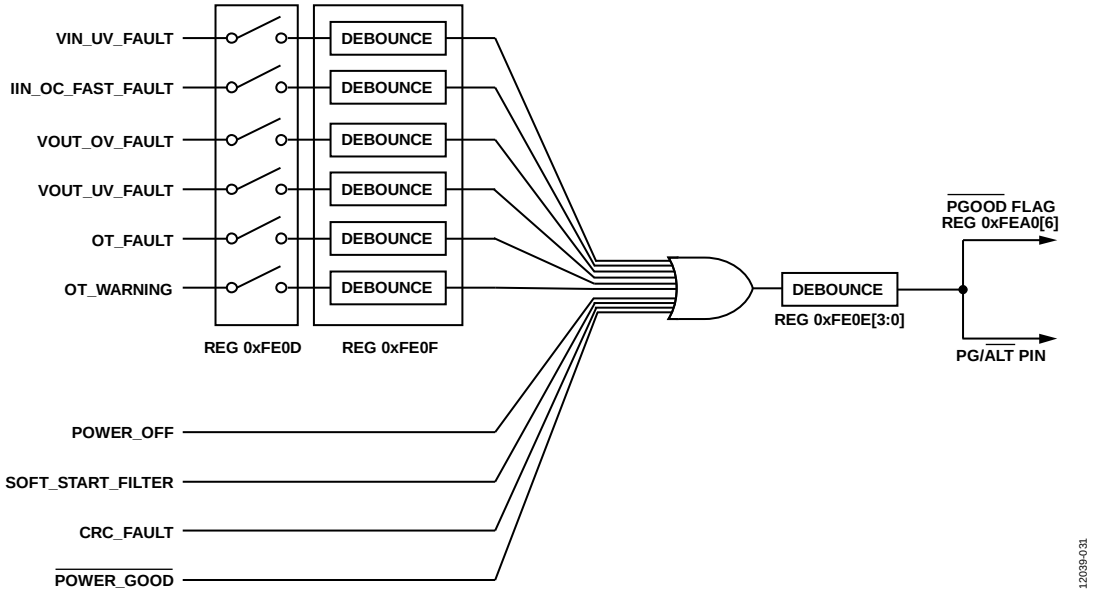


Figure 26. $\overline{\text{PGOOD}}$ Programming

PULSE SKIPPING

The pulse skipping function can reduce the switching loss under very light load current conditions while keeping the output voltage stable. Register 0xFE67[6] can be set to activate this function.

As the output current falls, the supply enters discontinuous conduction mode (DCM). In DCM, the modulation value is a function of the load current. If a very light load current requires a modulation value (duty cycle) of less than the threshold set by Register 0xFE69, pulse skipping mode is enabled. In pulse skipping mode, the PWM output appears intermittently. If the digital compensator signals an error requiring a modulation value that is less than the threshold set by Register 0xFE69, no PWM pulses are generated. If the digital compensator signals an error requiring a modulation value that is greater than the threshold that is set by Register 0xFE69, PWM pulses are generated. Pulse skipping mode is always blanked during soft start.

PREBIAS STARTUP

The prebias start-up function provides the capability to start up the ADP1050 with a prebiased voltage on the output. It protects the power supply against existing external voltage on the output during startup and ensures a monotonic startup before the power supply reaches full regulation (see Figure 27).

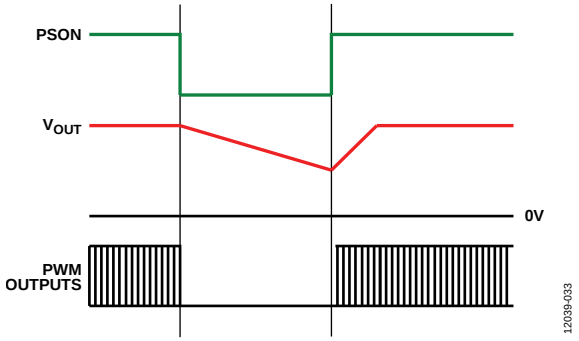


Figure 27. Prebias Startup

The prebias start-up function is enabled by Register 0xFE25[7]. During prebias startup, the ADP1050 soft start ramp starts at the existing voltage value sensed on the VS± pins, and the soft start ramp time is reduced proportionally. The initial PWM modulation value does not begin with zero but, instead, with a value that builds a balanced relationship between the input voltage and the output voltage. This balance avoids the sudden charging or discharging of the output capacitor and achieves a monotonic and smooth startup. The initial modulation value is calculated by the following equation:

$$t_{MODU\_INI} = t_{MODU\_NOM} \times \frac{V_{OUT}}{V_{OUT\_NOM}} \times \frac{V_{IN\_NOM}}{V_{IN}}$$

where:
t_{MODU_INI} is the initial modulation value when the controller begins to generate PWM pulses during startup.
t_{MODU_NOM} is the modulation value set by Register 0xFE39. This value emulates the modulation value when the input voltage and the output voltage are in the nominal condition.
V_{OUT} is the output voltage sensed on the VS± pins.
V_{OUT_NOM} is the nominal output voltage set by VOUT_COMMAND (Register 0x21).
V_{IN_NOM} is the nominal input voltage when the VF pin voltage = 1 V.
V_{IN} is the sensed input voltage.

In addition, Register 0xFE6C[1] is set for correct operation. To sense the input voltage (represented by VF) when the power supply is off, use additional circuitry, such as an auxiliary power circuit, to sense the input voltage.

If the input voltage signal is not available when the power is off, the t_{MODU_INI} value is calculated based on the t_{MODU_NOM} and the output voltage information. In this case, Register 0xFE6C[1] is cleared to 0.

The initial modulation value is calculated as follows:

$$t_{MODU\_INI} = t_{MODU\_NOM} \times \frac{V_{OUT}}{V_{OUT\_NOM}}$$

where:
t_{MODU_INI} is the initial modulation value when the controller begins to generate PWM pulses during startup.
t_{MODU_NOM} is the modulation value set by Register 0xFE39. This value emulates the modulation value when the input voltage and the output voltage are in the nominal condition.
V_{OUT} is the output voltage sensed on the VS± pins.
V_{OUT_NOM} is the nominal output voltage set by VOUT_COMMAND (Register 0x21).

If the closed-loop line voltage feedforward function is selected, the input voltage is introduced from the feedforward loop, and the V_{IN} value is always included for calculation of the initial modulation value.

SR soft start can also be enabled in this mode to achieve a smooth transition. See the Synchronous Rectification section for more information.

VDD AND VCORE

When the voltage of the VDD pin (V_{DD}) is applied, there is a delay before the ADP1050 can regulate the power supply. When V_{DD} rises above the power-on reset and UVLO levels, it takes ~20 µs for the VCORE pin (Pin 15) to reach its operational point of 2.6 V. The EEPROM contents are then downloaded to the registers. The download takes approximately 120 µs. After the EEPROM contents are downloaded, the ADP1050 is ready for operation; however, it takes a maximum of 52 ms for the ADP1050 to complete initialization of the address after a power-on reset. Therefore, it is recommended that the master device access the ADP1050 at least 52 ms after a power-on reset.

If the ADP1050 is programmed to power up at this time, the soft start ramp begins. Otherwise, the device waits for a PSON signal, as programmed in Register 0x01 and Register 0x02.

To minimize trace length, the proper amount of decoupling capacitance must be placed between the VDD pin (Pin 16) and the AGND pin (Pin 17), as close as possible to the device. The same requirement applies to the VCORE pin (Pin 15). It is recommended that the VCORE pin not be used as a reference or to generate other logic levels using resistive dividers.

CHIP PASSWORD

On power-up, some registers in the ADP1050 are locked and protected from being written to or read from. When the chip is locked, the following commands and all read only registers are accessible:

- Operation
- ON_OFF_CONFIG
- CLEAR_FAULTS
- WRITE_PROTECT
- RESTORE_DEFAULT_ALL
- VOUT_COMMAND
- VOUT_TRIM
- VOUT_CAL_OFFSET

Unlock the Chip Password

To unlock the chip password, perform two consecutive writes with the correct password (default value = 0xFFFF) using the CHIP_PASSWORD command (Register 0xD7). Between the two write actions, any read or write action to another register in this device interrupts the unlocking of the chip password. The CHIP_PASSWORD_UNLOCKED flag (Register 0xFEA0[7]) is set to indicate that the chip password is unlocked for access.

Lock the Chip Password

To lock the chip password, use the CHIP_PASSWORD command (Register 0xD7) to write any value other than the correct password. The CHIP_PASSWORD_UNLOCKED flag (Register 0xFEA0[7]) is then cleared to indicate that the chip password is locked from access.

Change the Chip Password

To change the chip password, first write the old password using the CHIP_PASSWORD command (Register 0xD7). Next, write the new password using the same command. The chip password is changed to the new password. If the chip password is to be changed permanently, the register contents must be saved in the EEPROM after the chip password is changed. If the correct chip password is lost, the RESTORE_DEFAULT_ALL command (Register 0x12) restores the factory default settings. In this case, all the user settings are reset.

POWER MONITORING, FLAGS, AND FAULT RESPONSES

The ADP1050 has extensive system and fault condition monitoring capabilities for the sensed signals. The system monitoring functions include current, voltage, power, and temperature readings. The fault conditions include out-of-limit values for current, voltage, power, and temperature. The limits for the fault conditions are programmable, and flags are set when the limits are exceeded.

FLAGS

The ADP1050 has an extensive set of flags, including the PMBus standard flags and manufacturer specific flags, that are set when certain limits, thresholds are exceeded or certain conditions are met. A setting of 1 indicates that a fault or warning event has occurred. A setting of 0 indicates that a fault or warning event has not occurred.

PMBus Standard Flags

Figure 28 shows a summary of the ADP1050 PMBus standard fault status registers. The CLEAR_FAULTS command (Register 0x03) is used to clear all bits in the PMBus status registers (Register 0x78 to Register 0x7E) simultaneously.

Manufacturer Specific Flags

Register 0xFEA0 to Register 0xFEA2 store the manufacturer specific flags. These flags include the following:

- Housekeeping flags, such as CHIP_PASSWORD_UNLOCKED, VDD_OV, EEPROM_UNLOCKED, and CRC_FAULT.
- Flags that can be programmed for protection responses, such as CS3_OC_FAULT and FLAGIN.
- Status flags, such as PGOOD, SYNC_LOCKED, CHIP_ID, PULSE_SKIPPING, modulation, and SOFT_START_FILTER.

For detailed descriptions of these flags, see the Manufacturer Specific Fault Flag Registers section.

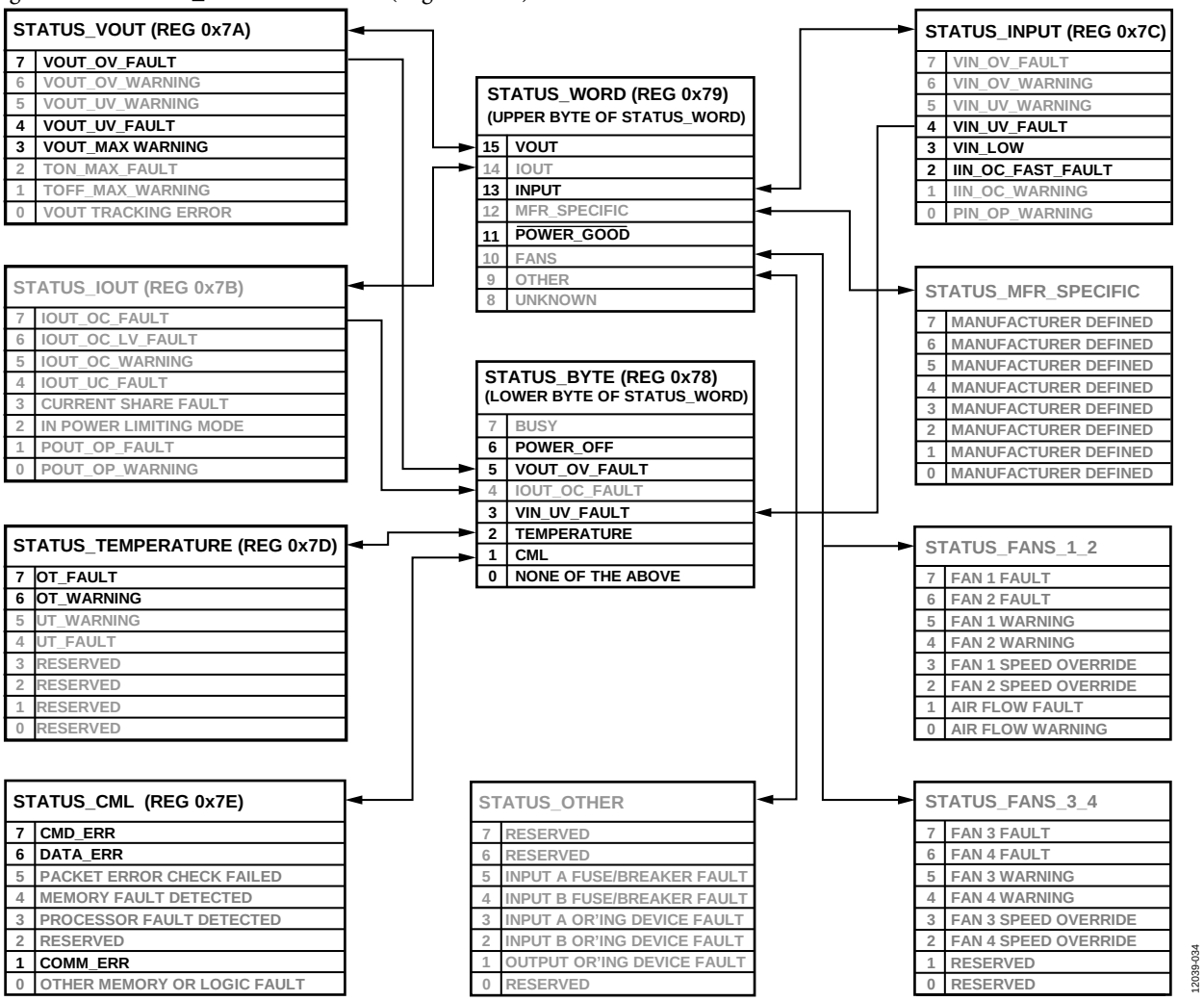


Figure 28. Summary of the Fault Status Registers (Only the Commands in Black Are Supported by the ADP1050; the Commands in Gray are Not Supported.)

Manufacturer Specific Latched Flags

The ADP1050 has a set of latched flag registers (Register 0xFEA3 to Register 0xFEA5). The latched flag registers have the same flags as Register 0xFEA0 to Register 0xFEA2, but the flags in the latched registers remain set so that intermittent faults can be detected. Reading a latched flag register resets all the flags in that register. A PSON signal can also reset the latched flags.

Flags Debounce Time

The debounce timing of the manufacturer specific flags and the PMBus standard flags is programmable (see Table 6). The debounce time is the time during which the fault condition must be continuously triggered before the flag is set. Refer to the corresponding register settings for more information.

The debounce time is used for flag setting. Only the $\overline{\text{PGOOD}}$ flag has a debounce time for flag clearing. For all other flags, the flag reenable delay, specified in Register 0xFE05[7:6] (see Table 99), functions as the debounce time for flag clearing. Refer to the Manufacturer Specific Protection Responses section for details.

Housekeeping Flags

The CHIP_PASSWORD_UNLOCKED flag (Register 0xFEA0[7]) indicates that the chip password is in the unlocked state, and all the registers can be accessed.

The VDD_OV flag (Register 0xFEA0[0]) is set when the V_{DD} voltage exceeds the V_{DD} overvoltage lockout (OVLO) threshold. The debounce time is programmable as 2 µs or 500 µs, using Register 0xFE05[4]. When the flag is set, the ADP1050 shuts down. The flag is always cleared when Register 0xFE05[5] is set, regardless of the V_{DD} voltage.

The EEPROM_UNLOCKED flag (Register 0xFEA2[3]) indicates that the EEPROM is in the unlocked state and can be updated.

The CRC_FAULT flag (Register 0xFEA2[2]) indicates that an error has occurred when downloading the EEPROM contents to the internal registers. The device shuts down and requires a PSON signal (programmed in Register 0x01 and Register 0x02) and/or the toggling of the CTRL pin (Pin 13) to restart.

Flag Blanking During Soft Start

Flag blanking means that when a fault condition is met, the corresponding flag is set, but there are no related actions.

The following flags are always blanked during soft start:

- VOUT_UV_FAULT
- OT_FAULT

The following flags can be programmed to be blanked during soft start, using Register 0xFE0B:

- VOUT_OV_FAULT (Bit 0)
- CS3_OC_FAULT (Bit 1)
- IIN_OC_FAST_FAULT (Bit 3)
- VIN_UV_FAULT (Bit 4)
- FLAGIN (Bit 6)

If a flag is blanked during soft start, it is also blanked during the TON_DELAY time.

Table 6. Flag Debounce Time

Flag	Debounce Time	Register
VOUT_OV_FAULT	0 µs, 1 µs, 2 µs, 8 µs	0xFE26[7:6]
VOUT_UV_FAULT	0 ms, 20 ms, 40 ms, 80 ms, 160 ms, 320 ms, 640 ms, 1280 ms	0x45[2:0]
OT_FAULT	1 sec	0x50[2:0]
OT_WARNING	0 ms, 100 ms	0xFE2F[2]
CS3_OC_FAULT	0 ms, 10 ms, 20 ms, 200 ms	0xFE19[6:5]
VIN_UV_FAULT	0 ms, 2.5 ms, 10 ms, 100 ms	0xFE29[1:0]
FLAGIN	0 µs, 100 µs	0xFE12[1]
VDD_OV	2 µs, 500 µs	0xFE05[4]
$\overline{\text{PGOOD}}$	0 ms, 200 ms, 320 ms, 600 ms	0xFE0E[3:0]

First Flag ID Recording

When the ADP1050 registers one or several fault conditions, it stores the first flag in a dedicated first flag ID register (Register 0xFEA6). The first flag ID represents the first flag that triggers a shutdown response. The following types of flags are not recorded in the first flag ID register:

- Flags that are configured to be ignored
- Flags that have a configured response causing the PWM outputs to be disabled, but that do not use a soft start to reenable the PWM outputs after the fault is resolved
- Flags that have a configured response causing the synchronous rectifiers to be disabled

The first flag ID register gives the user more information for fault diagnosis than a simple flag. This register also stores the previous first fault ID.

The status of the first flag ID register can be saved to the EEPROM, as well, by setting Register 0xFE0C[3]. To limit the number of writes to the EEPROM, only the first flag after a VDD power reset can be saved to the EEPROM. During the next VDD power-on, the first flag ID is downloaded from the EEPROM and loaded to the first flag ID register (Register 0xFEA6).

Figure 29 shows the timing diagram for the first flag ID recording scheme. Table 7 describes the actions shown in Figure 29.

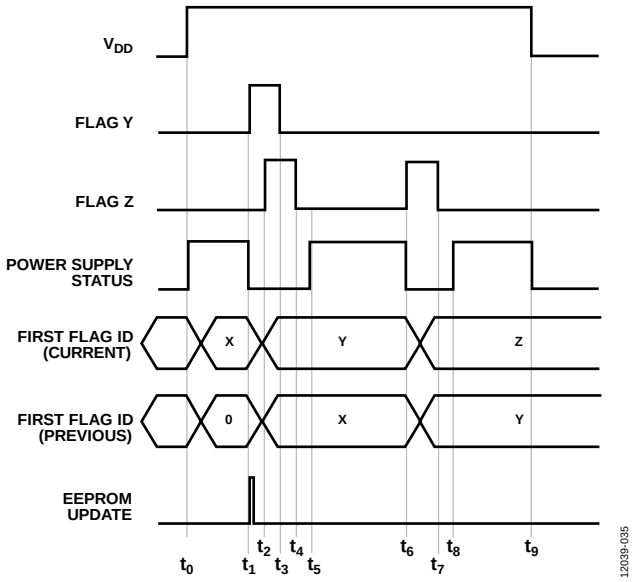


Figure 29. First Flag Timing

Table 7. First Flag ID Timing[1]

Step	Action	Power Supply	First Flag ID in Register		First Flag ID in EEPROM	
			Previous ID	Current ID	Previous ID	Current ID
t_0	As an example, the previous ID and the current ID in the EEPROM are 0 and Flag X, respectively. When the V_{DD} voltage is applied on the ADP1050, the first flag ID is downloaded from the EEPROM to the first flag ID register (Register 0xFEA6).	On	0	Flag X	0	Flag X
t_1	A fault (Flag Y) shuts down the power supply. In the first flag ID register, Flag Y is now the current flag ID, and Flag X is the previous flag ID. The first flag ID register is updated accordingly. The EEPROM is then updated to save this information.	Off	Flag X	Flag Y	Flag X	Flag Y
t_2	Another fault (Flag Z) occurs while the power supply is off. Because Flag Z is not the first flag that caused the shutdown, neither the first flag ID register nor the EEPROM is updated.	Off	Flag X	Flag Y	Flag X	Flag Y
t_3	Flag Y is cleared, but Flag Z keeps the power supply off. The first flag ID register and the EEPROM are not updated.	Off	Flag X	Flag Y	Flag X	Flag Y
t_4	Flag Z is cleared. The first flag ID register is not updated.	Off	Flag X	Flag Y	Flag X	Flag Y
t_5	The power supply is turned on again after the flag reenable delay. The first flag ID register is not updated.	On	Flag X	Flag Y	Flag X	Flag Y
t_6	The fault indicated by Flag Z shuts down the power supply. Flag Z is now the current first flag ID, and Flag Y is the previous flag ID. The first flag ID register is updated accordingly. The EEPROM is not updated to save the information.	Off	Flag Y	Flag Z	Flag X	Flag Y
t_7	Flag Z is cleared. The first flag ID register is not updated.	Off	Flag Y	Flag Z	Flag X	Flag Y
t_8	The power supply is turned on again after the flag reenable delay. The first flag ID register is not updated.	On	Flag Y	Flag Z	Flag X	Flag Y
t_9	The V_{DD} voltage is removed and the power supply is turned off.	Off	N/A	N/A	N/A	N/A

[1] N/A means not applicable.

VOLTAGE READINGS

Input Voltage Reading

The input voltage, which is reported in the READ_VIN command (Register 0x88), is updated every 10 ms. The VIN_SCALE_MONITOR command (Register 0xD8) is set for correct input voltage reading.

The input voltage is sensed through the VF pin (Pin 4). The VF ADC has an input range of 1.6 V. The raw data is stored in Register 0xFEAC. The reading is 11 bits, meaning that the LSB size is 1.6 V/2048 = 781.25 µV.

Because the input voltage signal can be sensed through the switching node of the secondary windings, the voltage drop caused by the conduction current in the primary switches, transformer windings, and copper trace adds to the error to the input voltage sense. The following equation is used to compensate for the error:

$$Y_{COMP} = Y_{UNCOMP} \pm (N \times X \div 2^{11})$$

where:
Y_{COMP} is the compensated VF value in Register 0xFEAC[15:5].
Y_{UNCOMP} is the uncompensated VF value in Register 0xFEAC[15:5].
N is the compensation coefficient set in Register 0xFE59[7:0], and the polarity is set in Register 0xFE58[0].
X is the CS1 current value in Register 0xFEA7[15:4].

The compensated VF value is used for conversion of the READ_VIN value.

Output Voltage Reading

The output voltage is reported in the READ_VOUT command (Register 0x8B) and updated every 10 ms. The VOUT_SCALE_MONITOR command (Register 0x2A) is programmed for correct output voltage reading.

The VS voltage value register (Register 0xFEAA) is updated every 10 ms via the VS low frequency ADC.

The VS low frequency ADC has an input range of 1.6 V. The raw data is stored in Register 0xFEAA. The reading is 12 bits, which means that the LSB size is 1.6 V/4096 = 390.625 µV.

CURRENT READINGS

By default, the current readings are updated every 10 ms; however, Register 0xFE65[1:0] can be used to change the update rate to 52 ms, 105 ms, or 210 ms.

Input Current Reading

The input current is reported in the READ_IIN command (Register 0x89). The IIN_SCALE_MONITOR command (Register 0xD9) is set for correct input current reading.

The input current reading is derived from the CS1 ADC, which has an input range of 1.6 V. The raw data is stored in Register 0xFEA7. The reading is 12 bits, which means that the LSB size is 1.6 V/4096 = 390.625 µV.

CS3 Current Reading

The CS3 reading is an alternative output current reading that is calculated using the CS1 reading and the duty cycle values. The CS3 reading can be used as an alternate output current reading and protection when the current sense resistor is not used. The output current reading is derived from the following equation:

$$I_{OUT} = I_{CS3} \times n$$

where I_{CS3} is read from Register 0xFEA9[15:4], and n is the turns ratio of the main transformer ($n = N_{PRI}/N_{SEC}$).

Each LSB size in Register 0xFEA9[15:4] is 4× the LSB size of the CS1 reading in Register 0xFEA7. For example, if 1 LSB = 0.1 A in Register 0xFEA7[15:4], 1 LSB in Register 0xFEA9[15:4] = 0.4 A.

POWER READINGS

Input Power Reading

The input power value (Register 0xFEAE) is the product of the VF voltage value in Register 0xFEAC[15:5] and the CS1 current value in Register 0xFEA7[15:4]. Therefore, a combination of both voltage and current formulas is used to calculate the power reading in watts (W). Register 0xFEAE is a 16-bit word. It multiplies two 12-bit numbers and then discards the eight LSBs.

For example, if 1 LSB in Register 0xFEAC[15:5] is 0.01 V and 1 LSB in Register 0xFEA7[15:4] is 0.01 A, 1 LSB in Register 0xFEAE[15:0] is 0.01 V × 0.01 A × 2^8 = 0.0256 W.

DUTY CYCLE READING

The READ_DUTY_CYCLE command (Register 0x94, which gives the duty cycle of the PWM output value) is updated every 10 ms. Register 0xFE58[3:2] is set for correct reading of general PWM type topologies; these bits select the PWM channel (OUTA or OUTB) for which the duty cycle value is reported.

SWITCHING FREQUENCY READING

The READ_FREQUENCY command (Register 0x95) is used to report the switching frequency information in kHz.

TEMPERATURE READING

The RTD pin (Pin 20) is set up for use with an external negative temperature coefficient (NTC) thermistor. The RTD pin has an internal programmable current source. An ADC monitors the voltage on the RTD pin. The RTD ADC has an input range of 1.6 V. The raw data is stored in Register 0xFEAB. It is a 12-bit reading, which means that the LSB size is 1.6 V/4096 = 390.625 µV.

Using Register 0xFE2D[7:6], an internal precision current source can be configured to generate a 10 µA, 20 µA, 30 µA, or 40 µA current. This current source can be trimmed, by means of an internal DAC, to compensate for thermistor accuracy. To set the current source to the factory default value of 46 µA, write 0xE6 to Register 0xFE2D.

The output of the RTD ADC is linearly proportional to the voltage on the RTD pin; however, thermistors exhibit a nonlinear function of resistance vs. temperature. Therefore, it is necessary to perform postprocessing on the RTD ADC reading to accurately read the temperature.

By connecting an external resistor in parallel with the NTC thermistor, linearization is achieved. Figure 31 shows the RTD and OTP operation. Using the factory default value of 46 µA and the linearization scheme, the temperature, expressed in degrees Celsius (°C), can be read directly via the READ_TEMPERATURE command (Register 0x8D). The temperature reading is derived from the RTD ADC output, and it is updated every 10 ms. The ADP1050 implements a linearization scheme that is based on a preselected combination of external components and current selection (see the Temperature Linearization Scheme section).

Optionally, the user can process the RTD reading and perform postprocessing in the form of a lookup table or polynomial equation to match the specific NTC thermistor used.

In this case, the external resistor in parallel is not needed. With an internal current source of 46 µA, the equation to calculate the ADC code at a certain NTC value (R_X) is given by the following formula:

$$ADC\ CODE = 46\ \mu A \times R_X/390.7\ \mu V$$

For example, at 60°C, the NTC thermistor connected to the RTD pin is 21.82 kΩ. Therefore,

$$RTD\ ADC\ CODE = 46\ \mu A \times 21.82\ k\Omega/390.7\ \mu V = 2570$$

For the overtemperature function, the RTD threshold (in volts) can be transferred through the OT_FAULT_LIMIT command in Register 0x4F, using the linearization equations shown in the Temperature Linearization Scheme section.

Alternatively, the temperature reading and overtemperature protection function can be implemented by applying an external analog temperature sensor, such as the STLM20. See Figure 30 for more information. Using this solution, the temperature sense range can be as low as −40°C. To facilitate this approach, disable the internal current source by writing 0x00 to Register 0xFE2D and setting Register 0xFE2B[2]. The temperature reading in degrees Celsius can be derived by the following formula:

$$T = 159.65 - \frac{ADC\ CODE}{29.92} \times \frac{R1 + R2}{R2}$$

where the *ADC CODE* is the reading in Register 0xFEAB[15:4]. The recommended values of R1 and R2 are 20 kΩ and 10 kΩ, respectively.

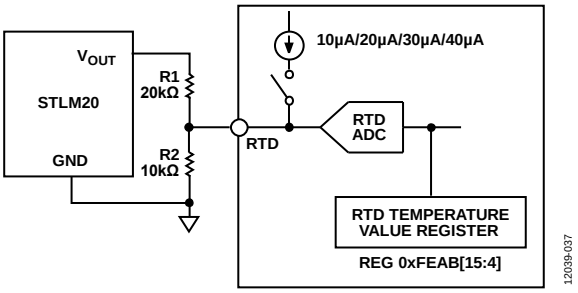


Figure 30. Temperature Sensing by an Analog Temperature Sensor

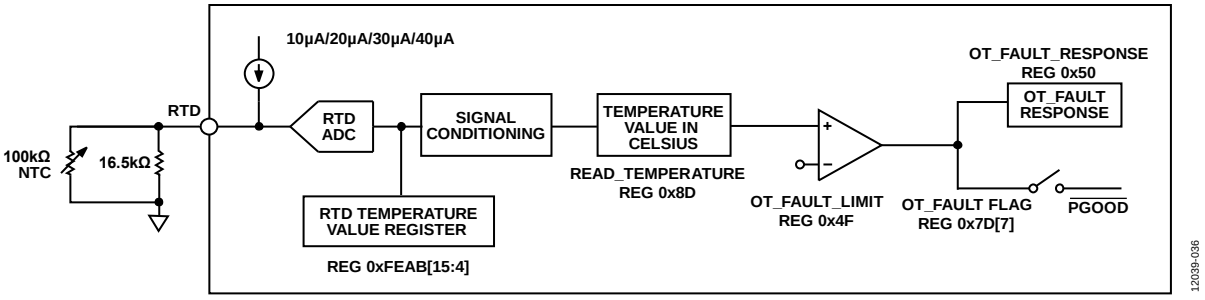


Figure 31. RTD and OTP Operation

TEMPERATURE LINEARIZATION SCHEME

The ADP1050 linearization scheme is based on a combination of a thermistor (R25 = 100 kΩ, 1%), an external resistor (16.5 kΩ, 1%), and the 46 µA current source, preselected for best performance when linearizing measured temperatures in the industrial range.

The NTC thermistor that is required must have a resistance of R25 = 100 kΩ, 1%, such as the NCP15WF104F03RC (beta = 4250, 1%). It is recommended that 1% tolerance be used for both the resistor and beta values. The linearization equations show the relationship between the RTD voltage, V_{RTD} (in volts), and temperature reading, T (in degrees Celsius).

If T < 104°C,

$$V_{RTD} = (130 - T) \times \frac{1.6}{256}$$

If T ≥ 104°C,

$$V_{RTD} = (156 - T) \times \frac{1.6}{512}$$

where *T* represents the temperature reading in Register 0x8D.

Figure 32 shows the temperature linearization curves.

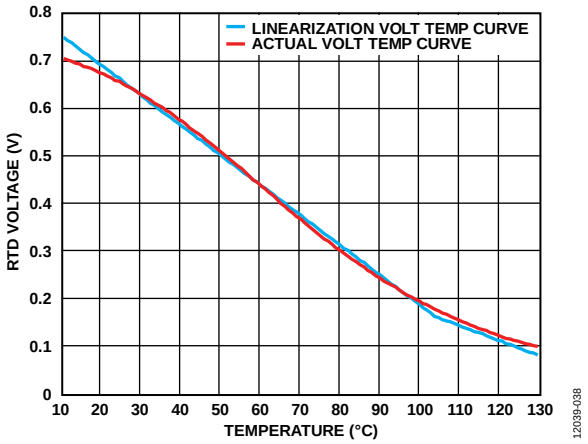


Figure 32. Temperature Linearization Scheme Curves

Using the internal linearization scheme, the READ_TEMPERATURE command (Register 0x8D) returns the current temperature in degrees Celsius. For overtemperature protection, the user can directly set the OT_FAULT_LIMIT command (Register 0x4F) in degrees Celsius. See the OT_FAULT and OT_WARNING section for more information.

PMBus PROTECTION COMMANDS

V_{OUT} Overvoltage Protection (OVP)

The V_{OUT} overvoltage protection feature in the ADP1050 follows PMBus specifications. The limits are programmed in the VOUT_OV_FAULT_LIMIT command (Register 0x40) to correspond to the voltage between 75% and 150% of the nominal output voltage. The responses are programmed using the VOUT_OV_FAULT_RESPONSE command (Register 0x41). The VOUT_OV_FAULT flag (Register 0x78[5], Register 0x79[5], and Register 0x7A[7]) is set when the voltage reading exceeds the overvoltage limit.

In a direct parallel system, multiple power supply units are connected directly in parallel without any OR'ing device. An overvoltage condition in one power supply can raise the common bus voltage, causing the activation of overvoltage protection in the other power supplies connected to the common bus. As a result of this overvoltage protection action, the common bus may fail. The ADP1050 provides a highly flexible, conditional overvoltage protection function for redundant control in a direct parallel system. It consists of an overvoltage detection block, a modulation flag triggering block, and an overvoltage response block (see Figure 33).

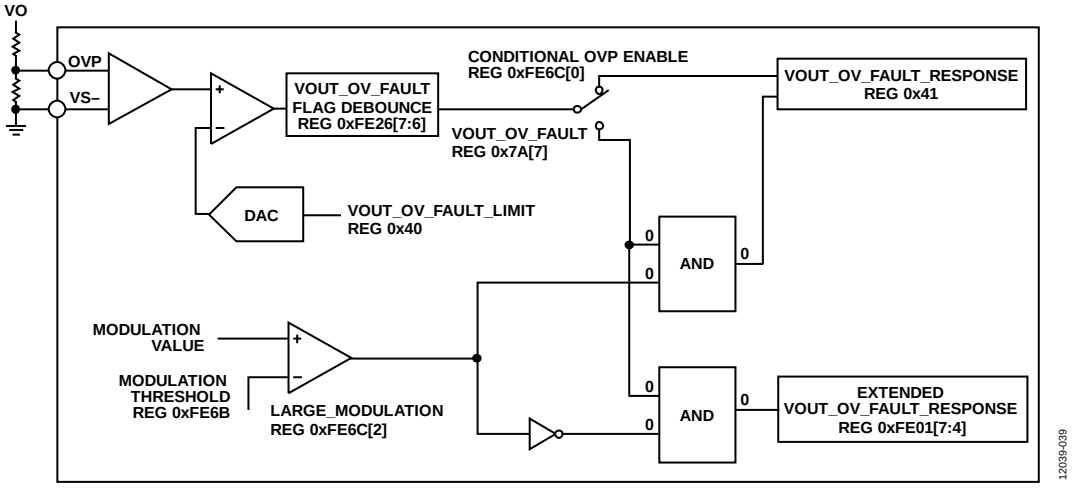


Figure 33. V_{OUT} Overvoltage Protection Circuit Implementation

In the overvoltage detection block, there is an internal analog comparator to detect the output voltage and generate the VOUT_OV_FAULT flag when an overvoltage condition occurs. The overvoltage reference voltage is set in Register 0x40. The debounce time of the flag setting can be programmed for 0 µs, 1 µs, 2 µs, or 8 µs, using Register 0xFE26[7:6]. There is also a 40 ns propagation delay, which is measured from the time when the OVP voltage exceeds the threshold to the time when the comparator output status is changed.

In the modulation flag triggering block, the real-time modulation value is compared to the internal reference to generate the LARGE_MODULATION flag. Register 0xFE6C[2] sets the LARGE_MODULATION flag when the real-time modulation value exceeds the modulation threshold set by Register 0xFE6B.

In the overvoltage responses block, there are two groups of overvoltage protection responses: the VOUT_OV_FAULT_RESPONSE PMBus command, set in Register 0x41, and the extended VOUT_OV_FAULT_RESPONSE, set in Register 0xFE01[7:4].

There is a conditional OVP enable switch in Register 0xFE6C[0]. If the switch is cleared to 0, the conditional OVP function is disabled and the OVP response always follows the VOUT_OV_FAULT_RESPONSE PMBus command (Register 0x41). If the switch is set to 1, the OVP response follows the VOUT_OV_FAULT_RESPONSE command or the extended VOUT_OV_FAULT_RESPONSE, depending on the status of the LARGE_MODULATION flag.

For example, when using a direct parallel system, if the VS+ pin (Pin 3) and the VS− pin (Pin 2) in one power supply unit (PSU) are shorted and this PSU experiences overvoltage failure, all the PSUs detect the overvoltage signal. The LARGE_MODULATION flag is used to identify the failed PSU. Typically, the failed PSU is shut down, and the other PSUs continue to operate normally.

The modulation threshold is typically set with a value that is slightly less than the modulation limit setting in Register 0xFE3C; however, the modulation limit can change when the ADP1050 unit acts as a slave device to synchronize with an external clock (see the Switching Frequency and Synchronization Registers section for more information).

For more information about extended overvoltage protection, see the Manufacturer Specific Protection Responses section and the related register settings.

V_{OUT} Undervoltage Protection (UVP)

The V_{OUT} undervoltage protection feature follows PMBus specifications. The limits are programmed using the VOUT_UV_FAULT_LIMIT command (Register 0x44), and the responses are programmed in the VOUT_UV_FAULT_RESPONSE command (Register 0x45). When the voltage reading in the READ_VOUT command (Register 0x8B) falls below the VOUT_UV_FAULT_LIMIT value, the VOUT_UV_FAULT flag in Register 0x7A[4] is set.

During the period of the soft start ramp, the turn-on delay time is specified by the TON_DELAY command (Register 0x60), and the flag reenable delay time is specified by Register 0xFE05[7:6]. The VOUT_UV_FAULT flag is always blanked. Under these conditions, the VOUT_UV_FAULT flag is never triggered by an undervoltage condition.

OT_FAULT and OT_WARNING

The overtemperature protection feature in the ADP1050 follows PMBus specifications. With the default setting, the OTP limit is programmed using the OT_FAULT_LIMIT command in Register 0x4F, and the response is programmed using the OT_FAULT_RESPONSE command (Register 0x50).

There is an overtemperature warning flag, OT_WARNING, in Register 0x7D[6]. The OT_WARNING limit is less than the OT_FAULT_LIMIT, with an overtemperature hysteresis specified by Register 0xFE2F[1:0].

When the temperature sensed at the RTD pin (Pin 20) exceeds the OT_WARNING limit, the OT_WARNING flag (Register 0x7D[6]) is set. When the temperature sensed at RTD pin exceeds the OT_FAULT_LIMIT, the OT_FAULT flag (Register 0x7D[7]) is set. The OT_FAULT and OT_WARNING flags are cleared when the temperature falls below the OT_WARNING limit (see Figure 34).

The OT_FAULT flag and the OT_WARNING flag can each be separately set to trigger the $\overline{\text{PGOOD}}$ flag and drive the PG/$\overline{\text{ALT}}$ pin (Pin 14) low.

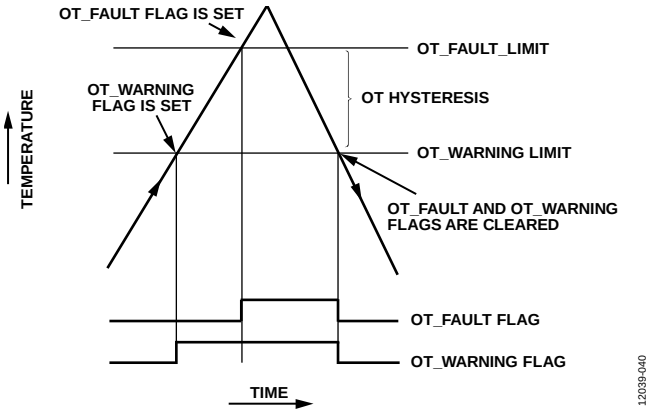


Figure 34. OT Protection and OT Warning Operation

Optionally, the user can process the RTD reading and use the linearization equation to determine the overtemperature protection setting. This allows the user to program the RTD threshold for greater overtemperature protection accuracy.

Alternatively, if an analog temperature sensor, such as the STLM20, is used, the OT_FAULT limit can still be programmed using the OT_FAULT_LIMIT command (Register 0x4F), but a conversion equation is needed.

Using Figure 30 as an example, assume that R1 and R2 are 20 kΩ and 10 kΩ, respectively, and the value in Register 0x4F is $T_{OT\_SET\_LIMIT}$.

If $T_{OT\_SET\_LIMIT}$ < 104 decimal,

$$T_{OT\_ACTUAL\_LIMIT} = 1.6039 \times T_{OT\_SET\_LIMIT} - 48.8623$$

If $T_{OT\_SET\_LIMIT}$ ≥ 104 decimal

$$T_{OT\_ACTUAL\_LIMIT} = 0.801967 \times T_{OT\_SET\_LIMIT} + 34.5423$$

Table 8 shows some typical OTP threshold settings when using an analog temperature sensor, such as the STLM20.

Table 8. Typical OT Fault Limit Settings When Using an Analog Temperature Sensor

$T_{OT\_SET\_LIMIT}$ OT Limit Programmed in Register 0x4F (In Decimal)	$T_{OT\_ACTUAL\_LIMIT}$ Actual OT Limit (°C)
55	39.35
60	47.37
65	55.39
70	63.41
75	71.43
80	79.45
85	87.47
90	95.49
95	103.51
100	111.53
105	118.75
110	122.76
115	126.77
120	130.78
125	134.79
130	138.80

If the STLM20 is used, the temperature hysteresis can be set using Register 0xFE2F[1:0], as follows:

00 = 3.21°C, 01 = 6.42°C, 10 = 9.62°C, or 11 = 12.83°C

VIN_ON and VIN_OFF

Two PMBus commands, VIN_ON (Register 0x35) and VIN_OFF (Register 0x36), allow the user to set the input voltage on and off limits independently.

The VIN_LOW flag in Register 0x7C[3] is set at initialization. When the input voltage exceeds the VIN_ON limit, the VIN_LOW flag is cleared. If the PSON signal is asserted, the power conversion starts. When the input voltage drops below the VIN_OFF limit, the VIN_LOW flag is set and the power conversion stops. The delay time for the power conversion start and stop can be set separately by Register 0xFE29[3:2] and Register 0xFE29[4].

Alternatively, if the input voltage signal is not available before startup, the VIN_ON and VIN_OFF commands can be set for input voltage undervoltage protection using Register 0xFE29[5].

The VIN_UV_FAULT flag in Register 0x78[3], Register 0x79[3], and Register 0x7C[4] is set if the input voltage reading falls below the VIN_OFF limit.

The debounce time of the VIN_UV_FAULT flag setting can be programmed at 0 ms, 2.5 ms, 10 ms, or 100 ms, using Register 0xFE29[1:0]. Because the V_{IN} reading is averaged every 1 ms, there is an additional debounce time of up to 1 ms.

The response to the VIN_UV_FAULT flag is programmed via the VIN_UV_FAULT_RESPONSE bits (Register 0xFE02[7:4]). Refer to the Manufacturer Specific Protection Responses section and Table 97 for details.

MANUFACTURER SPECIFIC PROTECTION COMMANDS

CS1 Cycle-by-Cycle Current Limit

The CS1 cycle-by-cycle current limit is implemented using an internal analog comparator (see Figure 23). When the voltage at the CS1 pin (Pin 5) exceeds the threshold set by Register 0xFE1B[6], the comparator output is triggered high and an internal flag (CS1_ OCP, which is not accessible by the user and, therefore, not listed in the register tables) is triggered. There is a 105 ns (maximum) propagation delay in the comparators.

A blanking time of 0 ns, 40 ns, 80 ns, 120 ns, 200 ns, 400 ns, 600 ns, or 800 ns can be set to ignore the current spike at the beginning of the current signal. The blanking time is set in Register 0xFE1F[6:4].

During this time, the comparator output is ignored. The blanking time of the CS1_OCP flag can be referenced to the rising edges of OUTA and OUTB, using Register 0xFE1D[1:0].

A debounce time of 0 ns, 40 ns, 80 ns, or 120 ns can also be added to improve the noise immunity of the CS1 OCP comparator output circuit. The debounce time is set using Register 0xFE1F[1:0]. This is the minimum time that the CS1 signal must be constantly above the threshold before the PWM outputs are shut down.

Figure 35 shows an example of CS1 cycle-by-cycle current-limit timing, with the rising edge of OUTA as the blanking time reference. When the CS1_OCP flag is set, it is not cleared until the beginning of the next switching cycle.

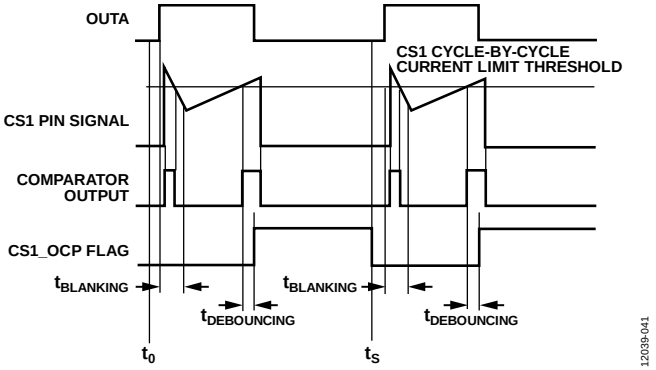


Figure 35. CS1 Cycle-by-Cycle Current-Limit Timing

When the CS1_OCP flag is triggered, Register 0xFE08[6:5] and Register 0xFE0E[5:4] can be used to disable all PWM outputs for the remainder of the switching cycle. They are reenabled at the start of the next switching cycle. During one switching cycle, if the rising edge of a PWM output occurs after the CS1_OCP flag is triggered, the PWM remains enabled for the switching cycle.

To avoid current overstress of the body diode of the synchronous rectifiers, the cycle-by-cycle current-limit actions of the SR1 and SR2 outputs can be further programmed by Register 0xFE1E[1:0].

They can be programmed in the same way as the other PWM outputs, or they can be programmed so that when the CS1_OCP flag is triggered, the SR PWM output is turned on. There is a 145 ns to 180 ns delay (dead time) between the CS1_OCP flag being triggered and the turning on of the SR PWM outputs. The falling edges continue to follow the programmed value.

The cycle-by-cycle current limit is always activated regardless of the I_{IN} overcurrent fast protection settings. The comparator output can be completely ignored by setting Register 0xFE1F[7].

I_{IN} Overcurrent Fast Protection

N, an internal counter, is a positive integer or zero, with an initial value of 0. The counters work as follows:

- When the CS1_OCP flag is triggered in one cycle (the CS1 OCP comparator is triggered high), N is counted as $N_{CURRENT} = N_{PREVIOUS} + 2$.
- If the CS1_OCP flag is not triggered in one cycle and $N_{PREVIOUS} > 0$, $N_{CURRENT} = N_{PREVIOUS} - 1$.
- If the CS1_OCP flag is not triggered in one cycle and $N_{PREVIOUS} = 0$, $N_{CURRENT} = 0$.

When the value of N reaches the limit specified by IIN_OC_FAST_FAULT_LIMIT, the IIN_OC_FAST_FAULT flag is triggered (see Figure 36).

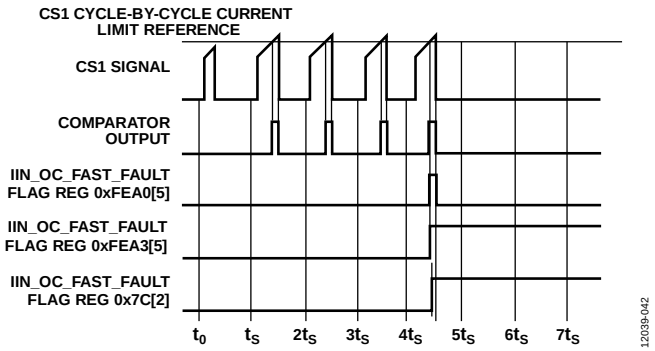


Figure 36. I_{IN} Overcurrent Fast Fault Triggering

For the single-ended topologies, such as forward converter and buck converter, a switching cycle consists of one cycle. For the double-ended topologies, such as full bridge converter, half bridge converter, and push pull converter, there are two cycles in a switching cycle. The IIN_OC_FAST_FAULT_LIMIT bits are in Register 0xFE1A[6:4]. In Figure 36, the IIN_OC_FAST_FAULT_LIMIT value is set to 8.

The response of the IIN_OC_FAST_FAULT flag can be programmed in the IIN_OC_FAST_FAULT_RESPONSE bits (Register 0xFE00[3:0]). See the Manufacturer Specific Protection Responses section and the register settings for the action details.

Matched Cycle-by-Cycle Current Limit in a Half Bridge Converter

For the half bridge converter, the cycle-by-cycle current-limit feature, described in the CS1 Cycle-by-Cycle Current Limit, cannot guarantee the balance of duty cycles between two half cycles in one switching cycle.

The imbalances of each half cycle can cause the center point voltage of the capacitive divider to drift from $V_{IN}/2$ toward either the ground or the input voltage, V_{IN}. This drift, in turn, can lead to output voltage regulation failure, transformer saturation, and doubling of the drain to source voltage (V_{DS}) stress of the synchronous rectifiers.

To compensate for these imbalances, matched cycle-by-cycle current limiting is implemented in the ADP1050 by forcing each cycle to be equalized, or matched, to the previous one.

When the matched cycle-by-cycle current limit is triggered, the duty cycle in the following half cycle exactly matches the actual duty cycle in the preceding half cycle. However, the cycle-by-cycle current limit is always the highest priority to terminate the PWM channels. For example, if one previous cycle has a duty cycle of 20% under a cycle-by-cycle current-limit condition, also match the following cycle to a duty cycle of 20%. However, if the cycle-by-cycle current limit occurs in the following cycle and it must terminate the PWM with a smaller duty cycle, the cycle-by-cycle current limit takes higher priority and the duty cycle can be a value that is smaller than 20%.

The matched cycle-by-cycle current limit is enabled by Register 0xFE1D[6].

CS3 Overcurrent Protection

CS3 overcurrent protection provides alternative output overcurrent protection if the direct output current sense is not available. The reading is calculated from the CS1 and duty cycle readings.

The CS3_OC_FAULT flag (Register 0xFEA0[3]) is set when the CS3 current reading of the eight most significant bits (MSBs) in Register 0xFEA9 exceeds the CS3_OC_FAULT_LIMIT that is programmed in Register 0xFE6A. The debounce time of the flag setting can be programmed at 0 ms, 10 ms, 20 ms, or 200 ms in Register 0xFE19[6:5]. The response of the CS3_OC_FAULT flag is programmed in the CS3_OC_FAULT_RESPONSE bits (Register 0xFE01[3:0]). See the Manufacturer Specific Protection Responses section.

FLAGIN Protection

The SYNI/FLGI pin (Pin 10) can be configured in flag input mode (FLGI). An external signal can be sent to the ADP1050 to trigger an action. The polarity of the external signal is configured by the FLGI polarity bit (Register 0xFE12[2]). When the ADP1050 detects an external signal, the FLAGIN flag is set. The response to the FLAGIN flag is programmed in the FLAGIN_RESPONSE bits (Register 0xFE03[3:0]). See the Manufacturer Specific Protection Responses section.

V_{DD} OVLO Protection

The ADP1050 has built-in overvoltage protection (OVP) on its supply rail. The V_{DD} overvoltage response bits (VDD_OV_RESPONSE), found in Register 0xFE05[5:4], are used to specify the response to a V_{DD} overvoltage condition.

- If Register 0xFE05[5] = 0, the VDD_OV flag is set and the ADP1050 shuts down when the V_{DD} voltage rises above the OVLO threshold. When the V_{DD} overvoltage condition ends, the VDD_OV flag is cleared and the ADP1050 downloads the EEPROM contents before restarting with a soft start process. The debounce time of the VDD_OV flag can be programmed using Register 0xFE05[4].
- If Register 0xFE05[5] = 1, the VDD_OV flag is always cleared, regardless of V_{DD} voltage conditions. The ADP1050 continues to operate without interruption.

It is recommended that the VDD_OV flag response not be programmed as always cleared.

MANUFACTURER SPECIFIC PROTECTION RESPONSES

For the VDD_OV flag and protection action, see the VDD OVLO Protection section.

The following flags can be configured to trigger protection responses: IIN_OC_FAST_FAULT, VOUT_OV_FAULT, CS3_OC_FAULT, VIN_UV_FAULT, and FLAGIN. The VOUT_OV_FAULT flag, which triggers the manufacturer specific protection in Register 0xFE01[7:4], is used only for conditional overvoltage protection. See the VOUT Overvoltage Protection (OVP) section for details.

Each of the aforementioned flags can be individually programmed to trigger one of the following responses:

- Continue operation without interruption (flag ignored)
- Disable SR1 and SR2
- Disable all PWM outputs

After the condition that triggered the flag is resolved and the flag is cleared, the ADP1050 can be programmed to respond as follows:

- After the flag reenable delay time elapses, reenable the disabled PWM outputs with a soft start sequence.
- Reenable the disabled PWM outputs immediately without the soft start process.
- Keep the PWM output disabled. A PSON reset signal must be used to reenable the PWM outputs with a soft start sequence.

The first flag that causes all PWM outputs to be disabled and requires a soft start if the PWM outputs are reenabled is recorded as the first flag ID. For more information about use of the first flag ID, see the First Flag ID Recording section.

A flag reenable delay can be set for the listed manufacturer specific flags. This delay is used if the configured action for a flag is to reenable the PWM outputs after the flag reenable delay. This delay can be set to 250 ms, 500 ms, 1 sec, or 2 sec, using Register 0xFE05[7:6].

POWER SUPPLY CALIBRATION AND TRIM

All the ADP1050 devices are factory trimmed. If the ADP1050 is not trimmed in the power supply production environment, it is recommended that components with a 0.1% tolerance be used for the inputs to the CS1, VS±, VF, and OVP pins to meet data sheet specifications (see the Specifications section).

In the power supply production environment, the ADP1050 can calibrate items, such as output voltage and trim, for tolerance errors that are introduced by sense resistors and resistor dividers, as well as its own internal circuitry. The ADP1050 allows the user enough trim capability to trim for external components with a tolerance of ≤0.5%.

To unlock the trim registers for write access, the user must perform two consecutive write actions with the correct password (factory default value = 0xFF), using the TRIM_PASSWORD command (Register 0xD6). Any read or write action to another register in this device, occurring between these two write actions, interrupts the unlocking of the chip password.

The trim registers are Register 0xFE14, Register 0xFE20, Register 0xFE28, and Register 0xFE2A through Register 0xFE2C. For complete information about these registers, see the Manufacturer Specific Extended Commands Descriptions section.

I_{IN} TRIM (CS1 TRIM)

Using a DC Signal

A known dc voltage (Vx) is applied at the CS1 pin. The IIN_SCALE_MONITOR command (Register 0xD9) is set to 0x0001. The READ_IIN input current reading command (Register 0x89) generates a digital code (representing the input current in amperes) that is equal to the Vx voltage value. The CS1 gain trim register (Register 0xFE14) is adjusted until the input current reading in Register 0x89 reads the correct digital code.

Using an AC Signal

A known ac current (Ix) is applied to the PSU input. This current passes through a current transformer, a diode rectifier, and an external resistor (R_{CS1}) to convert the current information to a voltage (Vx). This voltage is fed into the CS1 pin. The IIN_SCALE_MONITOR is calculated as follows:

$$IIN\_SCALE\_MONITOR = (N_{PRI}/N_{SEC}) \times R_{CS1}$$

where N_{PRI} and N_{SEC} are the turns of the primary side and secondary side windings, respectively, of the current transformer.

The READ_IIN input current reading command generates a digital code, representing the input current, Ix. The CS1 gain trim register (Register 0xFE14) is adjusted until the input current reading in Register 0x89 reads the correct digital code.

V_{OUT} TRIM (VS TRIM)

The voltage sense input at the VS± pins is optimized for sensing signals at 1 V and cannot sense a signal greater than 1.6 V. It is recommended that the nominal output voltage be reduced to 1 V for best performance. The resistor divider introduces errors that must be trimmed. The ADP1050 has enough trim range to trim errors that are introduced by resistors with a tolerance of ≤0.5%.

To trim the errors introduced by the resistor divider, use the following procedure:

1. Set the VOUT_COMMAND (Register 0x21) with the nominal output voltage value. Set the VOUT_SCALE_LOOP command (Register 0x29) and the VOUT_SCALE_MONITOR command (Register 0x2A) based on the resistor divider information.
2. Enable the power supply with the no-load current. The voltage of the VS± pins is divided down by the VS± resistor dividers to give a target of 1 V at the VS± pins.
3. Adjust the VOUT_CAL_OFFSET trim (Register 0x23) to ensure that the output voltage is exactly the target output voltage.
4. Adjust the VS gain trim register (Register 0xFE20) when the READ_VOUT reading in Register 0x8B is the exact output voltage reading.

V_{IN} TRIM (VF GAIN TRIM)

The voltage sense inputs are optimized for the VF pin signals at 1 V and cannot sense a signal greater than 1.6 V. A resistor divider is required to divide the sensed voltage signal into a voltage of less than 1.6 V. It is recommended that the VF voltage signal be reduced to 1 V for best performance. The resistor divider introduces errors, which must be trimmed.

Use the following procedure:

1. Set the VIN_SCALE_MONITOR command in Register 0xD8 based on the resistor divider information (see Figure 20) and the turns ratio information of the transformer.

$$\text{IN\_SCALE\_MONITOR} = \frac{R2}{R1 + R2} \times \frac{N_{SEC}}{N_{PRI}}$$

   where N_{PRI} and N_{SEC} are the turns of the primary side and secondary side windings, respectively, of the transformer.
2. Apply the nominal input voltage at the no load condition to achieve a targeted voltage of approximately 1 V at the VF pin.
3. Adjust the VF gain trim register (Register 0xFE28) when the READ_VIN reading in Register 0x88 is the exact nominal voltage reading.
4. Adjust the input voltage compensation multiplier (Register 0xFE59) to make the READ_VIN reading match the exact input voltage at the full load condition.

RTD AND OTP TRIM

The RTD requires two trims, one for the ADC and one for the current source. To use the internal linearization scheme, additional trimming procedures are required.

Trimming the Current Source

Register 0xFE2D[7:6] sets the value of the RTD current source to 10 µA, 20 µA, 30 µA, or 40 µA. Register 0xFE2D[5:0] can be used to fine-tune the current value. By fine-tuning the internal current source, component tolerance can be compensated and errors can be minimized. One LSB in Bits[5:0] = 160 nA.

A decimal value of 1 adds 160 nA to the current source set by Register 0xFE2D[5:0]; a decimal value of 63 adds 63 × 160 nA = 10.08 µA to the current source set by Register 0xFE2D[7:6].

Use Register 0xFE2D[7:6] to program a value for the current source, selecting the nearest possible option (10 µA, 20 µA, 30 µA, or 40 µA). Then use Register 0xFE2D[5:0] to achieve the finer step size.

For example, to use a value of 46 µA as the current source, complete the following steps:

1. Place a known resistor (Rx) from the RTD pin to AGND.
2. Set Register 0xFE2D[7:6] to 11 binary (40 µA).
3. Increase the value of Register 0xFE2D[5:0], 1 LSB at a time, until the voltage at the RTD pin is V_{RTD} = 46 µA × Rx.

The current source is now calibrated and set to the factory default value.

Trimming the ADC

The first option for trimming the ADC uses the internal linearization scheme with 46 µA RTD current, which provides an accurate reading, expressed in degrees Celsius, read in the READ_TEMPERATURE command (Register 0x8D) in decimal format.

Use an R25 = 100 kΩ, 1% accuracy NTC thermistor with beta = 4250, 1% accuracy (such as the NCP15WF104F03RC) in parallel with an external resistor of 16.5 kΩ, 1% accuracy, with the ADP1050. With this NTC thermistor and resistor combination, the ADP1050 default current source trim is set to 46 µA to achieve the best possible accuracy over temperatures ranging from 85°C to 125°C.

If an external microcontroller is used, the RTD ADC value in Register 0xFEAB can be fed into the microcontroller, and a different linearization scheme can be implemented in terms of a best-fit polynomial for the selected NTC characteristics.

LAYOUT GUIDELINES

This section explains best practices to ensure optimal performance of the ADP1050. In general, place all components of the ADP1050 control circuit as close to the ADP1050 as possible. The OVP and VS+ signals are referred to VS−. All other signals are referred to the AGND plane.

CS1 PIN

Route the traces from the current sense transformer to the ADP1050, parallel to each other. Keep the traces near each other, but far away from the switch nodes.

VS+ AND VS− PINS

Route the traces from the remote voltage sense point to the ADP1050 parallel to each other. Connect VS− to AGND, with a low ohmic connection. Keep the traces near each other, but far away from the switch nodes. Place a 100 nF capacitor from VS− to AGND to reduce the common-mode noise. If VS− is connected directly to AGND, the capacitor is not needed.

Place 10 Ω resistors between the PWM outputs and isolators or drivers inputs, especially if the isolators and drivers are far from the ADP1050. Keep the traces far away from the switch nodes.

VDD PIN

Place decoupling capacitors as close as possible to the ADP1050. A 2.2 µF capacitor connected from VDD to AGND is recommended.

VCORE PIN

Place a 330 nF decoupling capacitor from the VCORE pin to AGND, as close as possible to the ADP1050.

RES PIN

Place a 10 kΩ (±0.1%) resistor from the RES pin to AGND, as close as possible to the ADP1050.

SDA AND SCL PINS

Route the traces to the SDA and SCL pins parallel to each other. Keep the traces near each other, but far away from the switch nodes.

EXPOSED PAD

Solder the exposed pad under the ADP1050 to the PCB AGND plane.

RTD PIN

Route the traces (including the ground returning trace) from the thermistor to the ADP1050. Place the thermistor near the hotspot of the power supply, and keep the thermistor and the traces away from the switching node. Place the 1 nF filtering capacitor nearby, in parallel with the thermistor.

AGND PIN

Create an AGND ground plane on the adjacent layer of the ADP1050 and make a single-point (star) connection to the power supply system ground.

PMBus/I²C COMMUNICATION

The PMBus slave allows a device to interface with a PMBus-compliant master device, as specified by the *PMBus Power System Management Protocol Specification* (Revision 1.2, September 6, 2010). The PMBus slave is a 2-wire interface that can be used to communicate with other PMBus compliant devices and is compatible in a multimaster, multislave bus configuration.

PMBus FEATURES

The function of the PMBus slave is to decode the command that is sent from the master device and respond as requested. Communication is established using an I²C-like, 2-wire interface with a clock line (SCL) and data line (SDA). The PMBus slave is designed to externally move chunks of 8-bit data (bytes) while maintaining compliance with the PMBus protocol. The PMBus protocol is based on the *System Management Bus (SMBus) Specification*, Version 2.0, August 2000. The SMBus specification is, in turn, based on the Philips *I²C Bus Specification*, Version 2.1, dated January 2000. The PMBus incorporates the following features:

- Slave operation on multiple device systems
- 7-bit addressing
- 100 kbps and 400 kbps data rates
- General call address support
- Support for clock low extension (clock stretching)
- Separate multibyte receive and transmit FIFOs
- Extensive fault monitoring

OVERVIEW

The PMBus slave module is a 2-wire interface that can be used to communicate with other PMBus compliant devices. Its transfer protocol is based on the Philips I²C transfer mechanism. The ADP1050 is always configured as a slave device in the overall system. The ADP1050 communicates with the master device using one data pin (SDA, Pin 12) and one clock pin (SCL, Pin 11). Because the ADP1050 is a slave device, it cannot generate the clock signal; however, it is capable of stretching the SCL line to put the master device in a wait state when it is not ready to respond to the request of the master.

Communication is initiated when the master device sends a command to the PMBus slave device. Commands can be read or write commands, and data is transferred between the devices in a byte wide format. Commands can also be send commands; in that case, the command is executed by the slave device upon receiving the stop bit. The stop bit is the last bit in a complete data transfer, as defined in the PMBus/I²C communication protocol. During communication, the master and slave devices send acknowledge (A) or no acknowledge ($\overline{A}$) bits as a method of handshaking between devices. See the PMBus specification for a more detailed description of the communication protocol.

When communicating with the master device, it is possible for illegal or corrupted data to be received by the PMBus slave. In this case, the PMBus slave must respond to the invalid command or data, as defined by the PMBus specification, and indicate to the master device that an error or fault condition has occurred. This method of handshaking can be used as a first level of defense against inadvertent programming of the slave device that can potentially damage the chip or system.

The PMBus specification defines a set of generic PMBus commands that is recommended for a power management system; however, each PMBus device manufacturer can choose to implement and support certain commands that are deemed fit for the system. In addition, the PMBus device manufacturer can choose to implement manufacturer specific commands, the functions of which are not included in the generic PMBus command set. The list of standard PMBus and manufacturer specific commands can be found in the PMBus Command Set and Manufacturer Specific Extended Command List sections.

PMBus/I²C ADDRESS

The PMBus address of the ADP1050 is set by connecting an external resistor from the ADD pin (Pin 19) to AGND. Table 9 lists the recommended resistor values and the associated PMBus addresses. Eight different addresses can be used.

Table 9. PMBus Address Settings and Resistor Values

PMBus Address	Resistor Value (kΩ)
0x70	10 (or connect the ADD pin directly to AGND)
0x71	31.6
0x72	51.1
0x73	71.5
0x74	90.9
0x75	110
0x76	130
0x77	150 (or connect the ADD pin directly to VDD)

The recommended resistor values in Table 9 can vary by ±2 kΩ. Therefore, it is recommended that 1% tolerance resistors be used on the ADD pin.

The ADP1050 responds to the standard PMBus broadcast address (general call) of 0x00. However, when more than one ADP1050 device is connected to the master device, it is not recommended that the general call address be used because the data returned by multiple slave devices is corrupted.

For more information, see the General Call Support section.

DATA TRANSFER

Format Overview

The PMBus slave follows the transfer protocol of the SMBus specification, which is based on the fundamental transfer protocol format of the I²C bus specification. Data transfers are byte wide, lower byte first. Each byte is transmitted serially, most significant bit (MSB) first. A typical transfer is shown in Figure 37. See the

SMBus and I²C specifications for in-depth descriptions of the transfer protocols.

Figure 37 through Figure 44 use the abbreviations listed in Table 10.

Table 10. Abbreviations Used in Data Transfer Diagrams

Abbreviation	Description	Setting[1]
S	Start condition	N/A
P	Stop condition	N/A
Sr	Repeated start condition	N/A
$\overline{W}$	Write bit	0
R	Read bit	1
A	Acknowledge bit	0
$\overline{A}$	No acknowledge bit	1

[1] N/A means not applicable.

Command Overview

Data transfer using the PMBus slave is established using PMBus commands. The PMBus specification requires that all PMBus commands start with a slave address, with the R/$\overline{W}$ bit cleared to 0, followed by the command code. All PMBus commands that are supported by the ADP1050 follow one of the protocol types shown in Figure 38 through Figure 44.

The ADP1050 also supports manufacturer specific extended commands. These commands follow the same protocol as the standard PMBus commands; however, the command code consists of two bytes that range from 0xFF00 to 0xFFAF.

Using the manufacturer specific extended commands, the PMBus device manufacturer can add an additional 256 manufacturer specific commands to its PMBus command set.

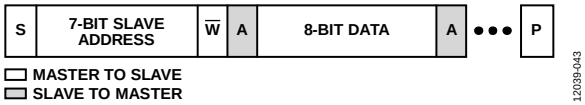


Figure 37. Basic Data Transfer

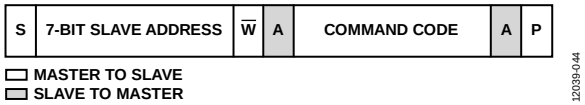


Figure 38. Send Byte Protocol

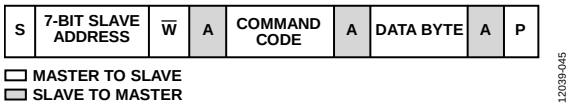


Figure 39. Write Byte Protocol

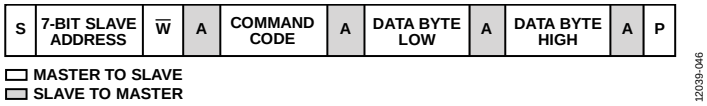


Figure 40. Write Word Protocol

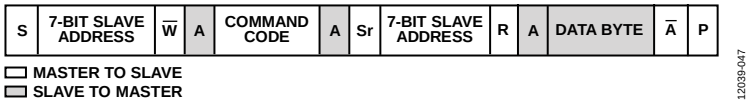


Figure 41. Read Byte Protocol

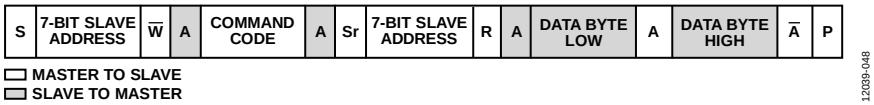


Figure 42. Read Word Protocol

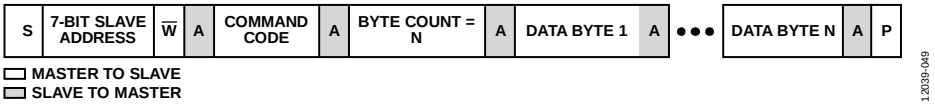


Figure 43. Block Write Protocol

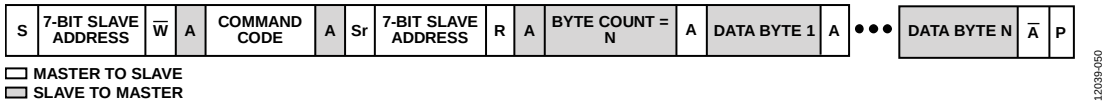


Figure 44. Block Read Protocol

Clock Generation and Stretching

The ADP1050 is always a PMBus slave device in the overall system; therefore, the device never needs to generate the clock, which is done by the master device in the system. However, the PMBus slave device is capable of clock stretching to put the master in a wait state. By stretching the SCL signal during the low period, the slave device communicates to the master device that it is not ready and the master device must wait.

Conditions in which the PMBus slave device stretches the SCL line low include the following:

- The master device is transmitting at a higher baud rate than the slave device.
- The receive buffer of the slave device is full and must be read before continuing. This prevents a data overflow condition.
- The slave device is not ready to send data that the master has requested.

Note that the PMBus slave device can stretch the SCL line only during the low period. Also, whereas the I²C specification allows indefinite stretching of the SCL line, the PMBus specification limits the maximum time that the SCL line can be stretched, or held low, to 25 ms. After this time period, the slave device must release the communication lines and reset its state machine.

Start and Stop Conditions

Start and stop conditions involve serial data transitions when the serial clock is at a logic high level. The PMBus slave device monitors the SDA and SCL lines to detect the start and stop conditions and transitions its internal state machine accordingly. Typical start and stop conditions are shown in Figure 45.

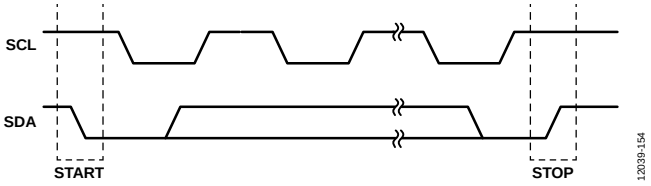


Figure 45. Start and Stop Conditions

GENERAL CALL SUPPORT

The PMBus slave is capable of decoding and acknowledging a general call address. The PMBus slave device responds to both its own address and the general call address (0x00). The general call address enables all devices on the PMBus to be written to simultaneously.

Note that all PMBus commands must start with a slave address, with the R/$\overline{W}$ bit cleared to 0 and followed by the command code. This is also true when using the general call address to communicate with the PMBus slave device.

10-BIT ADDRESSING

The ADP1050 does not support 10-bit addressing as defined in the I²C specification.

FAST MODE

Fast mode, with a data rate of 400 kbps, uses essentially the same mechanics as the standard mode of operation; the electrical specifications and timing are most affected. The PMBus slave is capable of communicating with a master device operating in fast mode or in standard mode, which has a data rate of 100 kbps.

FAULT CONDITIONS

The PMBus protocol provides a comprehensive set of fault conditions that must be monitored and reported. These fault conditions can be grouped into two major categories: communication faults and monitoring faults.

Communication faults are error conditions associated with the data transfer mechanism of the PMBus protocol. Monitoring faults are error conditions associated with the operation of the ADP1050, such as output overvoltage protection. These fault conditions are described in detail in the Power Monitoring, Flags, and Fault Responses section.

TIMEOUT CONDITIONS

The SMBus specification includes three clock stretching specifications related to timeout conditions.

A timeout condition occurs if any single SCL clock pulse is held low for longer than the minimum $t_{TIMEOUT}$ value of 25 ms. Upon detecting the timeout condition, the PMBus slave device has 10 ms to abort the transfer, release the bus lines, and be ready to accept a new start condition. The device that is initiating the timeout must hold the SCL clock line low for at least the maximum $t_{TIMEOUT}$ value of 35 ms, guaranteeing that the slave device is given enough time to reset its communication protocol.

DATA TRANSMISSION FAULTS

Data transmission faults occur when two communicating devices violate the PMBus communication protocol, as specified in the *PMBus Power System Management Protocol Specification* (Revision 1.2, September 6, 2010). See the specification for more details on each fault conditions.

Corrupted Data, Packet Error Checking (PEC)

Packet error checking is not supported by the ADP1050.

Sending Too Few Bits

Transmission is interrupted by a start or stop condition before a complete byte (eight bits) has been sent. This function is not supported; any transmitted data is ignored.

Reading Too Few Bits

Transmission is interrupted by a start or stop condition before a complete byte (eight bits) has been read. This function is not supported; any received data is ignored.

Host Sends or Reads Too Few Bytes

If a host ends a packet with a stop condition before the required bytes are sent/received, it is assumed that the host intended to stop the transfer. Therefore, the PMBus does not consider this to be an error and takes no action, except to flush any remaining bytes in the transmit FIFO.

Host Sends Too Many Bytes

If a host sends more bytes than are expected for the corresponding command, the PMBus slave considers this a data transmission fault and responds as follows:

- Issues a no acknowledge for all unexpected bytes as they are received
- Flushes and ignores the received command and data
- Sets the CML bit in the STATUS_BYTE command register (Register 0x78[1])

Host Reads Too Many Bytes

If a host reads more bytes than are expected for the corresponding command, the PMBus slave considers this a data transmission fault and responds as follows:

- Sends all 1s (0xFF) as long as the host continues to request data
- Sets the CML bit in the STATUS_BYTE command register (Register 0x78[1])

Device Busy

The PMBus slave device is too busy to respond to a request from the master device. This condition is not supported in the ADP1050.

DATA CONTENT FAULTS

Data content faults may occur when the data transmission is successful, but the PMBus slave device cannot process the data that is received from the master device.

Improperly Set Read Bit in the Address Byte

All PMBus commands start with a slave address with the R/$\overline{W}$ bit cleared to 0, followed by the command code. If a host starts a PMBus transaction with R/$\overline{W}$ set in the address phase (equivalent to an I²C read), the PMBus slave considers this a data content fault and responds as follows:

- Acknowledges (ACKs) the address byte
- Issues a no acknowledge for the command and data bytes
- Sends all 1s (0xFF) as long as the host continues to request data
- Sets the CML bit in the STATUS_BYTE command register (Register 0x78[1])

Invalid or Unsupported Command Code

If an invalid or unsupported command code is sent to the PMBus slave, the code is considered to be a data content fault, and the PMBus slave responds as follows:

- Issues a no acknowledge for the illegal/unsupported command byte and data bytes
- Flushes and ignores the received command and data
- Sets the CML bit in the STATUS_BYTE command register (Register 0x78[1])

Reserved Bits

Accesses to reserved bits are not a fault. Writes to reserved bits are ignored, and reads from reserved bits return undefined data.

Write to Read Only Commands

If a host performs a write to a read only command, the PMBus slave considers this a data content fault and responds as follows:

- Issues a no acknowledge for all unexpected data bytes as they are received
- Flushes and ignores the received command and data
- Sets the CML bit in the STATUS_BYTE command register (Register 0x78[1])

Note that this is the same error described in the Host Sends Too Many Bytes section.

Read from Write Only Commands

If a host performs a read from a write only command, the PMBus slave considers this a data content fault and responds as follows:

- Sends all 1s (0xFF) as long as the host continues to request data
- Sets the CML bit in the STATUS_BYTE command register (Register 0x78[1])

Note that this is the same error response that is described in the Host Reads Too Many Bytes section.

EEPROM

The ADP1050 has a built-in EEPROM controller that is used to communicate with the embedded 8000-byte EEPROM. The EEPROM, also called Flash/EE, is partitioned into two major blocks: the information block and the main block. The information block contains 128 8-bit bytes (for internal use only), and the main block contains 8000 8-bit bytes. The main block is further partitioned into 16 pages, with each page containing 512 bytes.

EEPROM FEATURES

The function of the EEPROM controller is to decode the operation that is requested by the ADP1050 and to provide the necessary timing to the EEPROM interface. Data is written to or read from the EEPROM, as requested by the decoded command. Features of the EEPROM controller include

- Separate page erase functions for each page in the EEPROM
- Single byte and multibyte (block) read of the information block with up to 128 bytes at a time
- Single byte and multibyte (block) write and read of the main block with up to 256 bytes at a time
- Automatic upload on startup, from the user settings to the internal registers
- Separate commands to upload and download data, from the factory default or user settings to the internal registers

EEPROM OVERVIEW

The EEPROM controller provides an interface between the ADP1050 core logic and the built-in EEPROM. The user can control data access to and from the EEPROM through this controller interface. Different PMBus commands are available for the read, write, and erase operations to the EEPROM.

Communication is initiated by the master device sending a command to the PMBus slave device to access data from or send data to the EEPROM. Read, write, and erase commands are supported. Data is transferred between devices in a byte wide format. Using a read command, data is received from the EEPROM and transmitted to the master device. Using a write command, data is received from the master device and stored in the EEPROM through the EEPROM controller.

EEPROM PASSWORD

On ADP1050 VDD power-up, the EEPROM is locked and protected from accidental writes or erases. Only reads from Page 2 to Page 15 are allowed when the EEPROM is locked. Before any data can be written (programmed) to the EEPROM, the EEPROM must be unlocked for write access. After it is unlocked, the EEPROM is opened for reading, writing, and erasing.

On power-up, Page 0 and Page 1 are also protected from read access. The EEPROM must first be unlocked to read these pages.

Unlock the EEPROM

To unlock the EEPROM, perform two consecutive writes with the correct password (default = 0xFF), using the EEPROM_PASSWORD command (Register 0xD5). The EEPROM_UNLOCKED flag (Register 0xFEA2[3]) is set to indicate that the EEPROM is unlocked for write access.

Lock the EEPROM

To lock the EEPROM, write any byte other than the correct password, using the EEPROM_PASSWORD command (Register 0xD5). The EEPROM_UNLOCKED flag is cleared to indicate that the EEPROM is locked from write access.

Change the EEPROM Password

To change the EEPROM password, first write the correct password, using the EEPROM_PASSWORD command (Register 0xD5). Immediately write the new password, using the same command. The password is now changed to the new password.

PAGE ERASE OPERATION

The main block consists of 16 equivalent pages of 512 bytes each, numbered Page 0 to Page 15. Page 0 and Page 1 of the main block are reserved for storing the default settings and user settings, respectively. The user cannot perform a page erase operation on Page 0 or Page 1. Page 3 is reserved for storing the power board parameters for the GUI.

Only Page 4 to Page 15 of the main block can be used to store data. To erase any page from Page 4 to Page 15, the EEPROM must first be unlocked for access. For instructions on how to unlock the EEPROM, see the Unlock the EEPROM section.

Each page of the main block, from Page 4 to Page 15, can be individually erased using the EEPROM_PAGE_ERASE command (Register 0xD4). For example, to perform a page erase of Page 10, execute the command shown in Figure 46.

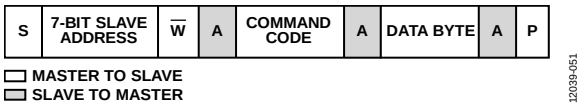


Figure 46. Example Erase Command

In this example, command code = 0xD4 and data byte = 0x0A.

Note that it is important to wait at least 35 ms for the page erase operation to complete before executing the next PMBus command.

The EEPROM allows erasing of whole pages only; therefore, to change the data of any single byte in a page, the entire page must first be erased (set to logic high) for that byte to be writeable. Subsequent writes to any bytes in that page are allowed as long as that byte has not been previously written to a logic low.

READ OPERATION (BYTE READ AND BLOCK READ)

Read from Main Block, Page 0 and Page 1

Page 0 and Page 1 of the main block are reserved for storing the default settings and the user settings, respectively, and are intended to prevent third party access to this data. To read from Page 0 or Page 1, the user must first unlock the EEPROM (see the Unlock the EEPROM section). After the EEPROM is unlocked, Page 0 and Page 1 are readable, using the EEPROM_DATA_xx commands as described in the Read from Main Block, Page 2 to Page 15 section. Note that when the EEPROM is locked, a read from Page 0 and Page 1 returns invalid data.

Read from Main Block, Page 2 to Page 15

Data in Page 2 to Page 15 of the main block is always readable, even with the EEPROM locked. The data in the EEPROM main block can be read one byte at a time or multiple bytes in series, using the EEPROM_DATA_xx commands (Register 0xB0 to Register 0xBF).

Before executing this command, the user must program the number of bytes to read, using the EEPROM_NUM_RD_BYTES command (Register 0xD2). Also, the user can program the offset from the page boundary where the first read byte is returned, using the EEPROM_ADDR_OFFSET command (Register 0xD3).

In the following example, three bytes from Page 4 are read from the EEPROM, starting from the sixth byte of that page.

1. Set number of return bytes = 3.

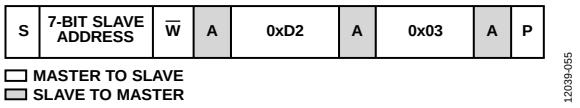


Figure 47. Set Number of Return Bytes = 3

2. Set address offset = 5.

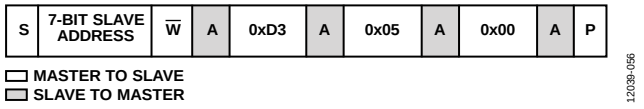


Figure 48. Set Address Offset = 5

3. Read three bytes from Page 4.

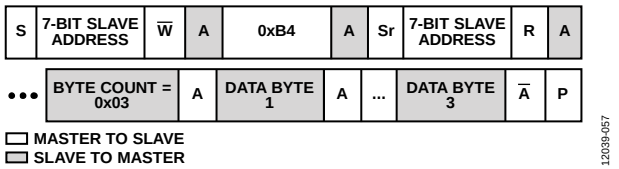


Figure 49. Read Three Bytes from Page 4

Note that the block read command can read a maximum of 256 bytes for any single transaction.

WRITE OPERATION (BYTE WRITE AND BLOCK WRITE)

The user cannot write directly to the information block; this block is used by the ADP1050 to store the first flag information (see the First Flag ID Recording section).

Write to Main Block, Page 0 and Page 1

Page 0 and Page 1 of the main block are reserved for storing the default settings and the user settings, respectively. The user cannot perform a direct write operation to Page 0 or Page 1 using the EEPROM_DATA_xx commands. If the user writes to Page 0, Page 1 returns a no acknowledge. To program the register contents of Page 1 of the main block, it is recommended that the STORE_USER_ALL command be used (Register 0x15). See the Save Register Settings to the User Settings section.

Write to Main Block, Page 2 to Page 15

Before performing a write to Page 2 through Page 15 of the main block, the user must first unlock the EEPROM (see the Unlock the EEPROM section).

Data in Page 2 to Page 15 of the EEPROM main block can be programmed (written to) one byte at a time or multiple bytes in series, using the EEPROM_DATA_xx commands (Register 0xB0 to Register 0xBF). Before executing this command, the user can program the offset from the page boundary where the first byte is written, using the EEPROM_ADDR_OFFSET command (Register 0xD3).

If the targeted page has not yet been erased, the user can erase the page, as described in the EEPROM Password section.

In the following example, four bytes are written to Page 9, starting from the 257th byte of that page.

1. Set address offset = 256.

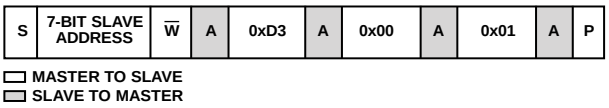


Figure 50. Set Address Offset = 256

2. Write four bytes to Page 9.

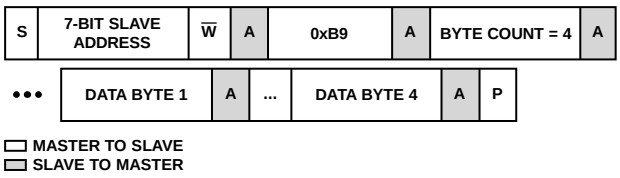


Figure 51. Write Four Bytes to Page 9

Note that the block write command can write a maximum of 256 bytes for any single transaction.

DOWNLOADING EEPROM SETTINGS TO INTERNAL REGISTERS

Download User Settings to Registers

The user settings are stored in Page 1 of the EEPROM main block. These settings are downloaded from the EEPROM into the registers under the following conditions:

- On power-up. The user settings are automatically downloaded into the internal registers, powering up the ADP1050 in a state previously saved by the user.
- On execution of the RESTORE_USER_ALL command (Register 0x16). This command allows the user to force a download of the user settings from Page 1 of the EEPROM main block into the internal registers.

Download Factory Settings to Registers

The factory default settings are stored in Page 0 of the EEPROM main block. The factory settings can be downloaded from the EEPROM into the internal registers, using the RESTORE_DEFAULT_ALL command (Register 0x12).

When this command is executed, the EEPROM password is also reset to the factory default setting of 0xFF.

SAVING REGISTER SETTINGS TO THE EEPROM

The register settings cannot be saved to the factory scratch pad located in Page 0 of the EEPROM main block. This is to prevent the user from accidentally overriding the factory trim settings and the default register settings.

Save Register Settings to the User Settings

The register settings can be saved to the user settings located in Page 1 of the EEPROM main block using the STORE_USER_ALL command (Register 0x15). Before this command can be executed, the EEPROM must first be unlocked for writing (see the Unlock the EEPROM section).

After the register settings are saved to the user settings, any subsequent power cycle automatically downloads the latest stored user information from the EEPROM into the internal registers.

Note that execution of the STORE_USER_ALL command automatically performs a page erase on Page 1 of the EEPROM main block, after which the registers are stored in the EEPROM. Therefore, it is important to wait at least 40 ms for the operation to complete before executing the next PMBus command.

EEPROM CRC CHECKSUM

As a simple method of checking that the values downloaded from the EEPROM and the internal registers are consistent, a CRC checksum is implemented.

- When the data from the internal registers is saved to the EEPROM (Page 1 of the main block), the total number of 1s from all the registers is counted and written into the EEPROM as the last byte of information. This is called the CRC checksum.
- When the data is downloaded from the EEPROM into the internal registers, a similar counter is saved that sums all 1s from the values loaded into the registers. This value is compared with the CRC checksum from the previous upload operation.

If the values match, the download operation was successful. If the values differ, the EEPROM download operation failed, and the CRC_FAULT flag is set (Register 0xFEA2[2]).

To read the EEPROM CRC checksum value, execute the EEPROM_CRC_CHKSUM command (Register 0xD1). This command returns the CRC checksum accumulated in the counter during the download operation.

Note that the CRC checksum is an 8-bit cyclical accumulator that wraps around to 0 when 255 is reached.

GUI SOFTWARE

Free GUI software is available for programming and configuring the ADP1050. The ADP1050 GUI, which is intuitive by design, dramatically reduces power supply design and development time.

The software includes filter design and power supply PWM topology windows. The ADP1050 GUI is also an information center, displaying the status of all readings, monitoring, and flags on the ADP1050.

For more information about the ADP1050 GUI, contact Analog Devices, Inc., for the latest software and a user guide. Evaluation boards are also available by contacting Analog Devices or by visiting http://www.analog.com/digitalpower.

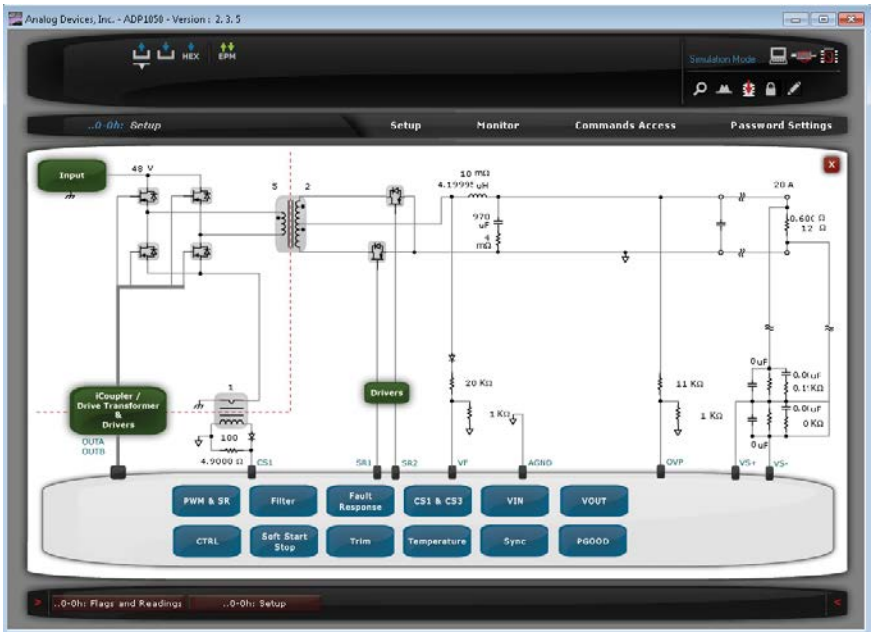


Figure 52. GUI Software

PMBus COMMAND SET

Table 11. PMBus/SMBus Command List Overview

Command Code	Command Name	PMBus/ SMBus Transaction Type	Number of Data Bytes	Default Value[1]	Description
0x01	OPERATION	R/W	1	0x00	Turns the unit on and off in conjunction with the input from the CTRL pin.
0x02	ON_OFF_CONFIG	R/W	1	0x00	The combination of CTRL pin and serial bus commands needed to turn the unit on and off.
0x03	CLEAR_FAULTS	Send byte	0	N/A	Clears all bits in the PMBus status registers simultaneously.
0x10	WRITE_PROTECT	R/W	1	0x00	Protects against accidental writes to the PMBus device. Reads are allowed.
0x12	RESTORE_DEFAULT_ALL	Send byte	0	N/A	Downloads the factory default settings from EEPROM (Page 0) to registers.
0x15	STORE_USER_ALL	Send byte	0	N/A	Saves the user settings from the registers to the EEPROM (Page 1).
0x16	RESTORE_USER_ALL	Send byte	0	N/A	Downloads the user settings from the EEPROM (Page 1) to the registers.
0x19	CAPABILITY	R	1	0x20	Allows the host system to determine the capabilities of the PMBus device.
0x20	VOUT_MODE	R	1	0x16	Sets/reads the formats for the output voltage related commands.
0x21	VOUT_COMMAND	R/W	2	0x0000	Sets the output voltage to the commanded value.
0x22	VOUT_TRIM	R/W	2	0x0000	Applies a fixed offset voltage to the output voltage command value.
0x23	VOUT_CAL_OFFSET	R/W	2	0x0000	Applies a fixed offset voltage to the output voltage command value.
0x24	VOUT_MAX	R/W	2	0x0000	Sets an upper limit on the output voltage.
0x25	VOUT_MARGIN_HIGH	R/W	2	0x0000	Defines the voltage to which the output is set when the OPERATION command is set to margin high.
0x26	VOUT_MARGIN_LOW	R/W	2	0x0000	Defines the voltage to which the output is set when the OPERATION command is set to margin low.
0x27	VOUT_TRANSITION_RATE	R/W	2	0x7BFF	Sets the rate at which the output changes voltage.
0x29	VOUT_SCALE_LOOP	R/W	2	0x0001	The scale factor for setting the output voltage, which is related to the resistor divider.
0x2A	VOUT_SCALE_MONITOR	R/W	2	0x0001	The scale factor for the READ_VOUT command, which typically is the same as the VOUT_SCALE_LOOP command.
0x33	FREQUENCY_SWITCH	R/W	2	0x0031	Sets the switching frequency of the output voltage.
0x35	VIN_ON	R/W	2	0x0000	Sets the input voltage at which the unit starts the power conversion.
0x36	VIN_OFF	R/W	2	0x0000	Sets the input voltage at which the unit stops the power conversion.
0x40	VOUT_OV_FAULT_LIMIT	R/W	2	0x0000	Sets the limit for triggering the VOUT_OV_FAULT flag.
0x41	VOUT_OV_FAULT_RESPONSE	R/W	1	0x00	The fault response for the VOUT_OV_FAULT flag.
0x44	VOUT_UV_FAULT_LIMIT	R/W	2	0x0000	Sets the limit for triggering the VOUT_UV_FAULT flag.
0x45	VOUT_UV_FAULT_RESPONSE	R/W	1	0x00	The fault response for the VOUT_UV_FAULT flag.
0x4F	OT_FAULT_LIMIT	R/W	2	0x0000	Sets the limit for triggering the OT_FAULT flag.
0x50	OT_FAULT_RESPONSE	R/W	1	0x00	The fault response for the OT_FAULT flag.
0x5E	POWER_GOOD_ON	R/W	2	0x0000	Sets the output voltage at which an optional POWER_GOOD signal is asserted.
0x5F	POWER_GOOD_OFF	R/W	2	0x0000	Sets the output voltage at which an optional POWER_GOOD signal is negated.

Command Code	Command Name	PMBus/ SMBus Transaction Type	Number of Data Bytes	Default Value[1]	Description
0x60	TON_DELAY	R/W	2	0x0000	The time from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.
0x61	TON_RISE	R/W	2	0xC00D	The time from when the output begins to rise until the voltage has entered the regulation band.
0x64	TOFF_DELAY	R/W	2	0x0000	The time from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output.
0x78	STATUS_BYTE	R	1	0x00	Returns the low byte of the STATUS_WORD command.
0x79	STATUS_WORD	R	2	0x0000	Returns the low byte and high byte of the STATUS_WORD command.
0x7A	STATUS_VOUT	R	1	0x00	Returns the fault flag for the output voltage.
0x7C	STATUS_INPUT	R	1	0x00	Returns the fault flag for the input voltage and current.
0x7D	STATUS_TEMPERATURE	R	1	0x00	Returns the fault flag for the OT fault and warning.
0x7E	STATUS_CML	R	1	0x00	Returns the fault flag for the communication memory and logic.
0x88	READ_VIN	R	2	0x0000	Returns the input voltage value.
0x89	READ_IIN	R	2	0x0000	Returns the input current value.
0x8B	READ_VOUT	R	2	0x0000	Returns the output voltage value.
0x8D	READ_TEMPERATURE	R	2	0x0000	Returns the temperature reading in degrees Celsius.
0x94	READ_DUTY_CYCLE	R	2	0x0000	Returns the duty cycle of the power converter.
0x95	READ_FREQUENCY	R	2	0x0000	Returns the switching frequency of the power converter.
0x98	READ_PMBUS_REVISION	R	1	0x22	Reads the PMBus revision to which the device is compliant.
0x99	MFR_ID	R/W	1	0x00	Reads/writes the ID of the manufacturer.
0x9A	MFR_MODEL	R/W	1	0x00	Reads/writes the model number of the manufacturer.
0x9B	MFR_REVISION	R/W	1	0x00	Reads/writes revision number of the manufacturer.
0xAD	IC_DEVICE_ID	R	2	0x4151	Reads the IC device ID.
0xAE	IC_DEVICE_REV	R	1	0x20	Reads the IC device revision.
0xB0	EEPROM_DATA_00	R block	Variable	N/A	Block reads from Page 0. The EEPROM must first be unlocked.
0xB1	EEPROM_DATA_01	R block	Variable	N/A	Block reads from Page 1. The EEPROM must first be unlocked.
0xB2	EEPROM_DATA_02	R/W block	Variable	N/A	Blocks reads/writes to Page 2. The EEPROM must first be unlocked for writes.
0xB3	EEPROM_DATA_03	R/W block	Variable	N/A	Blocks reads/writes to Page 3. The EEPROM must first be unlocked for writes.
0xB4	EEPROM_DATA_04	R/W block	Variable	N/A	Blocks reads/writes to Page 4. The EEPROM must first be unlocked for writes.
0xB5	EEPROM_DATA_05	R/W block	Variable	N/A	Blocks reads/writes to Page 5. The EEPROM must first be unlocked for writes.
0xB6	EEPROM_DATA_06	R/W block	Variable	N/A	Blocks reads/writes to Page 6. The EEPROM must first be unlocked for writes.
0xB7	EEPROM_DATA_07	R/W block	Variable	N/A	Blocks reads/writes to Page 7. The EEPROM must first be unlocked for writes.
0xB8	EEPROM_DATA_08	R/W block	Variable	N/A	Blocks reads/writes to Page 8. The EEPROM must first be unlocked for writes.
0xB9	EEPROM_DATA_09	R/W block	Variable	N/A	Blocks reads/writes to Page 9. The EEPROM must first be unlocked for writes.

Command Code	Command Name	PMBus/ SMBus Transaction Type	Number of Data Bytes	Default Value[1]	Description
0xBA	EEPROM_DATA_10	R/W block	Variable	N/A	Blocks reads/writes to Page 10. The EEPROM must first be unlocked for writes.
0xBB	EEPROM_DATA_11	R/W block	Variable	N/A	Blocks reads/writes to Page 11. The EEPROM must first be unlocked for writes.
0xBC	EEPROM_DATA_12	R/W block	Variable	N/A	Blocks reads/writes to Page 12. The EEPROM must first be unlocked for writes.
0xBD	EEPROM_DATA_13	R/W block	Variable	N/A	Blocks reads/writes to Page 13. The EEPROM must first be unlocked for writes.
0xBE	EEPROM_DATA_14	R/W block	Variable	N/A	Blocks reads/writes to Page 14. The EEPROM must first be unlocked for writes.
0xBF	EEPROM_DATA_15	R/W block	Variable	N/A	Blocks reads/writes to Page 15. The EEPROM must first be unlocked for writes.
0xD1	EEPROM_CRC_CHKSUM	R	1	N/A	Returns the CRC checksum value from the EEPROM download operation.
0xD2	EEPROM_NUM_RD_BYTES	R/W	1	N/A	Sets the number of return read bytes when using the EEPROM_DATA_xx commands.
0xD3	EEPROM_ADDR_OFFSET	R/W	2	N/A	Sets the address offset of the current EEPROM page.
0xD4	EEPROM_PAGE_ERASE	W	1	N/A	Performs a page erase on a selected page (Page 3 to Page 15). Wait at least 35 ms for each page erase operation. The EEPROM must first be unlocked. A page erase of Page 0 and Page 1 is not allowed.
0xD5	EEPROM_PASSWORD	W	1	0xFF	Writes the password to this register to unlock the EEPROM, and/or changes the EEPROM password.
0xD6	TRIM_PASSWORD	W	1	0xFF	Writes the password to this register to unlock the trim registers for write access.
0xD7	CHIP_PASSWORD	W	2	0xFFFF	Writes the password to this register to unlock the chip password for register access.
0xD8	VIN_SCALE_MONITOR	R/W	2	0x0001	The scale factor for the input voltage reading (READ_VIN).
0xD9	IIN_SCALE_MONITOR	R/W	2	0x0001	The scale factor for the input current reading (READ_IIN).
0xF1	EEPROM_INFO	Read block	Variable	N/A	Reads the first fault information.
0xFA	MFR_SPECIFIC_1	R/W	1	0x00	Stores the user customized information.
0xFB	MFR_SPECIFIC_2	R/W	1	0x00	Stores the user customized information.

[1] N/A = Not applicable.

MANUFACTURER SPECIFIC EXTENDED COMMAND LIST

Table 12. Manufacturer Specific Extended Command List Overview

Address	Register Function
Flag Configuration Registers	
0xFE00	IIN_OC_FAST_FAULT_RESPONSE
0xFE01	CS3_OC_FAULT_RESPONSE, extended VOUT_OV_FAULT_RESPONSE
0xFE02	VIN_UV_FAULT_RESPONSE
0xFE03	FLAGIN_RESPONSE
0xFE05	Flag reenable delay, VDD_OV_RESPONSE
Soft Start Software Reset Setting Registers	
0xFE06	Software reset go command
0xFE07	Software reset settings
0xFE08	Synchronous rectifier (SR) soft start settings
0xFE09	Soft start setting of open-loop operation
Blanking and $\overline{\text{PGOOD}}$ Setting Registers	
0xFE0B	Flag blanking during soft start
0xFE0C	Volt-second balance blanking and SR disable during soft start
0xFE0D	$\overline{\text{PGOOD}}$ mask settings
0xFE0E	$\overline{\text{PGOOD}}$ flag debounce
0xFE0F	Debounce time for asserting $\overline{\text{PGOOD}}$
Switching Frequency and Synchronization Setting Registers	
0xFE11	Synchronization delay time
0xFE12	Synchronization general settings
0xFE13	Dual-ended topology mode
Current Sense and Limit Setting Registers	
0xFE14	CS1 gain trim
0xFE19	CS3 OC debounce
0xFE1A	IIN_OC_FAST_FAULT_LIMIT
0xFE1B	CS1 cycle-by-cycle current limit reference
0xFE1D	Matched cycle-by-cycle current-limit settings
0xFE1E	SR1 and SR2 response to cycle-by-cycle current limit
0xFE1F	CS1 cycle-by-cycle current-limit settings
Voltage Sense and Limit Setting Registers	
0xFE20	VS gain trim
0xFE25	Prebias start-up enable
0xFE26	VOUT_OV_FAULT flag debounce
0xFE28	VF gain trim
0xFE29	VIN_ON and VIN_OFF delay
Temperature Sense and Protection Setting Registers	
0xFE2A	RTD gain trim
0xFE2B	RTD offset trim (MSBs)
0xFE2C	RTD offset trim (LSBs)
0xFE2D	RTD current source settings
0xFE2F	OT hysteresis settings
Digital Compensator and Modulation Setting Registers	
0xFE30	Normal mode compensator low frequency gain settings
0xFE31	Normal mode compensator zero settings
0xFE32	Normal mode compensator pole settings
0xFE33	Normal mode compensator high frequency gain settings
0xFE38	CS1 threshold for volt-second balance
0xFE39	Nominal modulation value for prebias startup
0xFE3A	SR driver delay
0xFE3B	PWM 180° phase shift settings
0xFE3C	Modulation limit
0xFE3D	Feedforward and soft start filter gain

Address	Register Function
PWM Outputs Timing Registers	
0xFE3E	OUTA rising edge timing
0xFE3F	OUTA falling edge timing
0xFE40	OUTA rising and falling edges timing (LSBs)
0xFE41	OUTB rising edge timing
0xFE42	OUTB falling edge timing
0xFE43	OUTB rising and falling edges timing (LSBs)
0xFE4A	SR1 rising edge timing
0xFE4B	SR1 falling edge timing
0xFE4C	SR1 rising and falling edges timing (LSBs)
0xFE4D	SR2 rising edge timing
0xFE4E	SR2 falling edge timing
0xFE4F	SR2 rising and falling edges timing (LSBs)
0xFE50	OUTA and OUTB modulation settings
0xFE52	SR1 and SR2 modulation settings
0xFE53	PWM output disable
Volt-Second Balance Control Registers	
0xFE54	Volt-second balance control general settings
0xFE55	Volt-second balance control on OUTA and OUTB
0xFE57	Volt-second balance control on SR1 and SR2
Duty Cycle Reading Setting Registers	
0xFE58	Duty cycle reading settings
0xFE59	Input voltage compensation multiplier
Other Setting Registers	
0xFE61	Go commands
0xFE62	Customized register
0xFE63	Modulation reference MSBs setting for open-loop input voltage feedforward operation
0xFE64	Modulation reference LSBs setting for open-loop input voltage feedforward operation
0xFE65	Current value update rate setting
0xFE67	Open-loop operation settings
0xFE69	Pulse skipping mode threshold
0xFE6A	CS3_OC_FAULT_LIMIT
0xFE6B	Modulation threshold for OVP selection
0xFE6C	Modulation flag for OVP selection
0xFE6D	OUTA and OUTB adjustment reference during synchronization
0xFE6F	SR1 and SR2 adjustment reference during synchronization
Manufacturer Specific Fault Flag Registers	
0xFEA0	Flag Register 1
0xFEA1	Flag Register 2
0xFEA2	Flag Register 3
0xFEA3	Latched Flag Register 1
0xFEA4	Latched Flag Register 2
0xFEA5	Latched Flag Register 3
0xFEA6	First flag ID
Manufacturer Specific Value Reading Registers	
0xFEA7	CS1 value
0xFEA9	CS3 value
0xFEAA	VS± value
0xFEAB	RTD value
0xFEAC	VF value
0xFEAD	Duty cycle value
0xFEAE	Input power value

PMBus COMMAND DESCRIPTIONS

BASIC PMBus COMMANDS

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the CTRL pin. It is also used to set the output voltage to the upper or lower voltage margin. The unit stays in the commanded operating mode until a subsequent OPERATION command instructs the device to change to another mode.

Table 13. Register 0x01—OPERATION

Bits	Bit Name/Function	R/W	Description		
[7:6]	Enable	R/W	These bits determine the response to the OPERATION command.		
			Bit 7	**Bit 6**	**Description**
			0	0	Immediate off (no sequencing)
			0	1	Soft off (power-down based on the programmed TOFF_DELAY command)
			1	0	Unit on
			1	1	Reserved
[5:4]	Margin control	R/W	These bits set the voltage margin level.		
			Bit 5	**Bit 4**	**Description**
			0	0	Off
			0	1	Margin low
			1	0	Margin high
			1	1	Reserved
[3:0]	Reserved	R	Reserved.		

ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of CTRL pin input and serial bus commands needed to turn the unit on and off, including how the unit responds when power is applied.

Table 14. Register 0x02—ON_OFF_CONFIG

Bits	Bit Name/Function	R/W	Description
[7:5]	Reserved	R	Reserved.
4	Power-up control	R/W	Controls how the device responds to the OPERATION command. 0 = the unit powers up whenever power is present. 1 = the unit powers up only when commanded by the CTRL pin and the OPERATION command (as programmed in Register 0x02, Bits[3:0]).
3	Command enable	R/W	Controls how the device responds to the OPERATION command. 0 = ignores the OPERATION command. 1 = requires that the OPERATION command be set to the on state to enable the unit (in addition to the setting of Bit 2).
2	Pin enable	R/W	Controls how the device responds to the value on the CTRL pin. 0 = ignores the CTRL pin. 1 = requires the CTRL pin to be asserted to enable the unit (in addition to the setting of Bit 3).
1	CTRL pin polarity	R/W	Sets the polarity for the CTRL pin. 0 = active low. 1 = active high.
0	Power-down delay setting	R/W	Action to take at power-down. 0 = uses the TOFF_DELAY value (TOFF_FALL is not supported by the ADP1050) to stop the transfer of energy to the output. 1 = turns off the output and stops energy transfer to the output as fast as possible.

CLEAR_FAULTS

The CLEAR_FAULTS command is a send byte, no data. This command clears all PMBus fault bits in all PMBus status registers simultaneously.

Table 15. Register 0x03—CLEAR_FAULTS

Bits	Bit Name/Function	Type	Description
N/A	CLEAR_FAULTS	Send	Clears all bits in PMBus status registers (Register 0x78 to Register 0x7E) simultaneously.

WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the PMBus device. This command provides protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the configuration or operation of the device.

Table 16. Register 0x10—WRITE_PROTECT

Bits	Bit Name/Function	R/W	Description
7	Write Protect 1	R/W	Disables writes to all commands except the WRITE_PROTECT command.
6	Write Protect 2	R/W	Disables writes to all commands except the WRITE_PROTECT and OPERATION commands.
5	Write Protect 3	R/W	Disables writes to all commands except the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND commands.
[4:0]	Reserved	R	Reserved.

RESTORE_DEFAULT_ALL

The RESTORE_DEFAULT_ALL command is a send byte, no data. This command downloads the factory default settings (including the basic PMBus commands, the manufacturer specific extended commands (starting with 0xFE), and other data such as the checksum, the EEPROM password, and the chip password) from the EEPROM (Page 0 of the main block) into the registers.

Table 17. Register 0x12—RESTORE_DEFAULT_ALL

Bits	Bit Name/Function	Type	Description
N/A	RESTORE_DEFAULT_ALL	Send	Restores the factory default settings from the EEPROM to the registers.

STORE_USER_ALL

The STORE_USER_ALL command is a send byte, no data. This command copies the entire contents of the registers into the EEPROM (Page 1 of the main block) as the user settings. The settings are automatically restored on power-up of VDD.

Table 18. Register 0x15—STORE_USER_ALL

Bits	Bit Name/Function	Type	Description
N/A	STORE_USER_ALL	Send	Saves the user settings from the registers to the EEPROM.

RESTORE_USER_ALL

The RESTORE_USER_ALL command is a send byte, no data. This command downloads the stored user settings including the basic PMBus commands, the manufacturer specific extended commands (starting with 0xFE), and other data (for example, the checksum, the EEPROM password, and the chip password) from the EEPROM (Page 1 of the main block) into the registers.

Table 19. Register 0x16—RESTORE_USER_ALL

Bits	Bit Name/Function	Type	Description
N/A	RESTORE_USER_ALL	Send	Restores the user settings from the EEPROM to the registers.

CAPABILITY

This command summarizes the PMBus optional communication protocols supported by the ADP1050. The reading of this command should result in 0x20.

Table 20. Register 0x19—CAPABILITY

Bits	Bit Name/Function	R/W	Description
[7]	Packet error	R	Checks the packet error capability of the device. 0 = not supported.
[6:5]	Maximum bus speed	R	Checks the PMBus speed capability of the device. 01 = maximum bus speed of 400 kHz.
4	$\overline{\text{SMBALERT}}$	R	Checks support of the $\overline{\text{SMBALERT}}$ pin and the SMBus alert response protocol. 0 = not supported.
[3:0]	Reserved	R	Reserved.

VOUT_MODE

The VOUT_MODE command sets the data format for output voltage related data. The data byte for the VOUT_MODE command consists of a 3-bit mode and 5-bit exponent parameter. The 3-bit mode determines whether the device uses linear format or direct format for the output voltage related commands. The 5-bit parameter sets the exponent value for linear format.

Table 21. Register 0x20—VOUT_MODE

Bits	Bit Name/Function	R/W	Description
[7:5]	Mode	R	Output voltage data format. The value is fixed at 000, meaning that only linear format is supported.
[4:0]	Exponent	R	The N value for the output voltage related commands in linear format: $V = Y \times 2^N$. The value is fixed at 10110 (twos complement, −10 decimal). The exponent for linear format values is −10.

VOUT_COMMAND

The VOUT_COMMAND command sets the output voltage. The VOUT_TRANSITION_RATE command is used if this command is modified while the output is active and in a steady state condition. The maximum programmable output voltage is 64 V.

Table 22. Register 0x21—VOUT_COMMAND

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R/W	Sets the output voltage reference value, in volts. 16-bit unsigned integer Y value for linear format: $V = Y \times 2^N$. N is defined in the VOUT_MODE command.

VOUT_TRIM

The VOUT_TRIM command applies a fixed offset voltage to the output voltage command value. It is typically set by the user to trim the output voltage at the time that the PMBus device is assembled into the system of the user. The trim range is −32 V to +32 V, and each LSB resolution is 2^{-10} = 0.9765625 mV.

Table 23. Register 0x22—VOUT_TRIM

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R/W	Sets the output voltage trim value. 16-bit twos complement Y value for linear format: $V = Y \times 2^N$. N is defined in the VOUT_MODE command.

VOUT_CAL_OFFSET

The VOUT_CAL_OFFSET command is used to apply a fixed offset voltage to the output voltage command value. It is typically used by the PMBus device manufacturer to calibrate the device in the factory. The trim range is −32 V to +32 V and each LSB size is 2^{-10} = 0.9765625 mV.

Table 24. Register 0x23—VOUT_CAL_OFFSET

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R/W	Sets the output voltage trim value. 16-bit twos complement Y value for linear format: $V = Y \times 2^N$. N is defined in the VOUT_MODE command.

VOUT_MAX

The VOUT_MAX command sets an upper limit on the output voltage the unit can attain, regardless of any other commands or combinations. If an attempt is made to program the output voltage higher than the limit set by this command, the device responds as follows:

- The commanded output voltage is set to the VOUT_MAX value.
- The NONE OF THE ABOVE bit is set in the STATUS_BYTE command (Register 0x78[0]).
- The VOUT bit is set in the STATUS_WORD command (Register 0x79[15]).
- The VOUT_MAX warning bit is set in the STATUS_VOUT command (Register 0x7A[3]).

Table 25. Register 0x24—VOUT_MAX

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R/W	Sets the output voltage upper limit. 16-bit unsigned integer Y value for linear format: $V = Y \times 2^N$. N is defined in the VOUT_MODE command.

VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command sets the target voltage to which the output changes when the OPERATION command is set to margin high. The VOUT_TRANSITION_RATE command is used if this command is modified while the output is active and in a steady state condition.

Table 26. Register 0x25—VOUT_MARGIN_HIGH

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R/W	Sets the margin high value for the output voltage, in volts. 16-bit unsigned integer Y value for linear format: $V = Y \times 2^N$. N is defined by the VOUT_MODE command.

VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command sets the target voltage, to which the output changes when the OPERATION command is set to margin low. The VOUT_TRANSITION_RATE command is used if this command is modified while the output is active and in a steady-state condition.

Table 27. Register 0x26—VOUT_MARGIN_LOW

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R/W	Sets the margin low value for the output voltage, in volts. 16-bit unsigned integer Y value for linear format: $V = Y \times 2^N$. N is defined by the VOUT_MODE command.

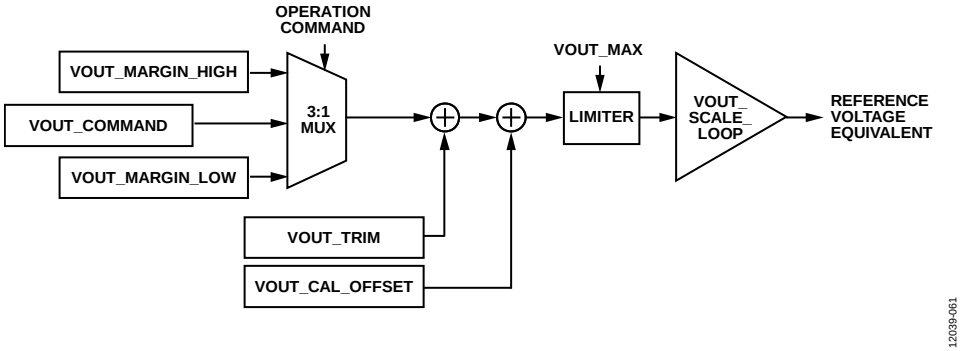


Figure 53. Conceptual View of the Output Voltage Related Commands

VOUT_TRANSITION_RATE

When the ADP1050 receives either a VOUT_COMMAND command or an OPERATION command (margin high, margin low) that causes the output voltage to change, this command sets the rate, in mV/µs, at which the VS± pins change voltage. This commanded rate of change does not apply when the unit is turned on or off. The maximum positive value (0x7BFF) of the two data bytes indicates that the unit makes the transition as quickly as possible. Only the limited options in Table 28 are supported by the ADP1050.

Table 28. Register 0x27—VOUT_TRANSITION_RATE (Rate-of-Change Options Supported by the ADP1050)

Register Setting	Rate of Change (mV/µs)
1001100000001101 (0x980D)	0.0015625
1010000000001101 (0xA00D)	0.003125
1010100000001101 (0xA80D)	0.00625
1011000000001101 (0xB00D)	0.0125
1011100000001101 (0xB80D)	0.025
1100000000001101 (0xC00D)	0.050
1100100000001101 (0xC80D)	0.1
1101000000001101 (0xD00D)	0.2
0111101111111111 (0x7BFF)	Infinite (default)

Table 29. Register 0x27—VOUT_TRANSITION_RATE

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $X = Y \times 2^N$.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

VOUT_SCALE_LOOP

The VOUT_SCALE_LOOP command is equal to the feedback resistor ratio. The nominal output voltage is set by a resistor divider and the internal 1 V reference voltage. For example, if the nominal output voltage is 12 V, the VOUT_SCALE_LOOP value = 1 V/12 V = 0.08333 and the VOUT_SCALE_LOOP can be set as 0xA155.

Table 30. Register 0x29—VOUT_SCALE_LOOP

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $K_R = Y \times 2^N$. N must be in the range of −12 to 0 decimal.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $K_R = Y \times 2^N$.

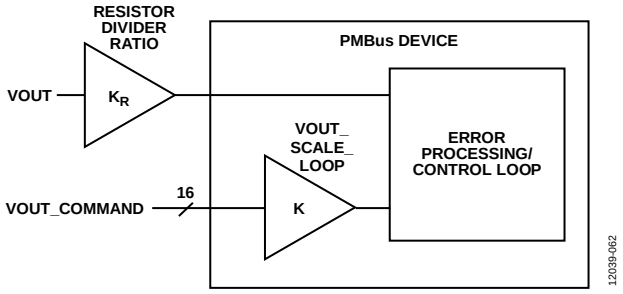


Figure 54. Conceptual View of the VOUT_SCALE_LOOP Command

VOUT_SCALE_MONITOR

This command is typically the same as the VOUT_SCALE_LOOP command. It is used for reading the output voltage with the READ_VOUT command (Register 0x8B).

Table 31. Register 0x2A—VOUT_SCALE_MONITOR

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $K_R = Y \times 2^N$. N must be in the range of −12 to 0 decimal.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $K_R = Y \times 2^N$.

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command, which sets the switching frequency in kHz, is in linear format. Only the limited switching frequency options in Table 32 are supported by the ADP1050. In the ADP1050, because the switching frequency is calculated from the switching period, the switching period value that is used is an accurate measure, whereas the switching frequency may not be. For example, for the first switching frequency option of 49 kHz (see Table 32), the actual switching frequency is calculated by 1/(20.48 µs) = 48.828125 kHz, which is simplified (rounded) to 49 kHz.

To avoid an incorrect switching frequency setting, the go commands in Register 0xFE61[2:1] must be used to latch this setting and the PWM setting.

Table 32. Register 0x33—FREQUENCY_SWITCH (Options Supported by the ADP1050)

Register Setting	Switching Frequency (kHz)	Accurate Switching Period (µs)
0000000000110001 (0x0031)	49	20.48
0000000000111000 (0x0038)	56	17.92
0000000000111100 (0x003C)	60	16.64
0000000001000001 (0x0041)	65	15.36
0000000001000111 (0x0047)	71	14.08
0000000001001110 (0x004E)	78	12.80
0000000001010111 (0x0057)	87	11.52
1111100011000011 (0xF8C3)	97.5	10.24
0000000001101000 (0x0068)	104	9.60
1111100011011111 (0xF8DF)	111.5	8.96
0000000001111000 (0x0078)	120	8.32
0000000010000010 (0x0082)	130	7.68
0000000010001000 (0x0088)	136	7.36
0000000010001110 (0x008E)	142	7.04
0000000010010101 (0x0095)	149	6.72
1111100100111001 (0xF939)	156.5	6.40
1111100101001001 (0xF949)	164.5	6.08
1111100101011011 (0xF95B)	173.5	5.76
0000000010111000 (0x00B8)	184	5.44
1111100110000111 (0xF987)	195.5	5.12
1111100110010011 (0xF993)	201.5	4.96
1111100110100001 (0xF9A1)	208.5	4.80
1111100110101111 (0xF9AF)	215.5	4.64
0000000011011111 (0xDF)	223	4.48
1111100111001111 (0xF9CF)	231.5	4.32
1111100111100001 (0xF9E1)	240.5	4.16
0000000011111010 (0x00FA)	250	4.00
1111101000001001 (0xFA09)	260.5	3.84
1111101000011111 (0xFA1F)	271.5	3.68
0000000100011100 (0x011C)	284	3.52
1111101001010011 (0xFA53)	297.5	3.36
1111101001110001 (0xFA71)	312.5	3.20
1111101010000001 (0xFA81)	320.5	3.12
0000000101001001 (0x0149)	329	3.04
0000000101010010 (0x0152)	338	2.96
0000000101011011 (0x15B)	347	2.88
0000000101100101 (0x0165)	357	2.80
1111101011011111 (0xFADF)	367.5	2.72
0000000101111011 (0x017B)	379	2.64
1111101100001101 (0xFB0D)	390.5	2.56
0000000110001101 (0x018D)	397	2.52
0000000110010011 (0x0193)	403	2.48
0000000110011010 (0x019A)	410	2.44

Register Setting	Switching Frequency (kHz)	Accurate Switching Period (µs)
1111101101000001 (0xFB41)	416.5	2.40
1111101101001111 (0xFB4F)	423.5	2.36
0000000110101111 (0x1AF)	431	2.32
1111101101101101 (0xFB6D)	438.5	2.28
1111101101111101 (0xFB7D)	446.5	2.24
1111101110001101 (0xFB8D)	454.5	2.20
0000000111001111 (0x01CF)	463	2.16
0000000111011000 (0x01D8)	472	2.12
0000000111100001 (0x01E1)	481	2.08
0000000111101010 (0x1EA)	490	2.04
0000000111110100 (0x1F4)	500	2.00
0000000111111110 (0x01FE)	510	1.96
0000001000001000 (0x0208)	520	1.92
0000001000010011 (0x0213)	531	1.88
0000001000011111 (0x0x21F)	543	1.84
0000001000101100 (0x022C)	556	1.80
0000001000111000 (0x0238)	568	1.76
0000001001000101 (0x0245)	581	1.72
0000001001010011 (0x0253)	595	1.68
0000001001100010 (0x0262)	610	1.64
0000001001110001 (0x0271)	625	1.60

Table 33. Register 0x33—FREQUENCY_SWITCH

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $X = Y \times 2^N$.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

VIN_ON

The VIN_ON command sets the value of the input voltage (in volts) at which the unit starts power conversion.

Table 34. Register 0x35—VIN_ON

Bit	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $X = Y \times 2^N$. N must be in the range of −12 to 0 decimal.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

VIN_OFF

The VIN_OFF command sets the value of the input voltage (in volts) at which the unit stops power conversion after operation has started.

Table 35. Register 0x36—VIN_OFF

Bit	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $X = Y \times 2^N$. N must be in the range of −12 to 0 decimal.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT command sets the threshold value for overvoltage protection of the output voltage.

Table 36. Register 0x40—VOUT_OV_FAULT_LIMIT

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R/W	16-bit unsigned integer Y value for linear mode format: $X = Y \times 2^N$. N is defined by the VOUT_MODE command. Note that the available OV protection limit value must be in the range of 75% to 150% of the nominal output voltage.

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command determines the fault response for the VOUT_OV_FAULT flag.

Table 37. Register 0x41—VOUT_OV_FAULT_RESPONSE

Bits	Bit Name/Function	R/W	Description			
[7:6]	Response	R/W	00 = continues operation without interruption. 01 = continues operation for the debounce time (Delay Time 1) specified by Register 0xFE26[7:6]. If the fault persists, retry the number of times specified by the retry setting of this command (Bits[5:3]). 10 = shuts down and responds according to the retry setting in Bits[5:3]. 11 = the output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.			
[5:3]	Retry setting	R/W	000 = restart not attempted. The output remains disabled until the fault is cleared. 001 to 110 = attempts to restart the number of times set by these bits. If the ADP1050 fails to restart in the allowed number of retries, the output is disabled and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the Delay Time 2 value in Bits[2:0], along with the delay time unit specified for that particular fault. 111 = attempts to restart continuously, without limitation, until it is commanded off (by the CTRL pin or the OPERATION command, or both), V_{DD} is removed, or another fault condition causes the unit to shut down.			
[2:0]	Delay time	R/W	These bits set the delay time between the start of each attempt to restart.			
			Bit 2	**Bit 1**	**Bit 0**	**Delay Time 2 (ms)**
			0	0	0	252
			0	0	1	588
			0	1	0	924
			0	1	1	1260
			1	0	0	1596
			1	0	1	1932
			1	1	0	2268
			1	1	1	2604

VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT command sets the threshold value for undervoltage protection of the output voltage.

Table 38. Register 0x44—VOUT_UV_FAULT_LIMIT

Bits	Bit Name/Function	R/W	Bit Name/Function
[15:0]	Mantissa	R/W	16-bit unsigned integer Y value for linear format: $X = Y \times 2^N$. N is defined by the VOUT_MODE command.

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command determines the fault response for the VOUT_UV_FAULT flag.

Table 39. Register 0x45—VOUT_UV_FAULT_RESPONSE

Bits	Bit Name/Function	R/W	Description
[7:6]	Response	R/W	00 = continues operation without interruption. 01 = continues operation for the Delay Time 1 (Bits[2:0]). If the fault persists, retry the number of times specified by the retry setting (Bits[5:3]). 10 = shuts down (disables the output) and responds according to the retry setting in Bits[5:3]. 11 = the output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
[5:3]	Retry setting	R/W	000 = restart not attempted. The output remains disabled until the fault is cleared. 001 to 110 = attempts to restart the number of times set by these bits. If the unit fails to restart in the allowed number of retries, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the Delay Time 2 value in Bits[2:0], together with the delay time unit specified for that particular fault. 111 = attempts to restart continuously, without limitation, until it is commanded off (by the CTRL pin or the OPERATION command, or both), V_{DD} is removed, or another fault condition causes the unit to shut down.
[2:0]	Delay time	R/W	These bits set the delay time for the VOUT_UV_FAULT_RESPONSE Delay Time 1 and Delay Time 2 as described in Bits[7:6] and Bits[5:3].

Bit 2	Bit 1	Bit 0	Delay Time 1 (ms)	Delay Time 2 (ms)
0	0	0	0	252
0	0	1	20	588
0	1	0	40	924
0	1	1	80	1260
1	0	0	160	1596
1	0	1	320	1932
1	1	0	640	2268
1	1	1	1280	2604

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the threshold value in degrees Celsius (°C) for overtemperature protection. The range is 0°C to 156°C. If the setting value is out of range, the limit is 156 and the return value is 156.

Table 40. Register 0x4F—OT_FAULT_LIMIT

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R	5-bit twos complement N value for linear format: $X = Y \times 2^N$. N is fixed at 0.
[10:8]	Mantissa high bits	R	Mantissa high bits Y[10:8] value fixed at 0.
[7:0]	Mantissa low bits	R/W	Mantissa low bits Y[7:0] value for linear format: $X = Y \times 2^N$.

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command determines the fault response for the OT_FAULT flag.

Table 41. Register 0x50—OT_FAULT_RESPONSE

Bits	Bit Name/Function	R/W	Description
[7:6]	Response	R/W	00 = continues operation without interruption. 01 = continues operation for the Delay Time 1 specified by Bits[2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the retry setting (Bits[5:3]). 10 = shuts down (disables the output) and responds according to the retry setting in Bits[5:3]. 11 = the output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
[5:3]	Retry setting	R/W	000 = restart not attempted. The output remains disabled until the fault is cleared. 001 to 110 = attempts to restart the number of times set by these bits. If the device fails to restart in the allowed number of retries, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the Delay Time 2 value in Bits[2:0], together with the delay time unit specified for that particular fault. 111 = attempts to restart continuously, without limitation, until commanded off (by the CTRL pin or the OPERATION command, or both), V_{DD} is removed, or another fault condition causes the unit to shut down.
[2:0]	Delay time	R/W	These bits set the delay time.

Bit 2	Bit 1	Bit 0	Delay Time 1 (sec)	Delay Time 2 (ms)
0	0	0	1	252
0	0	1	1	588
0	1	0	1	924
0	1	1	1	1260
1	0	0	1	1596
1	0	1	1	1932
1	1	0	1	2268
1	1	1	1	2604

POWER_GOOD_ON

The POWER_GOOD_ON command sets the output voltage (in volts) at which the POWER_GOOD signal is asserted. The POWER_GOOD status bit ($\overline{\text{POWER\_GOOD}}$) in the STATUS_WORD command is always reflective of V_{OUT} with regard to the POWER_GOOD_ON and POWER_GOOD_OFF limits.

Table 42. Register 0x5E—POWER_GOOD_ON

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R/W	Sets the output voltage for the POWER_GOOD_ON command. 16-bit unsigned integer Y value for linear format $X = Y \times 2^N$. N is defined by the VOUT_MODE command.

POWER_GOOD_OFF

The POWER_GOOD_OFF command sets the output voltage (in volts) at which the POWER_GOOD signal is negated. The POWER_GOOD status bit ($\overline{\text{POWER\_GOOD}}$) in the STATUS_WORD command is always reflective of V_{OUT} with regard to the POWER_GOOD_ON and POWER_GOOD_OFF limits.

Table 43. Register 0x5F—POWER_GOOD_OFF

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R/W	Sets the output voltage for the POWER_GOOD_OFF command. 16-bit unsigned integer Y value for linear format $X = Y \times 2^N$. N is defined by the VOUT_MODE command.

TON_DELAY

The TON_DELAY command sets the turn-on delay time in milliseconds (ms). Only the options in Table 44 are supported in the ADP1050.

Table 44. Register 0x60—TON_DELAY (Turn-On Delay Options Supported in the ADP1050)

Register Setting	Turn-On Delay Time (ms)
0000000000000000 (0x0000)	0
0000000000001010 (0x000A)	10
0000000000011001 (0x0019)	25
0000000000110010 (0x0032)	50
0000000001001011 (0x004B)	75
0000000001100100 (0x0064)	100
0000000011111010 (0x00FA)	250
0000001111101000 (0x03E8)	1000

Table 45. Register 0x60—TON_DELAY

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $X = Y \times 2^N$.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

TON_RISE

The TON_RISE command sets the turn-on rise time in milliseconds (ms). Only the values in Table 46 are supported in the ADP1050.

Table 46. Register 0x61—TON_RISE (Turn-On Rise Time Options Supported in the ADP1050)

Register Setting	Turn-On Rise Time (ms)
1100000000001101 (0xC00D)	0.05
1101000000001101 (0xD00D)	0.2
1111000000000111 (0xF007)	1.75
1111100000010101 (0xF815)	10.5
0000000000010101 (0x0015)	21
1111000010100001 (0xF0A1)	40.25
0000000000111100 (0x003C)	60
0000000001100100 (0x0064)	100

Table 47. Register 0x61—TON_RISE

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $X = Y \times 2^N$.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

TOFF_DELAY

The TOFF_DELAY command sets the turn-off delay time in milliseconds (ms). Only the values listed in Table 48 are supported in the ADP1050.

Table 48. Register 0x64—TOFF_DELAY (Turn-Off Delay Options Supported in the ADP1050)

Register Setting	Turn-Off Delay Time (ms)
0000000000000000 (0x0000)	0
0000000000110010 (0x0032)	50
0000000011111010 (0x00FA)	250
0000001111101000 (0x03E8)	1000

Table 49. Register 0x64—TOFF_DELAY

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $X = Y \times 2^N$.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

STATUS_BYTE

Table 50. Register 0x78—STATUS_BYTE

Bits	Bit Name/Function	R/W	Description
7	Reserved	R	Reserved.
6	POWER_OFF	R	This bit is asserted if the device is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	R	An output overvoltage fault has occurred.
4	Reserved	R	Reserved.
3	VIN_UV_FAULT	R	An input undervoltage fault has occurred.
2	TEMPERATURE	R	A temperature fault or warning has occurred.
1	CML	R	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	R	A fault or warning not listed in Bits[7:1] has occurred.

STATUS_WORD

Table 51. Register 0x79—STATUS_WORD

Bits	Bit Name/Function	R/W	Description
15	VOUT	R	Any bit asserted in STATUS_VOUT asserts this bit.
14	Reserved	R	Reserved.
13	INPUT	R	Any bit asserted in STATUS_INPUT asserts this bit.
12	Reserved	R	Reserved.
11	$\overline{\text{POWER\_GOOD}}$	R	$\overline{\text{POWER\_GOOD}}$ is a negation of POWER_GOOD, which means that the output power is not good. This bit is set when the sensed V_{OUT} is less than the limit programmed in the POWER_GOOD_OFF command. This bit is cleared when the sensed V_{OUT} voltage is greater than the limit that is programmed in the POWER_GOOD_ON command. This flag also triggers the $\overline{\text{PGOOD}}$ flag in Register 0xFEA0[6].
[10:7]	Reserved	R	Reserved.
6	POWER_OFF	R	This bit is asserted if the device is not providing power to the output, regardless of the reason, including not being enabled.
5	VOUT_OV_FAULT	R	An output overvoltage fault has occurred.
4	Reserved	R	Reserved.
3	VIN_UV_FAULT	R	An input undervoltage fault has occurred.
2	TEMPERATURE	R	An overtemperature fault or warning has occurred.
1	CML	R	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	R	A fault or warning not listed in Bits[7:1] has occurred.

STATUS_VOUT

Table 52. Register 0x7A—STATUS_VOUT

Bits	Bit Name/Function	R/W	Description
7	VOUT_OV_FAULT	R	An output overvoltage fault has occurred.
[6:5]	Reserved	R	Reserved.
4	VOUT_UV_FAULT	R	An output undervoltage fault has occurred.
3	VOUT_MAX warning		An attempt was made to set the output voltage to a value greater than allowed by the VOUT_MAX command.
[2:0]	Reserved	R	Reserved.

STATUS_INPUT

Table 53. Register 0x7C—STATUS_INPUT

Bits	Bit Name/Function	R/W	Description
[7:5]	Reserved	R	Reserved.
4	VIN_UV_FAULT	R	An input undervoltage fault has occurred.
3	VIN_LOW	R	The unit is off due to insufficient input voltage.
2	IIN_OC_FAST_FAULT	R	An input overcurrent fast fault has occurred.
[1:0]	Reserved	R	Reserved.

STATUS_TEMPERATURE

Table 54. Register 0x7D—STATUS_TEMPERATURE

Bits	Bit Name/Function	R/W	Description
7	OT_FAULT	R	An overtemperature fault has occurred.
6	OT_WARNING	R	An overtemperature warning has occurred.
[5:0]	Reserved	R	Reserved.

STATUS_CML

Table 55. Register 0x7E—STATUS_CML

Bits	Bit Name/Function	R/W	Description
7	CMD_ERR	R	An invalid or unsupported command is received.
6	DATA_ERR	R	Invalid or unsupported data is received.
[5:2]	Reserved	R	Reserved.
1	COMM_ERR	R	Other communication fault is detected.
0	Reserved	R	Reserved.

READ_VIN

The READ_VIN command returns the input voltage value (in V) in linear format.

Table 56. Register 0x88—READ_VIN

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R	5-bit twos complement N value for linear format: $X = Y \times 2^N$.
[10:0]	Mantissa	R	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

READ_IIN

The READ_IIN command returns the input current value (in A) in linear format.

Table 57. Register 0x89—READ_IIN

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R	5-bit twos complement N value for linear format: $X = Y \times 2^N$.
[10:0]	Mantissa	R	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

READ_VOUT

The READ_VOUT command returns the output voltage value (in V) in linear format.

Table 58. Register 0x8B—READ_VOUT

Bits	Bit Name/Function	R/W	Description
[15:0]	Mantissa	R	16-bit unsigned integer Y value for linear format: $X = Y \times 2^N$. N is defined in the VOUT_MODE command.

READ_TEMPERATURE

The READ_TEMPERATURE command returns the temperature value (in °C) in linear format.

Table 59. Register 0x8D—READ_TEMPERATURE

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R	5-bit N value for linear format: $X = Y \times 2^N$. 5-bit twos complement fixed at 00000.
[10:0]	Mantissa	R	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

READ_DUTY_CYCLE

The READ_DUTY_CYCLE command returns the duty cycle of the PWM output value in linear format.

Table 60. Register 0x94—READ_DUTY_CYCLE

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R	5-bit N value for linear format: $X = Y \times 2^N$. 5-bit twos complement fixed at 10110 (−10 decimal).
[10:0]	Mantissa	R	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

READ_FREQUENCY

The READ_FREQUENCY command returns the switching frequency value in linear format.

Table 61. Register 0x95—READ_FREQUENCY

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R	5-bit twos complement N value for linear format: $X = Y \times 2^N$.
[10:0]	Mantissa	R	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

READ_PMBUS_REVISION

The READ_PMBUS_REVISION command returns the PMBus version information. The ADP1050 supports PMBus Revision 1.2. Reading of this command results in a value of 0x22.

Table 62. Register 0x98—READ_PMBUS_REVISION

Bits	Bit Name/Function	R/W	Description
[7:4]	Part1 revision	R	Compliant to PMBus specifications, part 1: 0010 = Revision 1.2.
[3:0]	Part2 revision	R	Compliant to PMBus specifications, part 2: 0010 = Revision 1.2.

MFR_ID

Table 63. Register 0x99—MFR_ID

Bits	Bit Name/Function	R/W	Description
[7:0]	MFR_ID	R/W	Reads/writes the ID information of the manufacturer, which can be saved in the EEPROM.

MFR_MODEL

Table 64. Register 0x9A—MFR_MODEL

Bit	Bit Name/Function	R/W	Description
[7:0]	MFR_MODEL	R/W	Reads/writes the model information of the manufacturer, which can be saved in the EEPROM.

MFR_REVISION

Table 65. Register 0x9B—MFR_REVISION

Bit	Bit Name/Function	R/W	Description
[7:0]	MFR_REVISION	R/W	Reads/writes the revision information of the manufacturer, which can be saved in the EEPROM.

IC_DEVICE_ID

Table 66. Register 0xAD—IC_DEVICE_ID

Bit	Bit Name/Function	R/W	Description
[15:0]	IC_DEVICE_ID	R	Reads the IC device ID (default value = 0x4151).

IC_DEVICE_REV

Table 67. Register 0xAE—IC_DEVICE_REV

Bits	Bit Name/Function	R/W	Description
[7:0]	IC_DEVICE_REV	R	Reads the IC revision information. The value is 0x20 in the current silicon.

EEPROM_DATA_00

Table 68. Register 0xB0—EEPROM_DATA_00

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_00	R block	Block read data from Page 0 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_01

Table 69. Register 0xB1—EEPROM_DATA_01

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_01	R block	Block read data from Page 1 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_02

Table 70. Register 0xB2—EEPROM_DATA_02

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_02	R/W block	Block read/write data of Page 2 of the EEPROM main block. The EEPROM must first be unlocked. This page is not recommended for other use.

EEPROM_DATA_03

Table 71. Register 0xB3—EEPROM_DATA_03

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_03	R/W block	Block read/write data of Page 3 of the EEPROM main block. The EEPROM must first be unlocked. This page is reserved for storing power board parameter data for GUI use.

EEPROM_DATA_04

Table 72. Register 0xB4—EEPROM_DATA_04

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_04	R/W block	Block read/write data of Page 4 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_05

Table 73. Register 0xB5—EEPROM_DATA_05

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_05	R/W block	Block read/write data of Page 5 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_06

Table 74. Register 0xB6—EEPROM_DATA_06

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_06	R/W block	Block read/write data of Page 6 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_07

Table 75. Register 0xB7—EEPROM_DATA_07

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_07	R/W block	Block read/write data of Page 7 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_08

Table 76. Register 0xB8—EEPROM_DATA_08

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_08	R/W block	Block read/write data of Page 8 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_09

Table 77. Register 0xB9—EEPROM_DATA_09

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_09	R/W block	Block read/write data of Page 9 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_10

Table 78. Register 0xBA—EEPROM_DATA_10

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_10	R/W block	Block read/write data of Page 10 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_11

Table 79. Register 0xBB—EEPROM_DATA_11

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_11	R/W block	Block read/write data of Page 11 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_12

Table 80. Register 0xBC—EEPROM_DATA_12

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_12	R/W block	Block read/write data of Page 12 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_13

Table 81. Register 0xBD—EEPROM_DATA_13

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_13	R/W block	Block read/write data of Page 13 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_14

Table 82. Register 0xBE—EEPROM_DATA_14

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_14	R/W block	Block read/write data of Page 14 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_DATA_15

Table 83. Register 0xBF—EEPROM_DATA_15

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_DATA_15	R/W block	Block read/write data of Page 15 of the EEPROM main block. The EEPROM must first be unlocked.

EEPROM_CRC_CHKSUM

Table 84. Register 0xD1—EEPROM_CRC_CHKSUM

Bits	Bit Name/Function	R/W	Description
[7:0]	CRC checksum	R	Returns the CRC checksum value from the EEPROM download operation

EEPROM_NUM_RD_BYTES

Table 85. Register 0xD2—EEPROM_NUM_RD_BYTES

Bits	Bit Name/Function	R/W	Description
[7:0]	Number of read bytes returned	R/W	These bits set the number of read bytes that are returned when the EEPROM_DATA_xx commands are used.

EEPROM_ADDR_OFFSET

Table 86. Register 0xD3—EEPROM_ADDR_OFFSET

Bits	Bit Name/Function	R/W	Description
[15:0]	Address offset	R/W	These bits set the address offset of the current EEPROM page.

EEPROM_PAGE_ERASE

Table 87. Register 0xD4—EEPROM_PAGE_ERASE

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM page erase	W	Perform a page erase on the selected EEPROM page (Page 3 to Page 15). Wait at least 35 ms after each page erase operation. The EEPROM must first be unlocked. Page 0 and Page 1 are reserved for storing the default settings and user settings, respectively. The user cannot perform a page erase of Page 0 or Page 1. Page 2 is reserved for internal use; do not erase the contents of Page 2. Page 3 is reserved for storing the board parameters for GUI use; erase Page 3 before storing the board parameters. The following list shows the register setting used to access each page: 0x03 = Page 3. 0x04 = Page 4. 0x05 = Page 5. 0x06 = Page 6. 0x07 = Page 7. 0x08 = Page 8. 0x09 = Page 9. 0x0A = Page 10. 0x0B = Page 11. 0x0C = Page 12. 0x0D = Page 13. 0x0E = Page 14. 0x0F = Page 15.

EEPROM_PASSWORD

Table 88. Register 0xD5—EEPROM_PASSWORD

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM password	W	Writes the password using this command to unlock the EEPROM for read/write access. Writes the EEPROM password two consecutive times to unlock the EEPROM. Writes any other value to exit. The factory default password is 0xFF.

TRIM_PASSWORD

Table 89. Register 0xD6—TRIM_PASSWORD

Bits	Bit Name/Function	R/W	Description
[7:0]	Trim password	W	Writes the password using this command to unlock the trim registers for write access. Writes the trim password two consecutive times to unlock the registers. Writes any other value to exit. The trim password is the same as the EEPROM password. The factory default password is 0xFF.

CHIP_PASSWORD

Table 90. Register 0xD7—CHIP_PASSWORD

Bits	Bit Name/Function	R/W	Description
[15:0]	Chip password	W	Writes the correct chip password two consecutive times to unlock the chip registers for read/write access. Writes any other value to exit. The factory default password is 0xFFFF. This register cannot be read. Any read action on this register returns 0.

VIN_SCALE_MONITOR

The VIN_SCALE_MONITOR command is the scale factor between the V_{IN} ADC value and the real input voltage. It is typically used with the READ_VIN command. The value must be in the range of 0 to 1 decimal.

Table 91. Register 0xD8—VIN_SCALE_MONITOR

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear format: $X = Y \times 2^N$. N must be in the range of −12 to 0 decimal.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear format: $X = Y \times 2^N$.

IIN_SCALE_MONITOR

The IIN_SCALE_MONITOR command is the scale factor between the I_{IN} ADC value and the real input current. It is typically used with the READ_IIN command. The value must be in the range of 0 to 1 decimal.

Table 92. Register 0xD9—IIN_SCALE_MONITOR

Bits	Bit Name/Function	R/W	Description
[15:11]	Exponent	R/W	5-bit twos complement N value for linear mode format: $X = Y \times 2^N$. N must be in the range of −12 to 0 decimal.
[10:0]	Mantissa	R/W	11-bit twos complement Y value for linear mode format: $X = Y \times 2^N$.

EEPROM_INFO

Register 0xF1 is a read block. The EEPROM_INFO command reads the first flag data from the EEPROM.

Table 93. Register 0xF1—EEPROM_INFO

Bits	Bit Name/Function	R/W	Description
[7:0]	EEPROM_INFO	R block	Block read data of the EEPROM information block.

MFR_SPECIFIC_1

Table 94. Register 0xFA—MFR_SPECIFIC_1

Bits	Bit Name/Function	R/W	Description
[7:0]	Customized register	R/W	These bits are available to the user to store customized information.

MFR_SPECIFIC_2

Table 95. Register 0xFB—MFR_SPECIFIC_2

Bits	Bit Name/Function	R/W	Description
[7:0]	Customized register	R/W	These bits are available to the user to store customized information.

MANUFACTURER SPECIFIC EXTENDED COMMANDS DESCRIPTIONS

FLAG CONFIGURATION REGISTERS

Register 0xFE00 to Register 0xFE03 are used to set the fault flag response and the resolution after the flag is cleared. Register 0xFE05[5:4] sets the VDD_OV flag response. Register 0xFE05[7:6] sets the global flag reenable delay time.

Table 96. Register 0xFE00 to Register 0xFE05—Flag Response Registers

Register	Bits	Flag	Additional Settings
0xFE00	[7:4]	Reserved	Reserved
	[3:0]	IIN_OC_FAST_FAULT_RESPONSE	Register 0xFE08, Register 0xFE0E, Register 0xFE1A, Register 0xFE1F, Register 0xFEA0, Register 0xFEA3
0xFE01	[7:4]	Extended VOUT_OV_FAULT_RESPONSE	Register 0x40, Register 0x41, Register 0xFE26, Register 0xFE6B, Register 0xFE6C
	[3:0]	CS3_OC_FAULT_RESPONSE	Register 0xFE6A, Register 0xFEA0, Register 0xFEA3
0xFE02	[7:4]	VIN_UV_FAULT_RESPONSE	Register 0x35, Register 0x36, Register 0xFE29, Register 0xFEA1, Register 0xFEA4
	[3:0]	Reserved	Reserved
0xFE03	[7:4]	Reserved	Reserved
	[3:0]	FLAGIN_RESPONSE	Register 0xFE12, Register 0xFEA1, Register 0xFEA4
0xFE05	[5:4]	VDD_OV_RESPONSE	Register 0xFE05, Register 0xFEA0, Register 0xFEA3
	[3:0]	Reserved	Reserved

Table 97. Register 0xFE00 to Register 0xFE02—Flag Response Register Bit Descriptions

Bits	Bit Name/Function	R/W	Description		
[7:6]	Fault response	R/W	These bits specify the action when the flag is set.		
			Bit 7	**Bit 6**	**Flag Action**
			0	0	Continues operation without interruption.
			0	1	Disables SR1 and SR2.
			1	0	Disables all PWM outputs.
			1	1	Reserved.
[5:4]	Action after flag is cleared	R/W	These bits specify the action when the flag is cleared.		
			Bit 5	**Bit 4**	**Action After Flag Clearing**
			0	0	After the reenable delay time, the PWM outputs are reenabled with a soft start.
			0	1	The PWM outputs are reenabled immediately without a soft start.
			1	0	A PSON signal, through Register 0x01, Register 0x02, and/or the CTRL pin, is needed to reenable the PWM outputs.
			1	1	Reserved.
[3:2]	Fault response	R/W	These bits specify the action when the flag is set.		
			Bit 3	**Bit 2**	**Flag Action**
			0	0	Continues operation without interruption.
			0	1	Disables SR1 and SR2.
			1	0	Disables all PWM outputs.
			1	1	Reserved.
[1:0]	Action after flag is cleared	R/W	These bits specify the action when the flag is cleared.		
			Bit 1	**Bit 0**	**Action After Flag Clearing**
			0	0	After the reenable delay time, the PWM outputs are reenabled with a soft start.
			0	1	The PWM outputs are reenabled immediately without a soft start.
			1	0	A PSON signal, through Register 0x01, Register 0x02, and/or the CTRL pin, is needed to reenable the PWM outputs.
			1	1	Reserved.

Table 98. Register 0xFE03—Flag Response, FLAGIN_RESPONSE

Bits	Bit Name/Function	R/W	Description		
[7:4]	Reserved	R/W	Reserved.		
[3:2]	Fault response	R/W	These bits specify the action when the flag is set.		
			Bit 3	**Bit 2**	**Fault Response**
			0	0	Continues operation without interruption.
			0	1	Disable SR1 and SR2.
			1	0	Disable all PWM outputs.
			1	1	Reserved.
[1:0]	Action after the fault flag is cleared	R/W	These bits specify the action when the flag is cleared.		
			Bit 1	**Bit 0**	**Action After Fault Flag Clears**
			0	0	After the flag reenable delay time, the PWM outputs are reenabled with a soft start.
			0	1	The PWM outputs are reenabled immediately without a soft start.
			1	0	A PSON signal, programmed in Register 0x01, Register 0x02, and/or the CTRL pin, is needed to reenable the PWM outputs.
			1	1	Reserved.

Table 99. Register 0xFE05—Flag Reenable Delay, VDD_OV_RESPONSE

Bits	Bit Name/Function	R/W	Description		
[7:6]	Flag reenable delay	R/W	These bits specify the global delay from the time when a manufacturer specific flag is cleared to the soft start.		
			Bit 7	**Bit 6**	**Typical Delay Time**
			0	0	250 ms
			0	1	500 ms
			1	0	1 sec
			1	1	2 sec
5	VDD_OV flag ignore	R/W	This bit enables or disables the VDD_OV flag. 0 = VDD_OV flag is set when there is a V_{DD} overvoltage condition. When there is a V_{DD} overvoltage condition, the flag is set and the ADP1050 shuts down. When the V_{DD} overvoltage condition ends, the flag is cleared and the device downloads the EEPROM contents before restarting with a soft start process. 1 = VDD_OV flag is always cleared. When there is a V_{DD} overvoltage condition, the flag is always cleared and the device continues to operate without interruption.		
4	VDD_OV flag debounce	R/W	This bit sets the debounce time for the VDD_OV flag. 0 = 500 µs debounce time. 1 = 2 µs debounce time.		
[3:0]	Reserved	R/W	Reserved.		

SOFT START AND SOFTWARE RESET REGISTERS

Table 100. Register 0xFE06—Software Reset Go Command

Bits	Bit Name/Function	R/W	Description
[7:1]	Reserved	R/W	Reserved.
0	Software reset go	W	This bit lets the user perform a software reset of the ADP1050. Setting this bit resets the device with a restart delay period from the time the ADP1050 is turned off to the time ADP1050 restarts. The restart delay is set using Register 0xFE07[1:0] .

Table 101. Register 0xFE07—Software Reset Settings

Bits	Bit Name/Function	R/W	Description		
[7:3]	Reserved	R/W	Reserved.		
2	Additional flag reenable delay	R/W	This bit specifies whether an additional TON_DELAY value is added to the reenable delay after a manufacturer specific flag is cleared and before the ADP1050 begins a soft start. 0 = no additional delay is added to the reenable delay. 1 = additional delay is added to the reenable delay. The delay time is specified in the TON_DELAY command (Register 0x60).		
[1:0]	Restart delay	R/W	These bits specify the delay from the time when a PSON signal is set to the time when the soft start begins.		
			Bit 1	**Bit 0**	**Restart Delay**
			0	0	0 ms
			0	1	500 ms
			1	0	1 sec
			1	1	2 sec

Table 102. Register 0xFE08—Synchronous Rectifier (SR) Soft Start Settings

Bits	Bit Name/Function	R/W	Description		
7	Reserved	R/W	Reserved.		
6	CS1 cycle-by-cycle current limit to disable SR2	R/W	Setting this bit enables the CS1 cycle-by-cycle current limit to disable the SR2 output for the remainder of the switching cycle when cycle-by-cycle current limiting occurs.		
5	CS1 cycle-by-cycle current limit to disable SR1	R/W	Setting this bit enables the CS1 cycle-by-cycle current limit to disable the SR1 output for the remainder of the switching cycle when cycle-by-cycle current limiting occurs.		
4	SR soft start setting	R/W	0 = the synchronous rectifiers perform a soft start only the first time that they are enabled. 1 = the synchronous rectifiers perform a soft start every time that they are enabled.		
[3:2]	SR soft start speed	R/W	When an SR PWM output is configured to turn on with soft start (using Bits [1:0]), the rising edge of the output moves to the left in steps of 40 ns. These bits specify the number of switching cycles that are required to move the SR PWM output in 40 ns.		
			Bit 3	**Bit 2**	**SR Soft Start Timing**
			0	0	The SR PWM outputs change 40 ns in one switching cycle.
			0	1	The SR PWM outputs change 40 ns in four switching cycles.
			1	0	The SR PWM outputs change 40 ns in 16 switching cycles.
			1	1	The SR PWM outputs change 40 ns in 64 switching cycles.
1	SR2 soft start	R/W	Setting this bit enables soft start for SR2.		
0	SR1 soft start	R/W	Setting this bit enables soft start for SR1.		

Table 103. Register 0xFE09—Soft Start Setting of Open-Loop Operation

Bits	Bit Name/Function	R/W	Description
7	Open-loop operation soft start enable	R/W	Setting this bit enables the soft start of open-loop operation.
6	OUTA and OUTB edges	R/W	When this bit is set, the falling edges of OUTA and OUTB are always after the rising edges in one cycle during the soft start of open-loop operation.
5	SR1 and SR2 edges	R/W	This bit is valid only when Bit 7 of this register is set to 1. 0 = the rising edges of SR1 and SR2 always occur after the falling edges in one cycle during a soft start. 1 = the falling edges of SR1 and SR2 always occur after the rising edges in one cycle during a soft start.
[4:3]	Soft start speed of open-loop operation and open-loop feedforward operation	R/W	When the ADP1050 is configured for open-loop operation, the falling edge of the PWM output moves to the right in steps of 40 ns. When the ADP1050 is configured for open-loop feedforward operation, the modulation edge of the PWM output moves from the original position in steps of 40 ns. These bits specify how many switching cycles are required to move the PWM outputs in 40 ns.

Bit 4	Bit 3	Open-Loop Soft Start Timing
0	0	The PWM outputs change 40 ns in one switching cycle
0	1	The PWM outputs change 40 ns in four switching cycles
1	0	The PWM outputs change 40 ns in 16 switching cycles
1	1	The PWM outputs change 40 ns in 64 switching cycles

2	Soft start variation for open-loop operation	R/W	Setting this bit enables global variation during the soft start of open-loop operation. 1 = all outputs use the time variation calculated by OUTB ($t_{F2} - t_{R2}$).
[1:0]	Reserved	R/W	Reserved.

BLANKING AND $\overline{\text{PGOOD}}$ SETTING REGISTERS

Table 104. Register 0xFE0B—Flag Blanking During Soft Start

Bits	Bit Name/Function	R/W	Description
7	Reserved	R/W	Reserved.
6	Blank FLAGIN flag	R/W	0 = blank this flag during soft start. 1 = do not blank this flag during soft start.
5	Reserved	R/W	Reserved.
4	Blank VIN_UV_FAULT flag	R/W	0 = blank this flag during soft start. 1 = do not blank this flag during soft start.
3	Blank IIN_OC_FAST_FAULT flag	R/W	0 = blank this flag during soft start. 1 = do not blank this flag during soft start.
2	Reserved	R/W	Reserved.
1	Blank CS3_OC_FAULT flag	R/W	0 = blank this flag during soft start. 1 = do not blank this flag during soft start.
0	Blank VOUT_OV_FAULT flag	R/W	0 = blank this flag during soft start. 1 = do not blank this flag during soft start.

Table 105. Register 0xFE0C—Volt-Second Balance Blanking and SR Disable During Soft Start

Bits	Bit Name/Function	R/W	Description
[7:5]	Reserved	R/W	Reserved.
4	VIN_UV_FAULT reenable blank	R/W	0 = VIN_UV_FAULT flag is not blanked during the flag reenable delay. This is the recommended setting if the input voltage signal can be sensed by the ADP1050 before the PSU starts to operate. 1 = VIN_UV_FAULT flag is blanked during the flag reenable delay.
3	First flag ID update	R/W	This bit specifies whether the first flag ID is saved in the EEPROM. If it is set, the first flag ID is saved in the EEPROM. During the V_{DD} power reset, the first flag ID is downloaded from the EEPROM to Register 0xFEA6. 0 = the first flag ID is not saved in the EEPROM. 1 = the first flag ID is saved in the EEPROM.
2	Flag shutdown timing	R/W	Specifies when the PWM outputs are shut down after a manufacturer specific flag is triggered. 0 = the PWM outputs are shut down at the end of the switching cycle. 1 = the PWM outputs are shut down immediately.
1	Volt-second balance blanking	R/W	0 = the volt-second balance control is not blanked during soft start. 1 = the volt-second balance control is blanked during soft start.
0	SR disable	R/W	0 = SR1 and SR2 are not disabled during soft start. 1 = SR1 and SR2 are disabled during soft start.

Table 106. Register 0xFE0D—$\overline{\text{PGOOD}}$ Mask Settings

Bits	Bit Name/Function	R/W	Description
7	VIN_UV_FAULT flag	R/W	1 = the VIN_UV_FAULT flag is ignored by $\overline{\text{PGOOD}}$.
6	IIN_OC_FAST_FAULT flag	R/W	1 = the IIN_OC_FAST_FAULT flag is ignored by $\overline{\text{PGOOD}}$.
5	Reserved	R/W	Reserved.
4	VOUT_OV_FAULT flag	R/W	1 = the VOUT_OV_FAULT flag is ignored by $\overline{\text{PGOOD}}$.
3	VOUT_UV_FAULT flag	R/W	1 = the VOUT_UV_FAULT flag is ignored by $\overline{\text{PGOOD}}$.
2	OT_FAULT flag	R/W	1 = the OT_FAULT flag is ignored by $\overline{\text{PGOOD}}$.
1	OT_WARNING flag	R/W	1 = the OT_WARNING flag is ignored by $\overline{\text{PGOOD}}$.
0	Reserved	R/W	Reserved.

Table 107. Register 0xFE0E—$\overline{\text{PGOOD}}$ Flag Debounce

Bits	Bit Name/Function	R/W	Description		
[7:6]	Reserved	R/W	Reserved.		
5	CS1 cycle-by-cycle current limit to disable OUTB	R/W	Setting this bit enables the CS1 cycle-by-cycle current limit to disable the OUTB output for the remainder of the switching cycle when cycle-by-cycle current limiting occurs.		
4	CS1 cycle-by-cycle current limit to disable OUTA	R/W	Setting this bit enables the CS1 cycle-by-cycle current limit to disable the OUTA output for the remainder of the switching cycle when cycle-by-cycle current limiting occurs.		
[3:2]	$\overline{\text{PGOOD}}$ flag clearing debounce	R/W	These bits specify the $\overline{\text{PGOOD}}$ flag clearing debounce, which is the time from when the $\overline{\text{PGOOD}}$ clearing condition is met to the time when the $\overline{\text{PGOOD}}$ flag is cleared.		
			Bit 3	**Bit 2**	**$\overline{\text{PGOOD}}$ Flag Setting Debounce (ms)**
			0	0	0
			0	1	200
			1	0	320
			1	1	600
[1:0]	$\overline{\text{PGOOD}}$ flag setting debounce	R/W	These bits specify the $\overline{\text{PGOOD}}$ flag setting debounce, which is the time from when the $\overline{\text{PGOOD}}$ setting condition is met to the time when the $\overline{\text{PGOOD}}$ flag is set and the PG/$\overline{\text{ALT}}$ pin is pulled low.		
			Bit 1	**Bit 0**	**$\overline{\text{PGOOD}}$ Flag Clearing Debounce (ms)**
			0	0	0
			0	1	200
			1	0	320
			1	1	600

Table 108. Register 0xFE0F—Debounce Time for Asserting $\overline{\text{PGOOD}}$

Bits	Bit Name/Function	R/W	Debounce Time (ms)
7	VIN_UV_FAULT to assert $\overline{\text{PGOOD}}$	R/W	0 = 0 1 = 1.3
6	IIN_OC_FAST_FAULT to assert $\overline{\text{PGOOD}}$	R/W	0 = 0 1 = 1.3
5	Reserved	R/W	Reserved.
4	VOUT_OV_FAULT to assert $\overline{\text{PGOOD}}$	R/W	0 = 0 1 = 1.3
3	VOUT_UV_FAULT to assert $\overline{\text{PGOOD}}$	R/W	0 = 0 1 = 1.3
2	OT_FAULT to assert $\overline{\text{PGOOD}}$	R/W	0 = 0 1 = 1.3
1	OT_WARNING to assert $\overline{\text{PGOOD}}$	R/W	0 = 0 1 = 1.3
0	Reserved	R/W	Reserved.

SWITCHING FREQUENCY AND SYNCHRONIZATION REGISTERS

When synchronization is enabled, the ADP1050 takes the SYNI signal and adds the t_{SYNC_DELAY}, together with a 760 ns propagation delay, to generate the internal synchronization reference clock as shown in Figure 55. The ADP1050 uses the reference clock to generate its own clock.

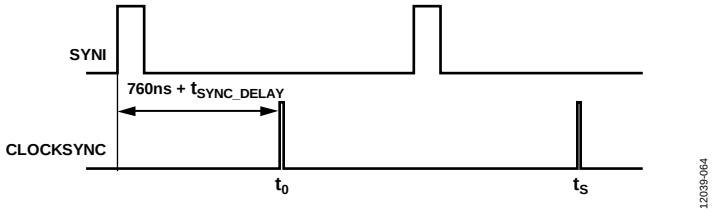


Figure 55. Synchronization Timing

Table 109. Register 0xFE11—Synchronization Delay Time

Bits	Bit Name/Function	R/W	Description
[7:0]	t_{SYNC_DELAY}	R/W	Sets the additional delay of the synchronization reference clock to the rising edge of the SYNI signal. Each LSB size is 40 ns. Note that this delay time cannot exceed one switching period. If the PWM 180° phase shift is enabled, this delay time cannot exceed half of one switching period.

Table 110. Register 0xFE12—Synchronization General Settings

Bits	Bit Name/Function	R/W	Description
7	Reserved	R/W	Reserved.
6	Phase capture range for synchronization	R/W	Sets the phase capture range. The ADP1050 detects the phase shift between the external and internal clocks when synchronization is enabled. When the phase shift falls within the range, synchronization starts. 0 = phase capture range is ±3.125% (±11.25°). 1 = phase capture range is ±6.25% (±22.5°). This is the recommended setting.
[5:4]	Reserved	R/W	Reserved.
3	Enable synchronization	R/W	This bit enables frequency synchronization as a slave device. The ADP1050 synchronizes with the external clock through the SYNI/FLGI pin. Bit 0 = 0 if synchronization is enabled.
2	FLGI polarity	R/W	Sets the polarity for the SYNI/FLGI pin when the pin is programmed as FLGI. 0 = a high logic level on the SYNI/FLGI pin sets the FLAGIN flag; a low logic level clears the FLAGIN flag. 1 = a low logic level on the SYNI/FLGI pin sets the FLAGIN flag; a high logic level sets the FLAGIN flag.
1	FLAGIN flag debounce time	R/W	0 = 0 µs debounce time for the FLAGIN flag. 1 = 100 µs debounce time for the FLAGIN flag.
0	SYNI/FLGI pin function selection	R/W	Configures the SYNI/FLGI pin as a flag input or a synchronization input. When SYNI is not enabled, this bit must be set to 1. 0 = the SYNI/FLGI pin is used as the synchronization input (SYNI). 1 = the SYNI/FLGI pin is used as the flag input (FLGI).

Table 111. Register 0xFE13—Dual-Ended Topology Mode

Bits	Bit Name/Function	R/W	Description
7	Reserved	R/W	Reserved.
6	Dual-ended topology enable	R/W	Setting this bit to 1 means that dual-ended topologies are used. It affects the modulation high limit. The modulation limit in each half cycle is half of the modulation limit that is programmed in Register 0xFE3C. 0 = operates in single-ended topologies, such as buck, forward, and flyback. 1 = operates in dual-ended topologies, such as full bridge, half bridge, and push pull.
[5:0]	Reserved	R/W	Reserved.

CURRENT SENSE AND LIMIT SETTING REGISTERS

Table 112. Register 0xFE14—CS1 Gain Trim

Bits	Bit Name/Function	R/W	Description
7	Gain polarity	R/W	Setting this bit to 1 means that negative gain is introduced. 0 = positive gain is introduced. 1 = negative gain is introduced.
[6:0]	CS1 gain trim	R/W	This value calibrates the CS1 current sense gain. Apply 1 V dc at the CS1 pin. This register is trimmed until the CS1 value reads 2560 decimal (0xA00).

Table 113. Register 0xFE19—CS3 OC Debounce

Bits	Bit Name/Function	R/W	Description		
7	Reserved	R/W	Reserved.		
[6:5]	CS3_OC_FAULT flag debounce	R/W	These two bits set the CS3_OC_FAULT flag debounce time.		
			Bit 6	**Bit 5**	**Debounce Time (ms)**
			0	0	0
			0	1	10
			1	0	20
			1	1	200
[4:0]	Reserved	R/W	Reserved.		

Table 114. Register 0xFE1A—IIN_OC_FAST_FAULT_LIMIT

Bits	Bit Name/Function	R/W	Description			
7	Reserved	R/W	Reserved.			
[6:4]	IIN_OC_FAST_FAULT_LIMIT	R/W	If the CS1 cycle-by-cycle current-limit comparator is set and the CS1_OCP flag is triggered, all PWM outputs that are on at that time can be programmed to be immediately disabled for the remainder of the switching cycle. The PWM outputs resume normal operation at the beginning of the next switching cycle. There is an internal counter, N, with an initial value of 0. N counts the CS1_OCP flag triggering number in consecutive switching cycles. If the CS1_OCP flag is triggered in one cycle, then $N_{CURRENT} = N_{PREVIOUS} + 2$. If the CS1_OCP flag is not triggered in one cycle and the previous $N > 0$, then $N_{CURRENT} = N_{PREVIOUS} - 1$. If the CS1_OCP flag is not triggered and the previous $N = 0$, then $N_{CURRENT} = 0$. When N reaches the IIN_OC_FAST_FAULT_LIMIT value, the IIN_OC_FAST_FAULT flag is set. Note that there is one cycle in single-ended topologies, such as buck converter and forward converter. There are two cycles in double-ended topologies, such as full bridge converter, half bridge converter, and push pull converter.			
			Bit 6	**Bit 5**	**Bit 4**	**Limit Value**
			0	0	0	2
			0	0	1	8
			0	1	0	16
			0	1	1	64
			1	0	0	128
			1	0	1	256
			1	1	0	512
			1	1	1	1024
[3:0]	Reserved	R/W	Reserved.			

Table 115. Register 0xFE1B—CS1 Cycle-by-Cycle Current-Limit Reference

Bits	Bit Name/Function	R/W	Description
7	Reserved	R/W	Reserved.
6	CS1 cycle-by-cycle current-limit ref	R/W	0 = the CS1 cycle-by-cycle current-limit reference is 1.2 V. 1 = the CS1 cycle-by-cycle current-limit reference is 0.25 V.
[5:0]	Reserved	R/W	Reserved.

Table 116. Register 0xFE1D—Matched Cycle-by-Cycle Current-Limit Settings

Bits	Bit Name/Function	R/W	Description
7	Reserved	R/W	Reserved.
6	Enable matched cycle-by-cycle current limit	R/W	Setting this bit enables the matched cycle-by-cycle current-limit function.
[5:2]	Reserved	R/W	Reserved.
1	OUTB rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1 cycle-by-cycle current-limit comparator is referenced to the rising edge of OUTB. 0 = no blanking at the OUTB rising edge. 1 = blanking time referenced to the OUTB rising edge.
0	OUTA rising edge blanking	R/W	This bit specifies whether the blanking time for the CS1 cycle-by-cycle current-limit comparator is referenced to the rising edge of OUTA. 0 = no blanking at the OUTA rising edge. 1 = blanking time referenced to the OUTA rising edge.

Table 117. Register 0xFE1E—SR1 and SR2 Response to Cycle-by-Cycle Current Limit

Bits	Bit Name/Function	R/W	Description
[7:2]	Reserved	R/W	Reserved.
1	SR2 response to cycle-by-cycle current limit	R/W	This bit is applicable only when the SR2 output is programmed to be in complement with the OUTA output. When this bit is set and there is a cycle-by-cycle current limit, the SR2 rising edge is turned on when the cycle-by-cycle current limit disables the OUTA. Its falling edge still follows the programmed value.
0	SR1 response to cycle-by-cycle current limit	R/W	This bit is applicable only when the SR1 output is programmed to be in complement with the OUTB output. When this bit is set and there is a cycle-by-cycle current limit, the SR1 rising edge is turned on when the cycle-by-cycle current limit disables the OUTB. Its falling edge still follows the programmed value.

Table 118. Register 0xFE1F—CS1 Cycle-by-Cycle Current-Limit Settings

Bits	Bit Name/Function	R/W	Description			
7	CS1 cycle-by-cycle current-limit comparator ignored	R/W	Setting this bit causes the CS1 OCP comparator output to be ignored. The CS1_OCP internal flag is always cleared.			
[6:4]	Leading edge blanking	R/W	These bits determine the leading edge blanking time. During this time, the CS1 OCP comparator output is ignored. This time is measured from the rising edges of OUTA and OUTB (programmable in Register 0xFE1D[1:0]).			
			Bit 6	**Bit 5**	**Bit 4**	**Leading Edge Blanking Time (ns)**
			0	0	0	0
			0	0	1	40
			0	1	0	80
			0	1	1	120
			1	0	0	200
			1	0	1	400
			1	1	0	600
			1	1	1	800
[3:2]	Reserved	R/W	Reserved.			
[1:0]	CS1 cycle-by-cycle current-limit debounce time	R/W	These bits set the CS1 cycle-by-cycle current-limit debounce time. This is the minimum time that the CS1 signal must be constantly above the CS1 cycle-by-cycle current-limit reference before the PWM outputs are shut down. When this happens, the selected PWM outputs can be disabled for the remainder of the switching cycle.			
			Bit 1	**Bit 0**	**Debounce Time (ns)**	
			0	0	0	
			0	1	40	
			1	0	80	
			1	1	120	

VOLTAGE SENSE AND LIMIT SETTING REGISTERS

Table 119. Register 0xFE20—VS Gain Trim

Bits	Bit Name/Function	R/W	Description
7	Trim polarity	R/W	0 = positive gain is introduced.
			1 = negative gain is introduced.
[6:0]	VS gain trim	R/W	These bits set the amount of gain trim that is applied to the VS ADC reading. This register trims the voltage reading in the READ_VOUT command after the VOUT_CAL_OFFSET trimming is completed. This register is trimmed until the READ_VOUT reading in the register exactly matches the output voltage measurement result.

Table 120. Register 0xFE25—Prebias Start-Up Enable

Bits	Bit Name/Function	R/W	Description
7	Prebias startup enable	R/W	Setting this bit enables the prebias start-up function. If it is enabled, the soft start ramp starts from the current output voltage. The initial PWM modulation value is generated based on the following: the Register 0xFE39 setting, the sensed V_{OUT} value, and the sensed V_{IN} value. To introduce the V_{IN} value for initial modulation calculation, set Register 0xFE6C[1] = 1, unless closed-loop input voltage feedforward operation mode is in use.
[6:0]	Reserved	R/W	Reserved.

Table 121. Register 0xFE26—VOUT_OV_FAULT Flag Debounce

Bits	Bit Name/Function	R/W	Description		
[7:6]	VOUT_OV_FAULT flag debounce	R/W	These bits set the VOUT_OV_FAULT flag debounce time.		
			Bit 7	**Bit 6**	**Typical Debounce Time (µs) (Delay Time 1)**
			0	0	0
			0	1	1
			1	0	2
			1	1	8
[5:0]	Reserved	R/W	Reserved		

Table 122. Register 0xFE28—VF Gain Trim

Bits	Bit Name/Function	R/W	Description
7	Trim polarity	R/W	0 = positive gain is introduced.
			1 = negative gain is introduced.
[6:0]	VF trim	R/W	These bits set the amount of gain trim that is applied to the VF ADC reading. This register trims the voltage at the VF pin for external resistor tolerances. When there is 1 V on the VF pin, this register is trimmed until the VF value register reads 1280 decimal (0x500).

Table 123. Register 0xFE29—VIN_ON and VIN_OFF Delay

Bits	Bit Name/Function	R/W	Description		
[7:6]	Reserved	R/W	Reserved		
5	VIN_UV_FAULT enable	R/W	Setting this bit enables the VIN_ON value and the VIN_OFF value used to generate the VIN_UV_FAULT flag.		
4	Power conversion stop delay	R/W	Sets the delay time from when the VIN_LOW flag is set to when the power conversion stops.		
			0 = 0 ms.		
			1 = 1 ms.		
[3:2]	Power conversion start delay	R/W	Sets the delay time from the clearing of the VIN_LOW flag to the start of the power conversion.		
			Bit 3	**Bit 2**	**Delay Time (ms)**
			0	0	0
			0	1	10
			1	0	40
			1	1	80
[1:0]	VIN_UV_FAULT flag debounce	R/W	When Bit 5 is set, sets the VIN_UV_FAULT flag debounce time.		
			Bit 1	**Bit 0**	**Typical Debounce Time (ms)**
			0	0	0
			0	1	2.5
			1	0	10
			1	1	100

TEMPERATURE SENSE AND PROTECTION SETTING REGISTERS

Table 124. Register 0xFE2A—RTD Gain Trim

Bits	Bit Name/Function	R/W	Description
7	Gain polarity	R/W	Setting this bit to 1 means that negative gain is introduced. Setting this bit to 0 means that positive gain is introduced.
[6:0]	RTD gain trim	R/W	This value calibrates the RTD sensing gain.

Table 125. Register 0xFE2B—RTD Offset Trim (MSBs)

Bits	Bit Name/Function	R/W	Description
[7:3]	Reserved	R/W	Reserved.
2	RTD current source disable	R/W	Setting this bit to 1 and writing 0x00 to Register 0xFE2D disables the RTD current source.
1	Trim polarity	R/W	Setting this bit to 1 means that negative offset is introduced. Setting this bit to 0 means that positive offset is introduced.
0	RTD offset trim, MSB	R/W	This bit, together with Register 0xFE2C as the LSBs, sets the amount of offset trim that is applied to the RTD ADC reading.

Table 126. Register 0xFE2C—RTD Offset Trim (LSBs)

Bits	Bit Name/Function	R/W	Description
[7:0]	RTD offset trim, LSBs	R/W	These eight bits, together with Bit 0 in Register 0xFE2B as the MSB, set the amount of offset trim that is applied to the RTD ADC reading.

Table 127. Register 0xFE2D—RTD Current Source Settings

Bits	Bit Name/Function	R/W	Description		
[7:6]	RTD current setting	R/W	These bits set the size of the current source on the RTD pin.		
			Bit 7	**Bit 6**	**Current Source (µA)**
			0	0	10
			0	1	20
			1	0	30
			1	1	40
[5:0]	RTD current trim	R/W	These six bits are used to trim the current source on the RTD pin. Each LSB corresponds to 160 nA, independent of the RTD current setting selected in Bits[7:6].		

Table 128. Register 0xFE2F—OT Hysteresis Settings

Bits	Bit Name/Function	R/W	Description		
[7:3]	Reserved	R/W	Reserved.		
2	OT_WARNING flag debounce	R/W	This bit sets the OT_WARNING flag debounce time. 0 = sets the flag actions debounce time to 100 ms. 1 = sets the flag actions debounce time to 0 ms.		
[1:0]	OT hysteresis	R/W	These bits set the OT hysteresis. Due to the negative temperature coefficient of the NTC thermistor or analog temperature sensor, the OT_FAULT flag clearing voltage threshold is programmed with a voltage greater than the OT_FAULT flag setting voltage threshold.		
			Bit 1	**Bit 0**	**OT Hysteresis**
			0	0	OT hysteresis = 12.5 mV (4 LSBs)
			0	1	OT hysteresis = 25 mV (8 LSBs)
			1	0	OT hysteresis = 37.5 mV (12 LSBs)
			1	1	OT hysteresis = 50 mV (16 LSBs)

DIGITAL COMPENSATOR AND MODULATION SETTING REGISTERS

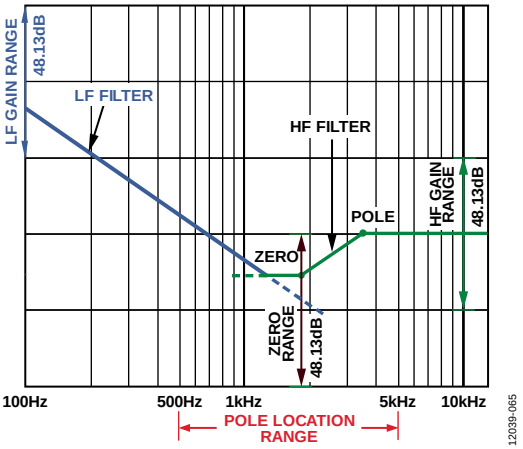


Figure 56. Digital Compensator Programmability

Table 129. Register 0xFE30—Normal Mode Compensator Low Frequency Gain Settings

Bits	Bit Name/Function	R/W	Description
[7:0]	Normal mode low frequency gain	R/W	This register determines the low frequency gain of the digital compensator in normal mode. It is programmable over a 48.13 dB range. See Figure 56.

Table 130. Register 0xFE31—Normal Mode Compensator Zero Settings

Bits	Bit Name/Function	R/W	Description
[7:0]	Normal mode zero settings	R/W	This register determines the position of the zero of the digital compensator in normal mode. See Figure 56.

Table 131. Register 0xFE32—Normal Mode Compensator Pole Settings

Bits	Bit Name/Function	R/W	Description
[7:0]	Normal mode pole settings	R/W	This register determines the position of the pole of the digital compensator in normal mode. See Figure 56.

Table 132. Register 0xFE33—Normal Mode Compensator High Frequency Gain Settings

Bits	Bit Name/Function	R/W	Description
[7:0]	Normal mode high frequency gain	R/W	This register determines the high frequency gain of the digital compensator in normal mode. It is programmable over a 48.13 dB range. See Figure 56.

Table 133. Register 0xFE38—CS1 Threshold for Volt-Second Balance

Bits	Bit Name/Function	R/W	Description
[7:0]	CS1 threshold for volt-second balance	R/W	This register sets the CS1 threshold to enable volt-second balance control. The volt-second balance control function is activated only if the CS1 value is greater than this threshold value. Each LSB is 6.25 mV.

Table 134. Register 0xFE39—Nominal Modulation Value for Prebias Startup

Bits	Bit Name/Function	R/W	Description	
[7:0]	Nominal modulation value for prebias start-up function	R/W	These bits set the nominal modulation value when the input voltage and the output voltage are in nominal conditions. It is used to calculate the initial modulation value, based on the sensed V_{OUT} value and the sensed V_{IN} value, for the prebias startup. If Register 0xFE6C[1] is cleared, the input voltage is always regarded as the nominal input condition unless closed-loop feedforward operation is in use.	
			Switching Frequency Range (kHz)	**Resolution Corresponding to LSB (ns)**
			49 to 87	80
			97.5 to 184	40
			195.5 to 379	20
			390.5 to 625	10

Table 135. Register 0xFE3A—SR Driver Delay

Bits	Bit Name/Function	R/W	Description
[7:6]	Reserved	R/W	Reserved.
[5:0]	SR gate drive delay	R/W	These bits set the SR gate drive delay in steps of 5 ns, from 0 ns to a maximum of 315 ns.

Table 136. Register 0xFE3B—PWM 180° Phase Shift Settings

Bits	Bit Name/Function	R/W	Description
7	Volt-second balance leading edge blanking	R/W	Setting this bit means that CS1 is blanked for volt-second balance calculations at the rising edge of those PWMs selected for volt-second balance. The blanking time is the same as for the CS1 cycle-by-cycle current-limit setting.
6	Volt-second balance 50% blanking of each phase	R/W	Setting this bit limits the sampling period for the current on CS1 to less than 50% of a half cycle.
5	SR2 180° phase shift	R/W	Setting this bit adds a 180° phase shift for the timing of the SR2 edges.
4	SR1 180° phase shift	R/W	Setting this bit adds a 180° phase shift for the timing of the SR1 edges.
[3:2]	Reserved	R/W	Reserved.
1	OUTB 180° phase shift	R/W	Setting this bit adds a 180° phase shift for the timing of the OUTB edges.
0	OUTA 180° phase shift	R/W	Setting this bit adds a 180° phase shift for the timing of the OUTA edges.

Figure 57 and Register 0xFE3C describe the modulation limit settings.

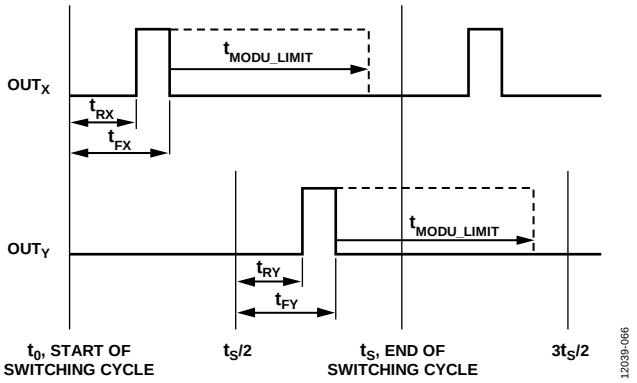


Figure 57. Setting Modulation Limits

Table 137. Register 0xFE3C—Modulation Limit

Bits	Bit Name/Function	R/W	Description	
[7:0]	Modulation limit	R/W	This register sets the modulation limit, t_{MODU_LIMIT} (maximum duty cycle). The modulation limit is the maximum time variation for the modulated edges from the default timing (see Figure 57). The step size of an LSB depends on the switching frequency.	
			Switching Frequency Range (kHz)	**LSB Step Size (ns)**
			49 to 87	80
			97.5 to 184	40
			195.5 to 379	20
			390.5 to 625	10

Table 138. Register 0xFE3D—Feedforward and Soft Start Filter Gain

Bits	Bit Name/Function	R/W	Description		
7	Soft start enable of open-loop input voltage feedforward operation	R/W	Setting this bit enables the soft start procedure of the open-loop input voltage feedforward operation. Set Bit 6 if this function is used.		
6	Open-loop input voltage feedforward operation enable	R/W	0 = open-loop input voltage feedforward operation is disabled. 1 = open-loop input voltage feedforward operation is enabled.		
5	High frequency ADC debounce time	R/W	This bit sets the debounce time for detecting the settling of the VS high frequency ADC. Bit 4 must be set to 1 to enable this function. 0 = 5 ms debounce time. 1 = 10 ms debounce time.		
4	High frequency ADC debounce enable	R/W	Setting this bit enables a debounce time for detecting the settling of the VS high frequency ADC at the end of a soft start. The debounce time is set using Bit 5.		
3	Feedforward ADC selection	R/W	Always set this bit to select the 11-bit VF ADC (factory default setting).		
2	Feedforward enable	R/W	This bit enables or disables feedforward control during closed-loop operation. 0 = closed-loop input voltage feedforward control is disabled. 1 = closed-loop input voltage feedforward control is enabled.		
[1:0]	Soft start filter gain	R/W	These bits set the soft start gain of the soft start filter.		
			Bit 1	**Bit 0**	**Soft Start Filter Gain**
			0	0	1
			0	1	2
			1	0	4
			1	1	8

PWM OUTPUTS TIMING REGISTERS

Figure 58 and Register 0xFE3E to Register 0xFE53 describe the implementation and programming of the four PWM signals that are generated by the ADP1050.

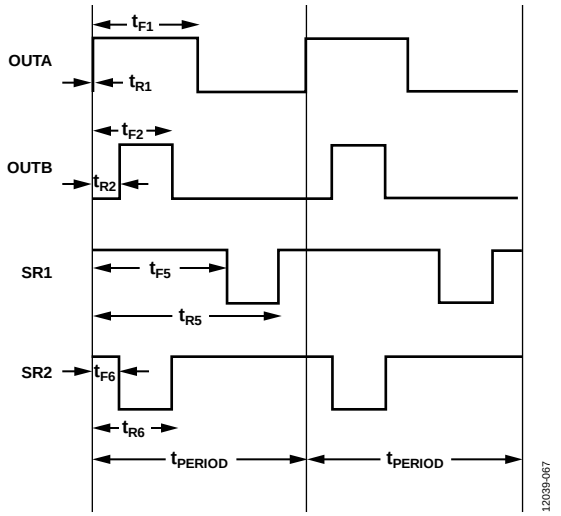


Figure 58. PWM Timing Diagram

Table 139. Register 0xFE3E/Register 0xFE41/Register 0xFE4A/Register 0xFE4D—OUTA/OUTB/SR1/SR2 Rising Edge Timing

Bits	Bit Name/Function	R/W	Description
[7:0]	Rising edge timing, t_{RX}, MSBs	R/W	These bits contain the eight MSBs of the 12-bit t_{RX} time. This value is always used with the four MSBs of Register 0xFE40, Register 0xFE43, Register 0xFE4C, and Register 0xFE4F, which contain the four LSBs of the t_{RX} time. t_{Rx} represents t_{R1}, t_{R2}, t_{R5}, and t_{R6}. Each LSB corresponds to 5 ns resolution.

Table 140. Register 0xFE3F/Register 0xFE42/Register 0xFE4B/Register 0xFE4E—OUTA/OUTB/SR1/SR2 Falling Edge Timing

Bits	Bit Name/Function	R/W	Description
[7:0]	Falling edge timing, t_{FX}, MSBs	R/W	These bits contain the eight MSBs of the 12-bit t_{FX} time. This value is always used with the four LSBs of Register 0xFE40, Register 0xFE43, Register 0xFE4C, and Register 0xFE4F, which contain the four LSBs of the t_{FX} time. t_{FX} represents t_{F1}, t_{F2}, t_{F5}, and t_{F6}. Each LSB corresponds to 5 ns resolution.

Table 141. Register 0xFE40/Register 0xFE43/Register 0xFE4C/Register 0xFE4F—OUTA/OUTB/ SR1/SR2 Rising and Falling Edge Timing (LSBs)

Bits	Bit Name/Function	R/W	Description
[7:4]	Rising edge timing, t_{RX}, LSBs	R/W	These bits contain the four LSBs of the 12-bit t_{RX} time. This value is always used with the eight bits of Register 0xFE3E, Register 0xFE41, Register 0xFE4A, and Register0xFE4D, which contain the eight MSBs of the t_{RX} time. t_{Rx} represents t_{R1}, t_{R2}, t_{R5}, and t_{R6}. Each LSB corresponds to 5 ns resolution.
[3:0]	Falling edge timing, t_{FX}, LSBs	R/W	These bits contain the four LSBs of the 12-bit t_{FX} time. This value is always used with the eight bits of Register 0xFE3F, Register 0xFE42, Register 0xFE4B, and Register 0xFE4E, which contain the eight MSBs of the t_{FX} time. t_{FX} represents t_{F1}, t_{F2}, t_{F5}, and t_{F6}. Each LSB corresponds to 5 ns resolution.

Table 142. Register 0xFE50—OUTA and OUTB Modulation Settings

Bits	Bit Name/Function	R/W	Description
7	OUTB t_{R2} modulation enable	R/W	0 = no PWM modulation of the t_{R2} edge. 1 = PWM modulation acts on the t_{R2} edge.
6	OUTB t_{R2} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{R2} to the right. 1 = negative sign. Increase of PWM modulation moves t_{R2} to the left.
5	OUTB t_{F2} modulation enable	R/W	0 = no PWM modulation of the t_{F2} edge. 1 = PWM modulation acts on the t_{F2} edge.
4	OUTB t_{F2} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{F2} to the right. 1 = negative sign. Increase of PWM modulation moves t_{F2} to the left.
3	OUTA t_{R1} modulation enable	R/W	0 = no PWM modulation of the t_{R1} edge. 1 = PWM modulation acts on the t_{R1} edge.
2	OUTA t_{R1} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{R1} to the right. 1 = negative sign. Increase of PWM modulation moves t_{R1} to the left.
1	OUTA t_{F1} modulation enable	R/W	0 = no PWM modulation of the t_{F1} edge. 1 = PWM modulation acts on the t_{F1} edge.
0	OUTA t_{F1} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{F1} to the right. 1 = negative sign. Increase of PWM modulation moves t_{F1} to the left.

Table 143. Register 0xFE52—SR1 and SR2 Modulation Settings

Bits	Bit Name/Function	R/W	Description
7	SR2 t_{R6} modulation enable	R/W	0 = no PWM modulation of the t_{R6} edge. 1 = PWM modulation acts on the t_{R6} edge.
6	SR2 t_{R6} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{R6} to the right. 1 = negative sign. Increase of PWM modulation moves t_{R6} to the left.
5	SR2 t_{F6} modulation enable	R/W	0 = no PWM modulation of the t_{F6} edge. 1 = PWM modulation acts on the t_{F6} edge.
4	SR2 t_{F6} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{F6} to the right. 1 = negative sign. Increase of PWM modulation moves t_{F6} to the left.
3	SR1 t_{R5} modulation enable	R/W	0 = no PWM modulation of the t_{R5} edge. 1 = PWM modulation acts on the t_{R5} edge.
2	SR1 t_{R5} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{R5} to the right. 1 = negative sign. Increase of PWM modulation moves t_{R5} to the left.
1	SR1 t_{F5} modulation enable	R/W	0 = no PWM modulation of the t_{F5} edge. 1 = PWM modulation acts on the t_{F5} edge.
0	SR1 t_{F5} modulation sign	R/W	0 = positive sign. Increase of PWM modulation moves t_{F5} to the right. 1 = negative sign. Increase of PWM modulation moves t_{F5} to the left.

Table 144. Register 0xFE53—PWM Output Disable

Bits	Bit Name/Function	R/W	Description
[7:6]	Reserved	R/W	Reserved.
5	SR2 disable	R/W	Setting this bit disables the SR2 output.
4	SR1 disable	R/W	Setting this bit disables the SR1 output.
[3:2]	Reserved	R/W	Reserved.
1	OUTB disable	R/W	Setting this bit disables the OUTB output.
0	OUTA disable	R/W	Setting this bit disables the OUTA output.

VOLT-SECOND BALANCE CONTROL REGISTERS

Table 145. Register 0xFE54—Volt-Second Balance Control General Settings

Bits	Bit Name/Function	R/W	Description
7	Volt-second balance enable control	R/W	Setting this bit enables volt-second balance control.
[6:5]	Reserved	R/W	Reserved.
4	Volt-second balance control source selection, OUTB	R/W	If this bit is set, OUTB rising edge is selected as the start of the integration period for volt-second balance control.
3	Volt-second balance control source selection, OUTA	R/W	If this bit is set, OUTA rising edge is selected as the start of the integration period for volt-second balance control.
2	Volt-second balance control limit	R/W	This bit sets the maximum amount of modulation from the volt-second control circuit. 0 = ±160 ns. 1 = ±80 ns.
[1:0]	Volt-second balance control gain	R/W	These bits set the gain of the volt-second balance control. The gain can be changed by a factor of 64. When these bits are set to 00, it takes approximately 700 ms to achieve volt-second balance. When these bits are set to 11, it takes approximately 10 ms to achieve volt-second balance.

Bit 1	Bit 0	Volt-Second Balance Loop Gain
0	0	1
0	1	4
1	0	16
1	1	64

Table 146. Register 0xFE55—Volt-Second Balance Control on OUTA and OUTB

Bits	Bit Name/Function	R/W	Description
7	t_{R2} balance setting	R/W	Setting this bit enables modulation from balancing control on the OUTB rising edge, t_{R2}.
6	t_{R2} balance direction	R/W	0 = positive sign. Increase of balancing control modulation moves t_{R2} right. 1 = negative sign. Increase of balancing control modulation moves t_{R2} left.
5	t_{F2} balance setting	R/W	Setting this bit enables modulation from balancing control on the OUTB falling edge, t_{F2}.
4	t_{F2} balance direction	R/W	0 = positive sign. Increase of balancing control modulation moves t_{F2} right. 1 = negative sign. Increase of balancing control modulation moves t_{F2} left.
3	t_{R1} balance setting	R/W	Setting this bit enables modulation from balancing control on the OUTA rising edge, t_{R1}.
2	t_{R1} balance direction	R/W	0 = positive sign. Increase of balancing control modulation moves t_{R1} right. 1 = negative sign. Increase of balancing control modulation moves t_{R1} left.
1	t_{F1} balance setting	R/W	Setting this bit enables modulation from balancing control on the OUTA falling edge, t_{F1}.
0	t_{F1} balance direction	R/W	0 = positive sign. Increase of balancing control modulation moves t_{F1} right. 1 = negative sign. Increase of balancing control modulation moves t_{F1} left.

Table 147. Register 0xFE57—Volt-Second Balance Control on SR1 and SR2

Bits	Bit Name/Function	R/W	Description
7	t_{R6} balance setting	R/W	Setting this bit enables modulation from balancing control on the SR2 rising edge, t_{R6}.
6	t_{R6} balance direction	R/W	0 = positive sign. Increase of balancing control modulation moves t_{R6} right. 1 = negative sign. Increase of balancing control modulation moves t_{R6} left.
5	t_{F6} balance setting	R/W	Setting this bit enables modulation from balancing control on the SR2 falling edge, t_{F6}.
4	t_{F6} balance direction	R/W	0 = positive sign. Increase of balancing control modulation moves t_{F6} right. 1 = negative sign. Increase of balancing control modulation moves t_{F6} left.
3	t_{R5} balance setting	R/W	Setting this bit enables modulation from balancing control on the SR1 rising edge, t_{R5}.
2	t_{R5} balance direction	R/W	0 = positive sign. Increase of balancing control modulation moves t_{R5} right. 1 = negative sign. Increase of balancing control modulation moves t_{R5} left.
1	t_{F5} balance setting	R/W	Setting this bit enables modulation from balancing control on the SR1 falling edge, t_{F5}.
0	t_{F5} balance direction	R/W	0 = positive sign. Increase of balancing control modulation moves t_{F5} right. 1 = negative sign. Increase of balancing control modulation moves t_{F5} left.

DUTY CYCLE READING SETTING REGISTERS

Table 148. Register 0xFE58—Duty Cycle Reading Settings

Bits	Bit Name/Function	R/W	Description
[7:4]	Reserved	R/W	Reserved.
3	OUTB duty cycle reporting	R/W	1 = READ_DUTY_CYCLE reports OUTB duty cycle value.
2	OUTA duty cycle reporting	R/W	1 = READ_DUTY_CYCLE reports OUTA duty cycle value.
1	Reserved	R/W	Reserved.
0	Polarity setting for input voltage compensation	R/W	Setting this bit applies an offset on the input voltage reading, READ_VIN, based on the reading of the input current, READ_IIN. The compensation multipler is set in Register 0xFE59. It is used to compensate the voltage drop caused by the current conduction. 0 = positive polarity compensation. 1 = negative polarity compensation.

Table 149. Register 0xFE59—Input Voltage Compensation Multiplier

Bits	Bit Name/Function	R/W	Description
[7:0]	Input voltage compensation multiplier	R/W	These bits specify the multiplier, N, for the input voltage compensation coefficient. The compensation equation is N × (Register 0xFEA7[15:4] value) ÷ 2^{11}, and the result is added to Register 0xFEAC[15:5]. The compensation polarity is set by Register 0xFE58[0].

OTHER REGISTER SETTINGS

Table 150. Register 0xFE61—Go Commands

Bits	Bit Name/Function	R/W	Description
[7:3]	Reserved	R/W	Reserved.
2	Frequency go	R/W	This bit synchronously latches the contents of Register 0x33 into the shadow registers used to calculate the switching frequency. Reading of this bit always returns 1.
1	PWM setting go	R/W	This bit synchronously latches the contents of Registers 0xFE3E to Register 0xFE53 into the shadow registers used to calculate the PWM edge timing. Reading this bit always returns 1.
0	Reserved	R/W	Reserved.

Table 151. Register 0xFE62—Customized Register

Bits	Bit Name/Function	R/W	Description
[7:0]	Customized register	R/W	These bits are available to the user to store customized information.

Table 152. Register 0xFE63—Modulation Reference MSBs Setting for Open-Loop Input Voltage Feedforward Operation

Bits	Bit Name/Function	R/W	Description	
[7:0]	Modulation reference setting MSBs	R/W	This register sets the eight MSBs of the modulation reference in open-loop feedforward operation mode. The step size of an LSB depends on the switching frequency.	
			Switching Frequency Range (kHz)	**LSB Step Size (ns)**
			49 to 87	80
			97.5 to 184	40
			195.5 to 379	20
			390.5 to 625	10

Table 153. Register 0xFE64—Modulation Reference LSBs Setting for Open-Loop Input Voltage Feedforward Operation

Bits	Bit Name/Function	R/W	Description	
[7:0]	Modulation reference setting LSBs	R/W	This register sets the eight LSBs of the modulation reference in open-loop feedforward operation mode. The step size of an LSB depends on the switching frequency.	
			Switching Frequency Range (kHz)	**LSB Step Size (ps)**
			49 to 87	312.5
			97.5 to 184	156.25
			195.5 to 379	78.125
			390.5 to 625	39.0625

Table 154. Register 0xFE65—Current Value Update Rate Setting

Bits	Bit Name/Function	R/W	Description		
[7:2]	Reserved	R/W	Reserved.		
[1:0]	Current value update rate	R/W	These bits specify the update rate for the current value of CS1 (READ_IIN command, Register 0x89). By default, the current values are updated every 10 ms.		
			Bit 1	**Bit 0**	**CS1 Value Update Rate (ms)**
			0	0	10 (defaut)
			0	1	52
			1	0	105
			1	1	210

Table 155. Register 0xFE67—Open-Loop Operation Settings

Bits	Bit Name/Function	R/W	Description
7	Reserved	R	Reserved.
6	Pulse skipping mode enable	R/W	1 = enables pulse skipping mode. If the ADP1050 requires a modulation value that is less than the threshold set by Register 0xFE69, pulse skipping is in use.
5	SR2 open-loop operation enable	R/W	This bit is set when SR2 is used in open-loop operation mode.
4	SR1 open-loop operation enable	R/W	This bit is set when SR1 is used in open-loop operation mode.
3	Reserved	R/W	Reserved.
2	Reserved	R/W	Reserved.
1	OUTB open-loop operation enable	R/W	This bit is set when OUTB is used in open-loop operation mode.
0	OUTA open-loop operation enable	R/W	This bit is set when OUTA is used in open-loop operation mode.

Table 156. Register 0xFE69—Pulse Skipping Mode Threshold

Bits	Bit Name/Function	R/W	Description
[7:0]	Pulse skipping mode threshold	R/W	These bits set the modulation pulse width threshold for pulse skipping. Each LSB is 5 ns.

Table 157. Register 0xFE6A—CS3_OC_FAULT_LIMIT

Bits	Bit Name/Function	R/W	Description
[7:0]	CS3_OC_FAULT_LIMIT	R/W	The eight MSB value of the CS3 value register in Register 0xFEA9 is compared with this 8-bit number. If the 8 MSB value is greater, the CS3_OC_FAULT flag is set.

Table 158. Register 0xFE6B—Modulation Threshold for OVP Selection

Bits	Bit Name/Function	R/W	Description	
[7:0]	Modulation threshold for conditional OVP responses	R/W	This value sets modulation threshold for conditional OVP response. When the real-time modulation value is above this threshold, the LARGE_MODULATION flag in Register 0xFE6C[2] is set.	
			Switching Frequency Range (kHz)	**Resolution Corresponding to LSB (ns)**
			49 to 87	80
			97.5 to 184	40
			195.5 to 379	20
			390.5 to 625	10

Table 159. Register 0xFE6C—Modulation Flag for OVP Selection

Bits	Bit Name/Function	R/W	Description
[7:3]	Reserved	R/W	Reserved.
2	LARGE_MODULATION	R	This bit is set when the modulation value is above the threshold set in Register 0xFE6B.
1	V_{IN} feedforward prebias startup	R/W	This bit is applicable only if the closed-loop feedforward operation is disabled (Register 0xFE3D[2] = 0). If the closed-loop feedforward operation is enabled, V_{IN} is always included for the calculation of the initial PWM modulation value. 1 = the initial PWM modulation value is calculated by the nominal modulation value (Register 0xFE39), the sensed V_{IN} voltage, and the sensed V_{OUT} voltage. 0 = the initial PWM modulation value is calculated by the nominal modulation value (Register 0xFE39) and the sensed V_{OUT} voltage. The V_{IN} voltage is ignored.
0	Conditional OVP enable	R/W	This bit sets the OVP actions when the VOUT_OV_FAULT flag is triggered. 0 = conditional OVP is disabled. The OVP action follows the PMBus VOUT_OV_FAULT_RESPONSE command (Register 0x41). 1 = conditional OVP is enabled. If Bit 2 = 1, OVP action follows the PMBus VOUT_OV_FAULT_RESPONSE (Register 0x41). If Bit 2 = 0, OVP action follows the extended VOUT_OV_FAULT_RESPONSE action (Register 0xFE01[7:4]).

Table 160. Register 0xFE6D—OUTA and OUTB Adjustment Reference During Synchronization

Bits	Bit Name/Function	R/W	Description
7	t_{R2} adjustment reference	R/W	Setting this bit enables edge adjustment on the OUTB rising edge, t_{R2}.
6	t_{R2} refers to t_S or $t_S/2$	R/W	0 = adjustment refers to $t_S/2$. 1 = adjustment refers to t_S.
5	t_{F2} adjustment reference	R/W	Setting this bit enables edge adjustment on the OUTB falling edge, t_{F2}.
4	t_{F2} refers to t_S or $t_S/2$	R/W	0 = adjustment refers to $t_S/2$. 1 = adjustment refers to t_S.
3	t_{R1} adjustment reference	R/W	Setting this bit enables edge adjustment on the OUTA rising edge, t_{R1}.
2	t_{R1} refers to t_S or $t_S/2$	R/W	0 = adjustment refers to $t_S/2$. 1 = adjustment refers to t_S.
1	t_{F1} adjustment reference	R/W	Setting this bit enables edge adjustment on the OUTA falling edge, t_{F1}.
0	t_{F1} refers to t_S or $t_S/2$	R/W	0 = adjustment refers to $t_S/2$. 1 = adjustment refers to t_S.

Table 161. Register 0xFE6F—SR1 and SR2 Adjustment Reference During Synchronization

Bits	Bit Name/Function	R/W	Description
7	t_{R6} adjustment reference	R/W	Setting this bit enables edge adjustment on the SR2 rising edge, t_{R6}.
6	t_{R6} refers to t_S or $t_S/2$	R/W	0 = adjustment refers to $t_S/2$. 1 = adjustment refers to t_S.
5	t_{F6} adjustment reference	R/W	Setting this bit enables edge adjustment on the SR2 falling edge, t_{F6}.
4	t_{F6} refers to t_S or $t_S/2$	R/W	0 = adjustment refers to $t_S/2$. 1 = adjustment refers to t_S.
3	t_{R5} adjustment reference	R/W	Setting this bit enables edge adjustment on the SR1 rising edge, t_{R5}.
2	t_{R5} refers to t_S or $t_S/2$	R/W	0 = adjustment refers to $t_S/2$. 1 = adjustment refers to t_S.
1	t_{F5} adjustment reference	R/W	Setting this bit enables edge adjustment on the SR1 falling edge, t_{F5}.
0	t_{F5} refers to t_S or $t_S/2$	R/W	0 = adjustment refers to $t_S/2$. 1 = adjustment refers to t_S.

Register 0xFE70 to Register 0xFE9F—Reserved

MANUFACTURER SPECIFIC FAULT FLAG REGISTERS

Table 162. Register 0xFEA0—Flag Register 1 and Register 0xFEA3—Latched Flag Register 1 (1 = Fault, 0 = Normal Operation)

Bits	Bit Name/Function	R/W	Description	Register[1]	Action[1]
7	CHIP_PASSWORD_UNLOCKED	R	Chip password is unlocked.		None
6	$\overline{\text{PGOOD}}$	R	At least one of the following flags has been set: VOUT_OV_FAULT, VOUT_UV_FAULT, OT_FAULT, OT_WARNING, VIN_UV_FAULT, IIN_OC_FAST_FAULT, POWER_OFF, CRC_FAULT, SOFT_START_FILTER, or POWER_GOOD. Some of the flags are maskable according to Register 0xFE0D.	0xFE0D and 0xFE0E	PG/$\overline{\text{ALT}}$ pin set low
5	IIN_OC_FAST_FAULT	R	An input overcurrent fast fault is triggered.	0xFE1F	Programmable
4	Reserved	R	Reserved.	N/A	N/A
3	CS3_OC_FAULT	R	A CS3 overcurrent fault is triggered.	0xFE6A	Programmable
[2:1]	Reserved	R	Reserved.	N/A	N/A
0	VDD_OV	R	V_{DD} is above the OVLO limit. The I²C/PMBus interface remains functional, but power conversion stops.	0xFE05	Programmable

[1] N/A means not applicable.

Table 163. Register 0xFEA1—Flag Register 2 and Register 0xFEA4—Latched Flag Register 2 (1 = Fault, 0 = Normal Operation)

Bits	Bit Name/Function	R/W	Description	Register[1]	Action[1]
[7:3]	Reserved	R	Reserved.	N/A	N/A
2	VIN_UV_FAULT	R	V_{IN} reading is below the VIN_OFF limit.	0xFE29	Programmable
1	SYNC_LOCKED	R	Cycle-by-cycle synchronization starts.	N/A	Programmable
0	FLAGIN	R	FLAGIN flag (SYNI/FLGI pin) is set.	0xFE12	Programmable

[1] N/A means not applicable.

Table 164. Register 0xFEA2—Flag Register 3 and Register 0xFEA5—Latched Flag Register 3 (1 = Fault, 0 = Normal Operation)

Bits	Bit Name/Function	R/W	Description	Register[1]	Action[1]
7	CHIP_ID	R	In the ADP1050, this bit is 0.	N/A	N/A
6	PULSE_SKIPPIING	R	Pulse skipping mode is in use.	0xFE69	Programmable
[5:4]	Reserved	R	Reserved.	N/A	N/A
3	EEPROM_UNLOCKED	R	The EEPROM is unlocked.	N/A	None
2	CRC_FAULT	R	The EEPROM contents that were downloaded are incorrect.	N/A	Immediate shutdown
1	Modulation	R	Digital compensator output is at its minimum or maximum limit.	N/A	None
0	SOFT_START_FILTER	R	The soft start filter is in use.	N/A	None

[1] N/A means not applicable.

Table 165. Register 0xFEA6—First Flag ID

Bits	Bit Name/Function	R/W	Description				
[7:4]	Previous first flag ID	R	These bits return the flag fault ID of the flag that caused the previous shutdown of the power supply. This previous shutdown occurred before the shutdown caused by the fault identified in Bits[3:0].				
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**First Flag**
			0	0	0	0	No flag
			0	0	0	1	IIN_OC_FAST_FAULT
			0	0	1	0	Reserved
			0	0	1	1	CS3_OC_FAULT
			0	1	0	0	VOUT_OV_FAULT
			0	1	0	1	VOUT_UV_FAULT
			0	1	1	0	VIN_UV_FAULT
			0	1	1	1	FLAGIN
			1	0	0	0	Reserved
			1	0	0	1	OT_FAULT
			1	0	1	0	Reserved
			1	0	1	1	Reserved
			1	1	0	0	Reserved
			1	1	0	1	Reserved
			1	1	1	0	Reserved
			1	1	1	1	Reserved
[3:0]	Current first flag ID	R	These bits return the flag fault ID of the fault that caused the shutdown of the power supply.				
			Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**First Flag**
			0	0	0	0	No flag
			0	0	0	1	IIN_OC_FAST_FAULT
			0	0	1	0	Reserved
			0	0	1	1	CS3_OC_FAULT
			0	1	0	0	VOUT_OV_FAULT
			0	1	0	1	VOUT_UV_FAULT
			0	1	1	0	VIN_UV_FAULT
			0	1	1	1	FLAGIN
			1	0	0	0	Reserved
			1	0	0	1	OT_FAULT
			1	0	1	0	Reserved
			1	0	1	1	Reserved
			1	1	0	0	Reserved
			1	1	0	1	Reserved
			1	1	1	0	Reserved
			1	1	1	1	Reserved

MANUFACTURER SPECIFIC VALUE READING REGISTERS

Table 166. Register 0xFEA7—CS1 Value

Bits	Bit Name/Function	R/W	Description
[15:4]	CS1 current value	R	This register contains 12-bit CS1 current information. The range of the CS1 input pin is from 0 V to 1.6 V. Each LSB corresponds to 390.625 µV. At 0 V input, the value in this register is 0 decimal. The nominal voltage at the CS1 pin is 1 V. At 1 V input, the value of these bits is 0xA00 (2560 decimal). The reading is equivalent to the READ_IIN command.
[3:0]	Reserved	R	Reserved.

Table 167. Register 0xFEA9—CS3 Value

Bits	Bit Name/Function	Type	Description
[15:4]	CS3 voltage value	R	This register contains 12-bit CS3 current information calculated by using the CS1 reading and duty cycle information. Each LSB corresponds to 4× the CS1 LSB in Register 0xFEA7, multiplied by the turns ratio of the main transformer, n ($n = N_{PRI}/N_{SEC}$).
[3:0]	Reserved	R	Reserved.

Table 168. Register 0xFEAA—VS Value

Bits	Bit Name/Function	R/W	Description
[15:4]	VS voltage value	R	This register contains the 12-bit VS± output voltage information. The range of the VS± input pins is from 0 V to 1.6 V. Each LSB corresponds to 390.625 µV. At 0 V input, the value in this register is 0. The nominal voltage at the VS+ and VS− pins is 1 V. At 1 V input, the value of these bits is 0xA00 (2560 decimal). The reading is equivalent to the READ_VOUT command.
[3:0]	Reserved	R	Reserved.

Table 169. Register 0xFEAB—RTD Value

Bits	Bit Name/Function	R/W	Description
[15:4]	RTD temperature value	R	These bits contain the 12-bit RTD temperature information, as determined from the RTD pin. The range of the RTD input pin is from 0 V to 1.6 V. Each LSB corresponds to 390.625 µV. At 0 V input, the value in this register is 0. The nominal voltage at the RTD pin is 1 V. At 1 V input, the value of these bits is 0xA00 (2560 decimal).
[3:0]	Reserved	R	Reserved.

Table 170. Register 0xFEAC—VF Value

Bits	Bit Name/Function	R/W	Description
[15:5]	VF voltage value	R	This register contains the 11-bit VF voltage information. The range of the VF input pin is from 0 V to 1.6 V. Each LSB corresponds to 781.25 µV. At 0 V input, the value in this register is 0. The nominal voltage at the VF pin is 1 V. At 1 V input, the value of these bits is 0x500 (1280 decimal). The reading is equivalent to the READ_VIN command.
[4:0]	Reserved	R	Reserved.

Table 171. Register 0xFEAD—Duty Cycle Value

Bits	Bit Name/Function	R/W	Description
[15:12]	Reserved	R	Reserved.
[11:0]	Duty cycle value	R	This register contains the 12-bit duty cycle information. Each LSB corresponds to 0.0244% duty cycle. At 100% duty cycle, the value of these bits is 0xFFF (4095 decimal).

Table 172. Register 0xFEAE—Input Power Value

Bits	Bit Name/Function	R/W	Description
[15:0]	Input power value	R	This register contains the 16-bit input power information. This value is the product of the input voltage value (VF) and input current value (CS1). The product of two 12-bit values is a 24-bit value, and the eight LSBs are discarded.

OUTLINE DIMENSIONS

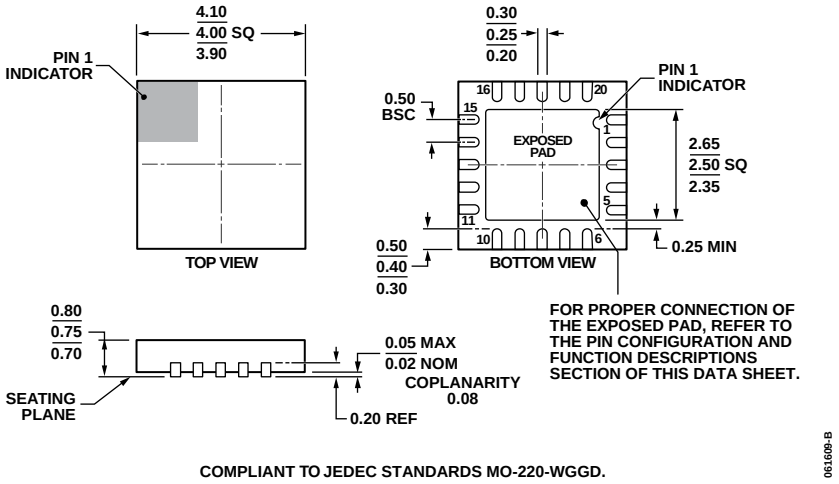


Figure 59. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1050ACPZ-RL	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
ADP1050ACPZ-R7	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
ADP1051-240-EVALZ		240 W Evaluation Board for the ADP1051 and the ADP1050	
ADP1050DC1-EVALZ		ADP1050 Daughter Card	
ADP-I2C-USB-Z		USB to I²C Adapter	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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