



THE DATASHEET OF AOD452A





AOD452A

N-Channel SDMOS™ POWER Transistor

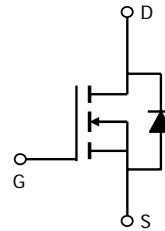
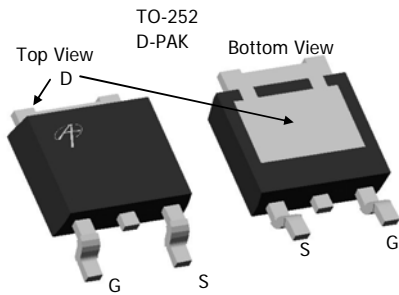
General Description

The AOD452A is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

Features

V_{DS} (V) = 25V
 I_D = 55A ($V_{GS} = 10V$)
 $R_{DS(ON)} < 8m\Omega$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 14m\Omega$ ($V_{GS} = 4.5V$)

100% UIS Tested!
 100% R_g Tested!



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	$T_C=25^\circ C$	55	A
	$T_C=100^\circ C$	43	
Pulsed Drain Current ^C	I_{DM}	120	
Pulsed Forward Diode Current ^C	I_{SM}	120	
Avalanche Current ^C	I_{AR}	35	
Repetitive avalanche energy $L=50\mu H$ ^C	E_{AR}	31	
Power Dissipation ^B	$T_C=25^\circ C$	50	W
	$T_C=100^\circ C$	25	
Power Dissipation ^A	$T_A=25^\circ C$	2.5	W
	$T_A=70^\circ C$	1.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	14.2	20	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	39	
Maximum Junction-to-Case ^B	$R_{\theta JC}$	2.5	3	$^\circ C/W$
Maximum Junction-to-TAB ^B	$R_{\theta JC-TAB}$	2.7	3.2	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	25			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =25V, V _{GS} =0V T _J =55°C			10 50	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	2	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	120			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =30A T _J =125°C		6 8.6	8 12	mΩ
		V _{GS} =4.5V, I _D =20A		11.5	14	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =30A		50		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				55	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance		990	1180	1450	pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =12.5V, f=1MHz	210	275	350	pF
C _{rss}	Reverse Transfer Capacitance		125	175	245	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.1	1.7	2.5	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge		18	21.7	26	nC
Q _g (4.5V)	Total Gate Charge	V _{GS} =10V, V _{DS} =12.5V, I _D =30A	9	11	13	nC
Q _{gs}	Gate Source Charge		3	4	5	nC
Q _{gd}	Gate Drain Charge		4.5	6.4	9	nC
t _{D(on)}	Turn-On Delay Time			6.8		ns
t _r	Turn-On Rise Time	V _{GS} =10V, V _{DS} =12.5V, R _L =0.42Ω,		13.8		ns
t _{D(off)}	Turn-Off Delay Time	R _{GEN} =3Ω		21.5		ns
t _f	Turn-Off Fall Time			8.7		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =30A, dI/dt=500A/μs	8.4	10.6	13	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =30A, dI/dt=500A/μs	13	16	20	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

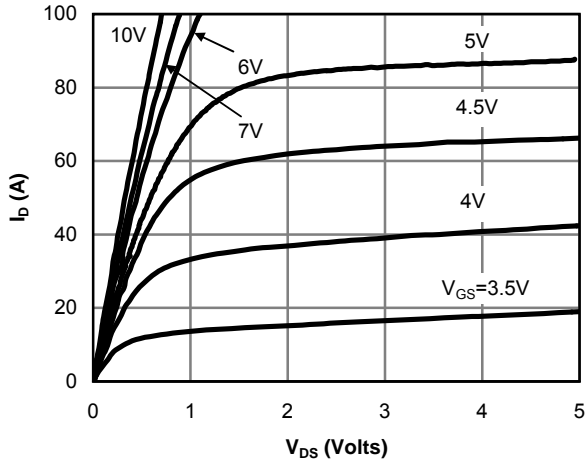


Fig 1: On-Region Characteristics

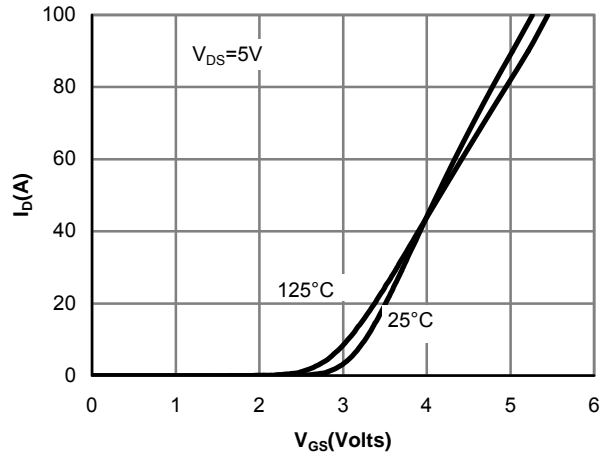


Figure 2: Transfer Characteristics

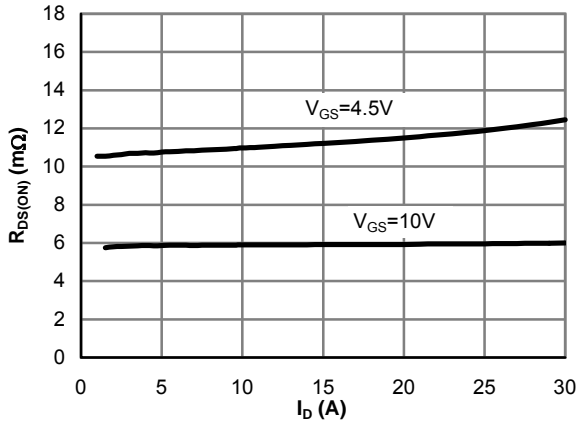


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

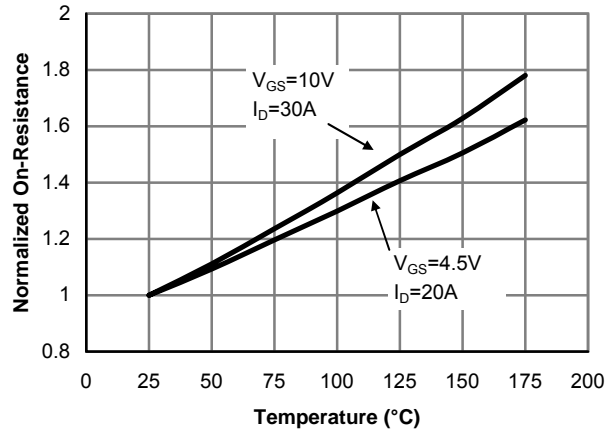


Figure 4: On-Resistance vs. Junction Temperature

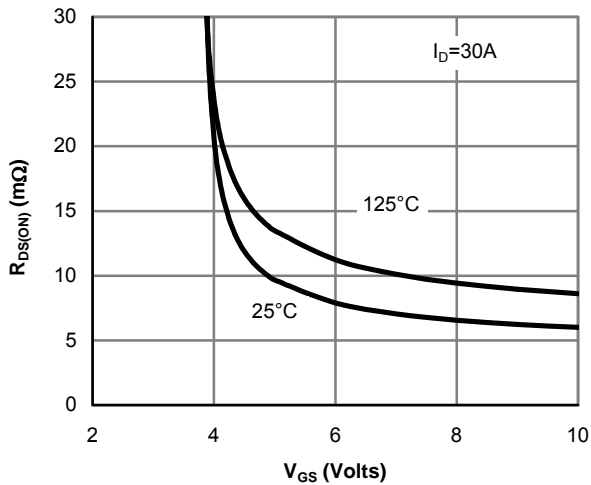


Figure 5: On-Resistance vs. Gate-Source Voltage

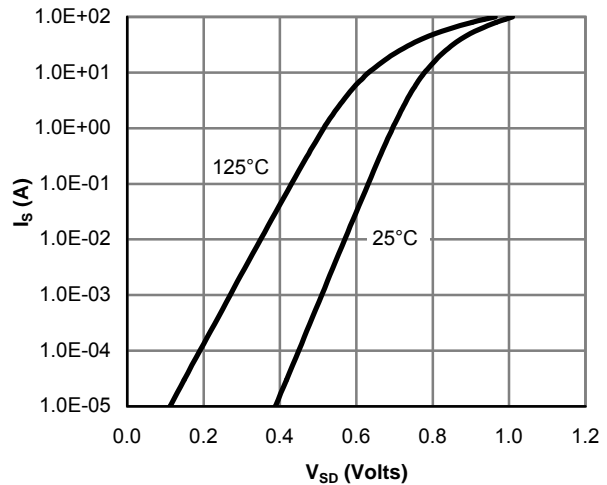


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

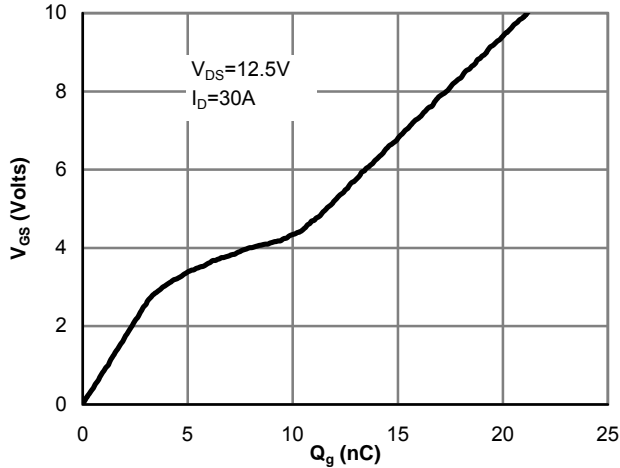


Figure 7: Gate-Charge Characteristics

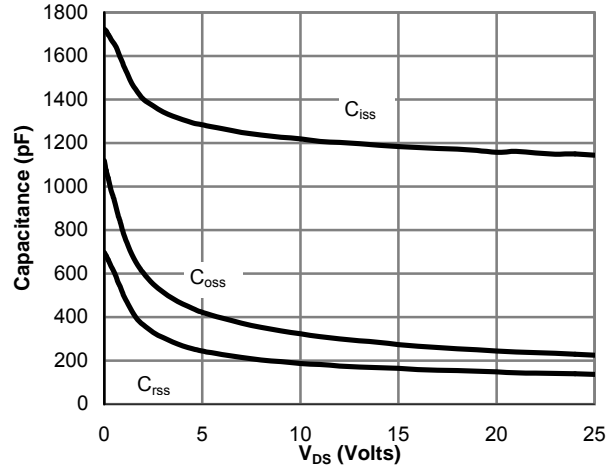


Figure 8: Capacitance Characteristics

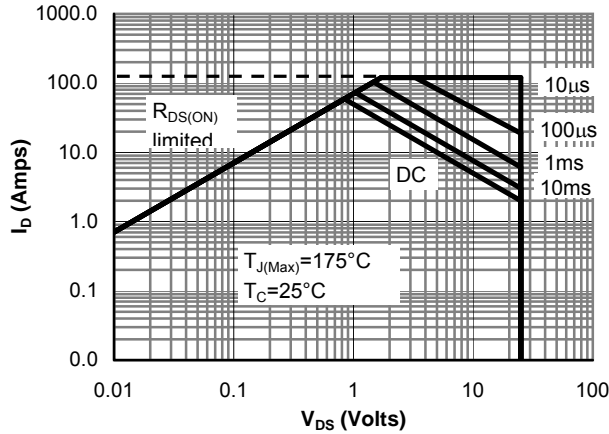


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

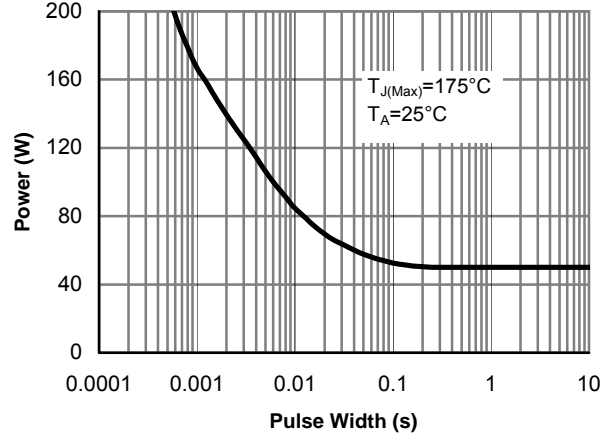


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

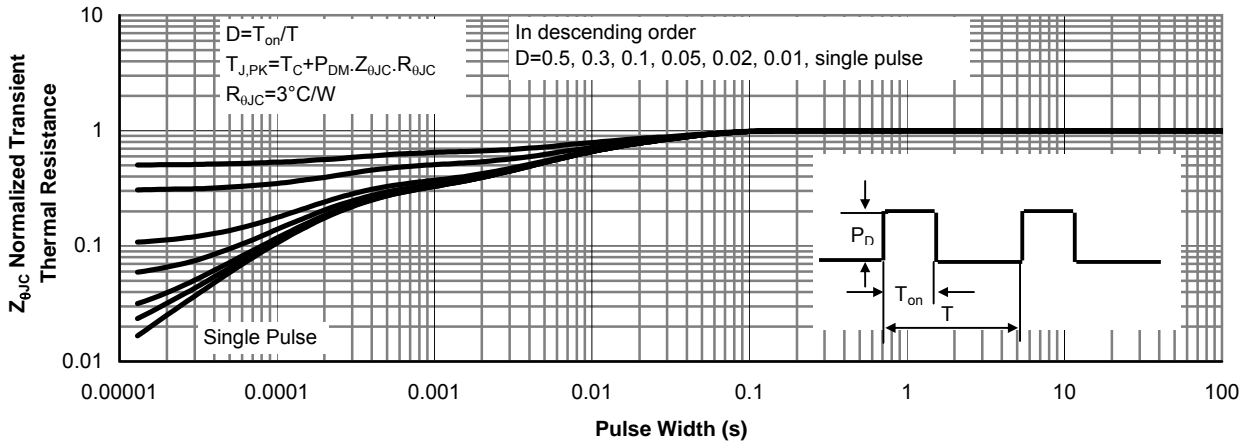


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

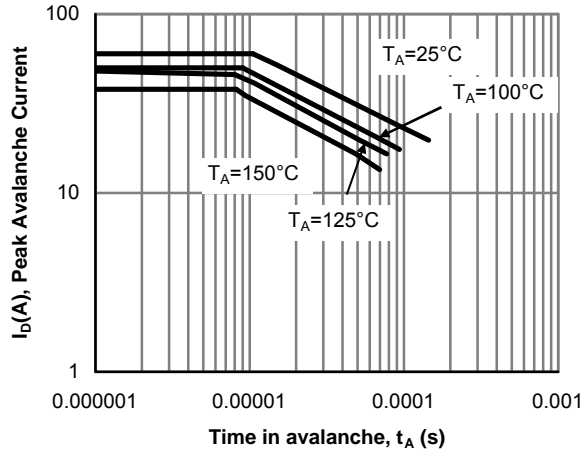


Figure 12: Single Pulse Avalanche capability

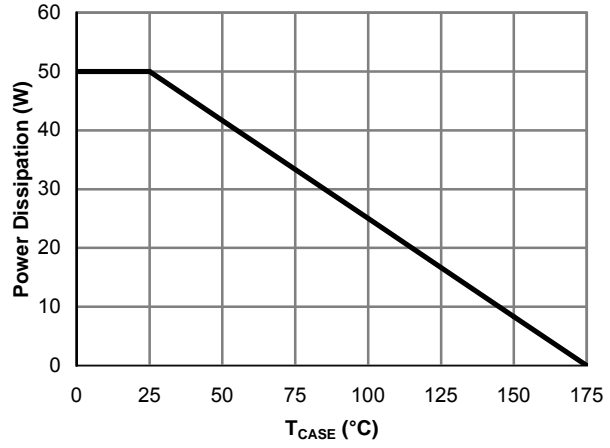


Figure 13: Power De-rating (Note B)

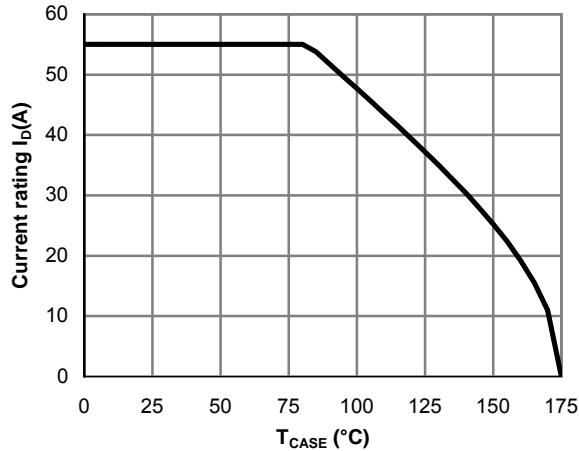


Figure 14: Current De-rating (Note B)

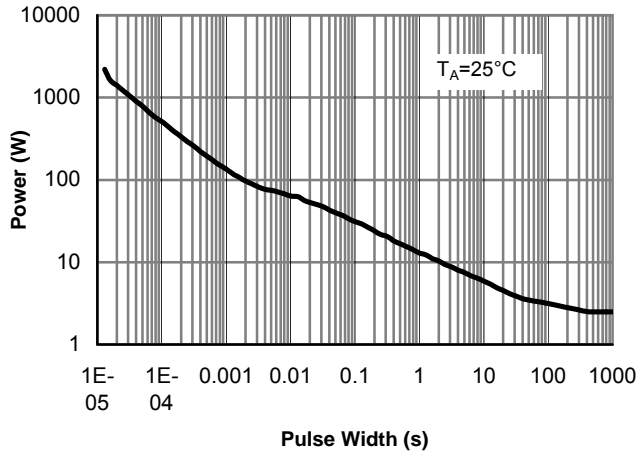


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

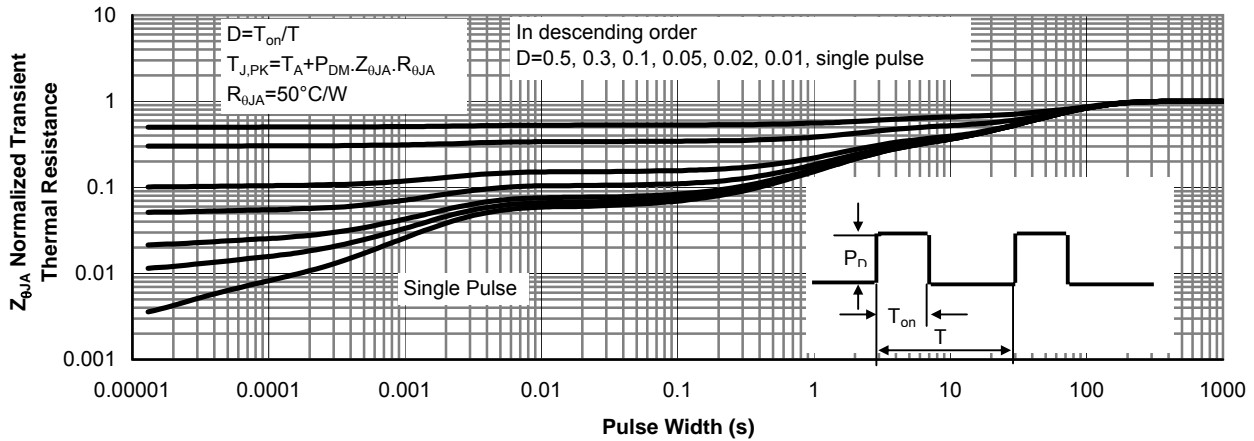


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

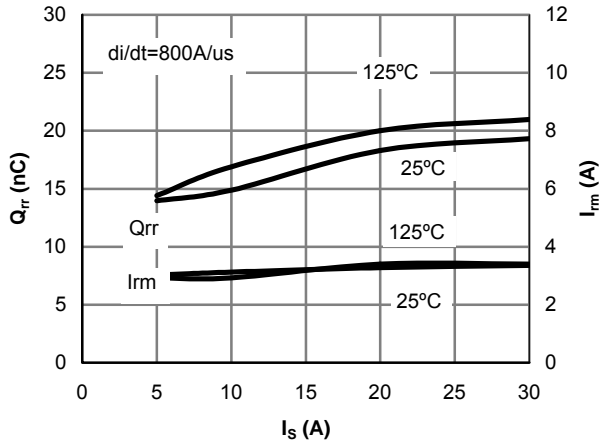


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

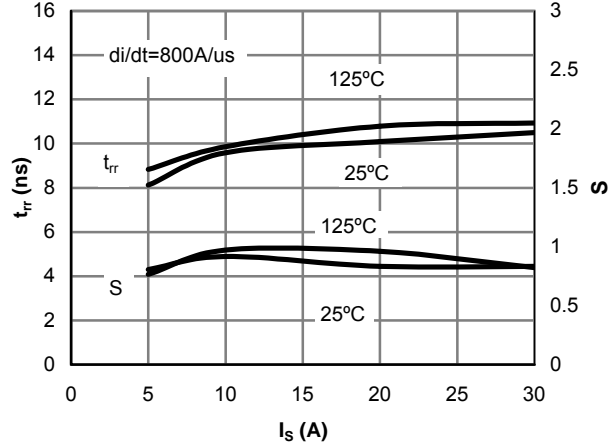


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

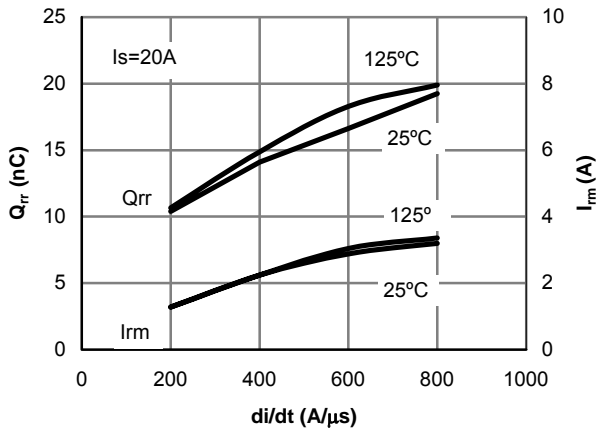


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

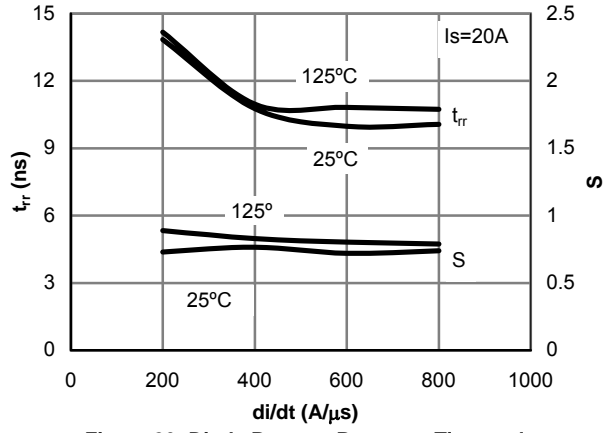
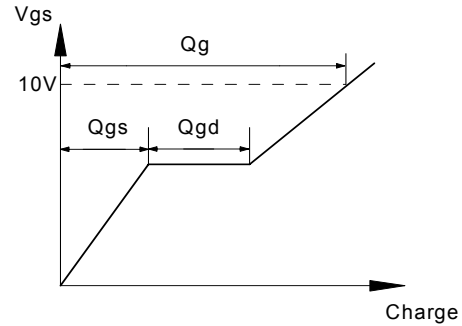
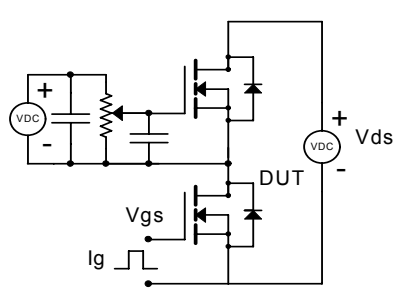
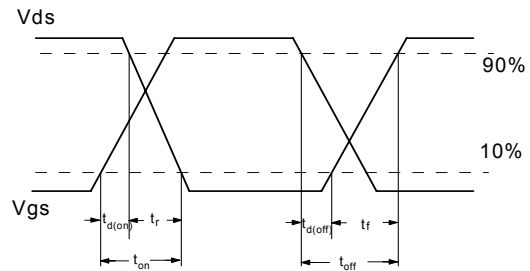
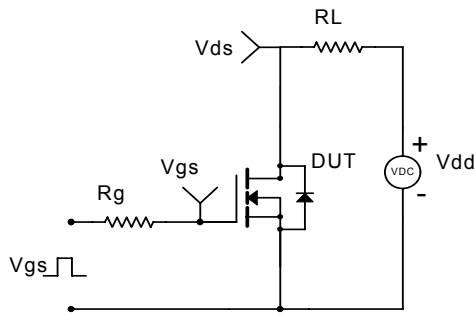


Figure 20: Diode Reverse Recovery Time and Softness Factor vs. di/dt

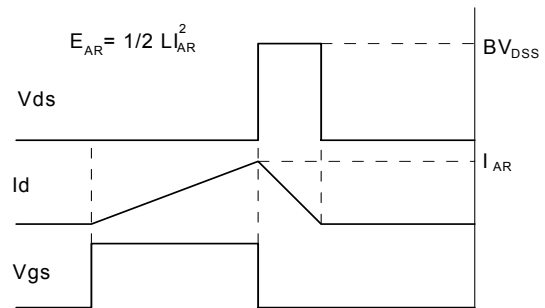
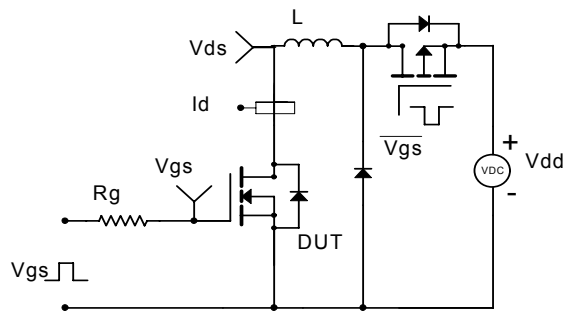
Gate Charge Test Circuit & Waveform



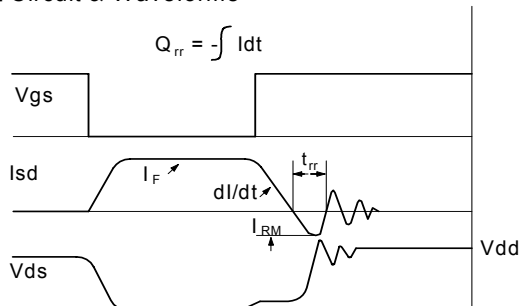
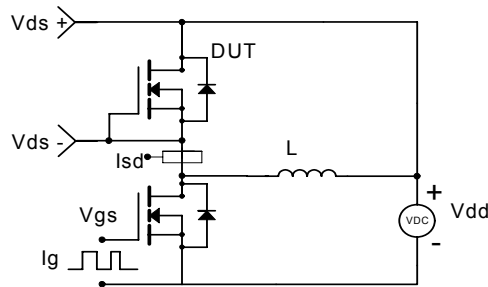
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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