



THE DATASHEET OF AOD603A



General Description

The AOD603A uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

Product Summary

N-Channel

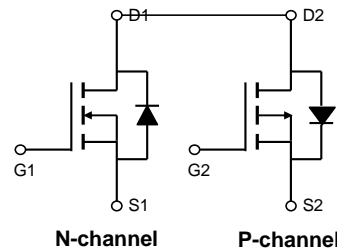
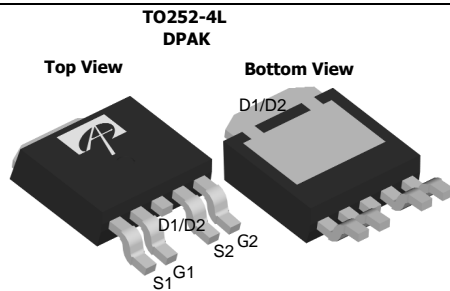
$V_{DS} = 60V$
 $I_D = 13A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 60m\Omega$ ($V_{GS} = 10V$)
 $< 85m\Omega$ ($V_{GS} = 4.5V$)

100% UIS Tested
 100% R_g Tested

P-Channel

$-60V$
 $-13A$ ($V_{GS} = -10V$)
 $R_{DS(ON)} < 115m\Omega$ ($V_{GS} = -10V$)
 $< 150m\Omega$ ($V_{GS} = -4.5V$)

100% UIS Tested
 100% R_g Tested



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Max N-channel	Max P-channel	Units
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^G	I_D	$T_C = 25^\circ C$	12	A
		$T_C = 100^\circ C$	9.5	
Pulsed Drain Current ^C	I_{DM}	30	-30	
Continuous Drain Current	I_{DSM}	$T_A = 25^\circ C$	3.5	A
		$T_A = 70^\circ C$	3	
Avalanche Current ^C	I_{AS}, I_{AR}	19	25	A
Avalanche energy $L=0.1mH$ ^C	E_{AS}, E_{AR}	18	31	mJ
Power Dissipation ^B	P_D	$T_C = 25^\circ C$	27	W
		$T_C = 100^\circ C$	13.5	
Power Dissipation ^A	P_{DSM}	$T_A = 25^\circ C$	2	W
		$T_A = 70^\circ C$	1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter N-channel	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	19	$^\circ C/W$
Maximum Junction-to-Ambient ^{A D}		Steady-State	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	4	5.5	$^\circ C/W$
Parameter P-channel	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	19	$^\circ C/W$
Maximum Junction-to-Ambient ^{A D}		Steady-State	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	2.5	3.5	$^\circ C/W$

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1	2.4	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =12A T _J =125°C		47 90	60 110	mΩ
		V _{GS} =4.5V, I _D =8A		67	85	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =12A		22		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.74	1	V
I _S	Maximum Body-Diode Continuous Current ^G				12	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz	360	450	540	pF
C _{oss}	Output Capacitance		40	61	80	pF
C _{rss}	Reverse Transfer Capacitance		16	27	40	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.6	1.35	2	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =12A		7.5	10	nC
Q _{g(4.5V)}	Total Gate Charge			3.8	5	nC
Q _{gs}	Gate Source Charge			1.2		nC
Q _{gd}	Gate Drain Charge			1.9		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =2.5Ω, R _{GEN} =3Ω		4.2		ns
t _r	Turn-On Rise Time			3.4		ns
t _{D(off)}	Turn-Off DelayTime			16		ns
t _f	Turn-Off Fall Time			2		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =12A, dI/dt=100A/μs		27	35	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =12A, dI/dt=100A/μs		30		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allow s it.

B. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

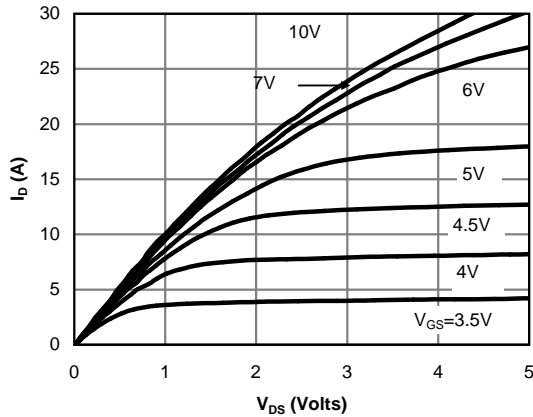


Figure 1: On-Region Characteristics (Note E)

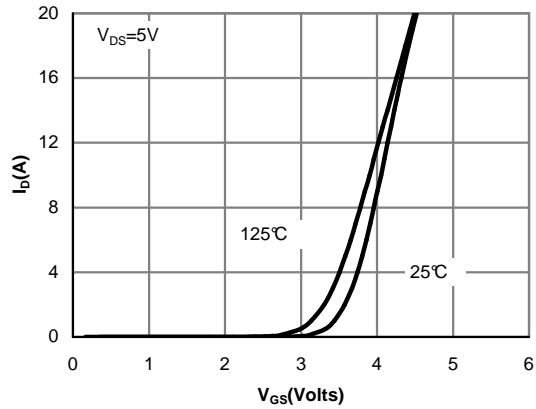


Figure 2: Transfer Characteristics (Note E)

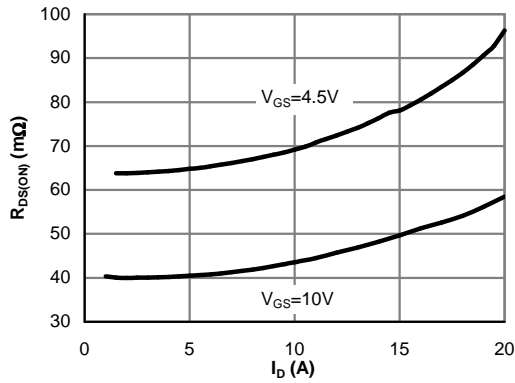


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

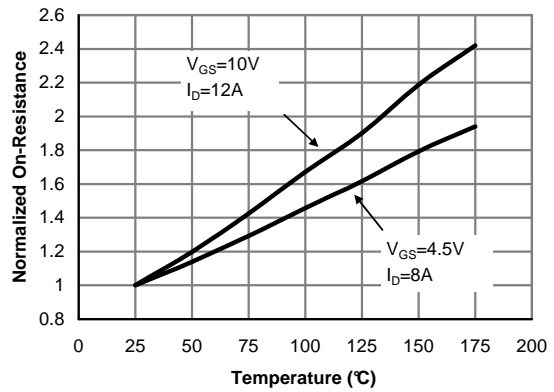


Figure 4: On-Resistance vs. Junction Temperature (Note E)

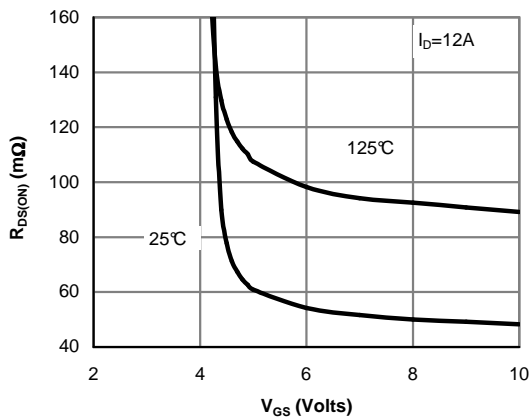


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

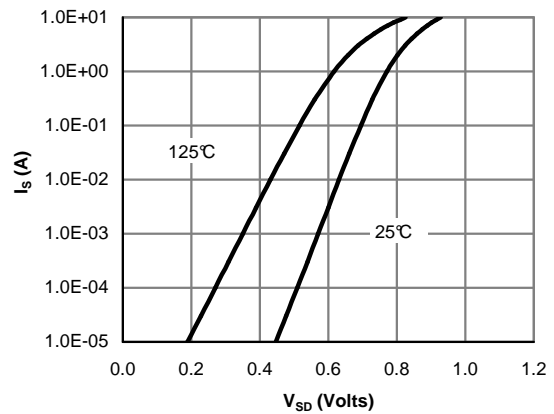


Figure 6: Body-Diode Characteristics (Note E)

N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

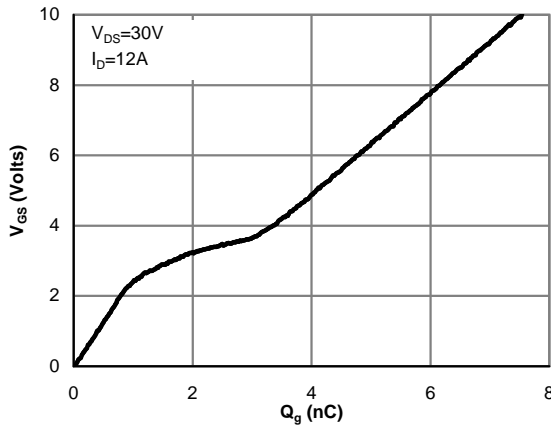


Figure 7: Gate-Charge Characteristics

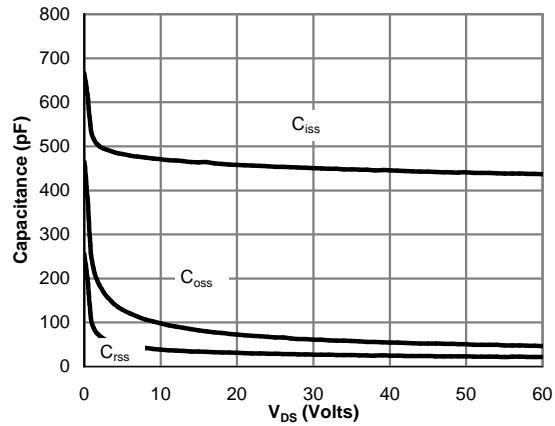


Figure 8: Capacitance Characteristics

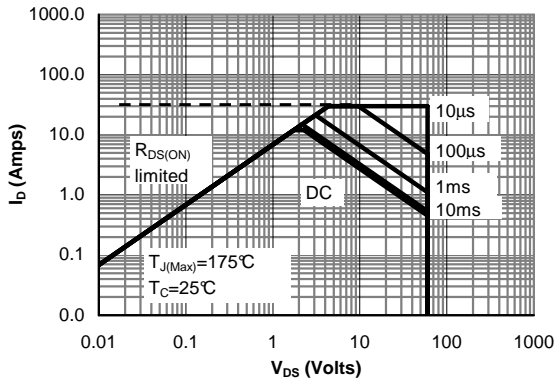


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

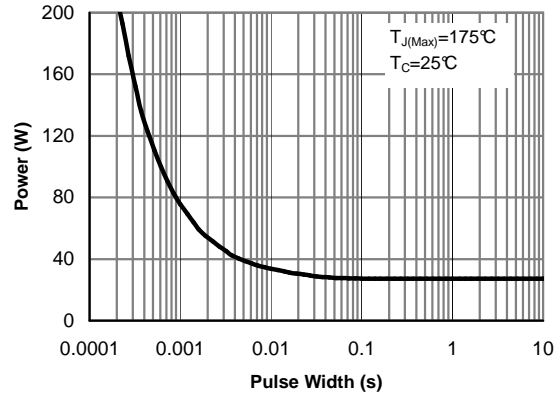


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

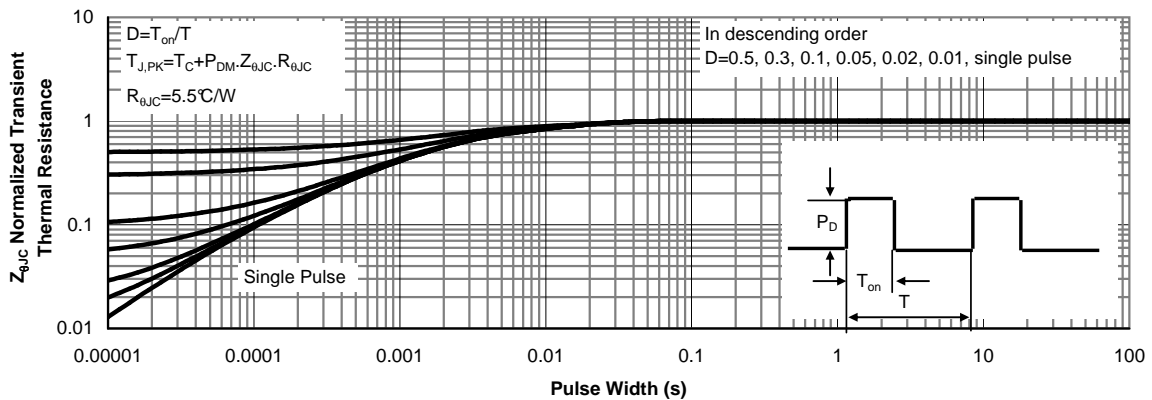


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

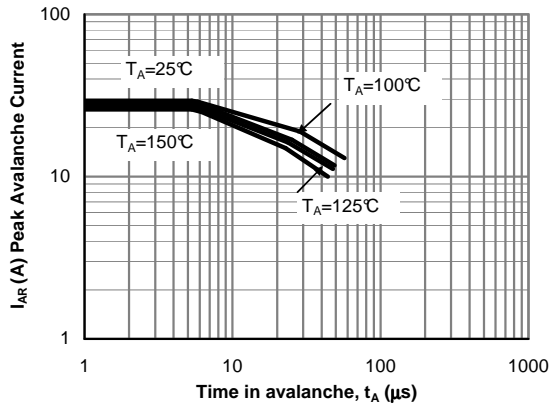


Figure 12: Single Pulse Avalanche capability (Note C)

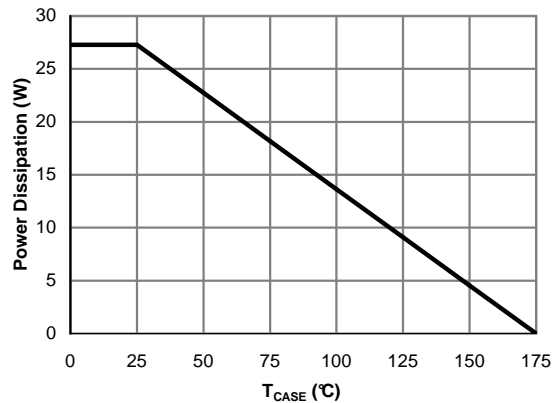


Figure 13: Power De-rating (Note F)

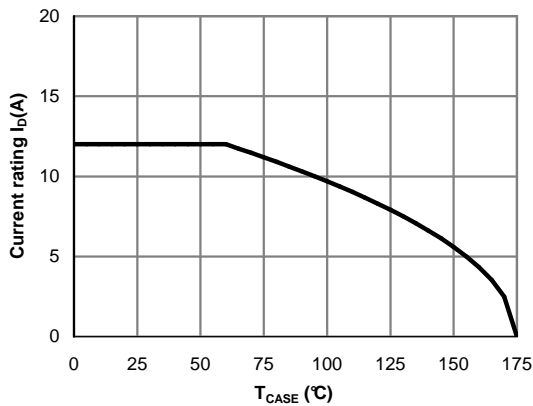


Figure 14: Current De-rating (Note F)

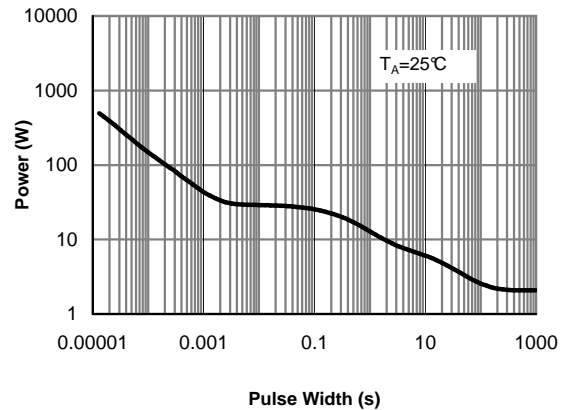


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

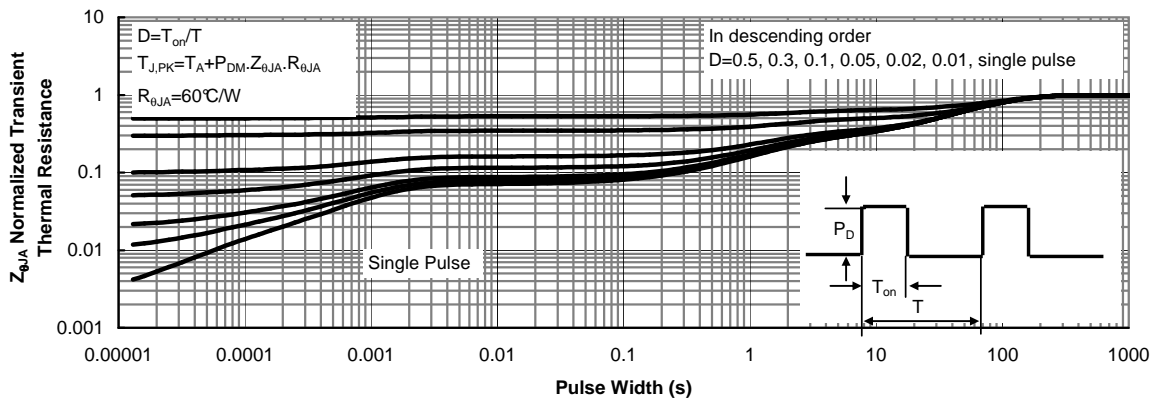
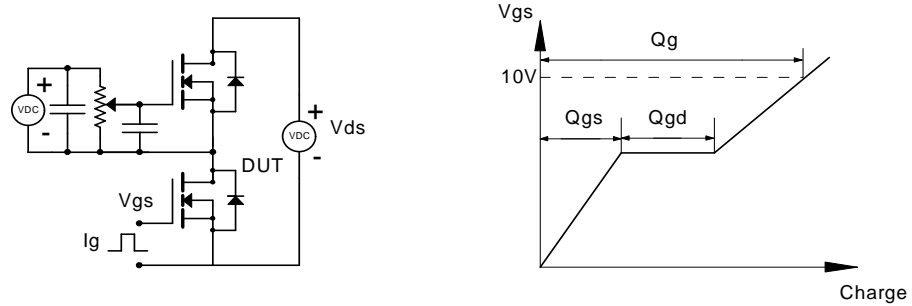
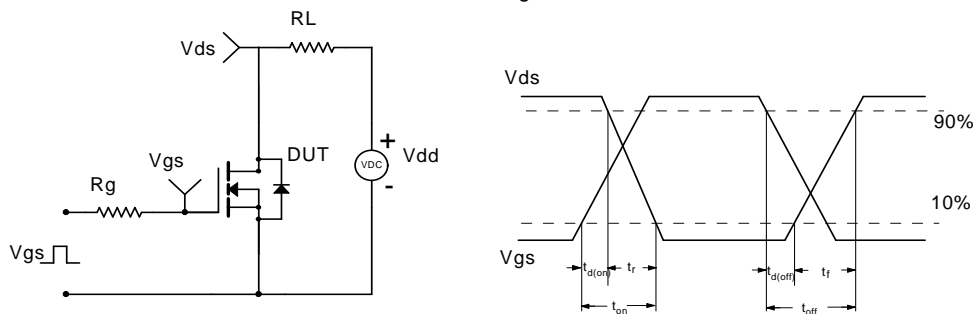


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

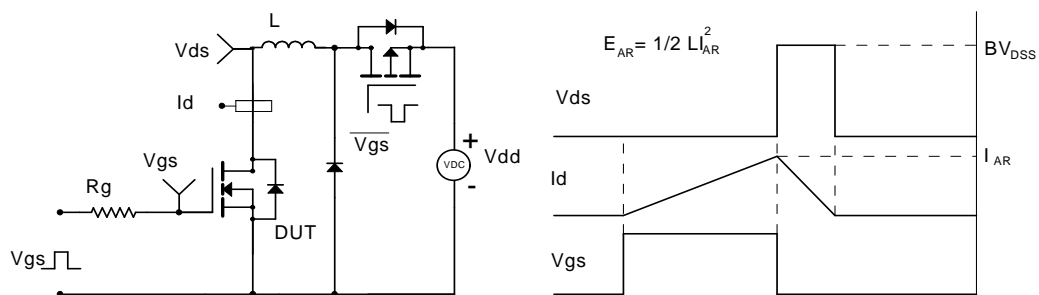
Gate Charge Test Circuit & Waveform



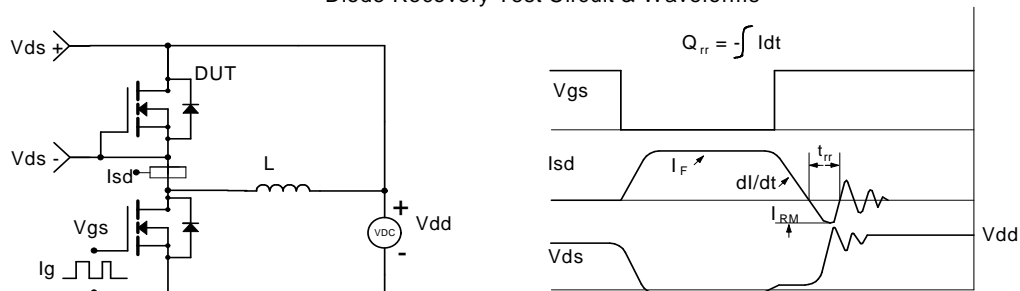
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-60V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-1.5	-2.1	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-12A T _J =125°C		91	115	mΩ
		V _{GS} =-4.5V, I _D =-8A		114	150	
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-12A		12		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.76	-1	V
I _S	Maximum Body-Diode Continuous Current ^G				-12	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-30V, f=1MHz	760	960	1160	pF
C _{oss}	Output Capacitance		60	86	120	pF
C _{rss}	Reverse Transfer Capacitance		20	38	55	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	3.5	7	10	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =-10V, V _{DS} =-30V, I _D =-12A	12	15.8	20	nC
Q _{g(4.5V)}	Total Gate Charge		5	7.4	9	nC
Q _{gs}	Gate Source Charge			3		nC
Q _{gd}	Gate Drain Charge			3.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-30V, R _L =2.5Ω, R _{GEN} =3Ω		9		ns
t _r	Turn-On Rise Time			10		ns
t _{D(off)}	Turn-Off DelayTime			25		ns
t _f	Turn-Off Fall Time			11		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-12A, dI/dt=100A/μs		27.5	35	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-12A, dI/dt=100A/μs		30		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allow s it.

B. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating g.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

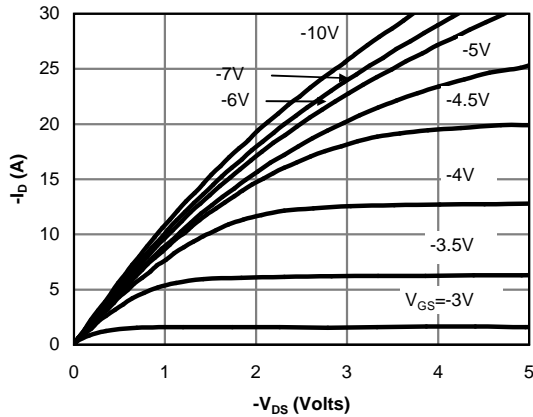


Fig 1: On-Region Characteristics (Note E)

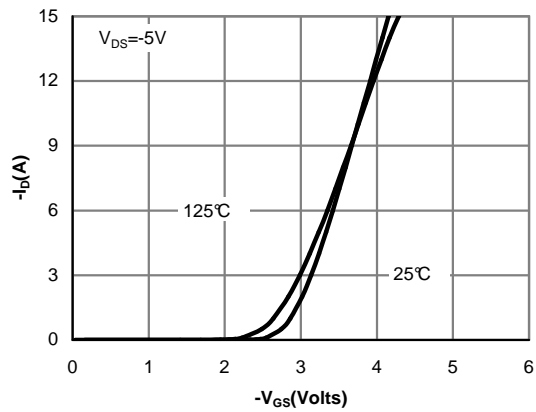


Figure 2: Transfer Characteristics (Note E)

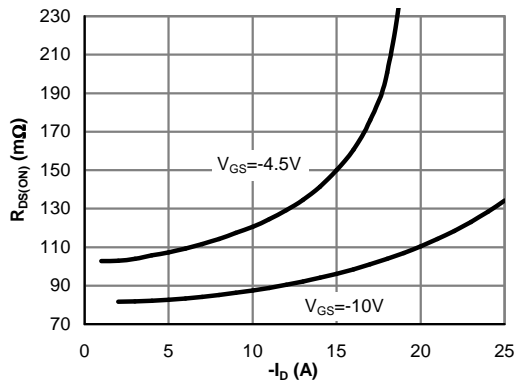


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

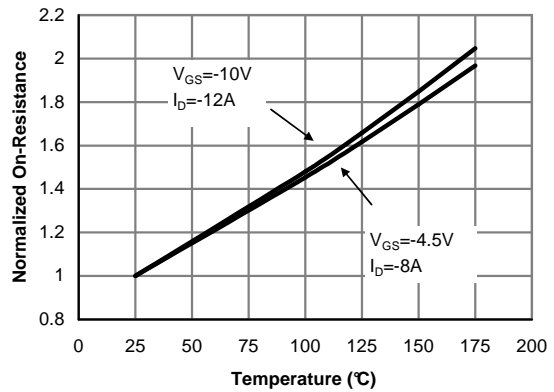


Figure 4: On-Resistance vs. Junction Temperature (Note E)

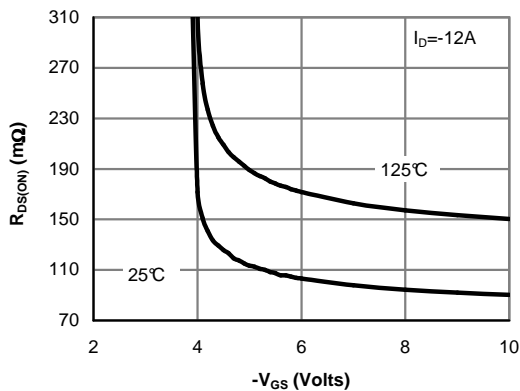


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

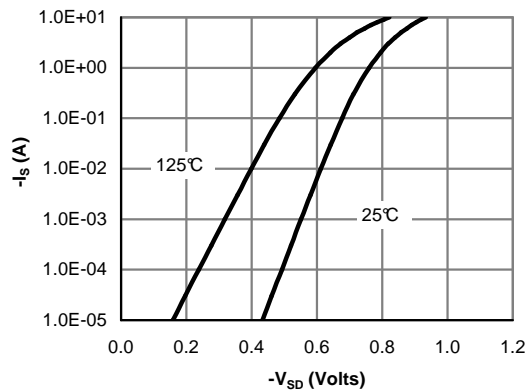


Figure 6: Body-Diode Characteristics (Note E)

P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

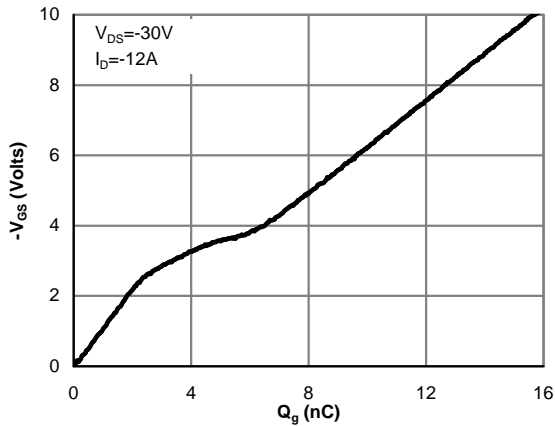


Figure 7: Gate-Charge Characteristics

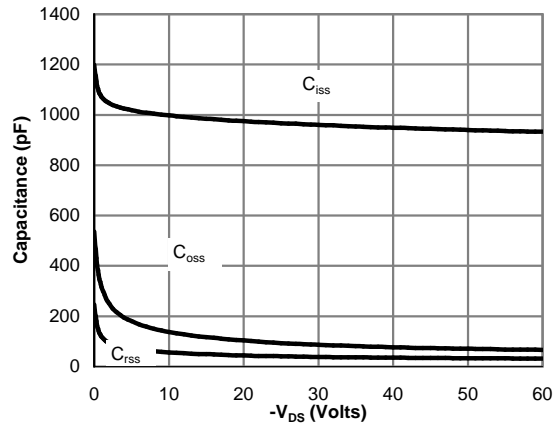


Figure 8: Capacitance Characteristics

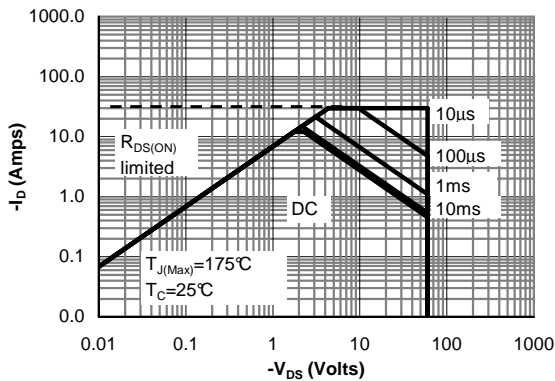


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

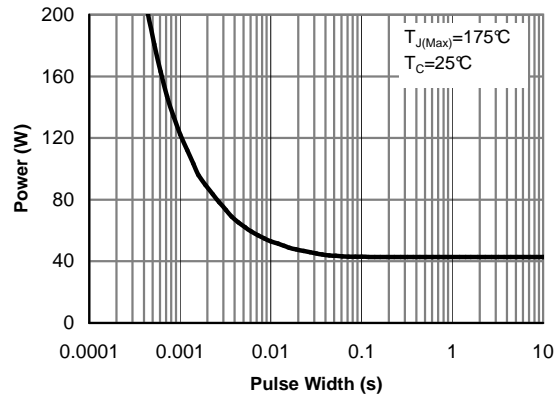


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

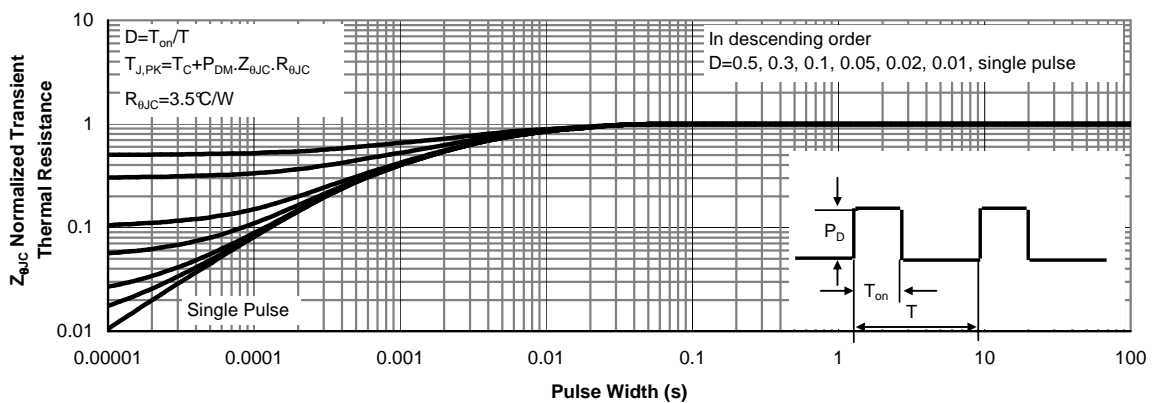


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

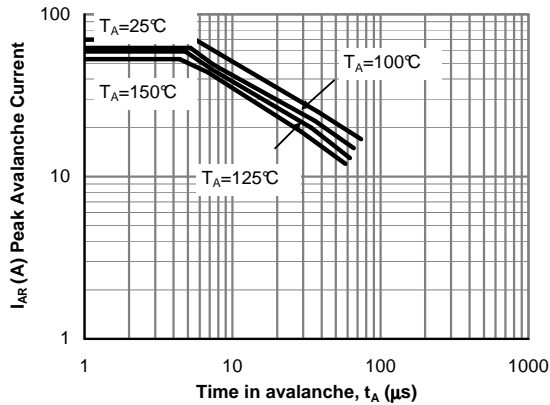


Figure 12: Single Pulse Avalanche capability (Note C)

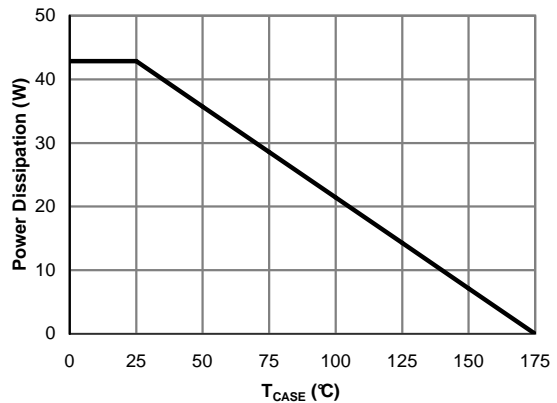


Figure 13: Power De-rating (Note F)

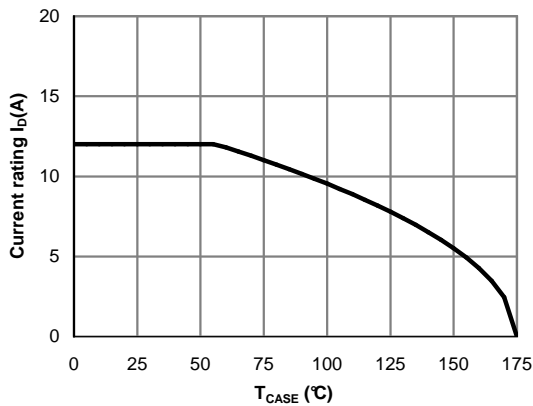


Figure 14: Current De-rating (Note F)

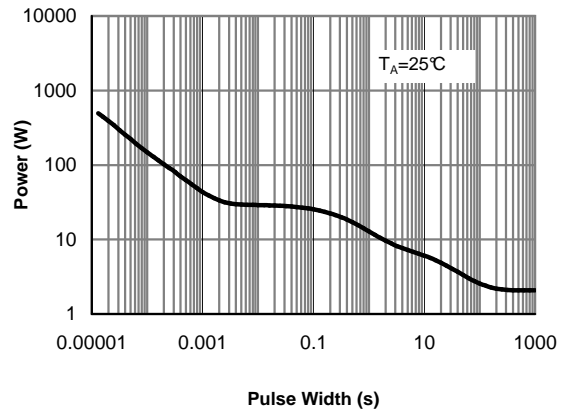


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

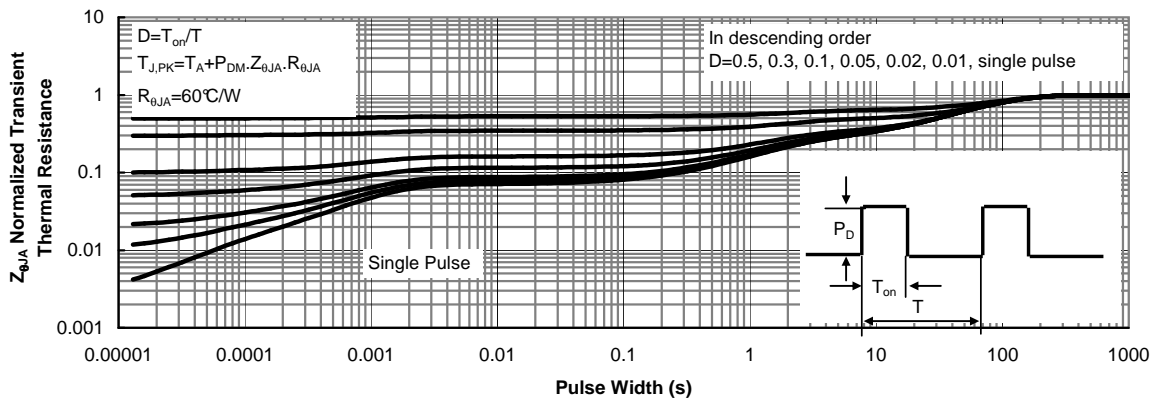
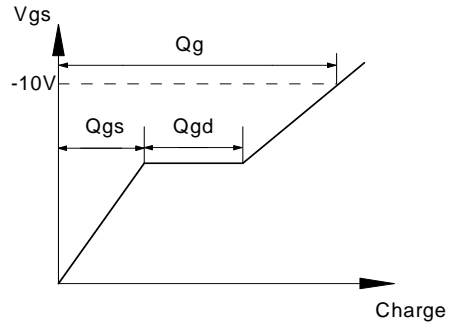
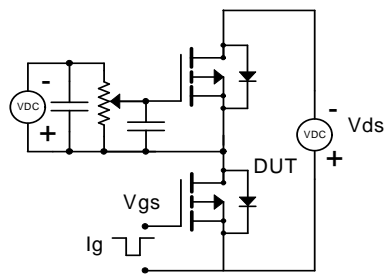
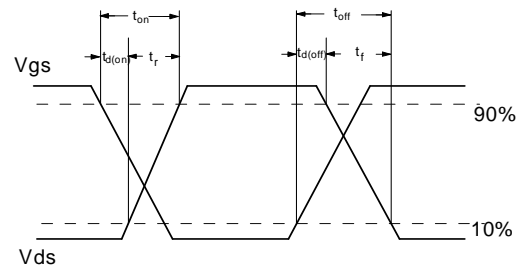
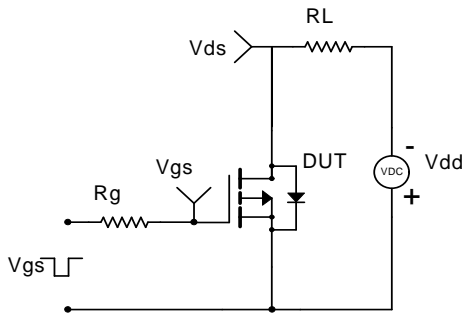


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

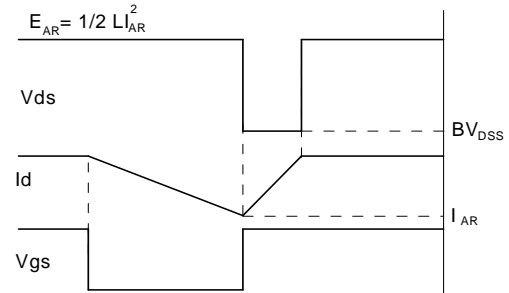
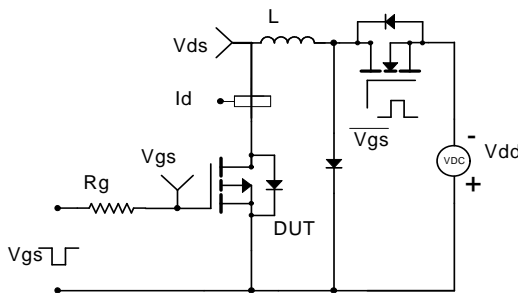
Gate Charge Test Circuit & Waveform



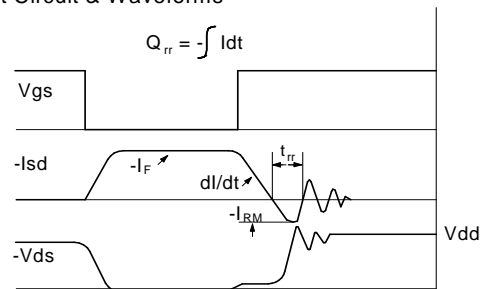
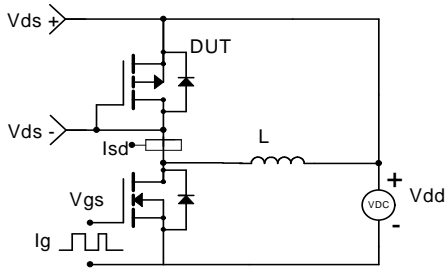
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