



THE DATASHEET OF AOD606



AOD606

Complementary Enhancement Mode Field Effect Transistor

General Description

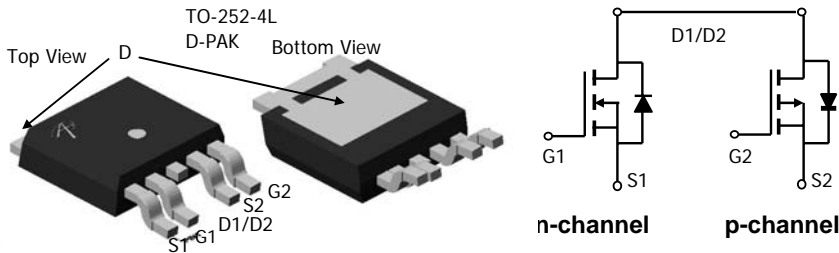
The AOD606 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

- RoHS Compliant
- Halogen Free*

Features

n-channel	p-channel
$V_{DS} (V) = 40V$	-40V
$I_D = 8A (V_{GS}=10V)$	-8A ($V_{GS} = -10V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 33 m Ω ($V_{GS}=10V$)	< 50 m Ω ($V_{GS} = -10V$)
< 47 m Ω ($V_{GS}=4.5V$)	< 70 m Ω ($V_{GS} = -4.5V$)

100% UIS Tested!



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^G	I_D	8	-8	A
$T_C=25^\circ C$		6.3	-6.3	
Pulsed Drain Current ^C	I_{DM}	30	-30	
Avalanche Current ^C	I_{AR}	12	14	A
Repetitive avalanche energy $L=0.3mH$ ^C	E_{AR}	21.6	29.4	mJ
Power Dissipation ^B	P_D	20	30	W
$T_C=25^\circ C$		10	15	
Power Dissipation ^A	P_{DSM}	1.6	1.7	W
$T_A=25^\circ C$		1	1.1	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	-55 to 175	$^\circ C$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	25	30	$^\circ C/W$
Maximum Junction-to-Ambient ^A		n-ch	66	80	$^\circ C/W$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	n-ch	7	7.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	17	25	$^\circ C/W$
Maximum Junction-to-Ambient ^A		p-ch	60	75	$^\circ C/W$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	p-ch	4	5	$^\circ C/W$

N-Channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=10\text{mA}$, $V_{GS}=0\text{V}$	40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.5	2.3	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=8\text{A}$		27	33	m Ω
		$T_J=125^\circ\text{C}$		39	52	
		$V_{GS}=4.5\text{V}$, $I_D=6\text{A}$		37	47	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=8\text{A}$		25		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				8	A
I_{SM}	Pulsed Body-Diode Current ^C				30	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$, $f=1\text{MHz}$		404		pF
C_{oss}	Output Capacitance			95		pF
C_{rss}	Reverse Transfer Capacitance			37		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		2.7		Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=8\text{A}$		9.2		nC
$Q_g(4.5\text{V})$	Total Gate Charge			4.5		nC
Q_{gs}	Gate Source Charge			1.6		nC
Q_{gd}	Gate Drain Charge			2.6		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $R_L=2.5\Omega$, $R_{GEN}=3\Omega$		3.5		ns
t_r	Turn-On Rise Time			6		ns
$t_{D(off)}$	Turn-Off Delay Time			13.2		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=8\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		22.9		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=8\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		18.3		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev5: Sep. 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

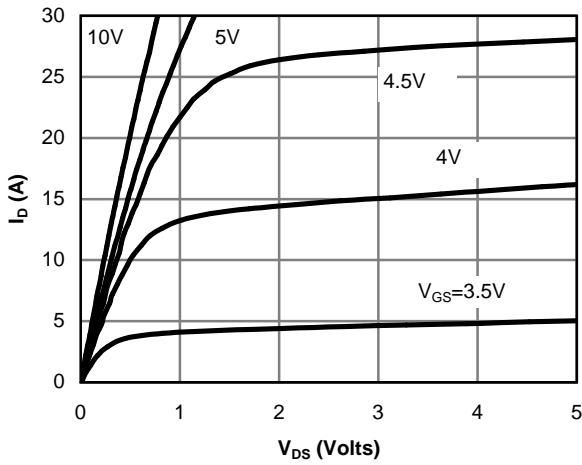


Fig 1: On-Region Characteristics

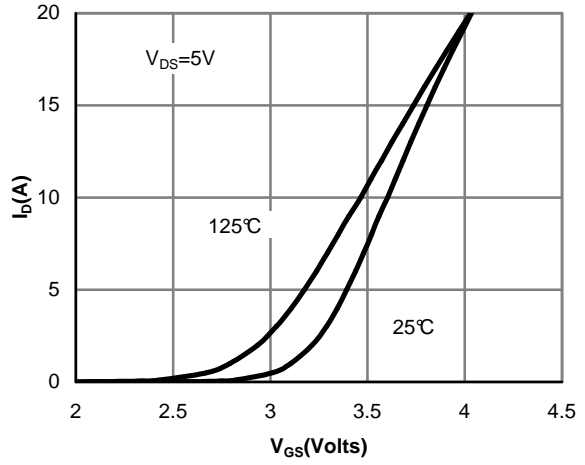


Figure 2: Transfer Characteristics

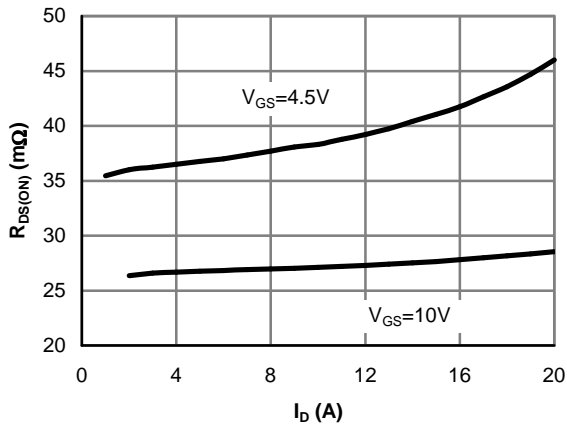


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

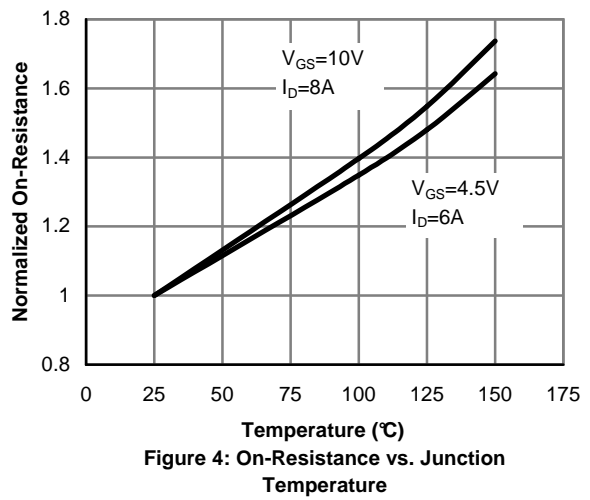


Figure 4: On-Resistance vs. Junction Temperature

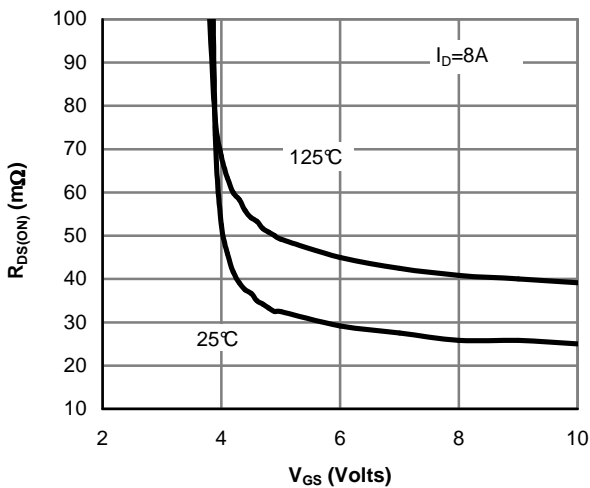


Figure 5: On-Resistance vs. Gate-Source Voltage

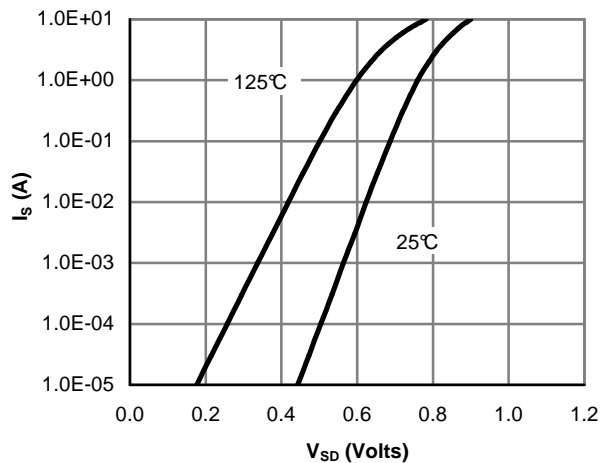


Figure 6: Body-Diode Characteristics

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

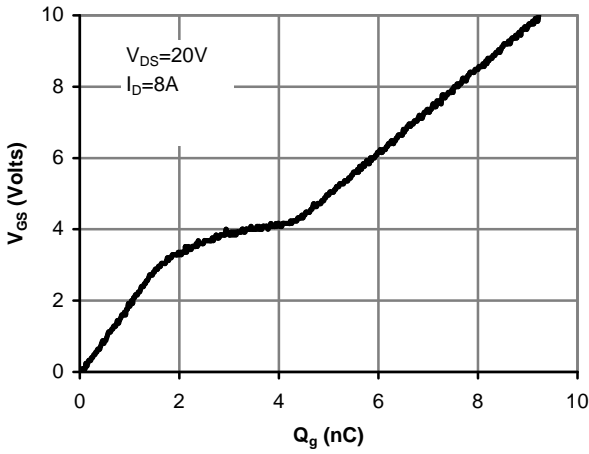


Figure 7: Gate-Charge Characteristics

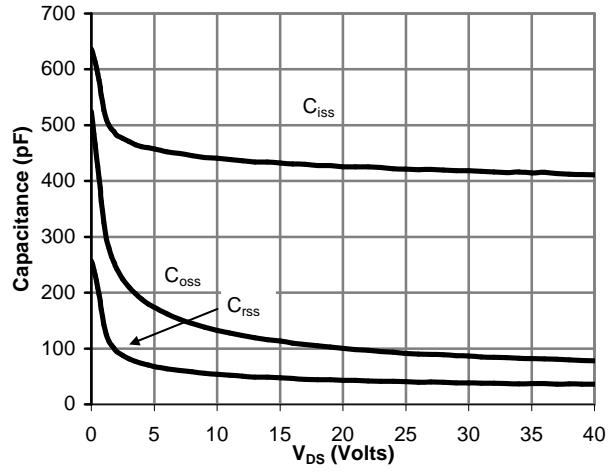


Figure 8: Capacitance Characteristics

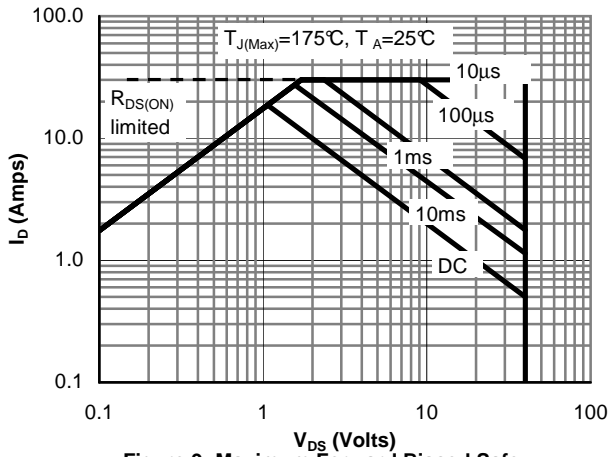


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

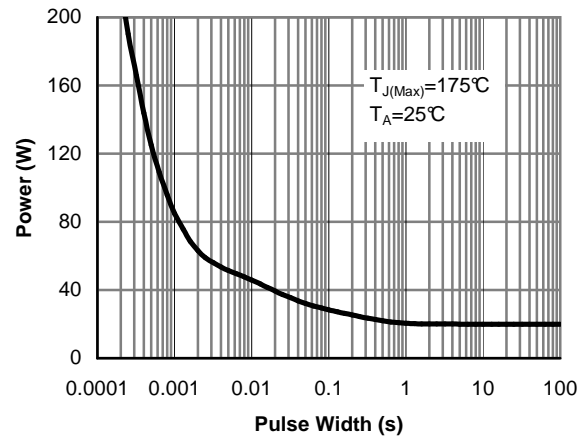


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

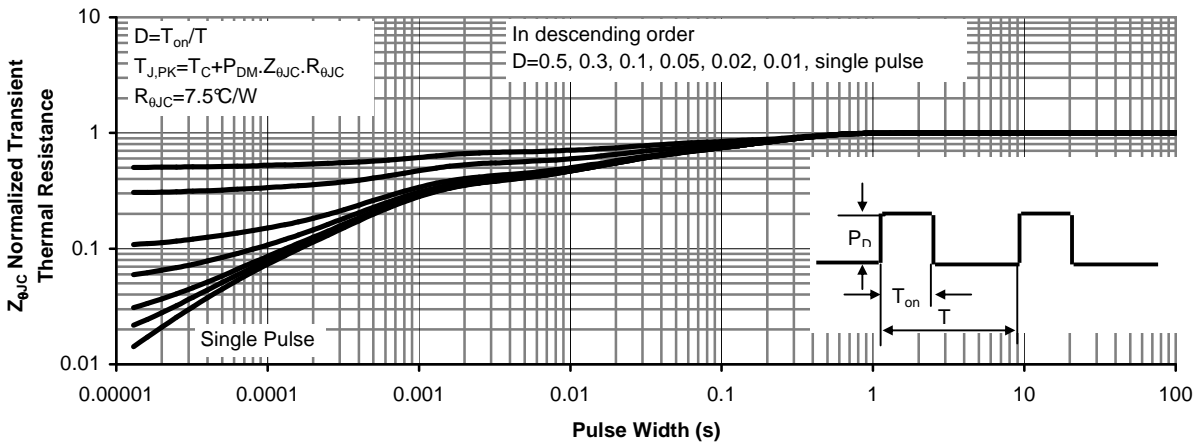


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

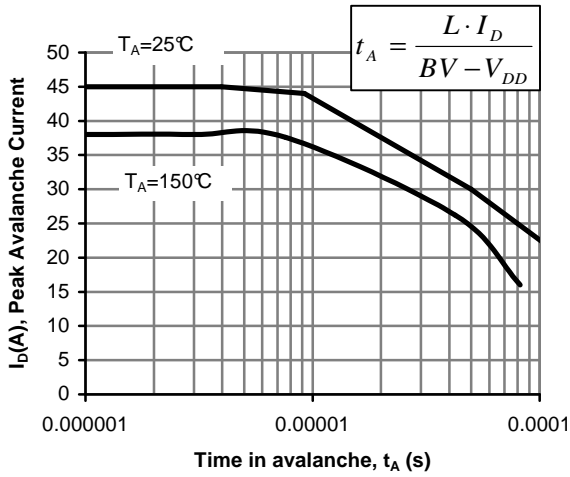


Figure 12: Single Pulse Avalanche capability

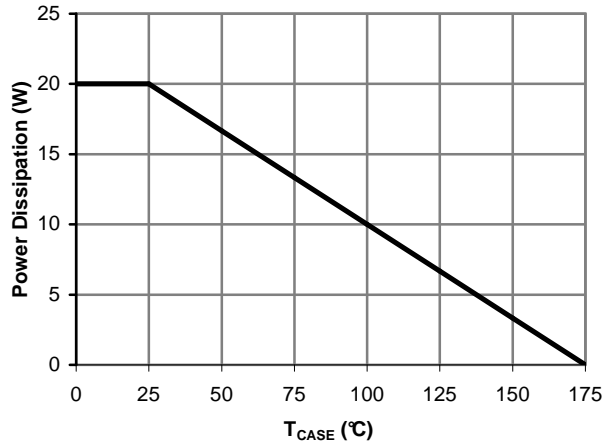


Figure 13: Power De-rating (Note B)

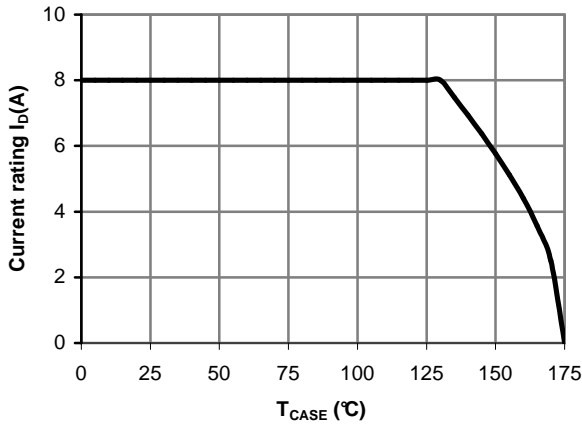


Figure 14: Current De-rating (Note B)

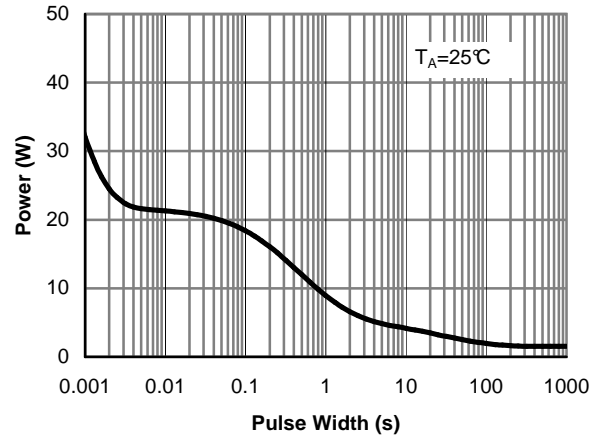


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

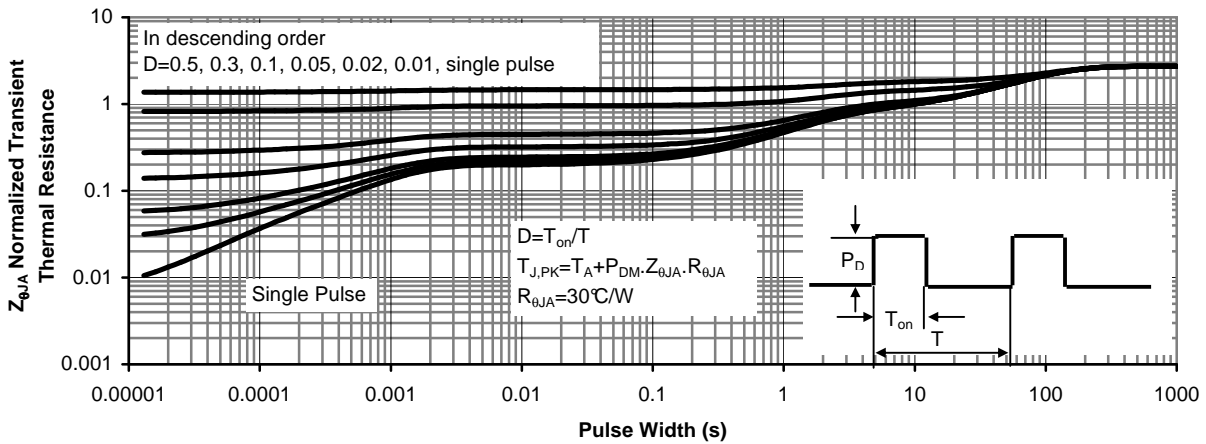


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

P-Channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-10\text{mA}, V_{GS}=0\text{V}$	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-32\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1.5	-1.8	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}, V_{DS}=-5\text{V}$	-30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}, I_D=-8\text{A}$ $T_J=125^\circ\text{C}$		35 62	50	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}, I_D=-4\text{A}$		55	70	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}, I_D=-8\text{A}$		16		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}, V_{GS}=0\text{V}$		-0.75	-1	V
I_S	Maximum Body-Diode Continuous Current				-8	A
I_{SM}	Pulsed Body-Diode Current ^C				-30	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=-20\text{V}, f=1\text{MHz}$		657		pF
C_{oss}	Output Capacitance			143		pF
C_{rss}	Reverse Transfer Capacitance			63		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		6.5		Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}, V_{DS}=-20\text{V}, I_D=-8\text{A}$		14.1		nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			7		nC
Q_{gs}	Gate Source Charge			2.2		nC
Q_{gd}	Gate Drain Charge			4.1		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}, V_{DS}=-20\text{V}, R_L=2.5\Omega,$ $R_{GEN}=3\Omega$		8		ns
t_r	Turn-On Rise Time			12.2		ns
$t_{D(off)}$	Turn-Off DelayTime			24		ns
t_f	Turn-Off Fall Time			12.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-8\text{A}, dI/dt=100\text{A}/\mu\text{s}$		23.2		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-8\text{A}, dI/dt=100\text{A}/\mu\text{s}$		18.2		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev5: Sep. 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

P-Channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

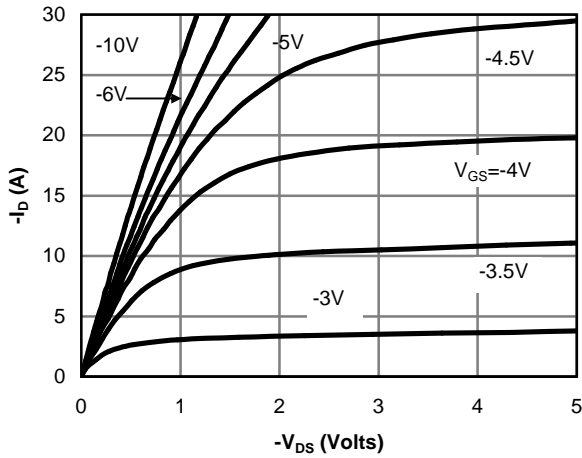


Fig 1: On-Region Characteristics

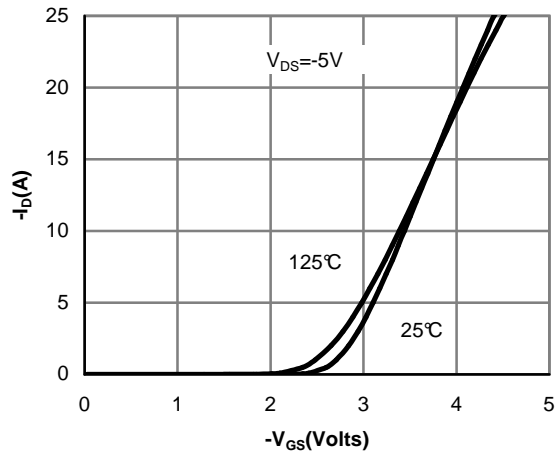


Figure 2: Transfer Characteristics

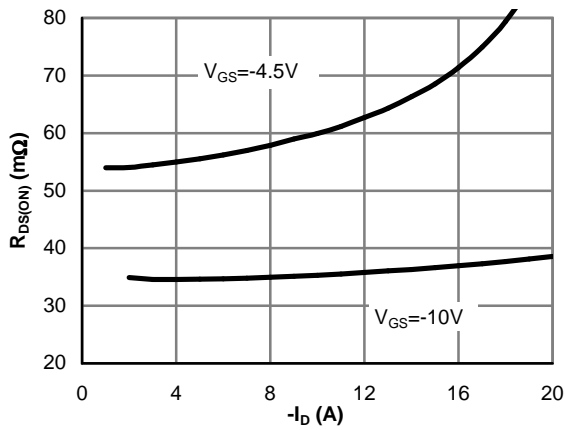


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

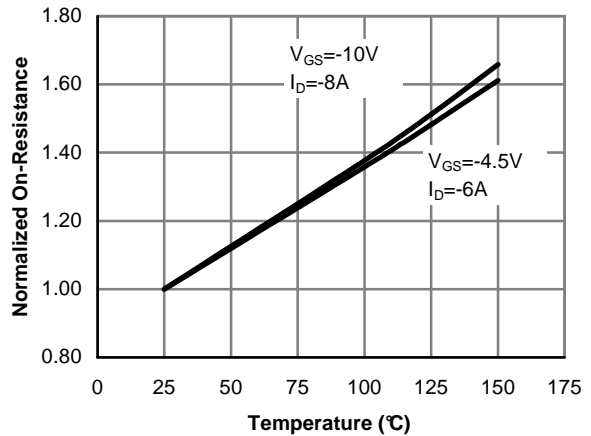


Figure 4: On-Resistance vs. Junction Temperature

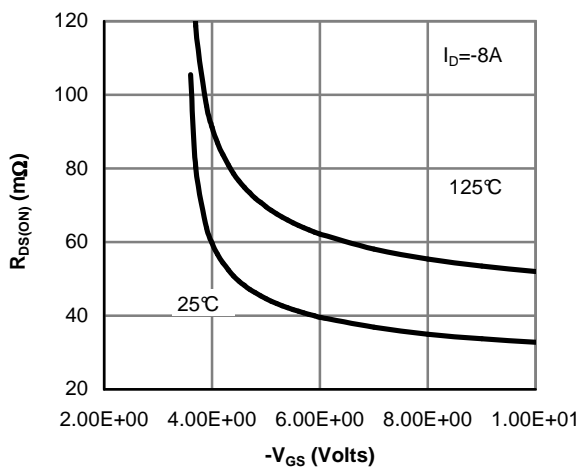


Figure 5: On-Resistance vs. Gate-Source Voltage

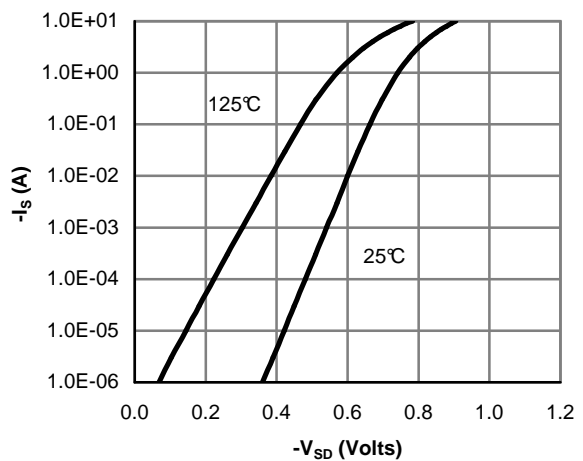


Figure 6: Body-Diode Characteristics

P-Channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

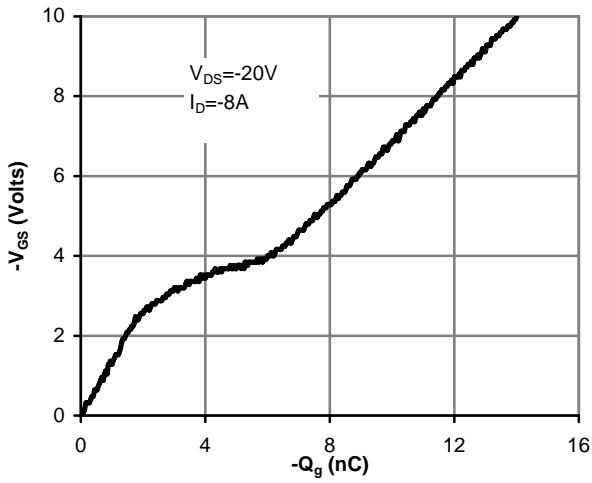


Figure 7: Gate-Charge Characteristics

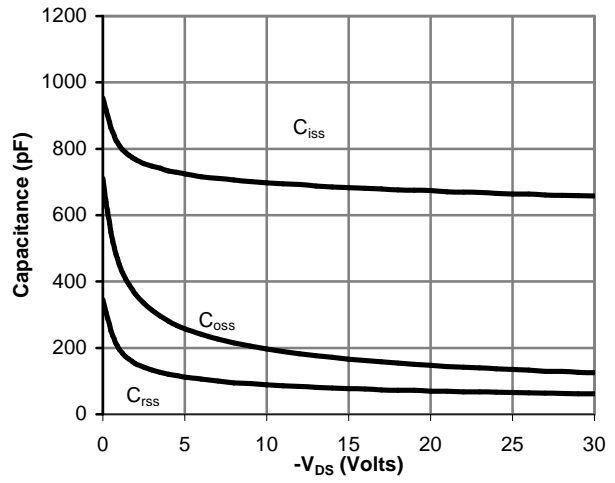


Figure 8: Capacitance Characteristics

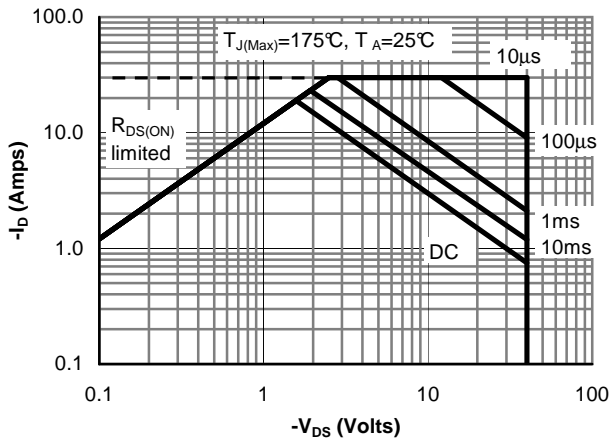


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

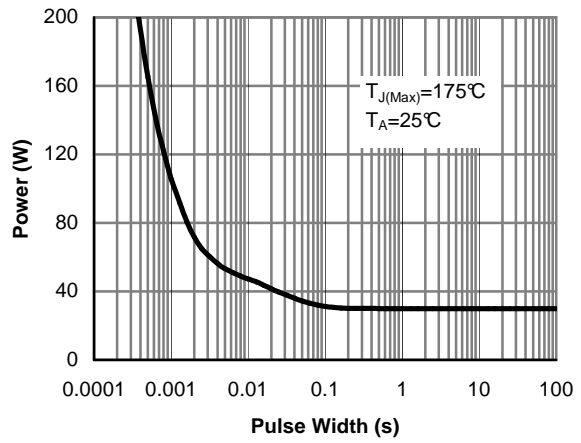


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

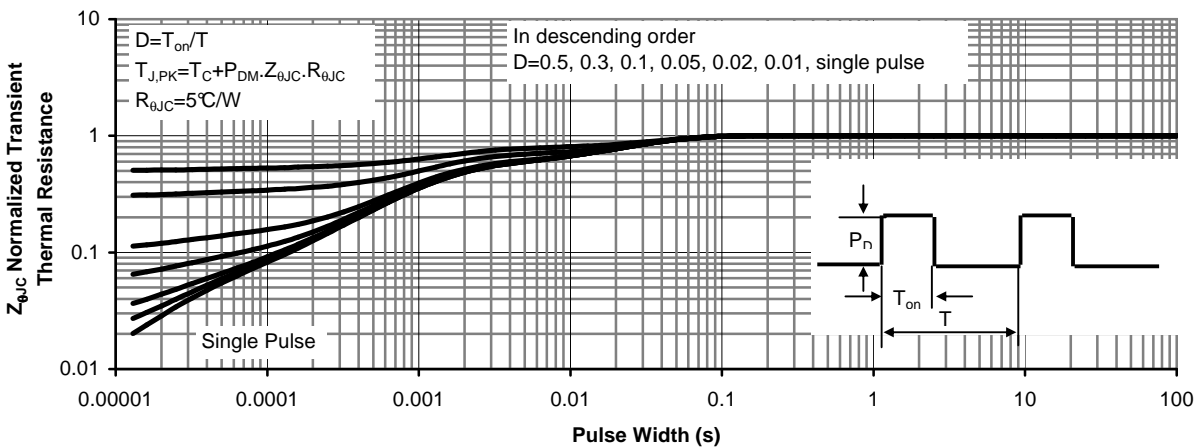


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

P-Channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

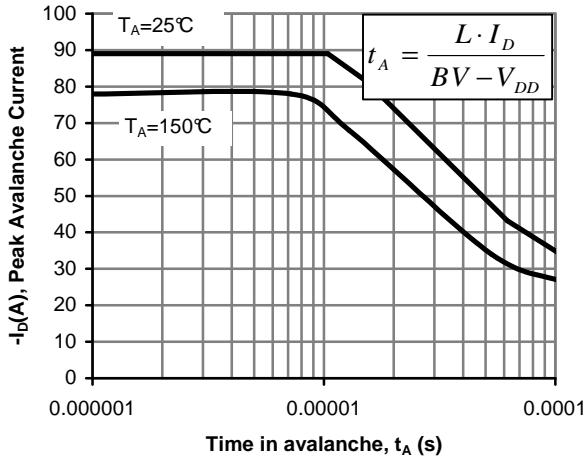


Figure 12: Single Pulse Avalanche capability

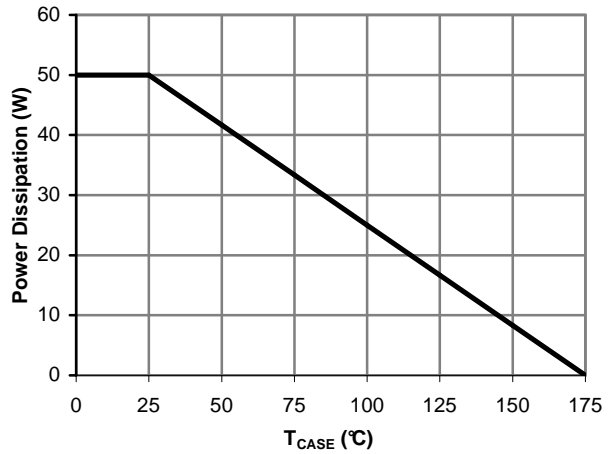


Figure 13: Power De-rating (Note B)

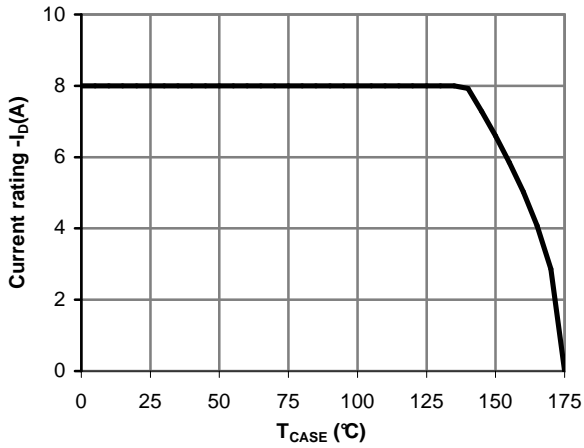


Figure 14: Current De-rating (Note B)

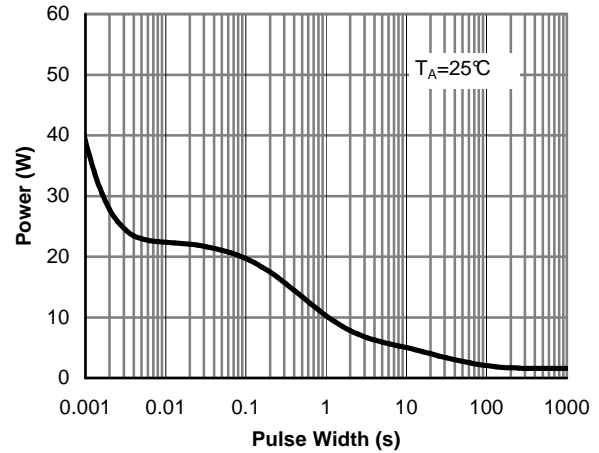


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

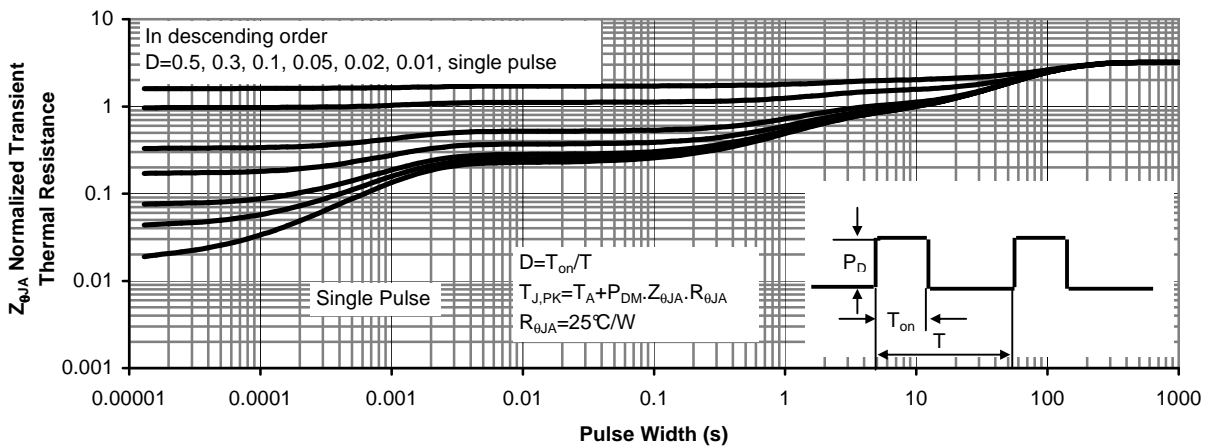
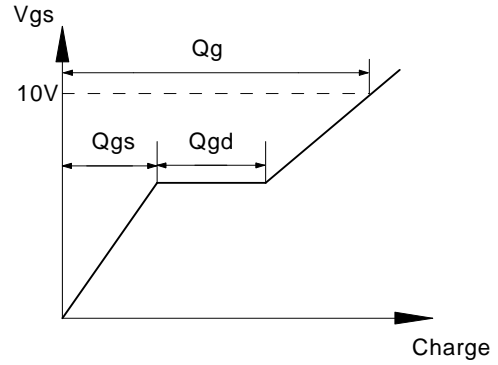
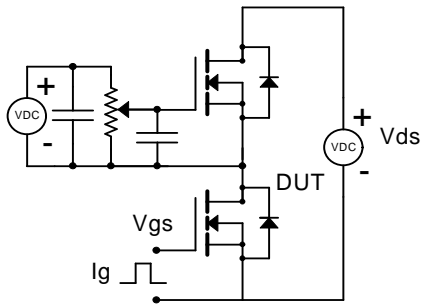
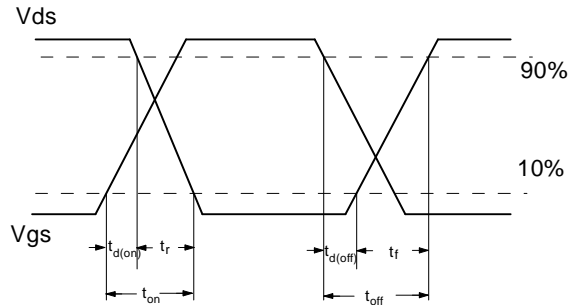
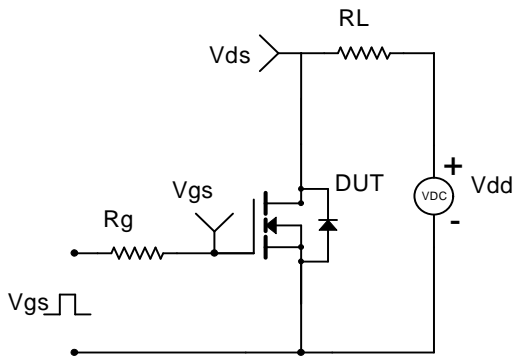


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

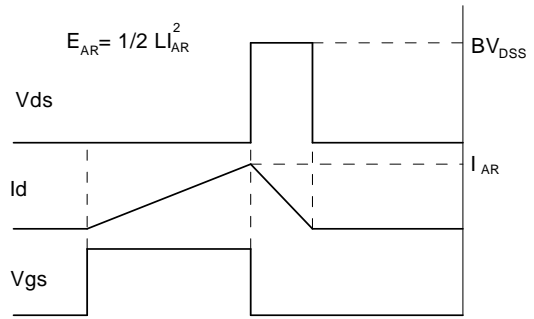
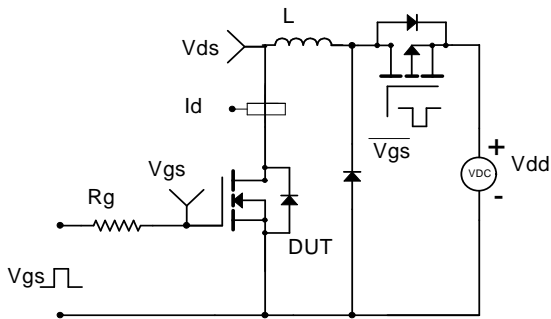
Gate Charge Test Circuit & Waveform



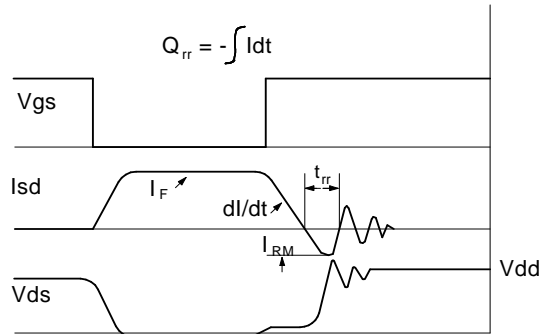
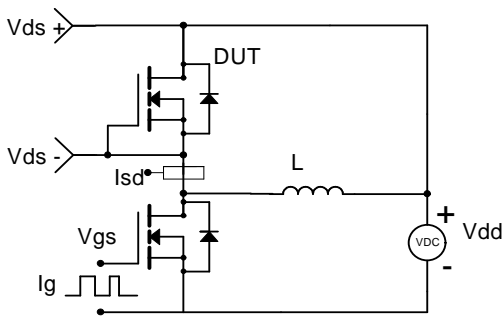
Resistive Switching Test Circuit & Waveforms



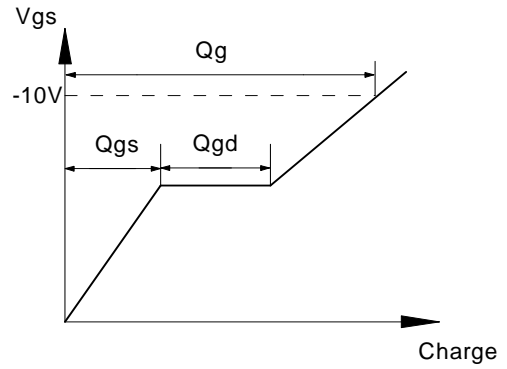
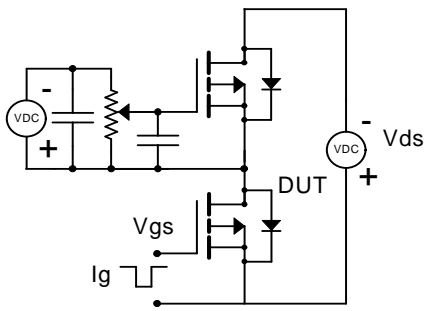
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



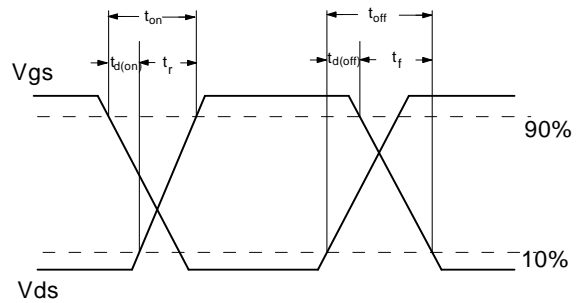
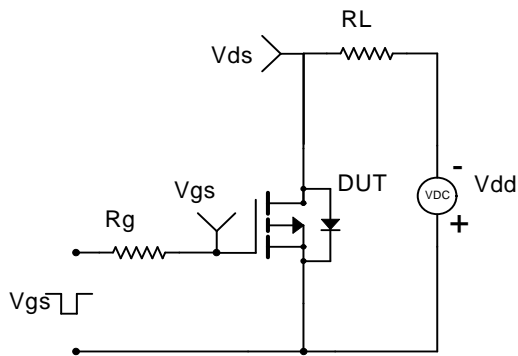
Diode Recovery Test Circuit & Waveforms



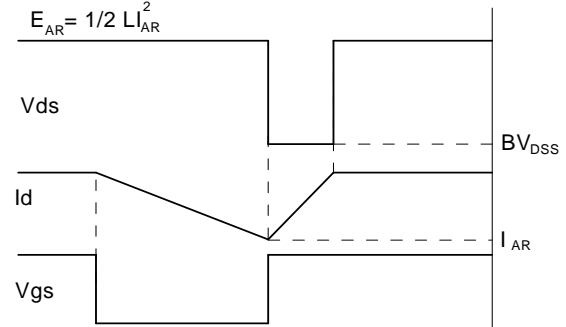
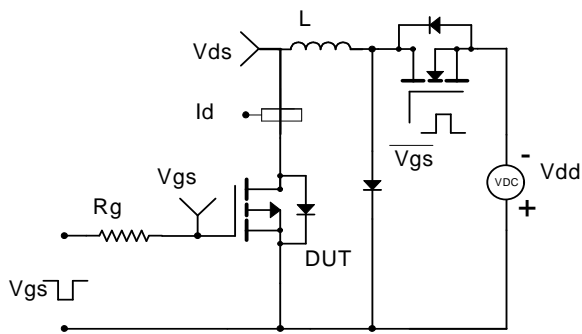
Gate Charge Test Circuit & Waveform



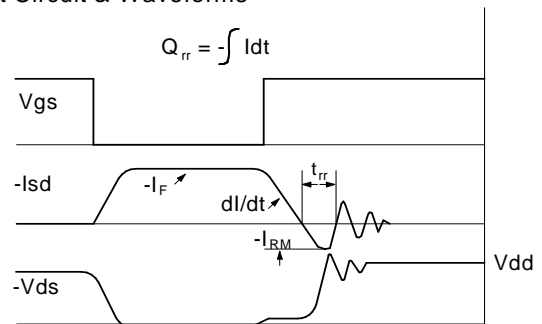
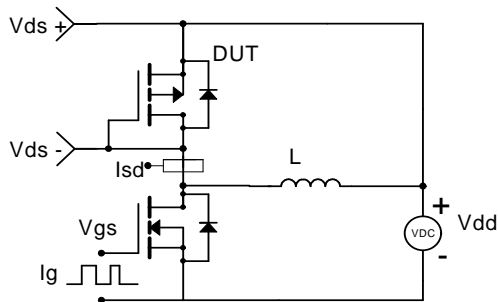
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View AOD606 on WIN SOURCE](#)
- ⊖ [Alpha & Omega Semiconductor Inc. Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management