THE DATASHEET OF

TPS77601PWP

TPS775xx with $\overline{\text{RESET}}$ Output, TPS776xx with PG Output FAST-TRANSIENT-RESPONSE 500mA LOW-DROPOUT VOLTAGE REGULATORS

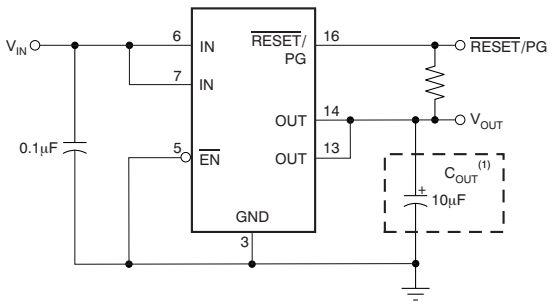
FEATURES

- **Open Drain Power-On Reset with 200ms Delay (TPS775xx)**
- **Open Drain Power Good (TPS776xx)**
- **500mA Low-Dropout Voltage Regulator**
- **Available in Fixed Output and Adjustable Versions**
- **Dropout Voltage to 169mV (Typ) at 500mA (TPS77x33)**
- **Ultralow 85μA Typical Quiescent Current**
- **Fast Transient Response**
- **2% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Packages**
- **Thermal Shutdown Protection**

APPLICATIONS

- **FPGA Power**
- **DSP Core and I/O Voltages**

Typical Application Circuit (Fixed Voltage Options)



DESCRIPTION

The TPS775xx and TPS776xx devices are designed to have a fast transient response and be stable with a 10μF low ESR capacitor. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 169mV at an output current of 500mA for the TPS77x33) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85μA over the full range of output current, 0mA to 500mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 1μA at T_J = +25°C.

The $\overline{\text{RESET}}$ output of the TPS775xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS775xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

Power good (PG) of the TPS776xx is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS775xx and TPS776xx are offered in 1.5V, 1.6V (TPS77516 only), 1.8V, 2.5V, 2.8V (TPS77628 only), and 3.3V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5V to 5.5V for the TPS77501 and 1.2V to 5.5V for the TPS77601). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS775xx and TPS776xx families are available in 8-pin SOIC and 20-pin TSSOP packages.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS775**xxyyyz**, TPS776**xxyyyz**	**XX** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Custom fixed output voltages are available; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

Over operating temperature range (unless otherwise noted)(1)

PARAMETER	TPS775xx, TPS776xx	UNIT
Input voltage range, V_{IN}(2)	–0.3 to +13.5	V
Voltage range at $\overline{EN}$	–0.3 to +16.5	V
Maximum $\overline{RESET}$ voltage (TPS775xx)	16.5	V
Maximum PG voltage (TPS776xx)	16.5	V
Peak output current	Internally limited	
Voltage range at OUT, FB	7	V
Continuous total power dissipation	See Dissipation Ratings Table	
Operating junction temperature range, T_J	–40 to +125	°C
Storage junction temperature range , T_{STG}	–65 to +150	°C
ESD rating, HBM	2	kV

(1) Stresses above these ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) All voltages are with respect to network terminal ground.

DISSIPATION RATINGS

BOARD	PACKAGE	AIRFLOW (CFM)	T_A < +25°C (mW)	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C (mW)	T_A = +85°C (mW)
—	D	0	568	5.68mW/°C	312	227
		250	904	9.04mW/°C	497	362
Low-K(1)	PWP	0	2350	23.5mW/°C	1300	940
		300	3460	34.6mW/°C	1900	1400
High-K(2)	PWP	0	2380	23.8mW/°C	1300	952
		300	5790	57.9mW/°C	3200	2300

(1) This parameter is measured with the recommended copper heat sink pattern on a 1-layer, 5in × 5in printed circuit board (PCB), 1-ounce copper, 2in × 2in coverage (4in^2).
(2) This parameter is measured with the recommended copper heat sink pattern on a 8-layer, 1.5in × 2in PCB, 1-ounce copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9in^2) and layers 3 and 6 at 100% coverage (6in^2). For more information, refer to TI technical brief SLMA002.

ELECTRICAL CHARACTERISTICS

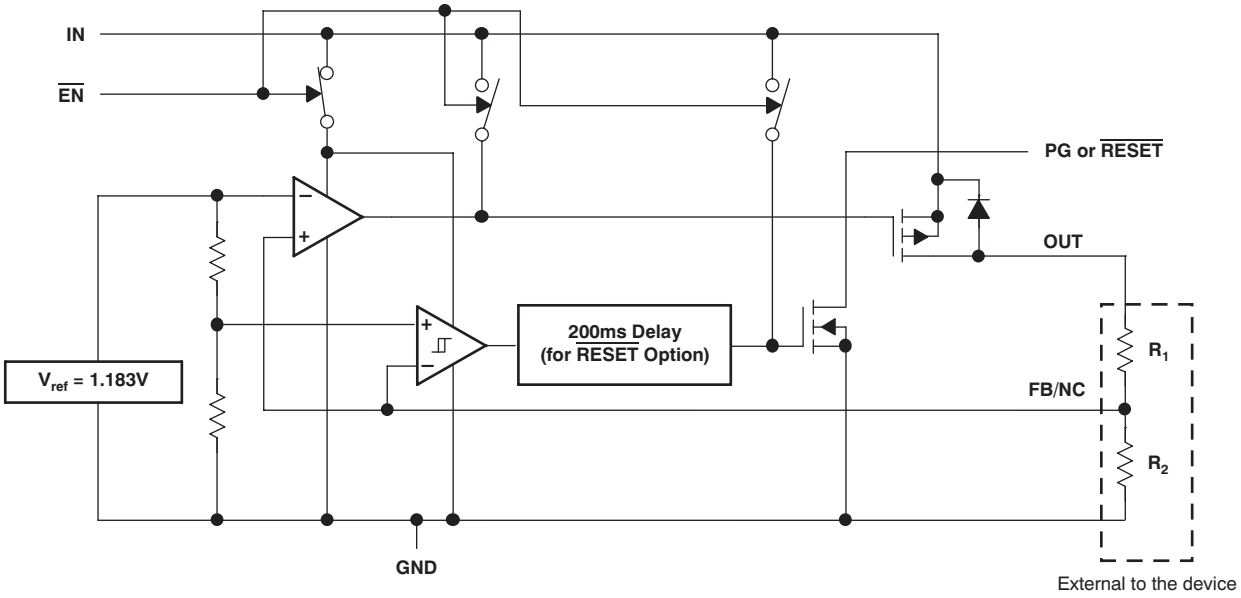
Over recommended operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 1V; I_{OUT} = 1mA, $V_{\overline{EN}}$ = 0V, C_{OUT} = 10µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.7		10	V
V_{OUT}	Output voltage range	TPS77501		1.5		5.5	V
		TPS77601		1.2		5.5	V
V_{OUT}	Accuracy		V_{OUT} + 1V ≤ V_{IN} ≤ 10V(1) 10µA < I_{OUT} < 500mA	–2.0		+2.0	%
I_{GND}	Ground pin current		I_{OUT} = 10mA		85		µA
			I_{OUT} = 500mA			125	
ΔV_{OUT}%/ ΔV_{IN}	Output voltage line regulation		V_{OUT} + 1V ≤ V_{IN} ≤ 10V(1)		0.01		%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation				3		mV
V_N	Output noise voltage BW = 200Hz to 100kHz	TPS77x18	I_C = 500mA, C_{OUT} = 10µF		53		μV_{RMS}
V_{DO}	Dropout voltage(2)	TPS77628	I_{OUT} = 500mA		285	410	mV
		TPS77533	I_{OUT} = 500mA		169	287	mV
		TPS77633	I_{OUT} = 500mA		169	287	mV
I_{CL}	Output current limit		V_{OUT} = 0V	1.2	1.6	1.9	A
T_{SD}	Shutdown temperature				150		°C
T_J	Operating junction temperature range			–40		+125	°C
I_{STBY}	Standby current		$\overline{EN}$ = V_{IN}, at T_J = +25°C, 2.7V < V_{IN} < 10V		1		µA
			$\overline{EN}$ = V_{IN}, 2.7V < V_{IN} < 10V			10	
I_{FB}	FB input current	TPS77x01	FB = 1.5V		2		nA
$V_{EN(HI)}$	High-level enable input voltage			1.7			V
$V_{EN(LO)}$	Low-level enable input voltage					0.9	V
PSRR	Power-supply ripple rejection		f = 100Hz, C_{OUT} = 10µF		60		dB
RESET (TPS775xx)	Minimum input voltage for valid $\overline{RESET}$		$I_{OUT(RESET)}$ = 300µA		1.1		V
	Trip threshold voltage		V_{OUT} decreasing	92		98	$\%V_{OUT}$
	Hysteresis voltage		Measured at V_{OUT}		0.5		$\%V_{OUT}$
	Output low voltage		V_{IN} = 2.7V, $I_{OUT(RESET)}$ = 1mA		0.15	0.4	V
	Leakage current		$V_{(RESET)}$ = 5V			1	µA
	RESET time-out delay				200		ms
PG (TPS776xx)	Minimum input voltage for valid PG		$I_{OUT(PG)}$ = 300µA		1.1		V
	Trip threshold voltage		V_{OUT} decreasing	92		98	$\%V_{OUT}$
	Hysteresis voltage		Measured at V_{OUT}		0.5		$\%V_{OUT}$
	Output low voltage		V_{IN} = 2.7V, $I_{OUT(PG)}$ = 1mA		0.15	0.4	V
	Leakage current		$V_{(PG)}$ = 5V			1	µA
	Input current ($\overline{EN}$)		$\overline{EN}$ = 0V	–1	0	1	µA
			$\overline{EN}$ = V_{IN}	–1		1	

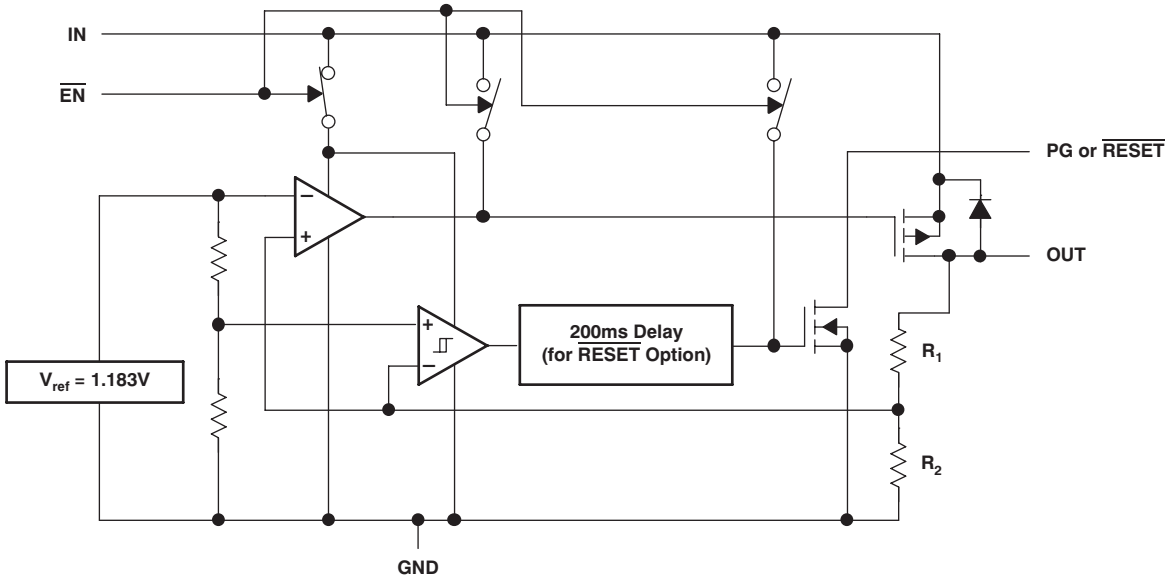
(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7V, whichever is greater.
(2) V_{DO} is not measured for fixed output versions with $V_{OUT(NOM)}$ < 2.8 V because mimimum V_{IN} = 2.7V.

FUNCTIONAL BLOCK DIAGRAMS

Adjustable Voltage Versions

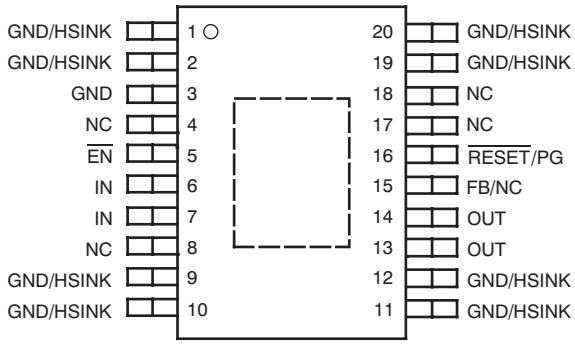


Fixed Voltage Versions



PIN CONFIGURATIONS

TSSOP-20
PWP
(TOP VIEW)



SOIC-8
D
(TOP VIEW)

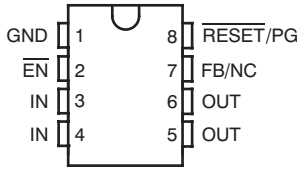
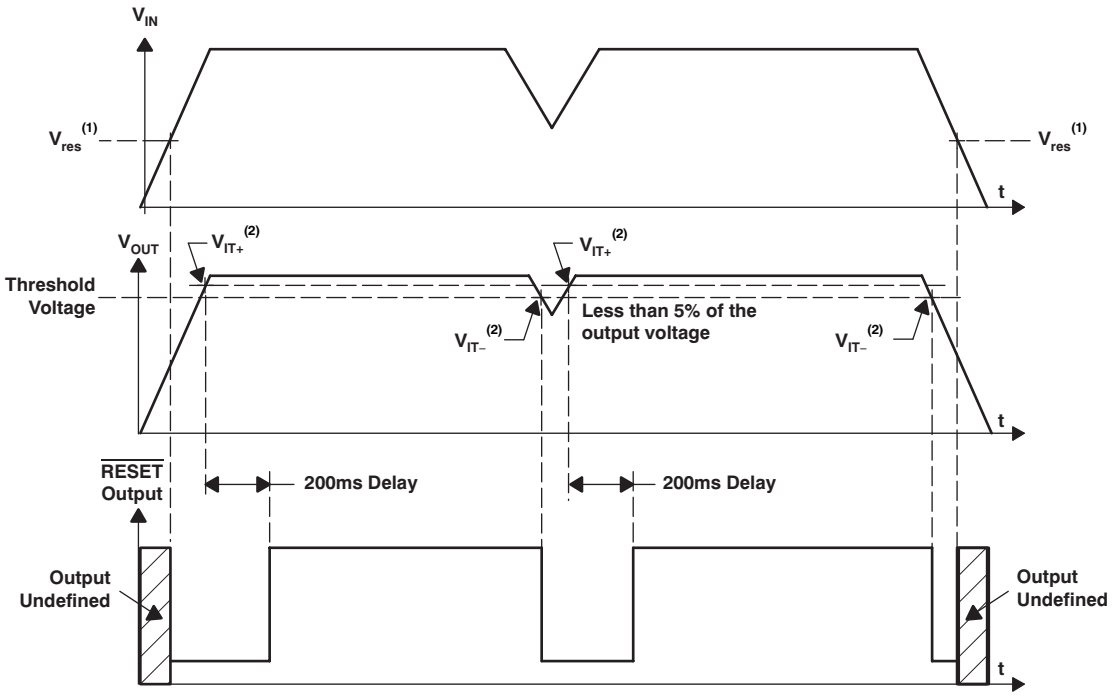


Table 1. PIN DESCRIPTIONS

TPS775xx, TPS776xx			
NAME	SOIC-8 (D) PIN NO.	TSSOP-20 (PWP) PIN NO.	DESCRIPTION
$\overline{EN}$	2	5	Negative polarity enable ($\overline{EN}$) input
FB	7	15	Adjustable voltage version only; feedback voltage for setting output voltage of the device. Not internally connected on adjustable versions.
GND	1	1, 2, 3, 9, 10, 11, 12, 19, 20	Ground
IN	3, 4	6, 7	Input voltage
OUT	5, 6	13, 14	Regulated output voltage
$\overline{RESET}$	8	16	TPS775xx devices only; open-drain $\overline{RESET}$ output.
PG	8	16	TPS776xx devices only; open-drain power-good (PG) output.
NC	—	4, 8, 17, 18	No internal connection
PAD/TAB	—	—	Should be soldered to ground plane and used for heat sinking.

TPS775xx $\overline{\text{RESET}}$ Timing Diagram



(1) V_{res} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

(2) V_{IT}: Trip voltage is typically 5% lower than the output voltage (95% V_{OUT}). V_{IT-} to V_{IT+} is the hysteresis voltage.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE NO.
V_{OUT}	Output Voltage	vs Output Current	Figure 3, Figure 4, Figure 5
		vs Free-Air Temperature	Figure 6, Figure 7, Figure 8
		vs Time	Figure 20
I_{GND}	Ground Current	vs Free-Air Temperature	Figure 9
PSRR	Power-Supply Ripple Rejection	vs Frequency	Figure 10
	Output Spectral Noise Density	vs Frequency	Figure 11
Z_{OUT}	Output Impedance	vs Frequency	Figure 12
V_{DO}	Dropout Voltage	vs Input Voltage	Figure 13
		vs Free-Air Temperature	Figure 14
V_{IN}	Input Voltage (Min)	vs Output Voltage	Figure 15
LINE	Line Transient Response		Figure 16, Figure 18
LOAD	Load Transient Response		Figure 17, Figure 19
ESR	Equivalent Series Resistance	vs Output Current	Figure 22, Figure 23

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

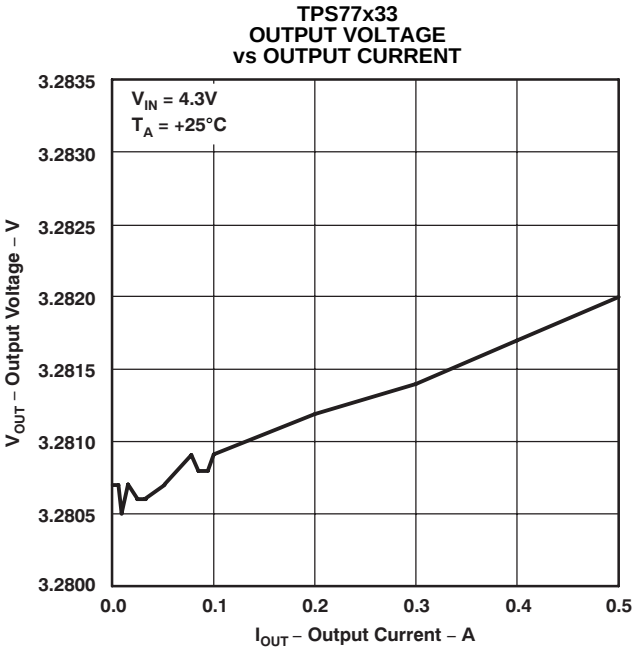


Figure 3.

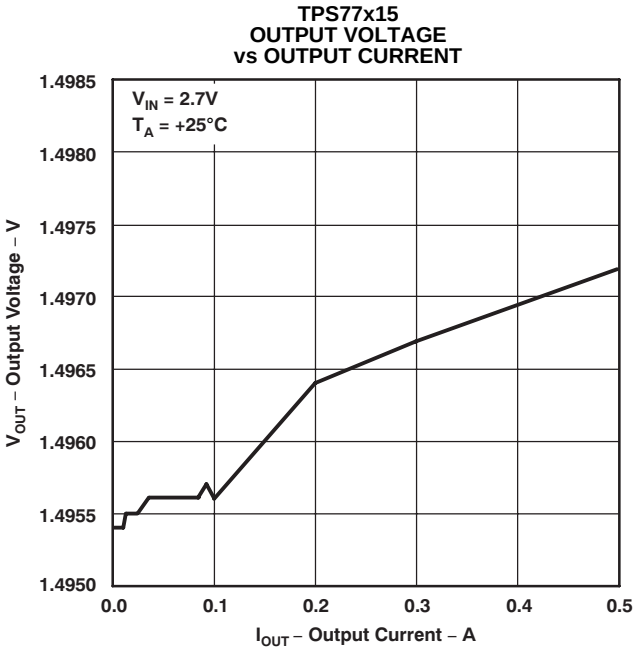


Figure 4.

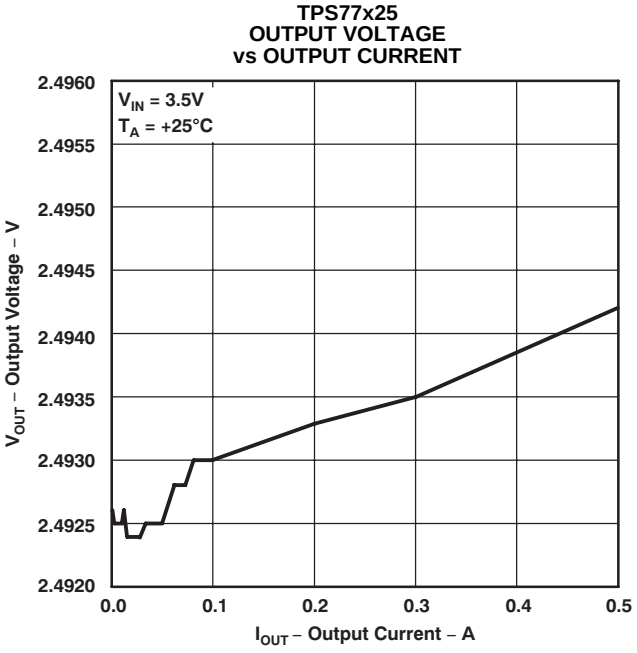


Figure 5.

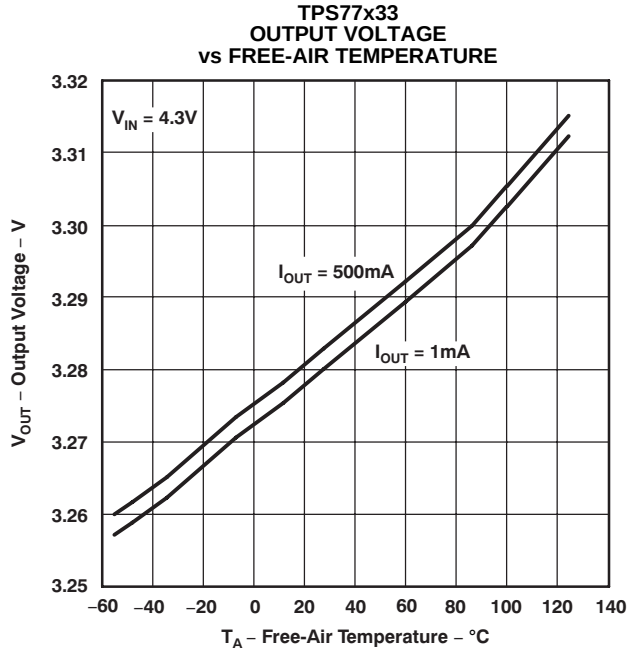


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

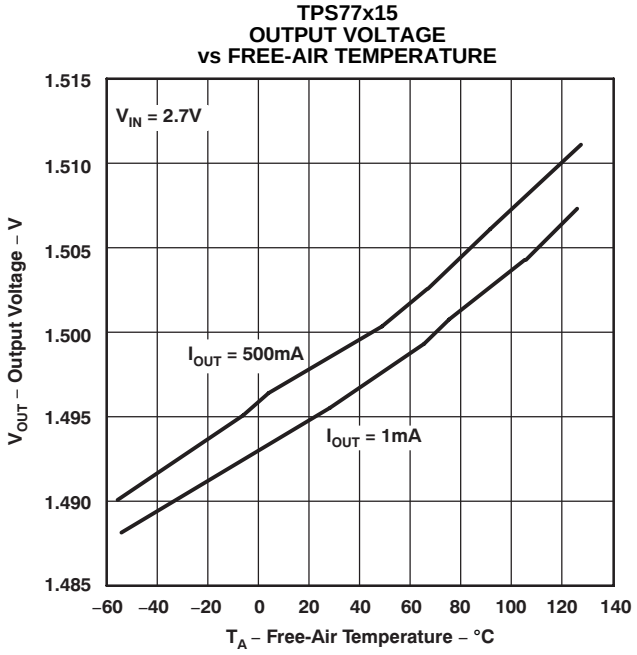


Figure 7.

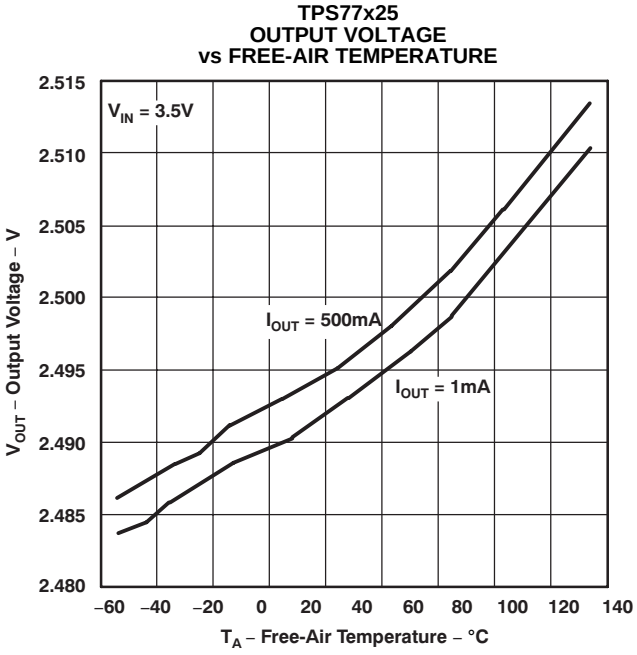


Figure 8.

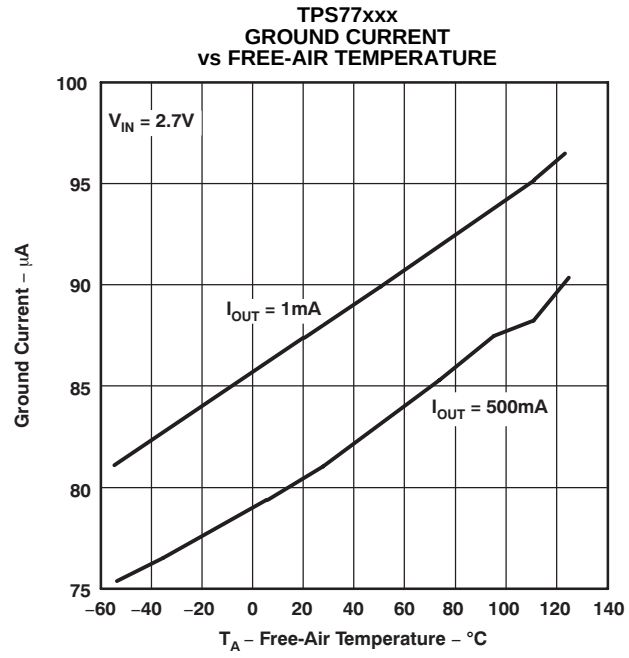


Figure 9.

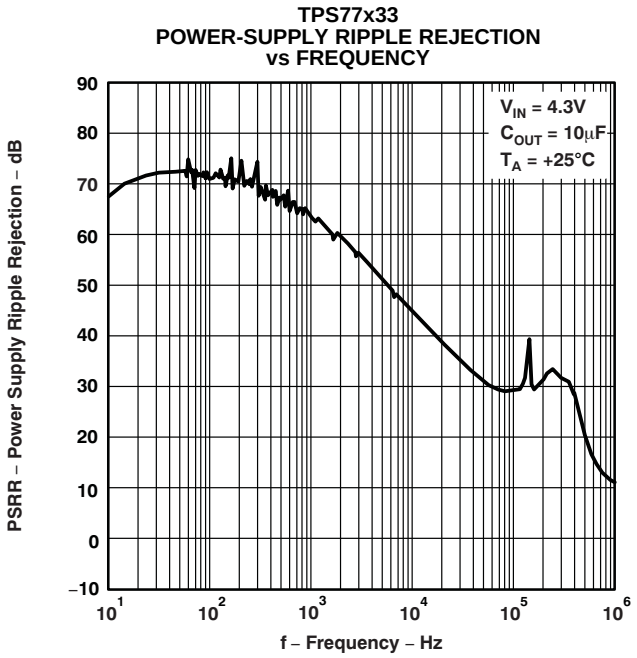


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

TPS77x33
OUTPUT SPECTRAL NOISE DENSITY
vs FREQUENCY

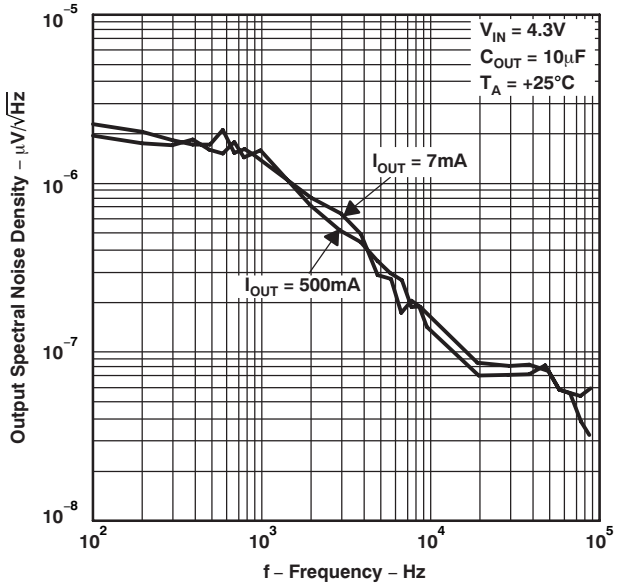


Figure 11.

TPS77x33
OUTPUT IMPEDANCE
vs FREQUENCY

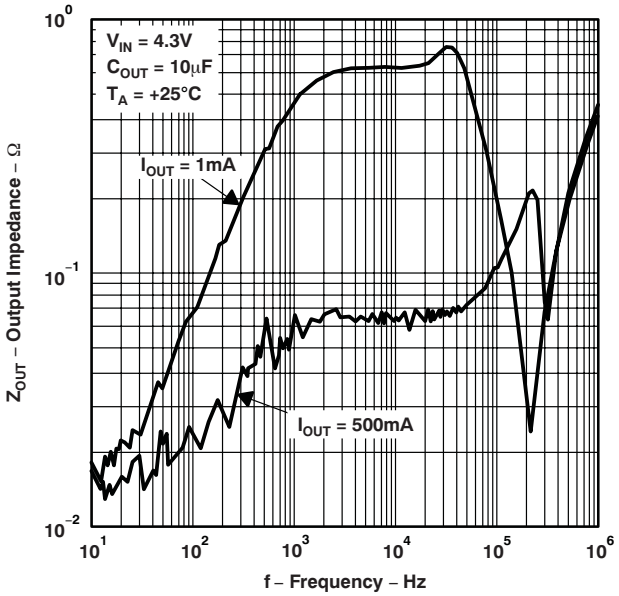


Figure 12.

TPS77x01
DROPOUT VOLTAGE
vs INPUT VOLTAGE

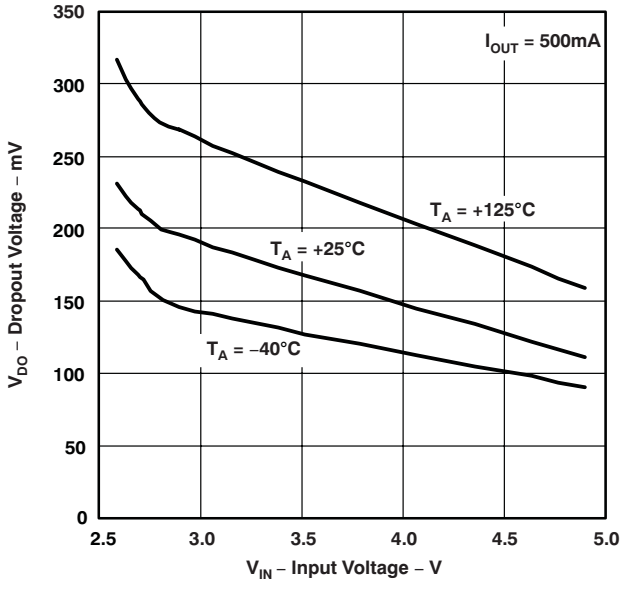


Figure 13.

TPS77x33
DROPOUT VOLTAGE
vs FREE-AIR TEMPERATURE

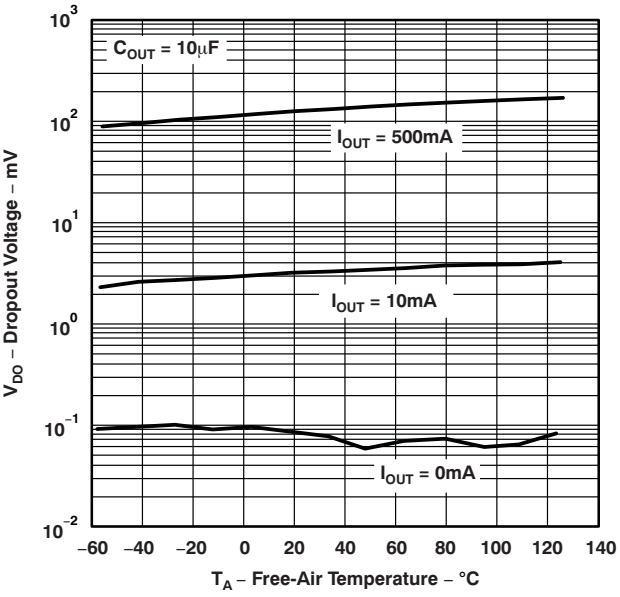


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

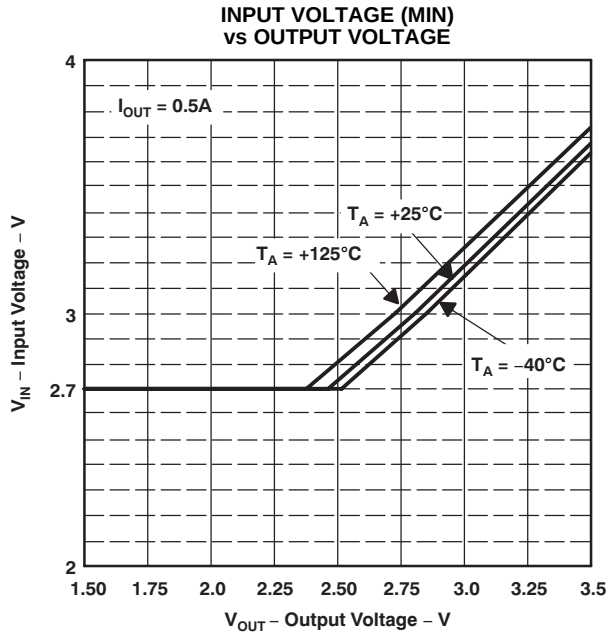


Figure 15.

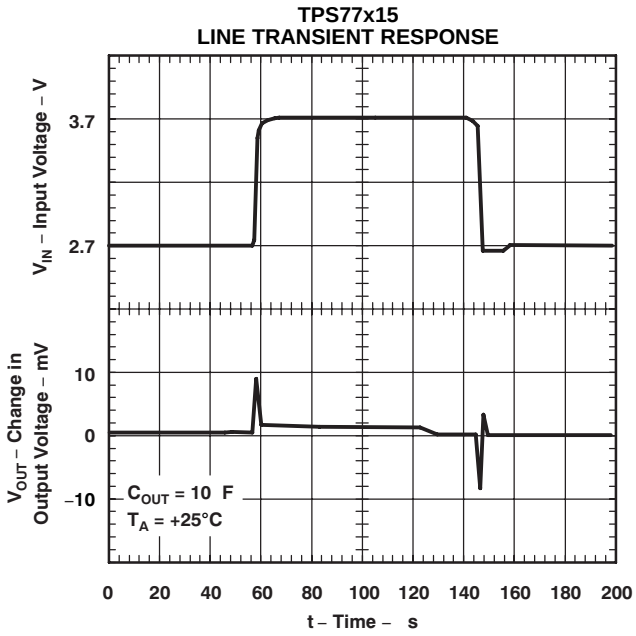


Figure 16.

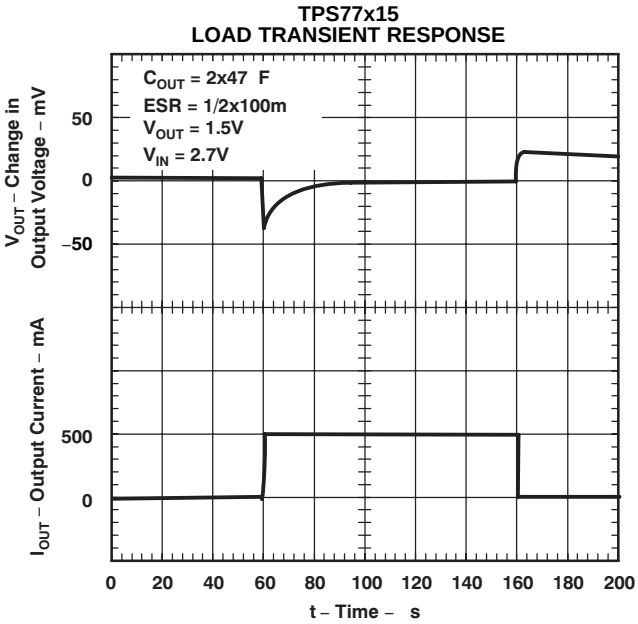


Figure 17.

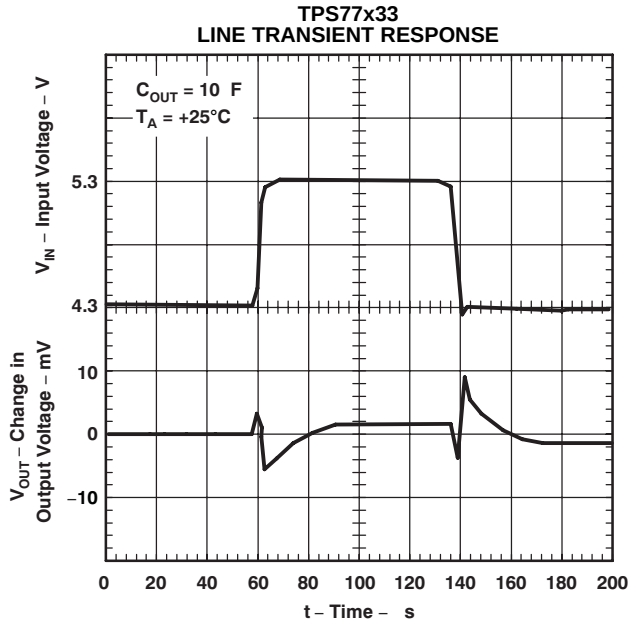


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

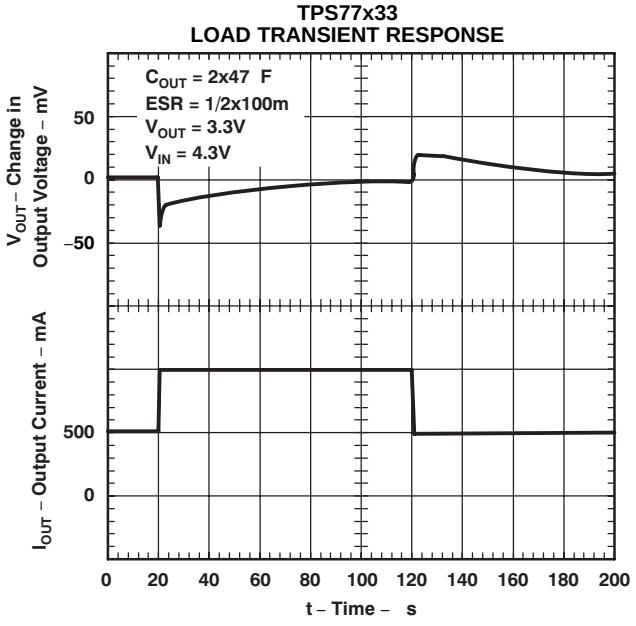


Figure 19.

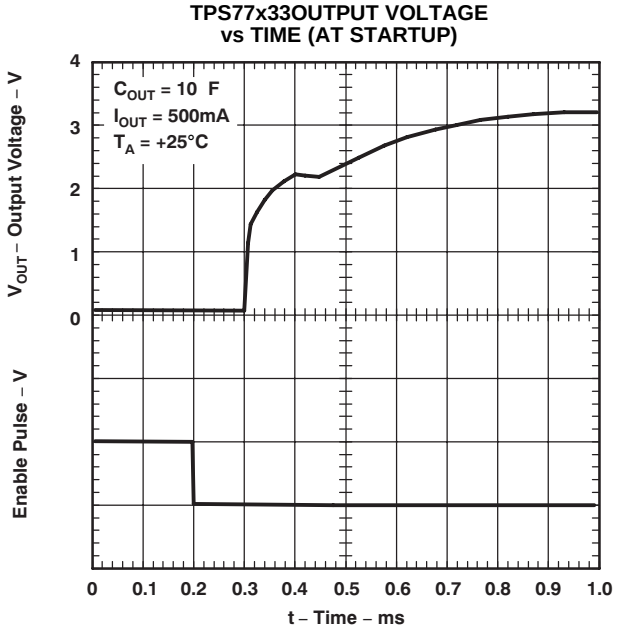


Figure 20.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J= –40°C to +125°C) unless otherwise noted. Typical values are at T_J = +25°C.

Test Circuit for Typical Regions of Stability (Figure 22 and Figure 23) (Fixed Output Options)

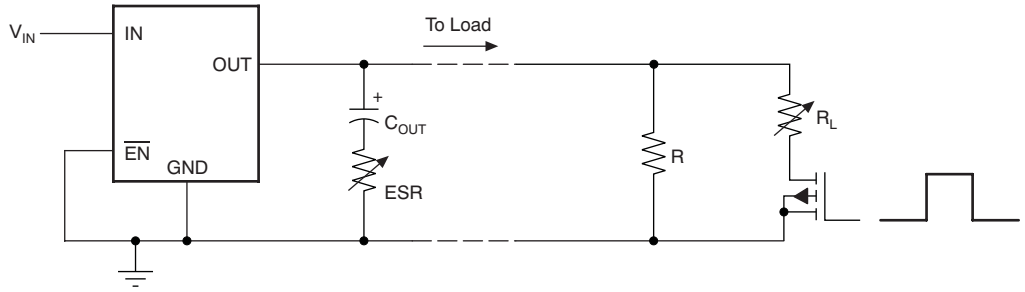
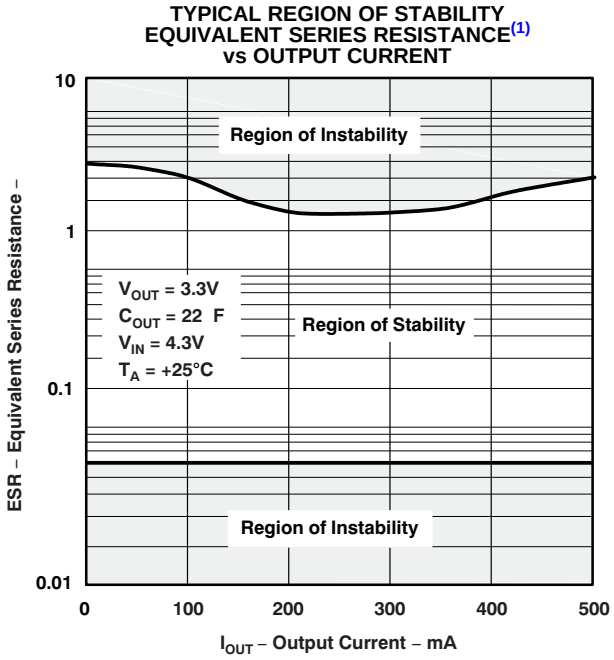
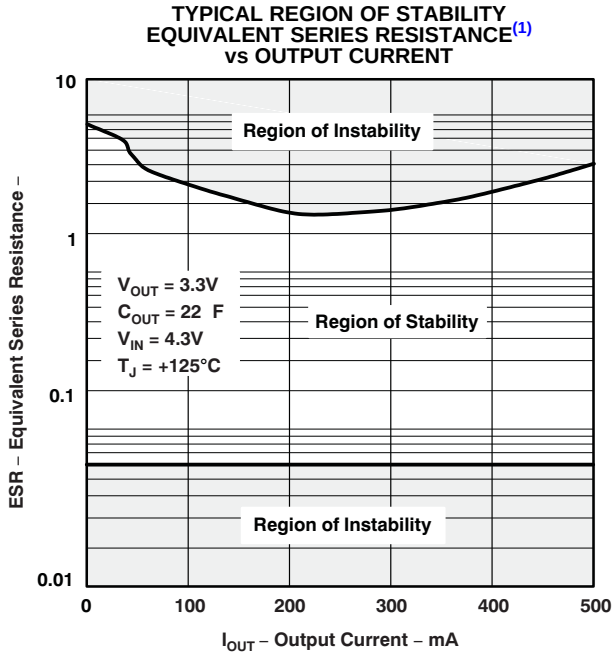


Figure 21.



(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_{OUT}.

Figure 22.



(1) Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_{OUT}.

Figure 23.

APPLICATION INFORMATION

The TPS775xx and TPS776xx feature very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS775xx and TPS776xx use a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this I_B increase translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS775xx and TPS776xx quiescent currents remain low even when the regulator drops out, eliminating both problems.

The TPS775xx and TPS776xx families also feature a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2μA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground.

Minimum Load Requirements

The TPS775xx and TPS776xx families are stable at zero load; no minimum load is required for operation.

FB—Pin Connection (Adjustable Version Only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 25. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

External Capacitor Requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047μF or larger) improves load transient response and noise rejection if the TPS775xx or TPS776xx are located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS775xx and TPS776xx require an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10μF and the ESR (equivalent series resistance) must be between 50mΩ and 1.5Ω. Capacitor values 10μF or larger are acceptable, provided the ESR is less than 1.5Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

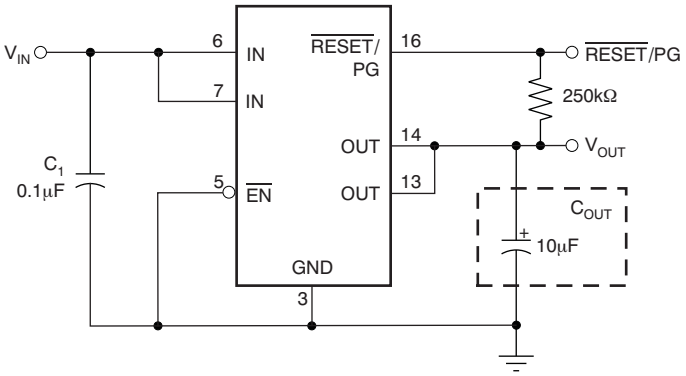


Figure 24. Typical Application Circuit (Fixed Versions)

Programming the TPS77x01 Adjustable LDO Regulator

The output voltage of the TPS77x01 adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using Equation 1:

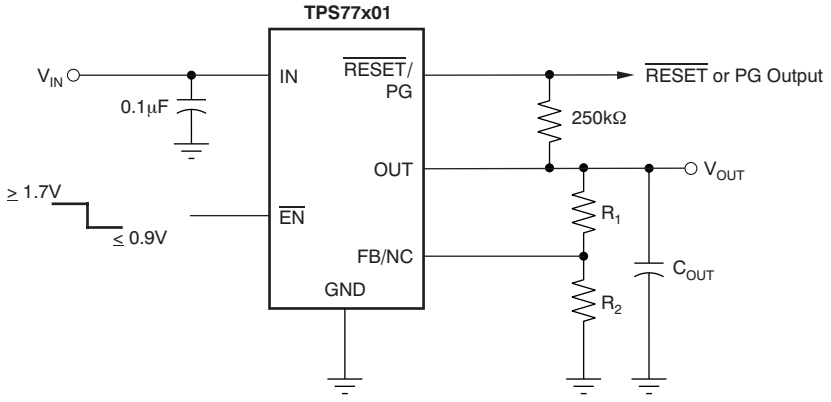
$$V_{OUT} = V_{ref} \times (1 + \frac{R_1}{R_2}) \quad (1)$$

Where:

- V_{ref} = 1.1834V typ (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 10µA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R_2 = 110kΩ to set the divider current at approximately 10µA and then calculate R_1 using Equation 2:

$$R_1 = (\frac{V_{OUT}}{V_{ref}} - 1) \times R_2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	UNIT
2.5V	121	110	kΩ
3.3V	196	110	kΩ
3.6V	226	110	kΩ
4.75V	332	110	kΩ

Figure 25. TPS77x01 Adjustable LDO Regulator Programming

Reset Indicator

The TPS775xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to Timing Diagram for start-up sequence).

Power-Good Indicator

The TPS776xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

Regulator Protection

The TPS775xx and TPS776xx PMOS-pass transistors have a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS775xx and TPS776xx also feature internal current limiting and thermal protection. During normal operation, the TPS775xx and TPS776xx limit output current to approximately 1.7A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C(typ), regulator operation resumes.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

where:

- $T_{J(max)}$ is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, and is calculated as $\frac{1}{\text{derating factor}}$ from the dissipation rating tables
- T_A is the ambient temperature

The regulator dissipation is calculated using:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS77501D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77501	Samples
TPS77501DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77501	Samples
TPS77501PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77501	Samples
TPS77501PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77501	Samples
TPS77515D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77515	Samples
TPS77515DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77515	Samples
TPS77515DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77515	Samples
TPS77515PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77515	Samples
TPS77515PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77515	Samples
TPS77516D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	77516	Samples
TPS77516DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	77516	Samples
TPS77516DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	77516	Samples
TPS77516PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PT77516	Samples
TPS77516PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PT77516	Samples
TPS77518D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77518	Samples
TPS77518DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77518	Samples
TPS77518PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77518	Samples
TPS77518PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77518	Samples
TPS77525D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77525	Samples
TPS77525DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77525	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS77525PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77525	Samples
TPS77533D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77533	Samples
TPS77533DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77533	Samples
TPS77533PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77533	Samples
TPS77533PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77533	Samples
TPS77601D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77601	Samples
TPS77601DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77601	Samples
TPS77601DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77601	Samples
TPS77601DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77601	Samples
TPS77601PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77601	Samples
TPS77601PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77601	Samples
TPS77615D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77615	Samples
TPS77615DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77615	Samples
TPS77615PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77615	Samples
TPS77618D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77618	Samples
TPS77618DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77618	Samples
TPS77618PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77618	Samples
TPS77618PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77618	Samples
TPS77625D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77625	Samples
TPS77625DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77625	Samples
TPS77625DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77625	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS77625DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77625	Samples
TPS77625PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77625	Samples
TPS77625PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77625	Samples
TPS77628D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77628	Samples
TPS77633D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77633	Samples
TPS77633DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77633	Samples
TPS77633DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77633	Samples
TPS77633DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	77633	Samples
TPS77633PWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77633	Samples
TPS77633PWPR	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PT77633	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS775, TPS776 :

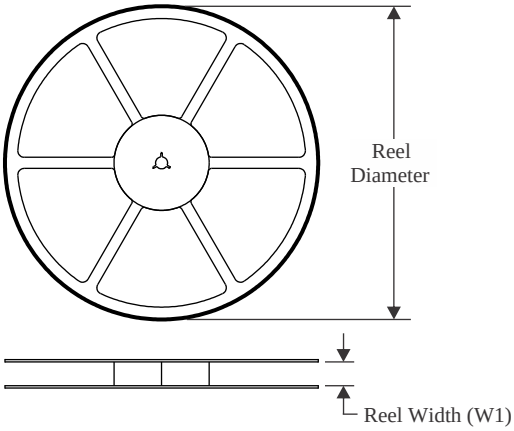
- Automotive : TPS775-Q1, TPS776-Q1

NOTE: Qualified Version Definitions:

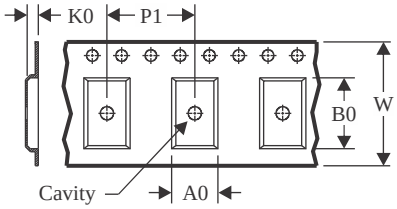
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

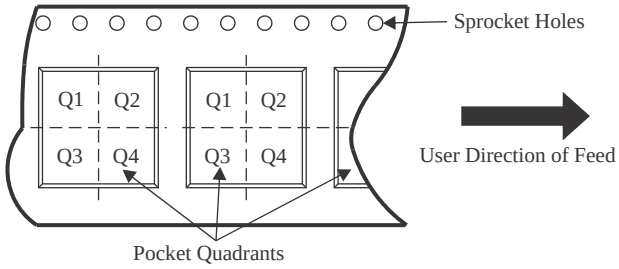


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

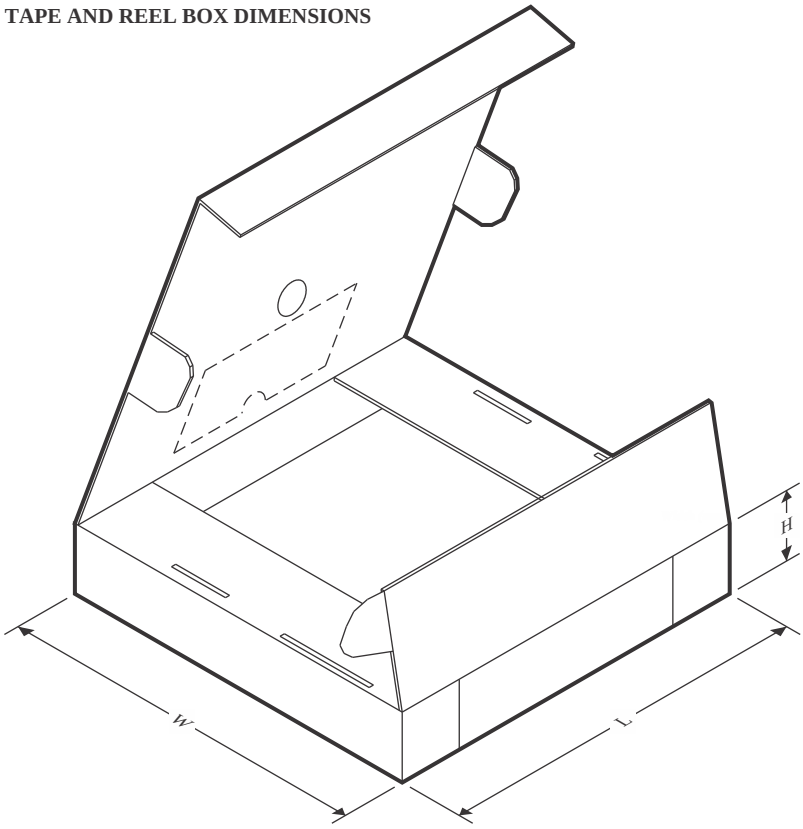


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77501DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77501PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77515DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77515PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77516DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77516PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77518DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77518PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77525DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77533DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77533PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77601DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77601PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77615DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77618DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77618PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS77625DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77625PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS77633DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS77633PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

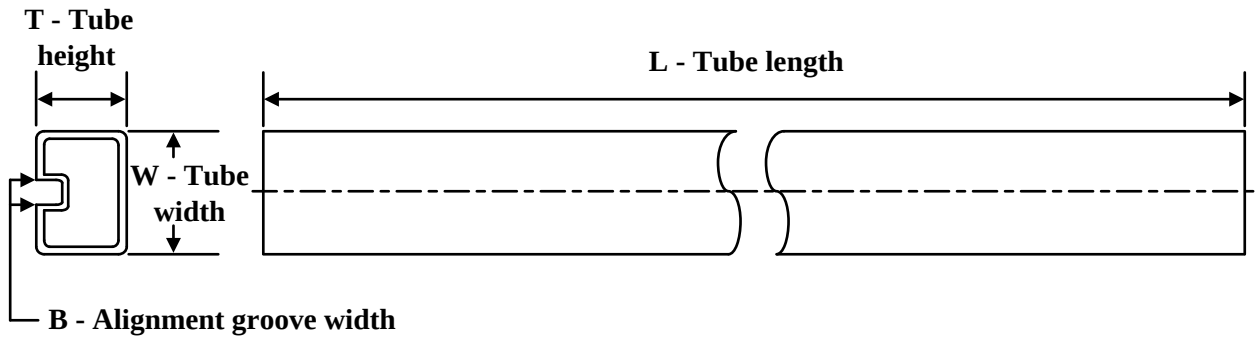


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS77501DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77501PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77515DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77515PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77516DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77516PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77518DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77518PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77525DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77533DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77533PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77601DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77601PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77615DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77618DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77618PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS77625DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77625PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

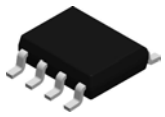
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS77633DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS77633PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS77501D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77501PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77515D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77515DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS77515PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77516D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77516DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS77516PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77518D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77518PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77525D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77525PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77533D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77533PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77601D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77601DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS77601PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77615D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77615PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77618D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77618PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77625D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77625DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS77625PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS77628D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77633D	D	SOIC	8	75	505.46	6.76	3810	4
TPS77633DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS77633PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5

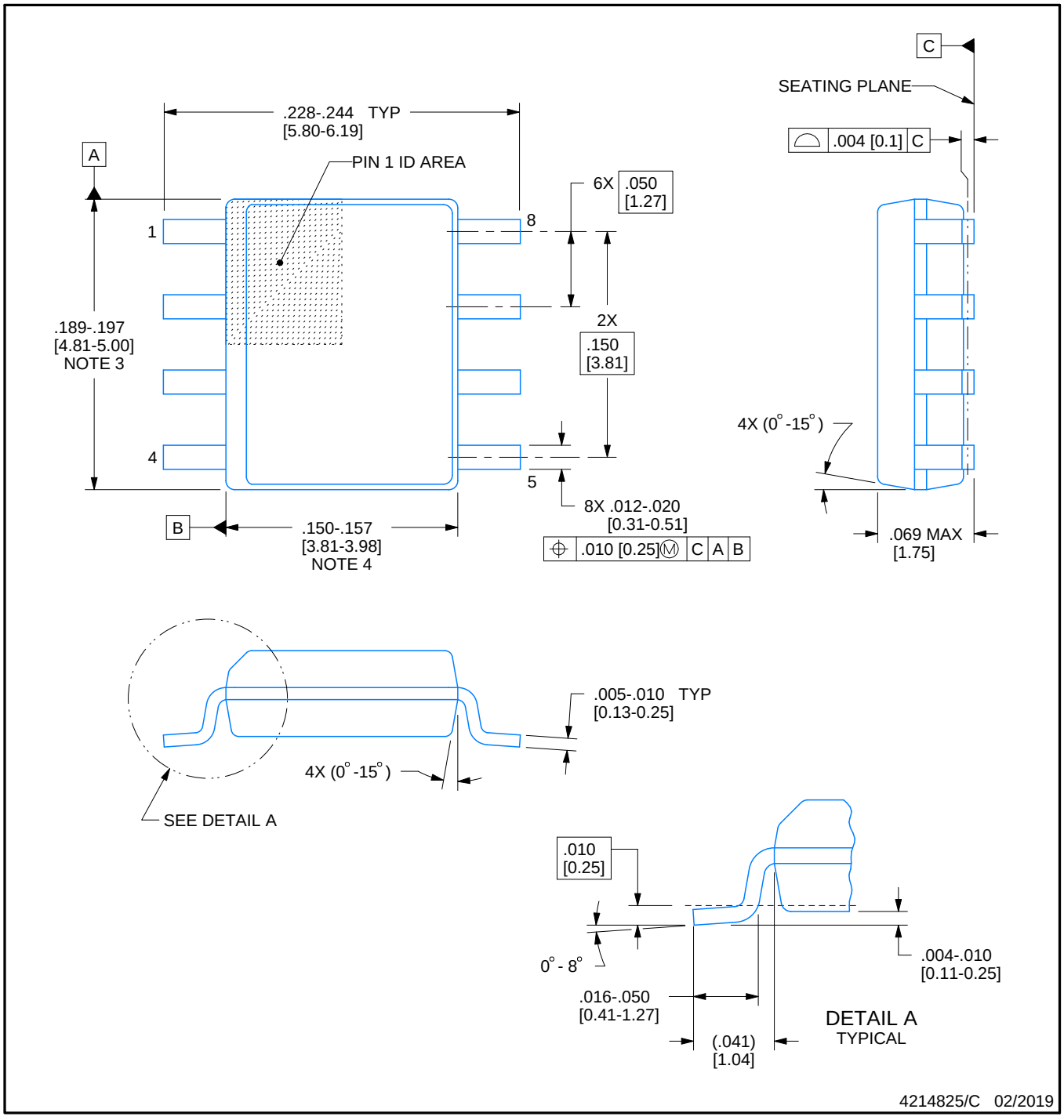


PACKAGE OUTLINE

D0008A

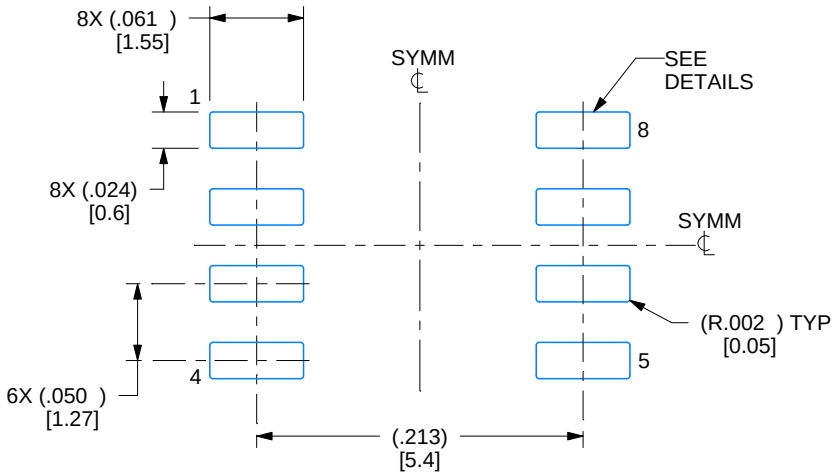
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

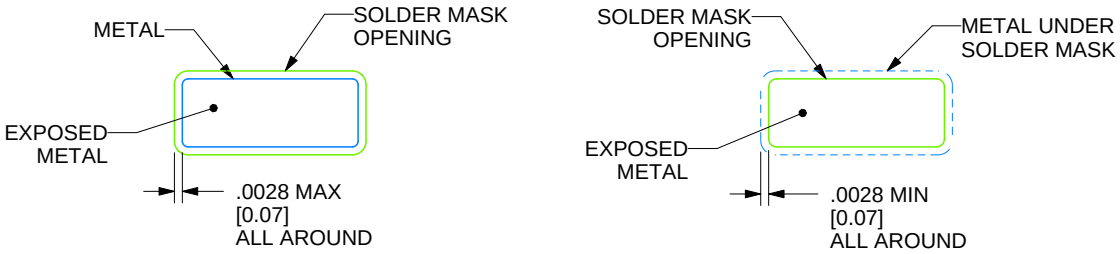


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

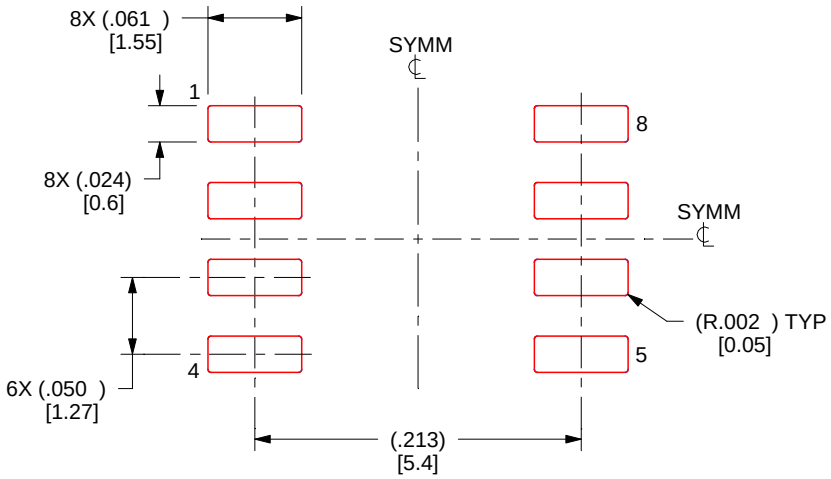
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



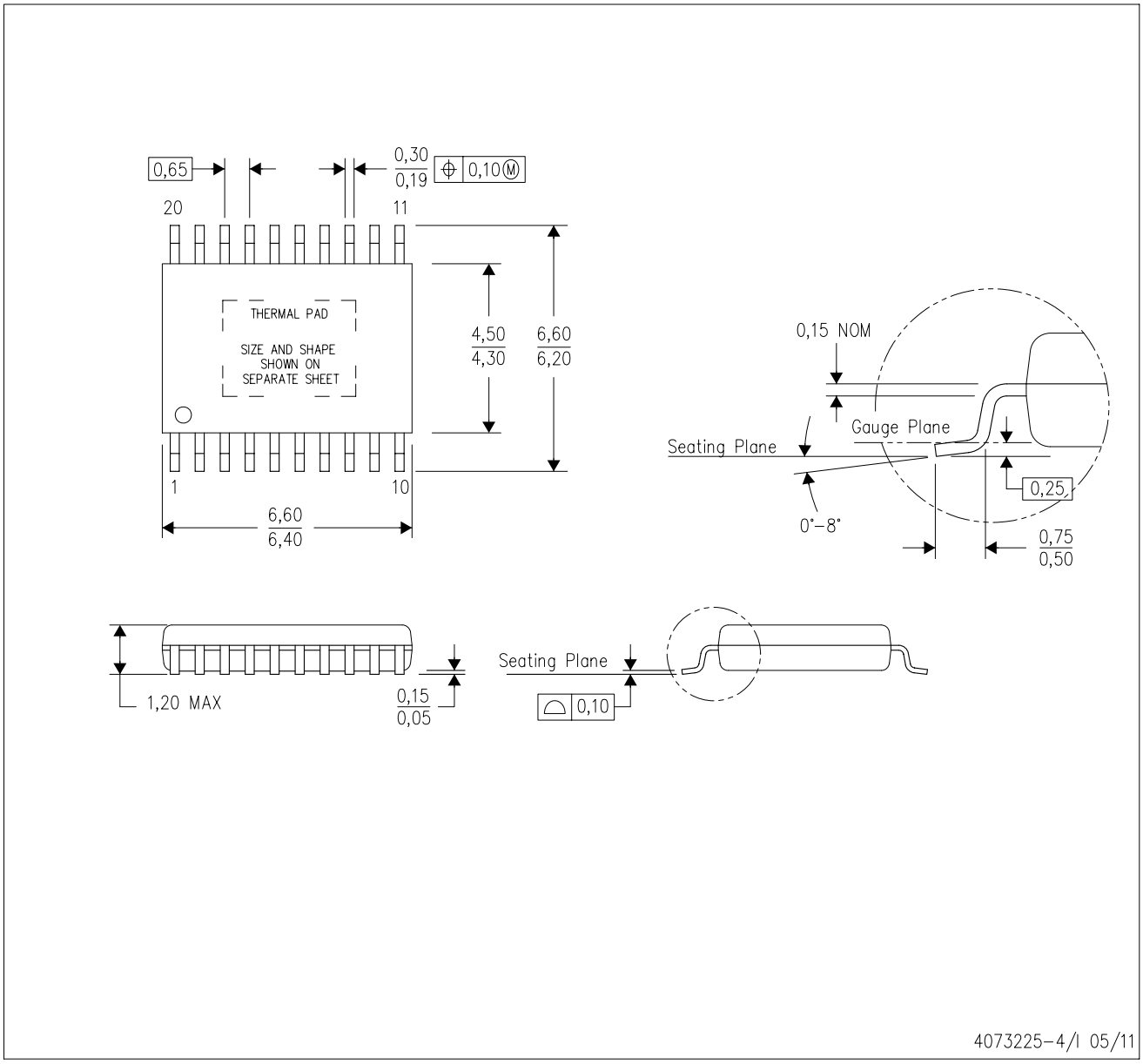
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

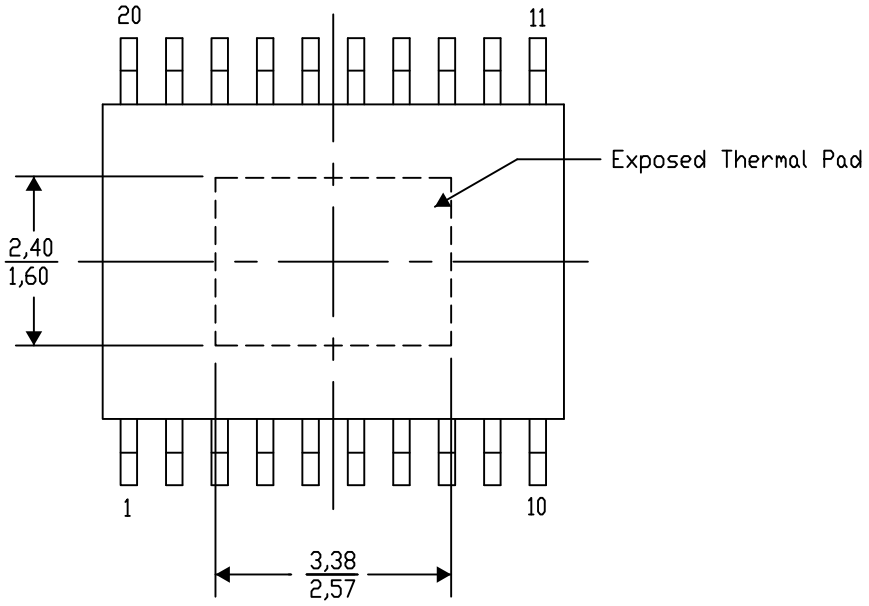
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

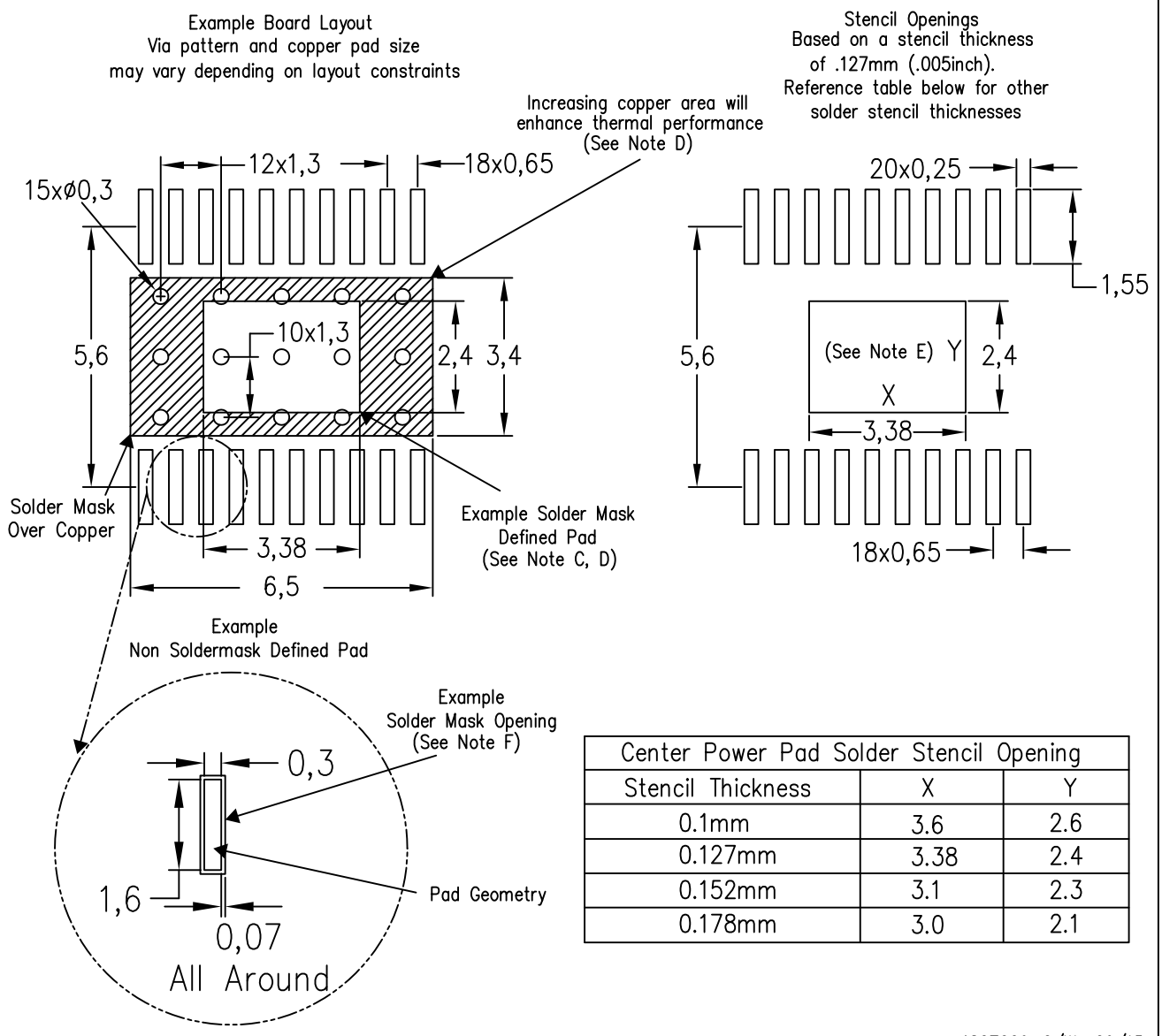
Exposed Thermal Pad Dimensions

4206332–13/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.6	2.6
0.127mm	3.38	2.4
0.152mm	3.1	2.3
0.178mm	3.0	2.1

4207609–6/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

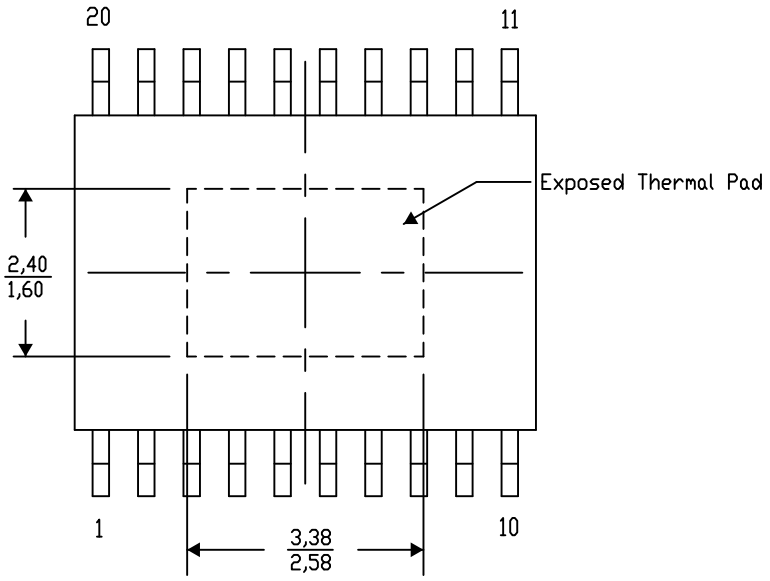
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–21/AO 01/16

NOTE: A. All linear dimensions are in millimeters

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