



# THE DATASHEET OF AON6504



### General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Very Low RDS(on) at 4.5V<sub>GS</sub>
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

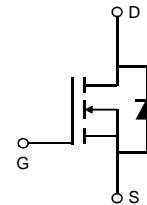
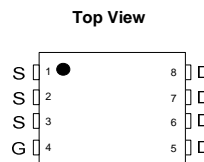
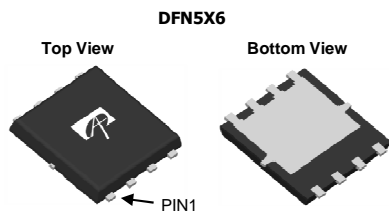
### Application

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

### Product Summary

V <sub>DS</sub>	30V
I <sub>D</sub> (at V <sub>GS</sub> =10V)	85A
R <sub>DS(ON)</sub> (at V <sub>GS</sub> =10V)	< 2.1mΩ
R <sub>DS(ON)</sub> (at V <sub>GS</sub> = 4.5V)	< 3.2mΩ

100% UIS Tested  
 100% R<sub>g</sub> Tested



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current <sup>G</sup>	I <sub>D</sub>	T <sub>C</sub> =25°C	85
		T <sub>C</sub> =100°C	66
Pulsed Drain Current <sup>C</sup>	I <sub>DM</sub>	322	A
Continuous Drain Current	I <sub>DSM</sub>	T <sub>A</sub> =25°C	51
		T <sub>A</sub> =70°C	41
Avalanche Current <sup>C</sup>	I <sub>AS</sub>	60	A
Avalanche energy L=0.05mH <sup>C</sup>	E <sub>AS</sub>	90	mJ
V <sub>DS</sub> Spike	V <sub>SPIKE</sub>	36	V
Power Dissipation <sup>B</sup>	P <sub>D</sub>	T <sub>C</sub> =25°C	83
		T <sub>C</sub> =100°C	33
Power Dissipation <sup>A</sup>	P <sub>DSM</sub>	T <sub>A</sub> =25°C	7.3
		T <sub>A</sub> =70°C	4.7
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	R <sub>θJA</sub>	t ≤ 10s	14	°C/W
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	40	°C/W
Maximum Junction-to-Case	R <sub>θJC</sub>	1.1	1.5	°C/W

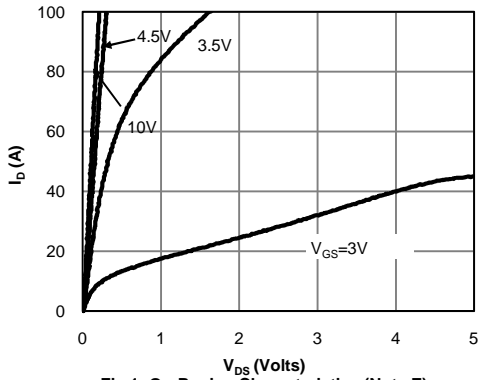
**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.3	1.7	2.1	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		1.75	2.1	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		2.55	3.15	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		120		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				85	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		2719		pF
C <sub>oss</sub>	Output Capacitance		1204		pF	
C <sub>rss</sub>	Reverse Transfer Capacitance		169		pF	
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.9	2.0	3	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		44	60	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge		21	28	nC	
Q <sub>gs</sub>	Gate Source Charge		9		nC	
Q <sub>gd</sub>	Gate Drain Charge		7		nC	
Q <sub>gs</sub>	Gate Source Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		9		nC
Q <sub>gd</sub>	Gate Drain Charge		7		nC	
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		9.7		ns
t <sub>r</sub>	Turn-On Rise Time		5.2		ns	
t <sub>D(off)</sub>	Turn-Off DelayTime		32.5		ns	
t <sub>f</sub>	Turn-Off Fall Time		10.3		ns	
t <sub>rr</sub>	Body Diode Reverse Recovery Time		I <sub>F</sub> =20A, di/dt=500A/μs		19.6	
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, di/dt=500A/μs		42.7		nC

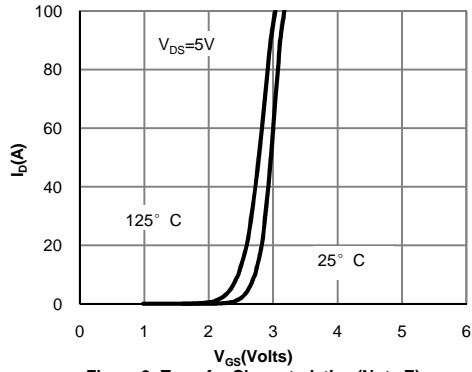
- A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
- B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.
- D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

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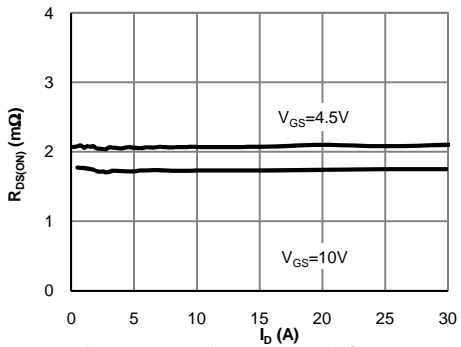
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



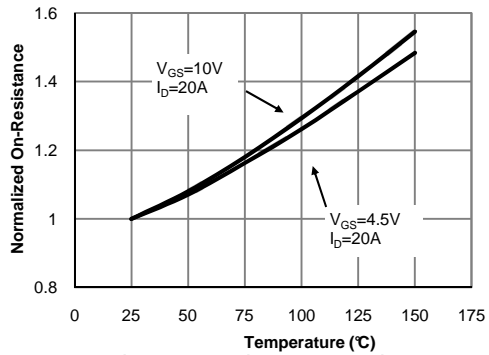
**Figure 1: On-Region Characteristics (Note E)**



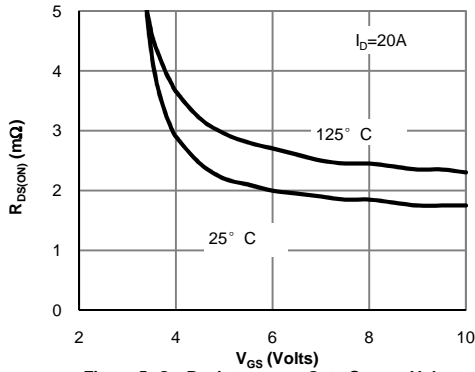
**Figure 2: Transfer Characteristics (Note E)**



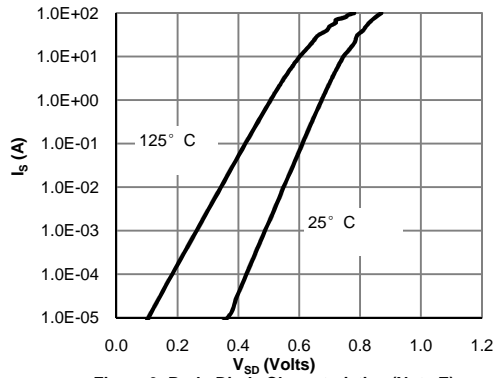
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



**Figure 6: Body-Diode Characteristics (Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

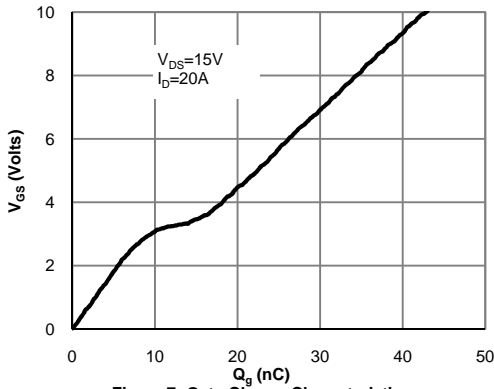


Figure 7: Gate-Charge Characteristics

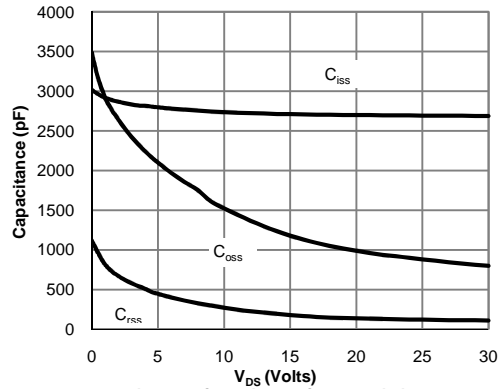


Figure 8: Capacitance Characteristics

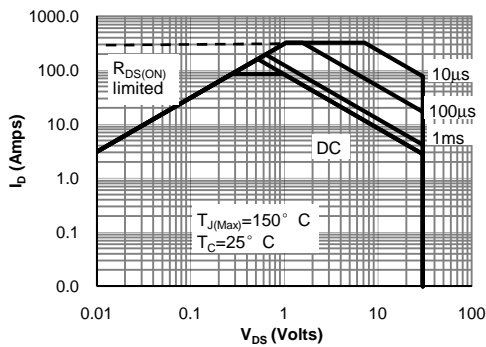


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

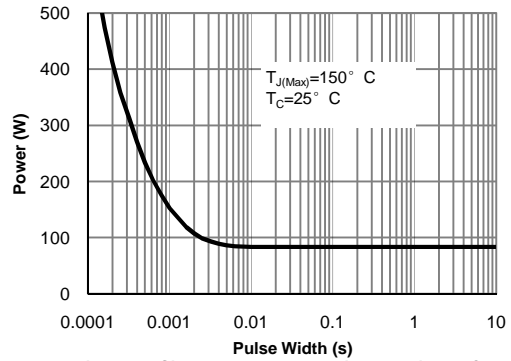


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

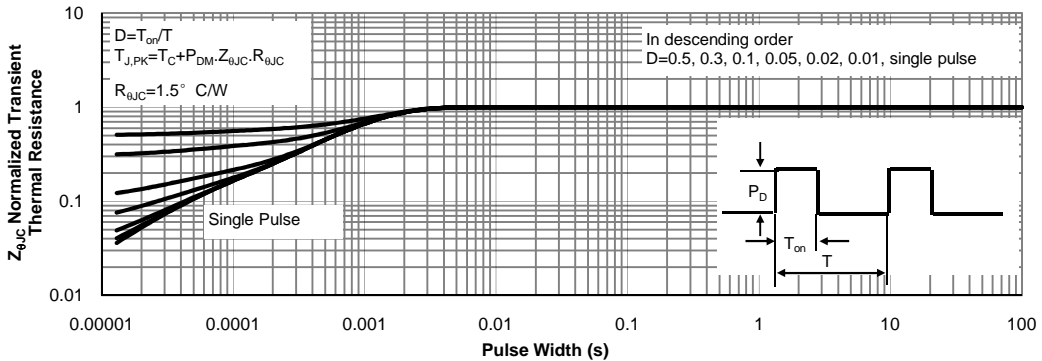


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

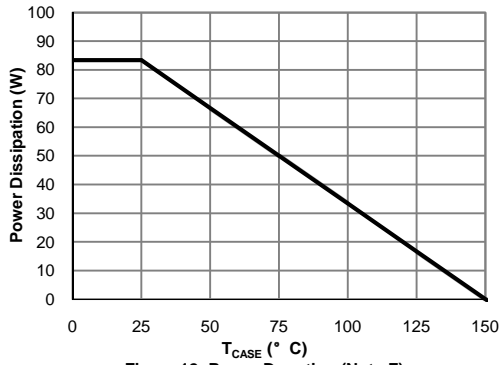


Figure 12: Power De-rating (Note F)

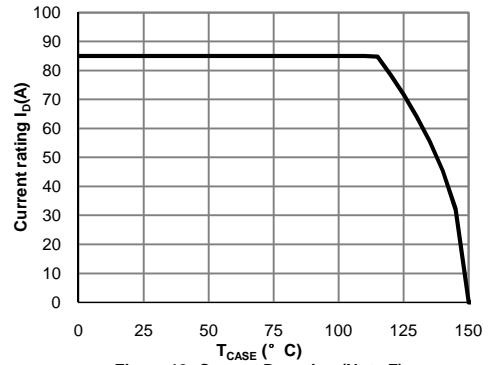


Figure 13: Current De-rating (Note F)

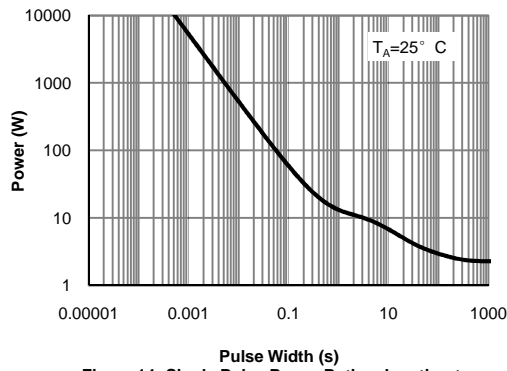


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

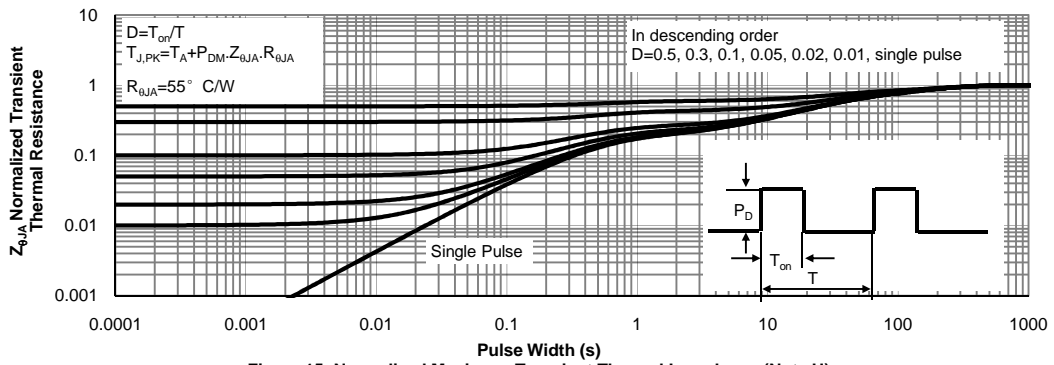
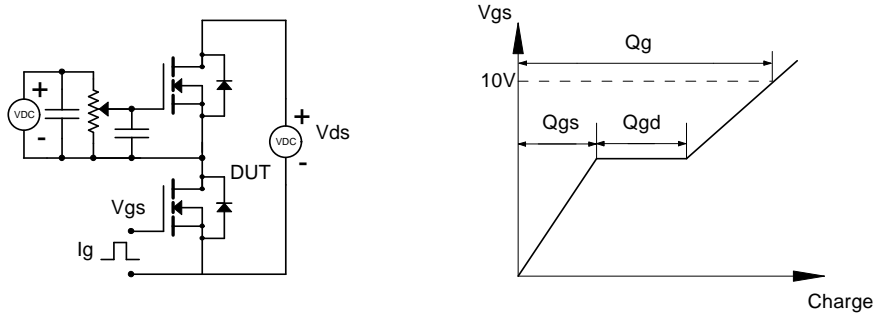
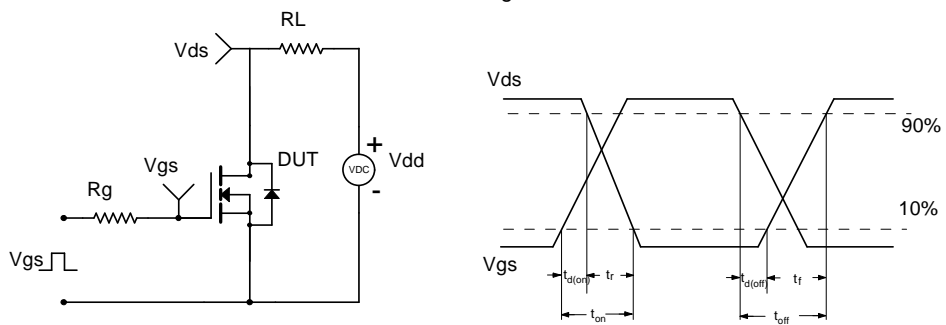


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

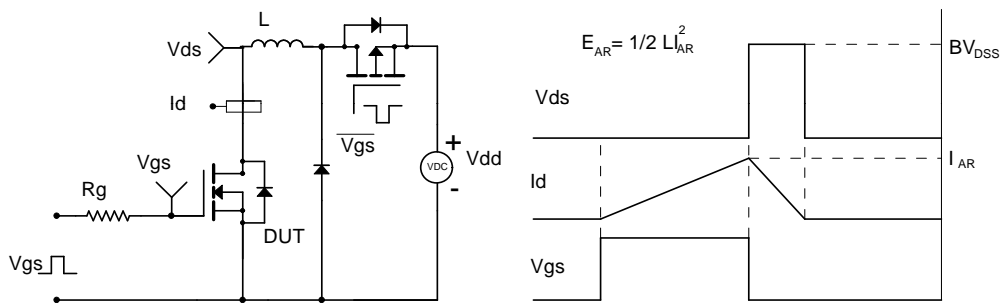
Gate Charge Test Circuit & Waveform



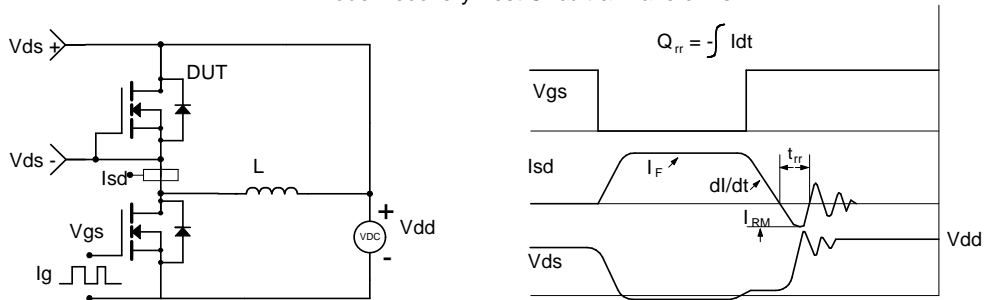
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms



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