



# THE DATASHEET OF OPA338UAG4





# MicroSIZE, Single-Supply CMOS OPERATIONAL AMPLIFIERS

## MicroAmplifier™ Series

### FEATURES

- **MicroSIZE PACKAGES:**  
SOT23-5, SOT23-8
- **SINGLE-SUPPLY OPERATION**
- **RAIL-TO-RAIL OUTPUT SWING**
- **FET-INPUT:  $I_B = 10\text{pA max}$**
- **HIGH SPEED:**  
OPA337: 3MHz, 1.2V/ $\mu\text{s}$  (G = 1)  
OPA338: 12.5MHz, 4.6V/ $\mu\text{s}$  (G = 5)
- **OPERATION FROM 2.5V to 5.5V**
- **HIGH OPEN-LOOP GAIN: 120dB**
- **LOW QUIESCENT CURRENT: 525 $\mu\text{A/amp}$**
- **SINGLE AND DUAL VERSIONS**

### APPLICATIONS

- **BATTERY-POWERED INSTRUMENTS**
- **PHOTODIODE PRE-AMPS**
- **MEDICAL INSTRUMENTS**
- **TEST EQUIPMENT**
- **AUDIO SYSTEMS**
- **DRIVING ADCs**
- **CONSUMER PRODUCTS**

SPIICE model available at [www.ti.com](http://www.ti.com).

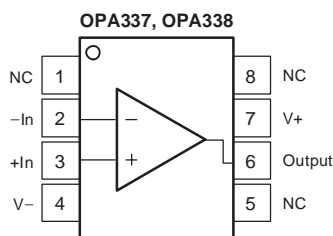
### DESCRIPTION

The OPA337 and OPA338 series rail-to-rail output CMOS operational amplifiers are designed for low cost and miniature applications. Packaged in the SOT23-8, the OPA2337EA and OPA2338EA are Texas Instruments' smallest dual op amps. At 1/4 the size of a conventional SO-8 surface-mount, they are ideal for space-sensitive applications.

Utilizing advanced CMOS technology, the OPA337 and OPA338 op amps provide low bias current, high-speed operation, high open-loop gain, and rail-to-rail output swing. They operate on a single supply with operation as low as 2.5V while drawing only 525 $\mu\text{A}$  quiescent current. In addition, the input common-mode voltage range includes ground—ideal for single-supply operation.

The OPA337 series is unity-gain stable. The OPA338 series is optimized for gains greater than or equal to 5. They are easy-to-use and free from phase inversion and overload problems found in some other op amps. Excellent performance is maintained as the amplifiers swing to their specified limits. The dual versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

PACKAGE	G = 1 STABLE		G ≥ 5 STABLE	
	SINGLE OPA337	DUAL OPA2337	SINGLE OPA338	DUAL OPA2338
SOT23-5	✓		✓	
SOT23-8		✓		✓
MSOP-8	✓			
SO-8	✓	✓	✓	✓
DIP-8	✓	✓		

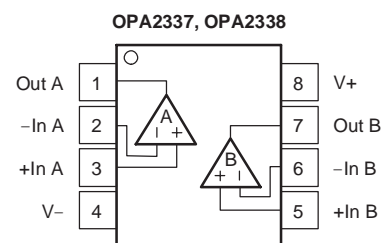


DIP-8<sup>(1)</sup>, SO-8, MSOP-8<sup>(1)</sup>  
NC = No Connection



SOT23-5

NOTE: (1) DIP AND MSOP-8 versions for OPA337, OPA2337 only.



DIP-8<sup>(1)</sup>, SO-8, SOT23-8



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**ABSOLUTE MAXIMUM RATINGS(1)**

Supply Voltage .....	7.5V
Input Voltage(2) .....	(V-) – 0.5V to (V+) + 0.5V
Input Current(2) .....	10mA
Output Short Circuit(3) .....	Continuous
Operating Temperature .....	–55°C to +125°C
Storage Temperature .....	–55°C to +125°C
Junction Temperature .....	150°C
Lead Temperature (soldering, 10s) .....	300°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input signal voltage is limited by internal diodes connected to power supplies. See text.
- (3) Short-circuit to ground, one amplifier per package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION(1)**

PRODUCT	DESCRIPTION	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA337 Series	Single, G = 1 Stable	SOT23-5	DBV	–40°C to +85°C	C37	OPA337NA/250	Tape and Reel, 250
		MSOP-8	DGK		G37	OPA337NA/3K	Tape and Reel, 3000
		DIP-8	P		OPA337PA	OPA337EA/250	Tape and Reel, 250
		SO-8 Surface-Mount	D		OPA337UA	OPA337EA/2K5	Tape and Reel, 2500
OPA2337	Dual, G = 1 Stable	SOT23-8	DCN	–40°C to +85°C	A7	OPA2337EA/250	Tape and Reel, 250
		DIP-8	P		OPA2337PA	OPA2337EA/3K	Tape and Reel, 3000
		SO-8	D		OPA2337UA	OPA2337PA	Rails
		SO-8 Surface-Mount	D		OPA2337UA	OPA2337UA	Rails
OPA338 Series	Single, G ≥ 5 Stable	SOT23-5	DBV	–40°C to +85°C	A38	OPA338NA/250	Tape and Reel, 250
		SO-8	D		OPA338UA	OPA338NA/3K	Tape and Reel, 3000
		SO-8 Surface-Mount	D		OPA338UA	OPA338UA	Rails
		SO-8 Surface-Mount	D		OPA338UA	OPA338UA/2K5	Tape and Reel, 2500
OPA2338	Dual, G ≥ 5 Stable	SOT23-8	DCN	–40°C to +85°C	A8	OPA2338EA/250	Tape and Reel, 250
		SO-8	D		OPA2338UA	OPA2338EA/3K	Tape and Reel, 3000
		SO-8 Surface-Mount	D		OPA2338UA	OPA2338UA	Rails
		SO-8 Surface-Mount	D		OPA2338UA	OPA2338UA/2K5	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

**ELECTRICAL CHARACTERISTICS:  $V_S = 2.7V$  to  $5.5V$**

**Boldface** limits apply over the specified temperature range,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_S = 5V$ .

At  $T_A = +25^\circ\text{C}$  and  $R_L = 25k\Omega$  connected to  $V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	OPA337, OPA2337, OPA338, OPA2338			UNIT
		MIN	TYP(1)	MAX	
<b>OFFSET VOLTAGE</b>					
Input Offset Voltage $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$V_{OS}$		$\pm 0.5$	$\pm 3$	mV
vs Temperature	$dV_{OS}/dT$		$\pm 2$	<b><math>\pm 3.5</math></b>	mV
vs Power-Supply Rejection Ratio $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	PSRR		25	125	$\mu\text{V}/^\circ\text{C}$
Channel Separation (dual versions)	dc		0.3	<b>125</b>	$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>					
Input Bias Current $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$I_B$		$\pm 0.2$	$\pm 10$	pA
Input Offset Current	$I_{OS}$		See Typical Curve		pA
<b>NOISE</b>					
Input Voltage Noise, $f = 0.1\text{Hz}$ to $10\text{Hz}$			6		$\mu\text{V}_{PP}$
Input Voltage Noise Density, $f = 1\text{kHz}$	$e_n$		26		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density, $f = 1\text{kHz}$	$i_n$		0.6		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>					
Common-Mode Voltage Range	$V_{CM}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	<b>-0.2</b>	<b>(V+) - 1.2</b>	V
Common-Mode Rejection Ratio	CMRR	$-0.2\text{V} < V_{CM} < (V+) - 1.2\text{V}$	74	90	dB
$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$-0.2\text{V} < V_{CM} < (V+) - 1.2\text{V}$	<b>74</b>		dB
<b>INPUT IMPEDANCE</b>					
Differential			$10^{13}    2$		$\Omega    \text{pF}$
Common-Mode			$10^{13}    4$		$\Omega    \text{pF}$
<b>OPEN-LOOP GAIN</b>					
Open-Loop Voltage Gain $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$A_{OL}$	$R_L = 25k\Omega, 125\text{mV} < V_O < (V+) - 125\text{mV}$	100	120	dB
		<b><math>R_L = 25k\Omega, 125\text{mV} &lt; V_O &lt; (V+) - 125\text{mV}</math></b>	<b>100</b>		dB
		$R_L = 5k\Omega, 500\text{mV} < V_O < (V+) - 500\text{mV}$	100	114	dB
$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		<b><math>R_L = 5k\Omega, 500\text{mV} &lt; V_O &lt; (V+) - 500\text{mV}</math></b>	<b>100</b>		dB
<b>OPA337 FREQUENCY RESPONSE</b>					
Gain-Bandwidth Product	GBW	$V_S = 5V, G = 1$		3	MHz
Slew Rate	SR	$V_S = 5V, G = 1$		1.2	$\text{V}/\mu\text{s}$
Settling Time: 0.1%		$V_S = 5V, 2V \text{ Step}, C_L = 100\text{pF}, G = 1$		2	$\mu\text{s}$
0.01%		$V_S = 5V, 2V \text{ Step}, C_L = 100\text{pF}, G = 1$		2.5	$\mu\text{s}$
Overload Recovery Time		$V_{IN} \times G = V_S$		2	$\mu\text{s}$
Total Harmonic Distortion + Noise	THD+N	$V_S = 5V, V_O = 3V_{PP}, G = 1, f = 1\text{kHz}$		0.001	%
<b>OPA338 FREQUENCY RESPONSE</b>					
Gain-Bandwidth Product	GBW	$V_S = 5V, G = 5$		12.5	MHz
Slew Rate	SR	$V_S = 5V, G = 5$		4.6	$\text{V}/\mu\text{s}$
Settling Time: 0.1%		$V_S = 5V, 2V \text{ Step}, C_L = 100\text{pF}, G = 5$		1.4	$\mu\text{s}$
0.01%		$V_S = 5V, 2V \text{ Step}, C_L = 100\text{pF}, G = 5$		1.9	$\mu\text{s}$
Overload Recovery Time		$V_{IN} \times G = V_S$		0.5	$\mu\text{s}$
Total Harmonic Distortion + Noise	THD+N	$V_S = 5V, V_O = 3V_{PP}, G = 5, f = 1\text{kHz}$		0.0035	%

(1)  $V_S = 5V$ .

(2) Output voltage swings are measured between the output and negative and positive power-supply rails.

**ELECTRICAL CHARACTERISTICS:  $V_S = 2.7V$  to  $5.5V$  (continued)**

**Boldface** limits apply over the specified temperature range,  $-40^{\circ}C$  to  $+85^{\circ}C$ ,  $V_S = 5V$ .

At  $T_A = +25^{\circ}C$  and  $R_L = 25k\Omega$  connected to  $V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	OPA337, OPA2337, OPA338, OPA2338			UNIT
		MIN	TYP(1)	MAX	
<b>OUTPUT</b>					
Voltage Output Swing from Rail(2)	$R_L = 25k\Omega, A_{OL} \geq 100dB$		40	125	mV
$T_A = -40^{\circ}C$ to $+85^{\circ}C$	<b><math>R_L = 25k\Omega, A_{OL} \geq 100dB</math></b>			<b>125</b>	mV
	$R_L = 5k\Omega, A_{OL} \geq 100dB$		150	500	mV
$T_A = -40^{\circ}C$ to $+85^{\circ}C$	<b><math>R_L = 5k\Omega, A_{OL} \geq 100dB</math></b>			<b>500</b>	mV
Short-Circuit Current			$\pm 9$		mA
Capacitive Load Drive		See Typical Curve			
<b>POWER SUPPLY</b>					
Specified Voltage Range	$V_S$	<b>2.7</b>		<b>5.5</b>	V
Minimum Operating Voltage			2.5		V
Quiescent Current (per amplifier)	$I_Q$		0.525	1	mA
$T_A = -40^{\circ}C$ to $+85^{\circ}C$	$I_O = 0$ <b><math>I_O = 0</math></b>			<b>1.2</b>	mA
<b>TEMPERATURE RANGE</b>					
Specified Range		-40		+85	$^{\circ}C$
Operating Range		-55		+125	$^{\circ}C$
Storage Range		-55		+125	$^{\circ}C$
Thermal Resistance	$\theta_{JA}$				
SOT23-5 Surface-Mount			200		$^{\circ}C/W$
SOT23-8 Surface-Mount			200		$^{\circ}C/W$
MSOP-8			150		$^{\circ}C/W$
SO-8 Surface-Mount			150		$^{\circ}C/W$
DIP-8			100		$^{\circ}C/W$

(1)  $V_S = 5V$ .

(2) Output voltage swings are measured between the output and negative and positive power-supply rails.

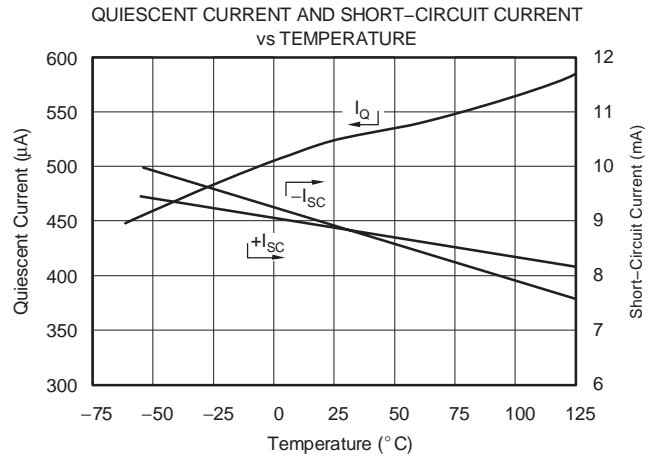
## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 25\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



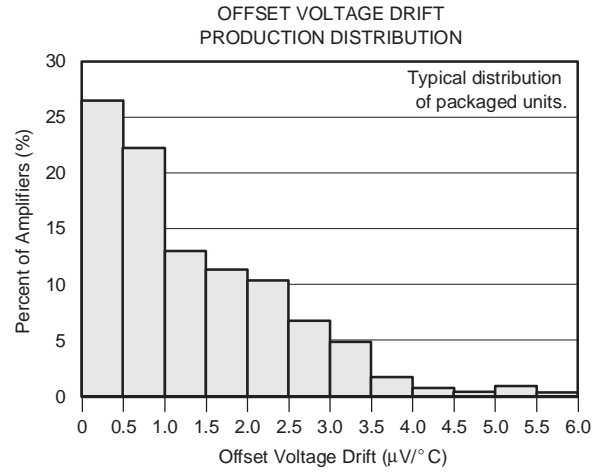
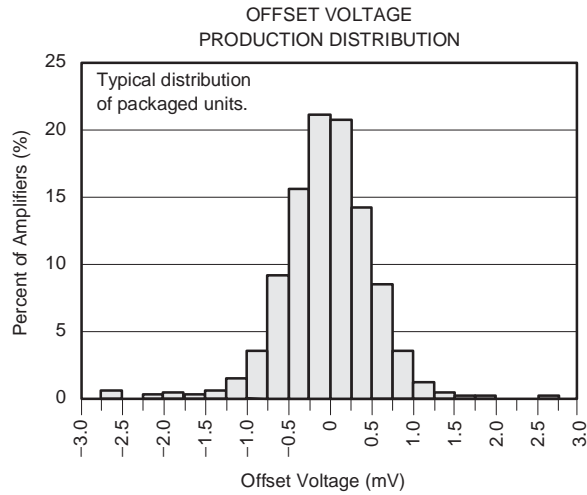
**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 25\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $R_L = 25\text{k}\Omega$  connected to  $V_S/2$ , unless otherwise noted.



## APPLICATIONS INFORMATION

The OPA337 and OPA338 series are fabricated on a state-of-the-art CMOS process. The OPA337 series is unity-gain stable. The OPA338 series is optimized for gains greater than or equal to 5. Both are suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 0.01μF ceramic capacitors.

### OPERATING VOLTAGE

The OPA337 series and OPA338 series can operate from a +2.5V to +5.5V single supply with excellent performance. Unlike most op amps which are specified at only one supply voltage, these op amps are specified for real-world applications; a single limit applies throughout the +2.7V to +5.5V supply range. This allows a designer to have the same assured performance at any supply voltage within the specified voltage range. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characteristic curves.

### INPUT VOLTAGE

The input common-mode range extends from (V-) - 0.2V to (V+) - 1.2V. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies. Inputs greater than the input common-mode range but less than maximum input voltage, while not valid, will not cause any damage to the op amp. Furthermore, if input current is limited the inputs may go beyond the power supplies without phase inversion (as shown in Figure 1) unlike some other op amps.

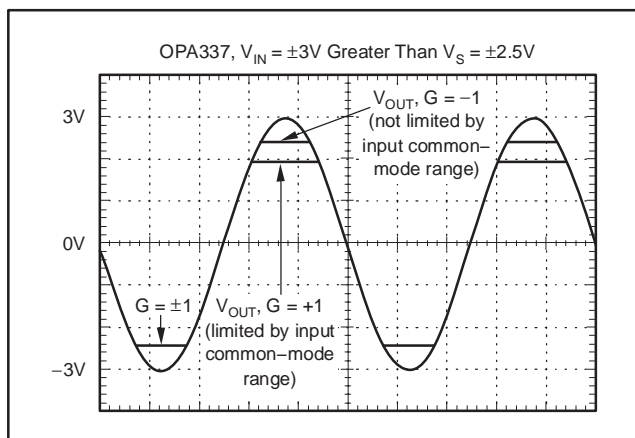


Figure 1. OPA337—No Phase Inversion with Inputs Greater than the Power-Supply Voltage

Normally, input currents are 0.2pA. However, large inputs (greater than 500mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10mA. This is easily accomplished with an input resistor as shown in Figure 2.

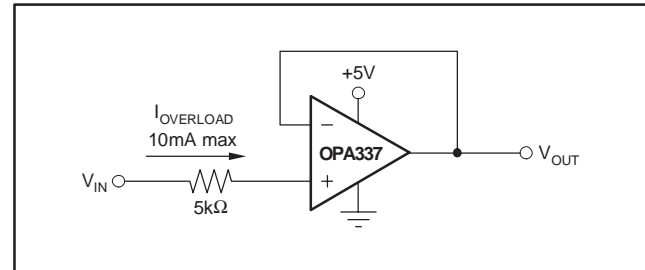


Figure 2. Input Current Protection for Voltages Exceeding the Supply Voltage

### USING THE OPA338 IN LOW GAINS

The OPA338 series is optimized for gains greater than or equal to 5. It has significantly wider bandwidth (12.5MHz) and faster slew rate (4.6V/μs) when compared to the OPA337 series. The OPA338 series can be used in lower gain configurations at low frequencies while maintaining its high slew rate with the proper compensation.

Figure 3 shows the OPA338 in a unity-gain buffer configuration. At dc, the compensation capacitor C<sub>1</sub> is effectively open resulting in 100% feedback (closed-loop gain = 1). As frequency increases, C<sub>1</sub> becomes lower impedance and closed-loop gain increases, eventually becoming 1 + R<sub>2</sub>/R<sub>1</sub> (in this case 5, which is equal to the minimum gain required for stability).

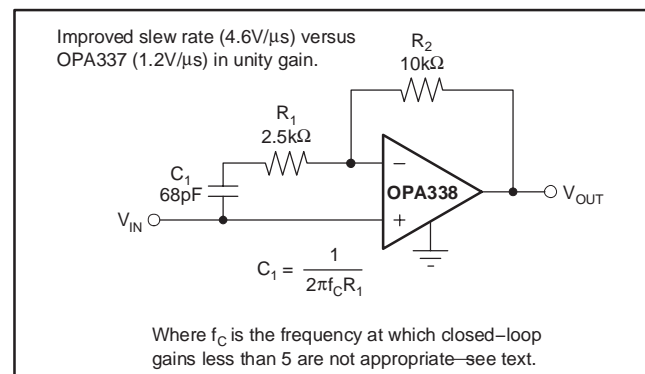


Figure 3. Compensation of the OPA338 for Unity-Gain Buffer

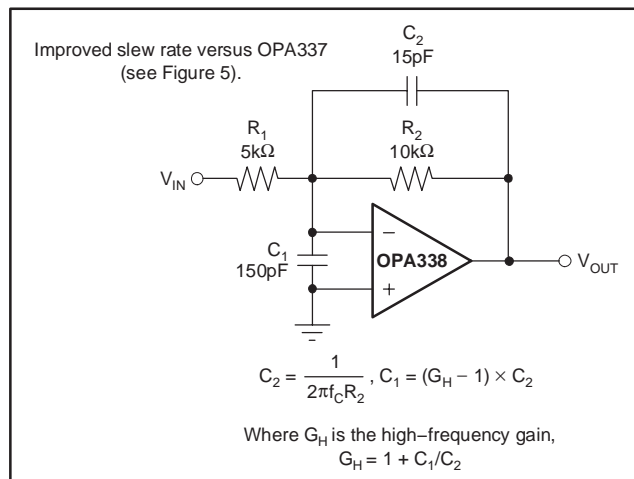
The required compensation capacitor value can be determined from the following equation:

$$C_1 = 1/(2\pi f_C R_1)$$

Since  $f_C$  may shift with process variations, it is recommended that a value less than  $f_C$  be used for determining  $C_1$ . With  $f_C = 1\text{MHz}$  and  $R_1 = 2.5\text{k}\Omega$ , the compensation capacitor is about 68pF.

The selection of the compensation capacitor  $C_1$  is important. A proper value ensures that the closed-loop circuit gain is greater than or equal to 5 at high frequencies. Referring to the *Open-Loop Gain vs Frequency* plot in the Typical Characteristics section, the OPA338 gain line (dashed in the curve) has a constant slope ( $-20\text{dB/decade}$ ) up to approximately 3MHz. This frequency is referred to as  $f_C$ . Beyond  $f_C$  the slope of the curve increases, suggesting that closed-loop gains less than 5 are not appropriate.

Figure 4 shows a compensation technique using an inverting configuration. The low-frequency gain is set by the resistor ratio while the high-frequency gain is set by the capacitor ratio. As with the noninverting circuit, for frequencies above  $f_C$  the gain must be greater than the recommended minimum stable gain for the op amp.



**Figure 4. Inverting Compensation Circuit of the OPA338 for Low Gain**

Resistors  $R_1$  and  $R_2$  are chosen to set the desired dc signal gain. Then the value for  $C_2$  is determined as follows:

$$C_2 = 1/(2\pi f_C R_2)$$

$C_1$  is determined from the desired high-frequency gain ( $G_H$ ):

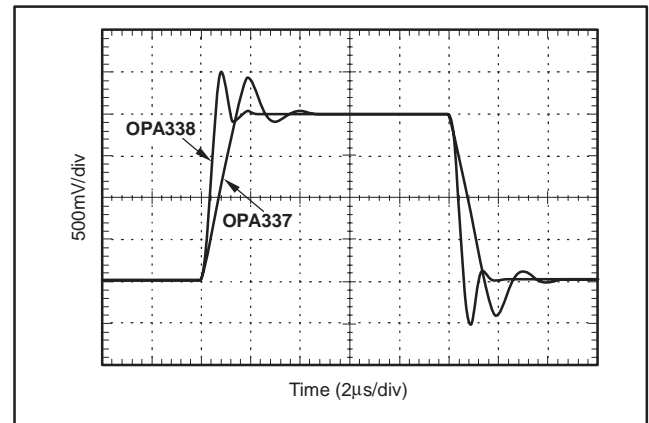
$$C_1 = (G_H - 1) \times C_2$$

For a desired dc gain of 2 and high-frequency gain of 10, the following resistor and capacitor values result:

$R_1 = 10\text{k}\Omega$	$C_1 = 150\text{pF}$
$R_2 = 5\text{k}\Omega$	$C_2 = 15\text{pF}$

The capacitor values shown are the nearest standard values. Capacitor values may need to be adjusted slightly to optimize performance. For more detailed information, consult the section on *Low Gain Compensation* in the OPA846 data sheet (SBOS250) located at www.ti.com.

Figure 5 shows the large-signal transient response using the circuit given in Figure 4. As shown, the OPA338 is stable in low gain applications and provides improved slew rate performance when compared to the OPA337.



**Figure 5.  $G = 2$ , Slew-Rate Comparison of the OPA338 and the OPA337**

## TYPICAL APPLICATION

See Figure 6 for the OPA2337 in a typical application. The ADS7822 is a 12-bit, micropower, sampling analog-to-digital converter available in the tiny MSOP-8 package. As with the OPA2337, it operates with a supply voltage as low as +2.7V. When used with the miniature SOT23-8 package of the OPA2337, the circuit is ideal for space-limited and low-power applications. In addition, the OPA2337's high input impedance allows large value resistors to be used which results in small physical capacitors, further reducing circuit size. For further information, consult the ADS7822 data sheet (SBAS062) located at www.ti.com.



Figure 6. Low-Power, Single-Supply, Speech Bandpass Filtered Data Acquisition System



Figure 7. Recommended SOT23-5 and SOT23-8 Solder Footprints

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2337EA/250	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		A7	<a href="#">Samples</a>
OPA2337EA/3K	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		A7	<a href="#">Samples</a>
OPA2337PA	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA2337PA	<a href="#">Samples</a>
OPA2337UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		OPA 2337UA	<a href="#">Samples</a>
OPA2337UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2337UA	<a href="#">Samples</a>
OPA2337UA/2K5G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2337UA	<a href="#">Samples</a>
OPA2338EA/250	ACTIVE	SOT-23	DCN	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		A8	<a href="#">Samples</a>
OPA2338EA/3K	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A8	<a href="#">Samples</a>
OPA2338UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		OPA 2338UA	<a href="#">Samples</a>
OPA2338UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2338UA	<a href="#">Samples</a>
OPA337EA/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	G37	<a href="#">Samples</a>
OPA337NA/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C37	<a href="#">Samples</a>
OPA337NA/250G4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C37	<a href="#">Samples</a>
OPA337NA/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C37	<a href="#">Samples</a>
OPA337NA/3KG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C37	<a href="#">Samples</a>
OPA337UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 337UA	<a href="#">Samples</a>
OPA337UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 337UA	<a href="#">Samples</a>
OPA337UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 337UA	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA338NA/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A38	<a href="#">Samples</a>
OPA338NA/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A38	<a href="#">Samples</a>
OPA338UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 338UA	<a href="#">Samples</a>
OPA338UAG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 338UA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

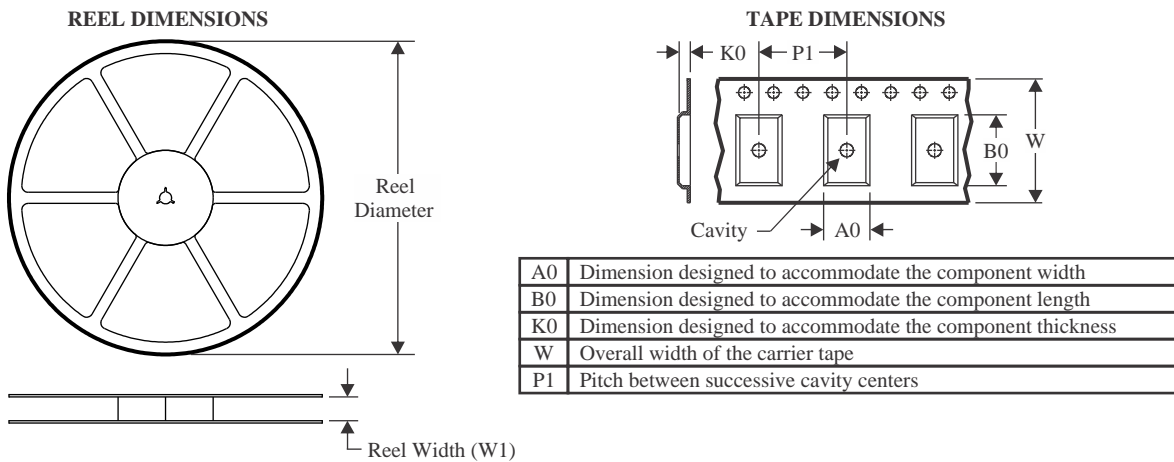
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2337EA/250	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2337EA/3K	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2337UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2338EA/250	SOT-23	DCN	8	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA2338EA/3K	SOT-23	DCN	8	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA2338UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA337NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA337NA/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA337NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA337NA/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA337UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA338NA/250	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA338NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2337EA/250	SOT-23	DCN	8	250	213.0	191.0	35.0
OPA2337EA/3K	SOT-23	DCN	8	3000	213.0	191.0	35.0
OPA2337UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2338EA/250	SOT-23	DCN	8	250	210.0	185.0	35.0
OPA2338EA/3K	SOT-23	DCN	8	3000	210.0	185.0	35.0
OPA2338UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA337NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA337NA/250	SOT-23	DBV	5	250	203.0	203.0	35.0
OPA337NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA337NA/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA337UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA338NA/250	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA338NA/3K	SOT-23	DBV	5	3000	565.0	140.0	75.0

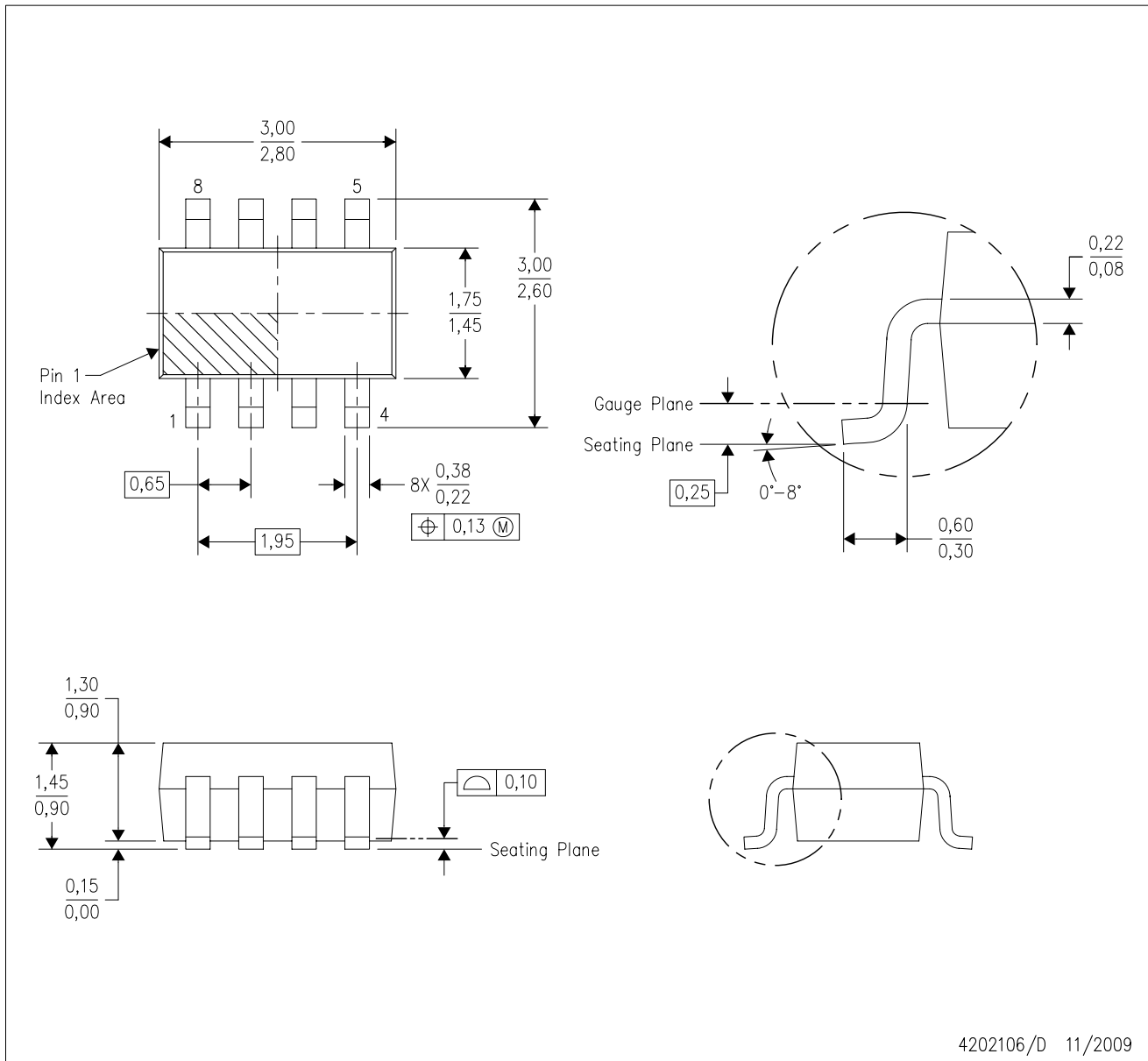
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA2337PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2337UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2338UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA337UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA337UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA338UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA338UAG4	D	SOIC	8	75	506.6	8	3940	4.32

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

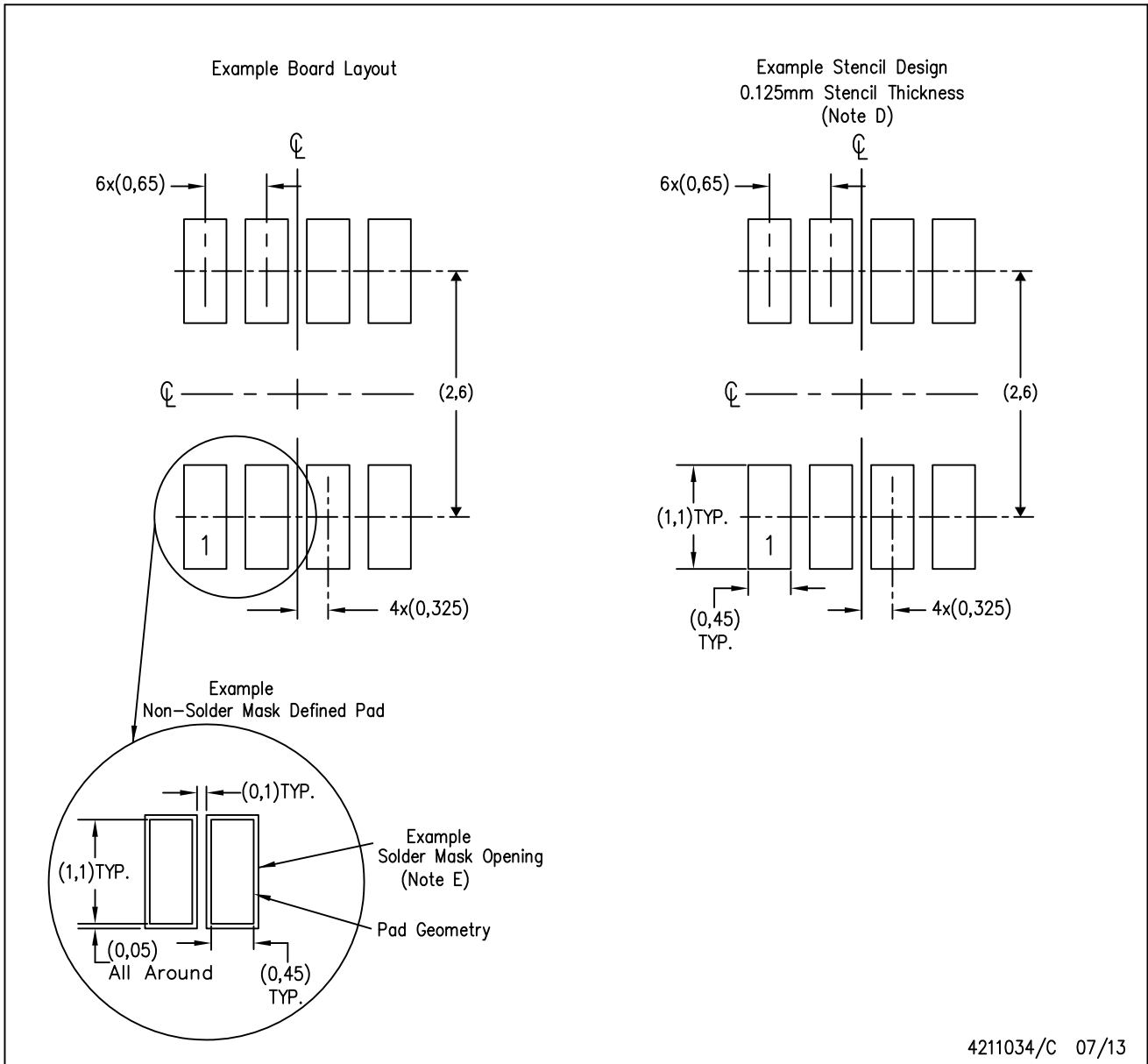


4202106/D 11/2009

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
  - D. Package outline inclusive of solder plating.
  - E. A visual index feature must be located within the Pin 1 index area.
  - F. Falls within JEDEC MO-178 Variation BA.
  - G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

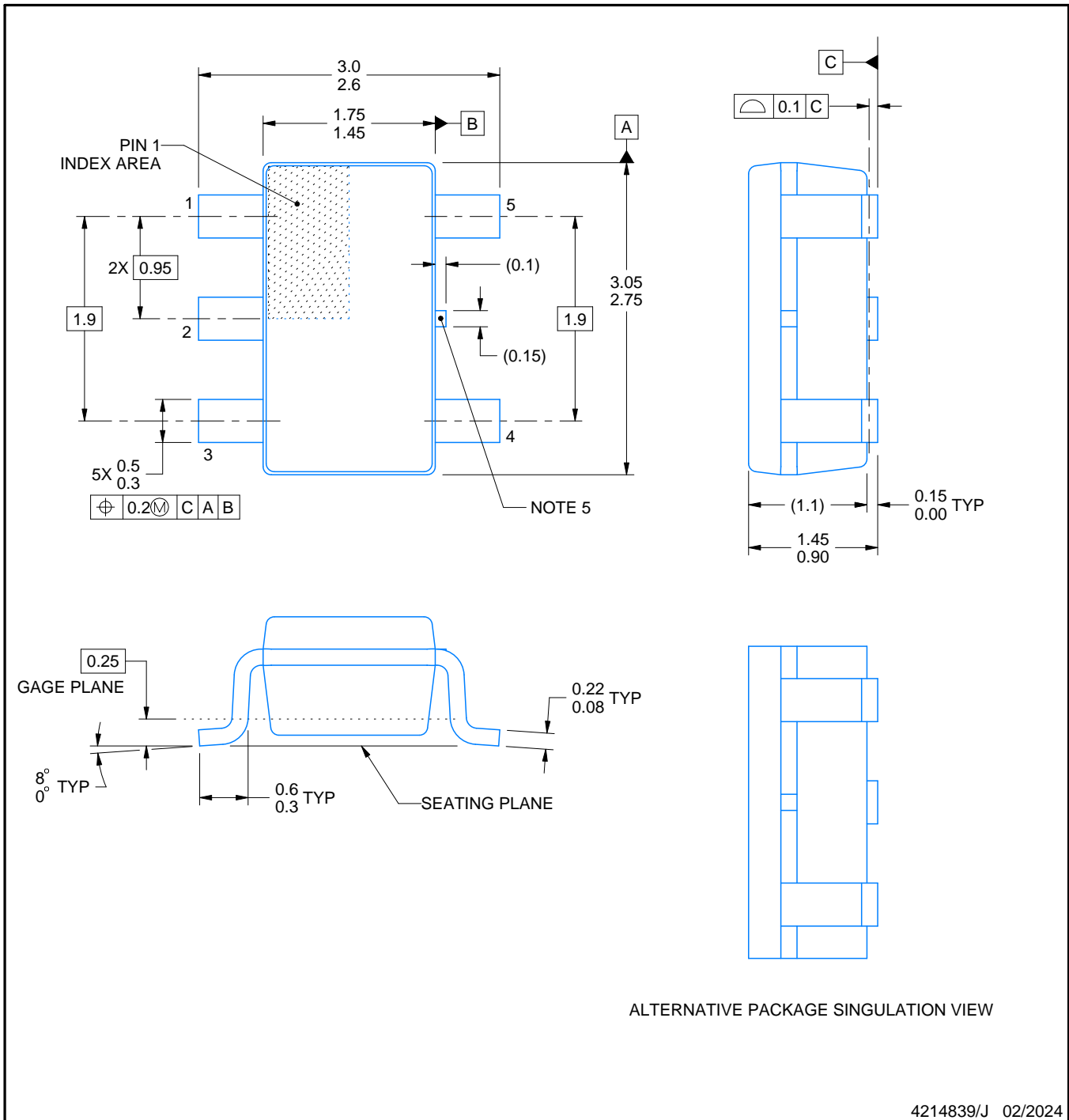
# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/J 02/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

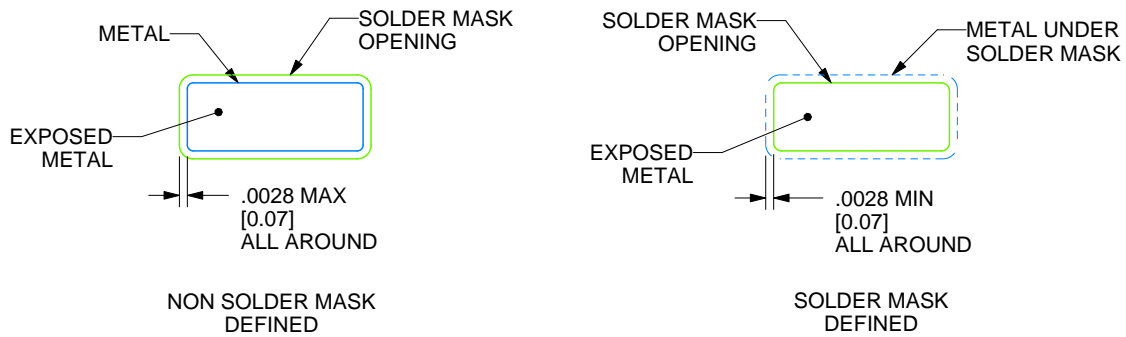
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

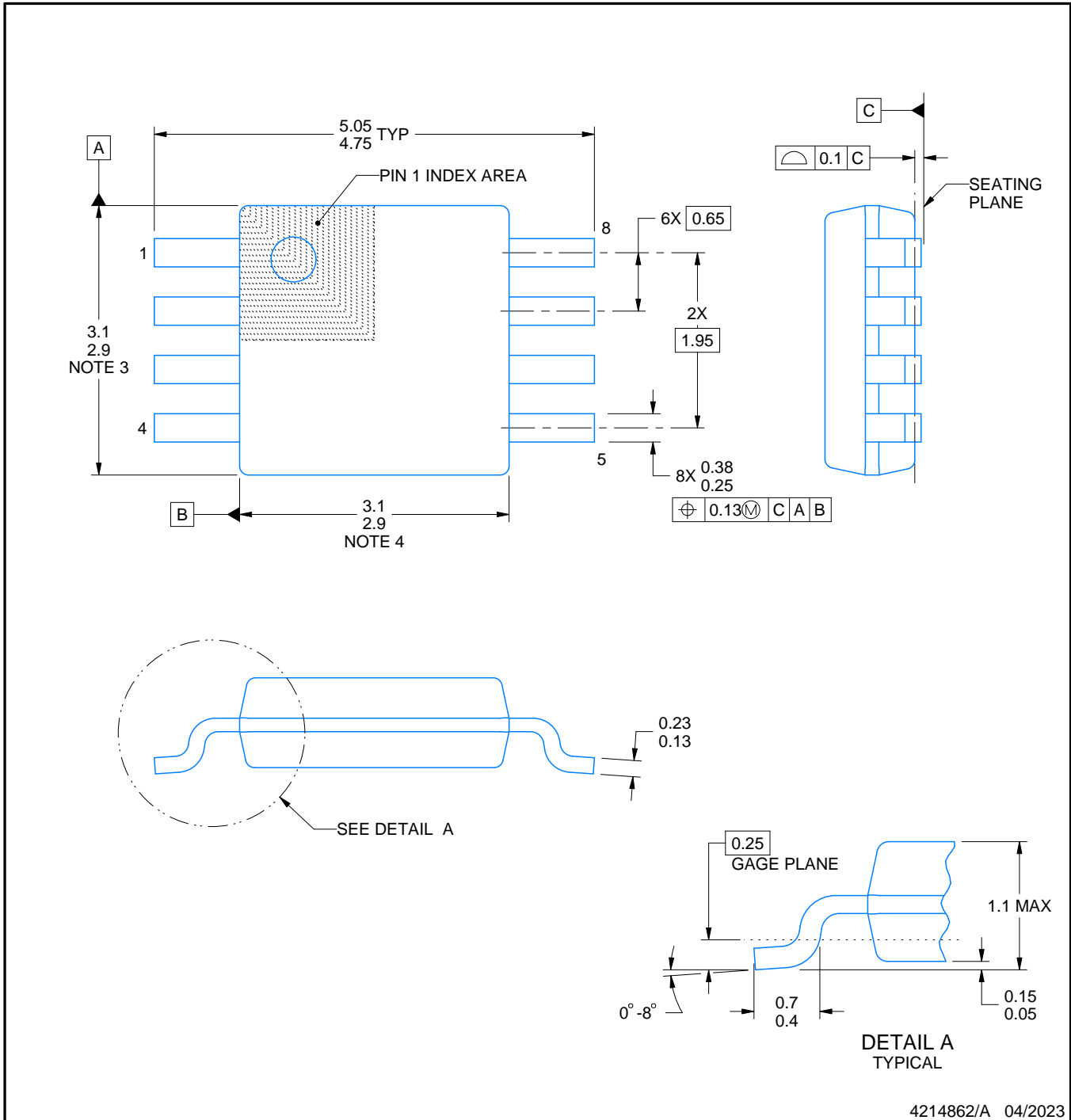
# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

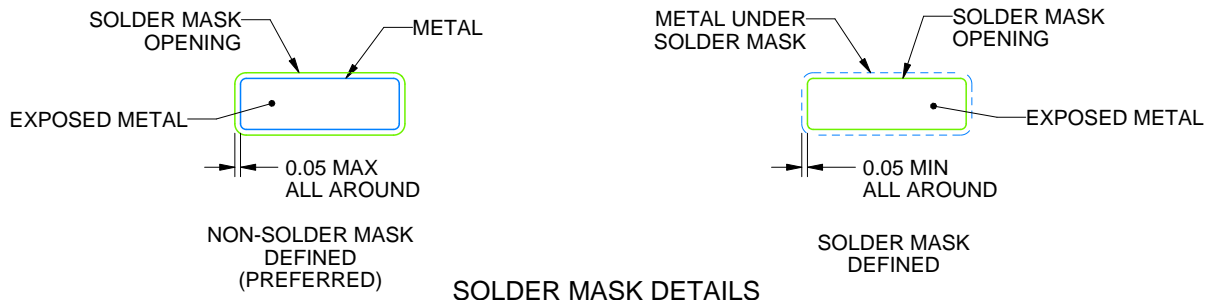
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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