



# THE DATASHEET OF AON7408



### General Description

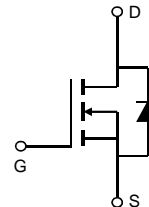
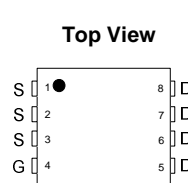
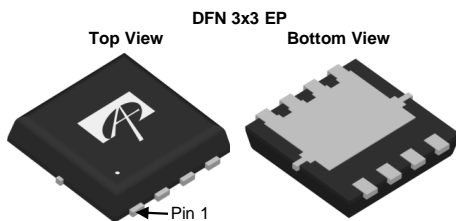
- The AON7408 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is suitable for use in general purpose applications.

- RoHS and Halogen-Free Compliant

### Product Summary

$V_{DS}$	30V
$I_D$ (at $V_{GS}=10V$ )	18A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 20m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	< 32m $\Omega$

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B</sup>	$I_D$	$T_C=25^\circ\text{C}$	18
		$T_C=100^\circ\text{C}$	11.5
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	64	A
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	$T_A=25^\circ\text{C}$	10
		$T_A=70^\circ\text{C}$	8
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	11
		$T_C=100^\circ\text{C}$	4.5
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup> $t \leq 10s$	$R_{\theta JA}$	25	40	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient <sup>A</sup> Steady-State		62	75	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case <sup>B</sup> Steady-State	$R_{\theta JC}$	8.8	11	$^\circ\text{C}/\text{W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.5	2.1	2.6	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	64			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =10A T <sub>J</sub> =125°C		15.3	20	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A		22.7	32	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =10A		17		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.75	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				12	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		373	448	pF
C <sub>oss</sub>	Output Capacitance			67		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			41		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.6	1.8	2.8	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =10A		7.1	8.6	nC
Q <sub>gs</sub>	Gate Source Charge			1.2		nC
Q <sub>gd</sub>	Gate Drain Charge			1.6		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =1.5Ω, R <sub>GEN</sub> =3Ω		4.3		ns
t <sub>r</sub>	Turn-On Rise Time			2.8		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			15.8		ns
t <sub>f</sub>	Turn-Off Fall Time			3		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =10A, dI/dt=100A/μs		10.5	12.6	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =10A, dI/dt=100A/μs		4.5		nC

A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25° C. The power dissipation P<sub>D</sub> and current rating I<sub>DSM</sub> are based on T<sub>J(MAX)</sub>=150° C, using t ≤ 10s junction-to-ambient thermal resistance.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

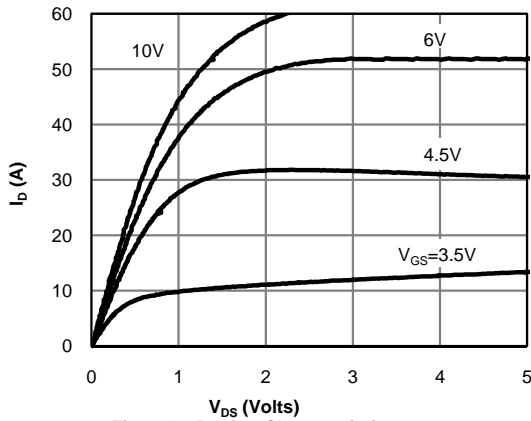
F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

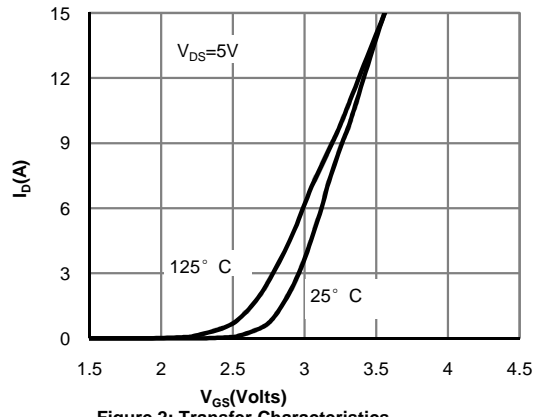
H: The maximum current rating is limited by bond-wires.

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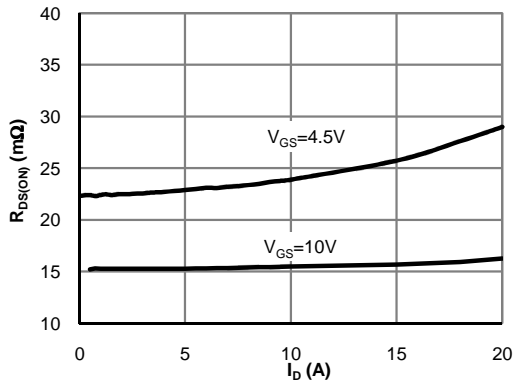
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



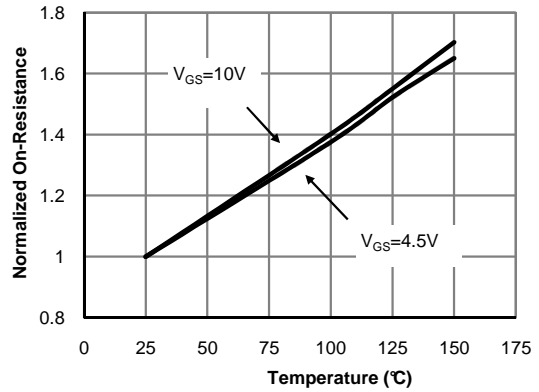
**Fig 1: On-Region Characteristics**



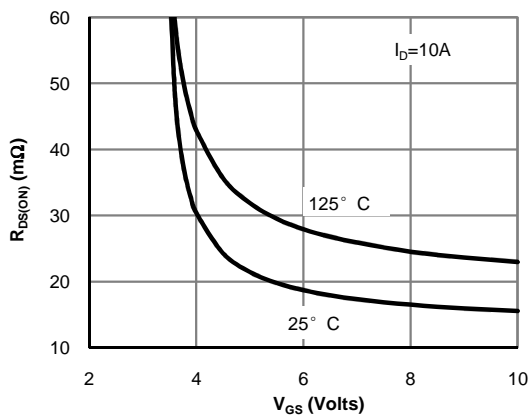
**Figure 2: Transfer Characteristics**



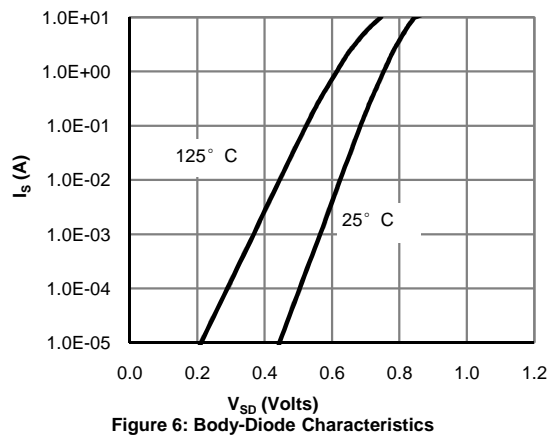
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**

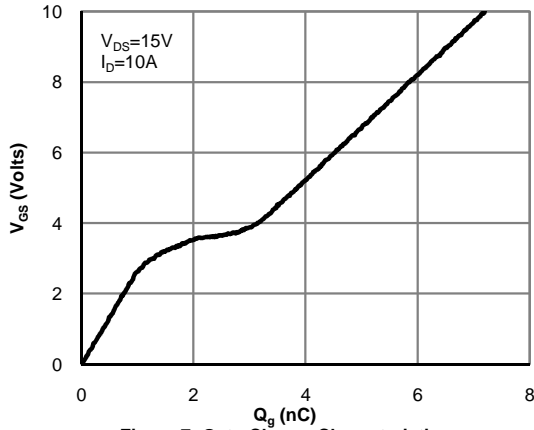


**Figure 5: On-Resistance vs. Gate-Source Voltage**

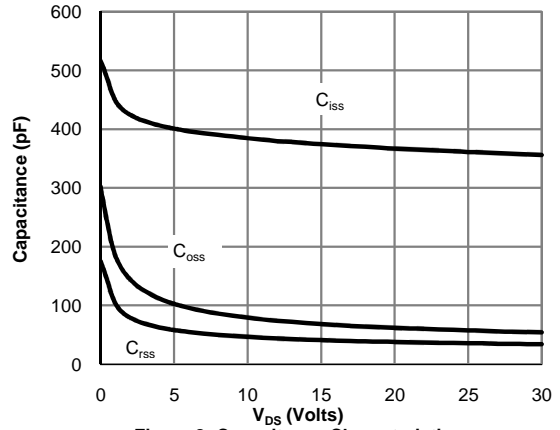


**Figure 6: Body-Diode Characteristics**

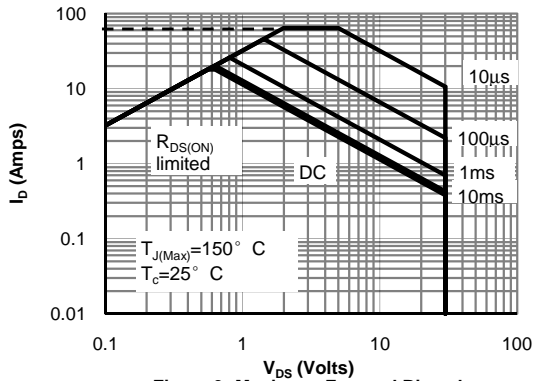
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



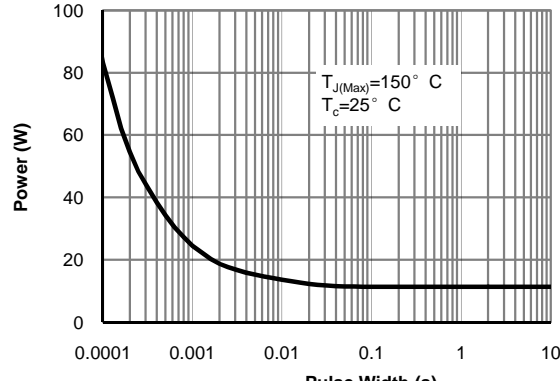
**Figure 7: Gate-Charge Characteristics**



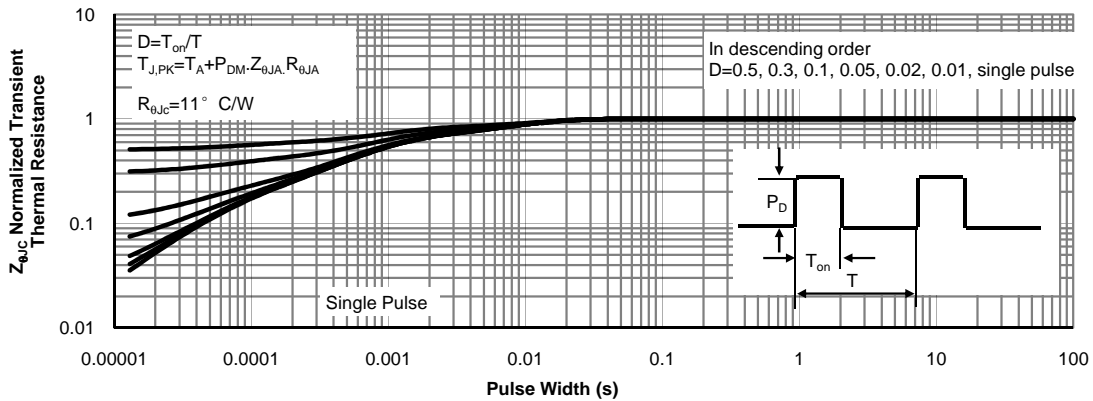
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note H)**



**Figure 10: Single Pulse Power Rating Junction-to-C: (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

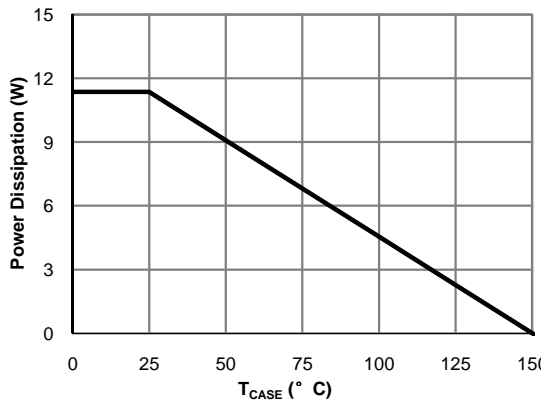


Figure 12: Power De-rating (Note F)

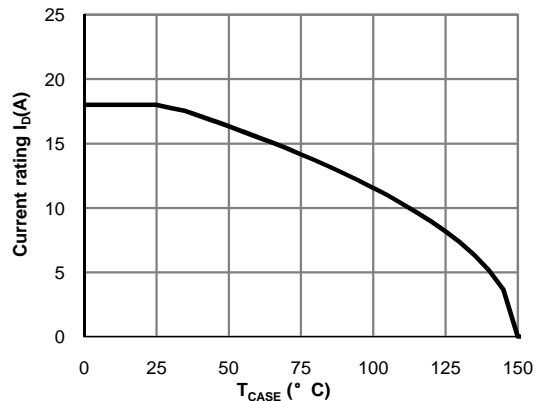


Figure 13: Current De-rating (Note F)

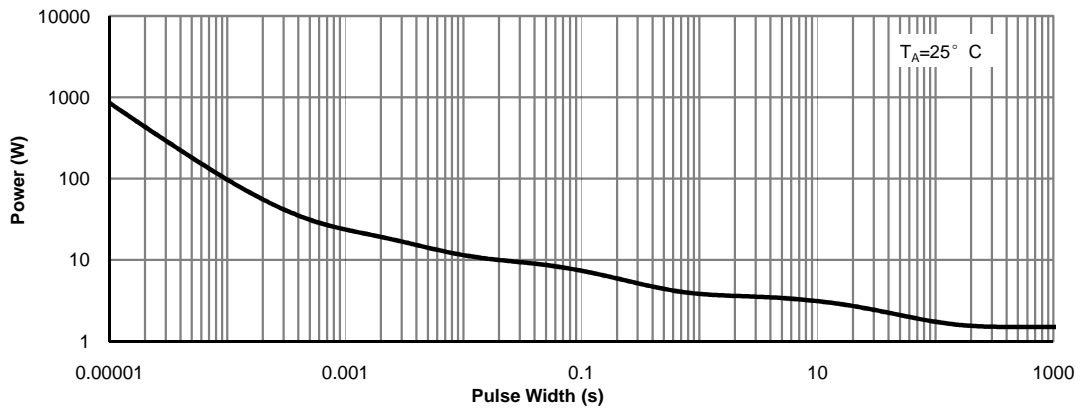


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

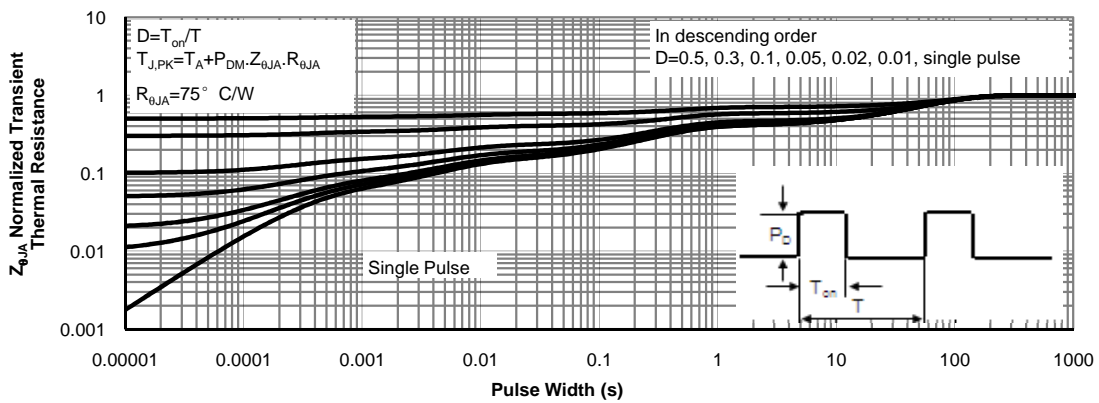
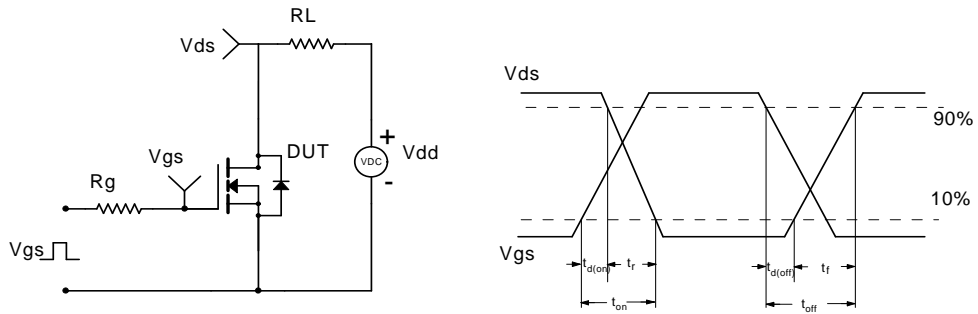


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

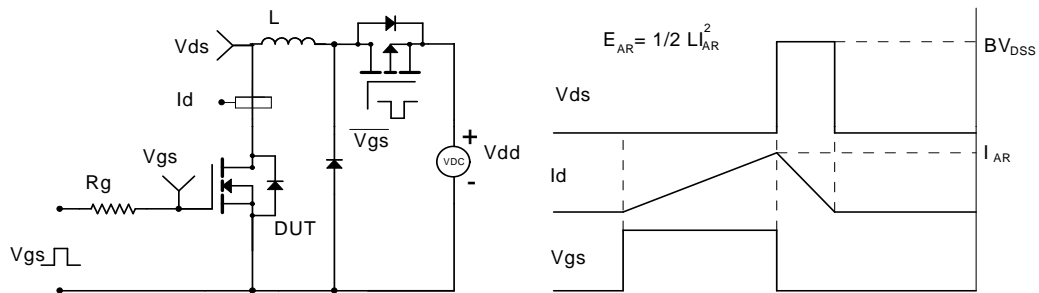
**Gate Charge Test Circuit & Waveform**



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