



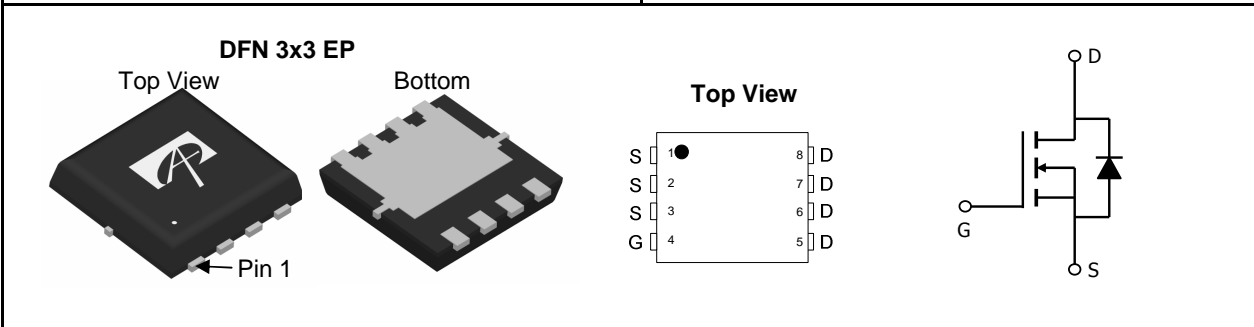
**THE DATASHEET OF  
AON7430**





**AON7430**  
**30V N-Channel MOSFET**

General Description	Features
<p>The AON7430 uses advanced trench technology to provide excellent <math>R_{DS(ON)}</math> with low gate charge. This device is suitable for high side switch in SMPS and general purpose applications.</p>	<p> <math>V_{DS}</math> (V) = 30V  <math>I_D</math> = 34A (<math>V_{GS} = 10V</math>)  <math>R_{DS(ON)} &lt; 12m\Omega</math> (<math>V_{GS} = 10V</math>)  <math>R_{DS(ON)} &lt; 16m\Omega</math> (<math>V_{GS} = 4.5V</math>)                 </p> <p>100% UIS Tested 100% <math>R_g</math> Tested</p>



**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	34
		$T_C=100^\circ C$	21
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	80	A
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	$T_A=25^\circ C$	13
		$T_A=70^\circ C$	10.2
Avalanche Current <sup>C</sup>	$I_{AR}$	22	A
Repetitive avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AR}$	24	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	23
		$T_C=100^\circ C$	9
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ C$	3.1
		$T_A=70^\circ C$	2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10s$	30	40
		Steady-State	60	75
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	4.5	5.4	$^\circ C/W$

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1.5	1.9	2.5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	80			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=20\text{A}$ $T_J=125^\circ\text{C}$		10 16	12 19	m $\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=20\text{A}$		13	16	
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=20\text{A}$		45		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.7	1	V
$I_S$	Maximum Body-Diode Continuous Current				25	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=15\text{V}$ , $f=1\text{MHz}$	610	760	910	pF
$C_{oss}$	Output Capacitance		88	125	160	pF
$C_{rss}$	Reverse Transfer Capacitance		40	70	100	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$	0.8	1.6	2.4	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $I_D=20\text{A}$	11	14	17	nC
$Q_g(4.5\text{V})$	Total Gate Charge		5	6.6	8	nC
$Q_{gs}$	Gate Source Charge		1.9	2.4	2.9	nC
$Q_{gd}$	Gate Drain Charge		1.8	3	4.2	nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $R_L=0.75\Omega$ , $R_{GEN}=3\Omega$		4.4		ns
$t_r$	Turn-On Rise Time			9		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
$t_f$	Turn-Off Fall Time			6		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=20\text{A}$ , $dI/dt=500\text{A}/\mu\text{s}$	5.6	7	8	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$ , $dI/dt=500\text{A}/\mu\text{s}$	6.4	8	9.6	nC

A. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$ ,  $t \leq 10\text{s}$  value and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $150^\circ\text{C}$  may be used if the PCB allows it.

B. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=150^\circ\text{C}$ .

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

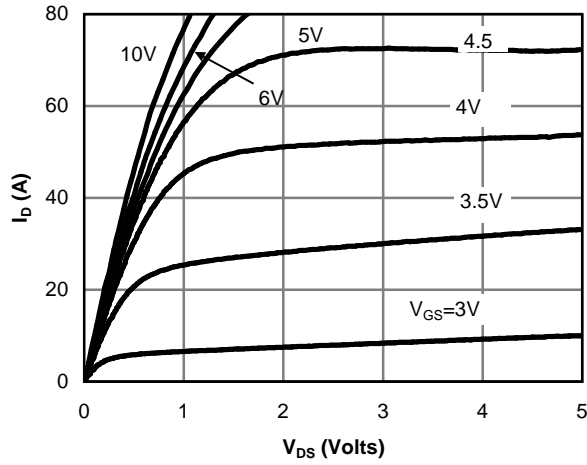


Fig 1: On-Region Characteristics

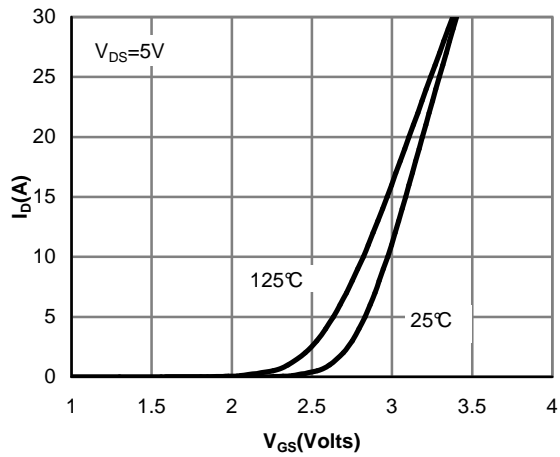


Figure 2: Transfer Characteristics

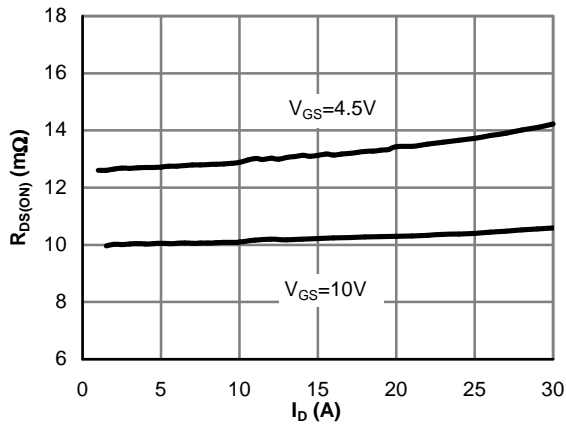


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

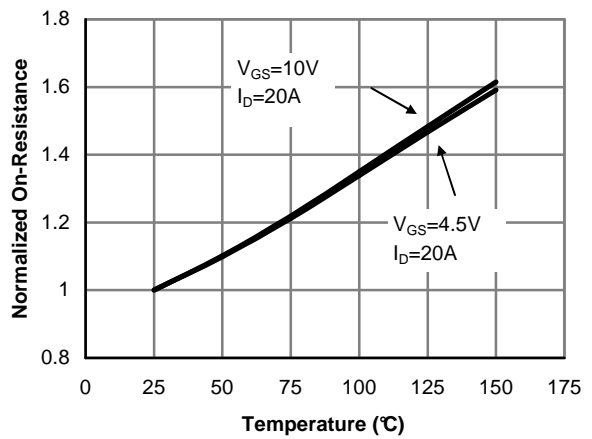


Figure 4: On-Resistance vs. Junction Temperature

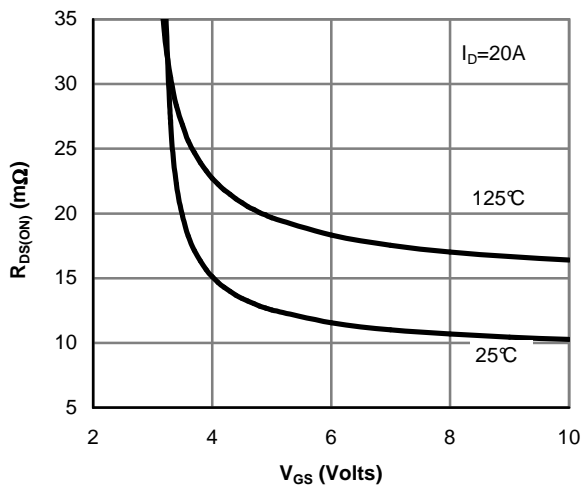


Figure 5: On-Resistance vs. Gate-Source Voltage

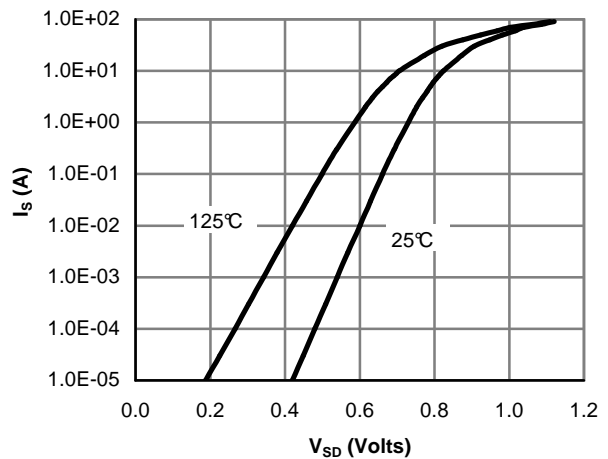


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

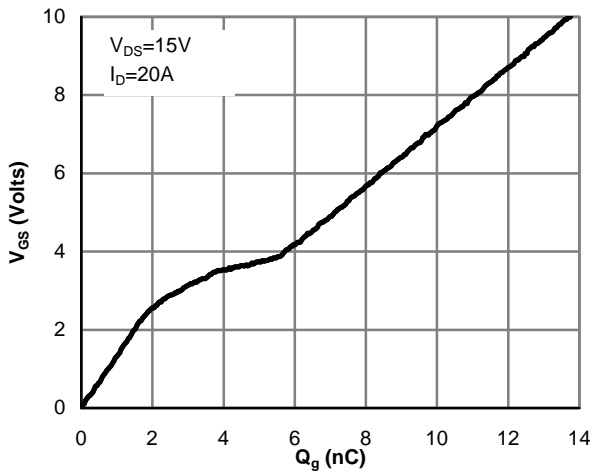


Figure 7: Gate-Charge Characteristics

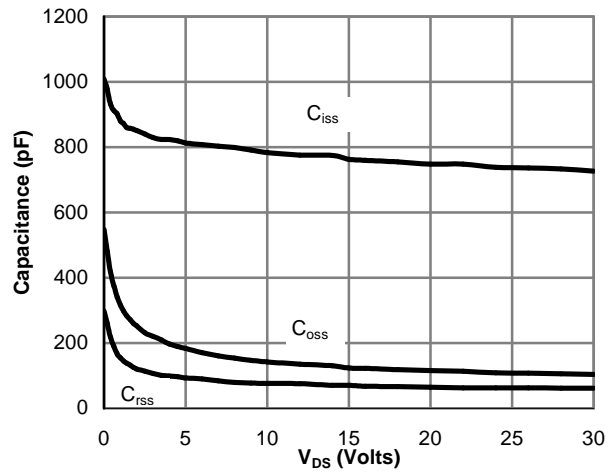


Figure 8: Capacitance Characteristics

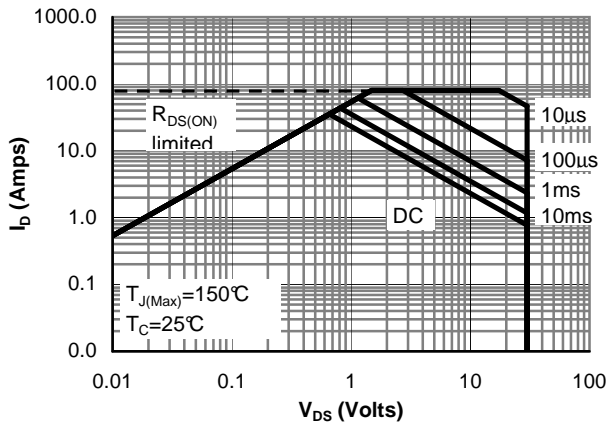


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

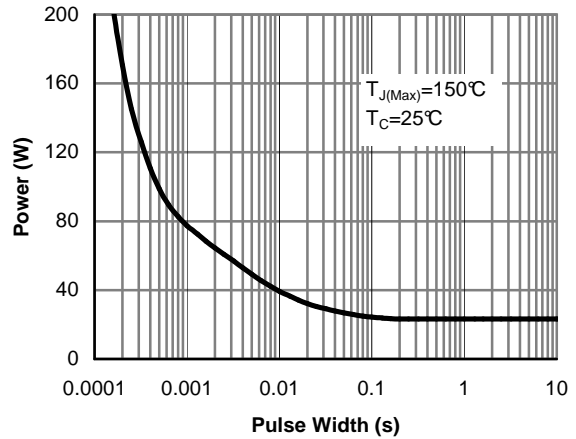


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

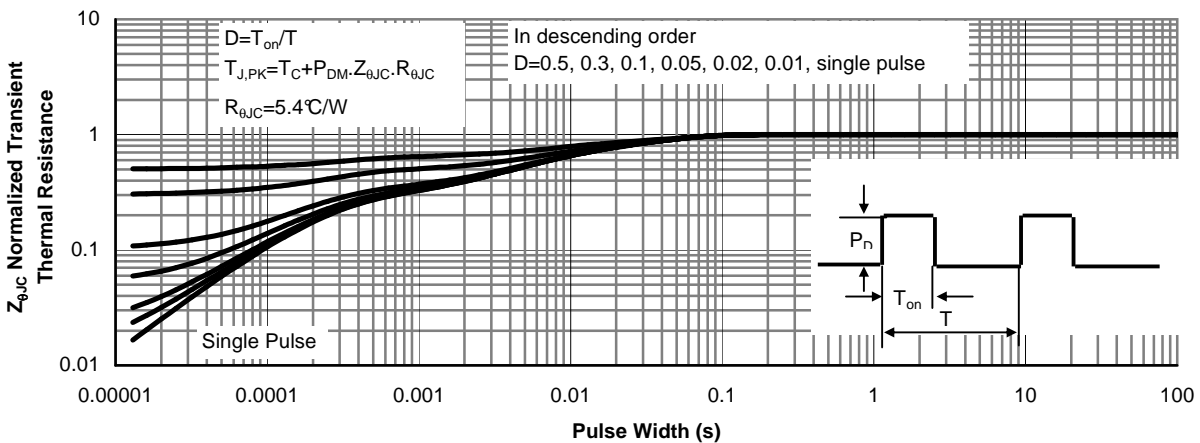


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

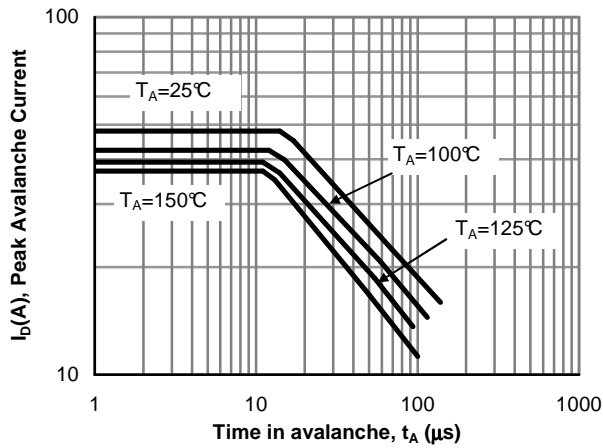


Figure 12: Single Pulse Avalanche capability (Note C)

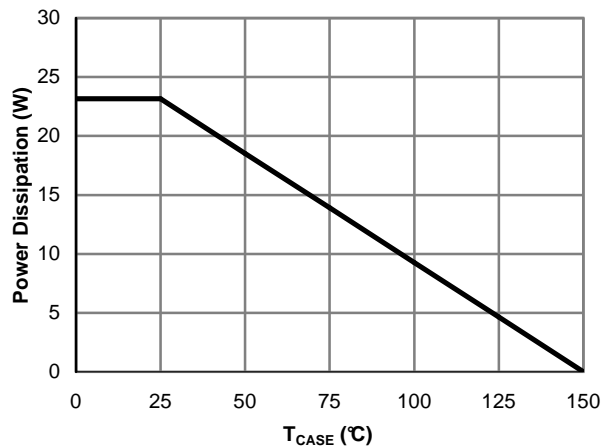


Figure 13: Power De-rating (Note F)

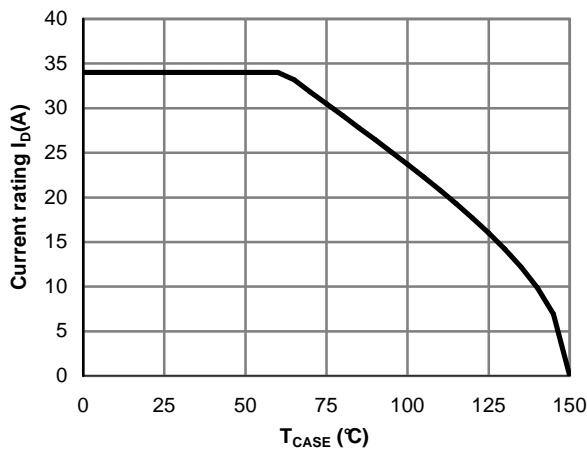


Figure 14: Current De-rating (Note F)

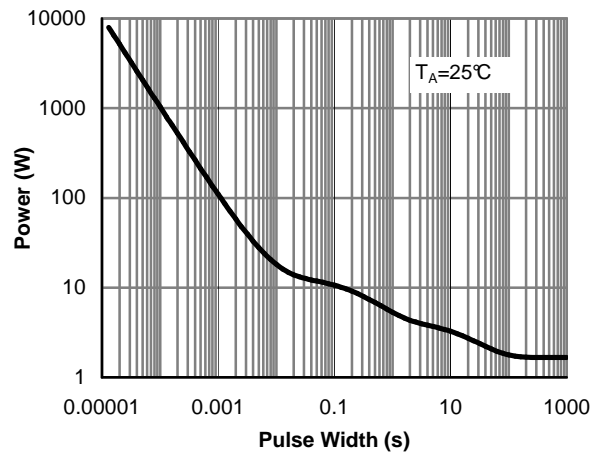


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

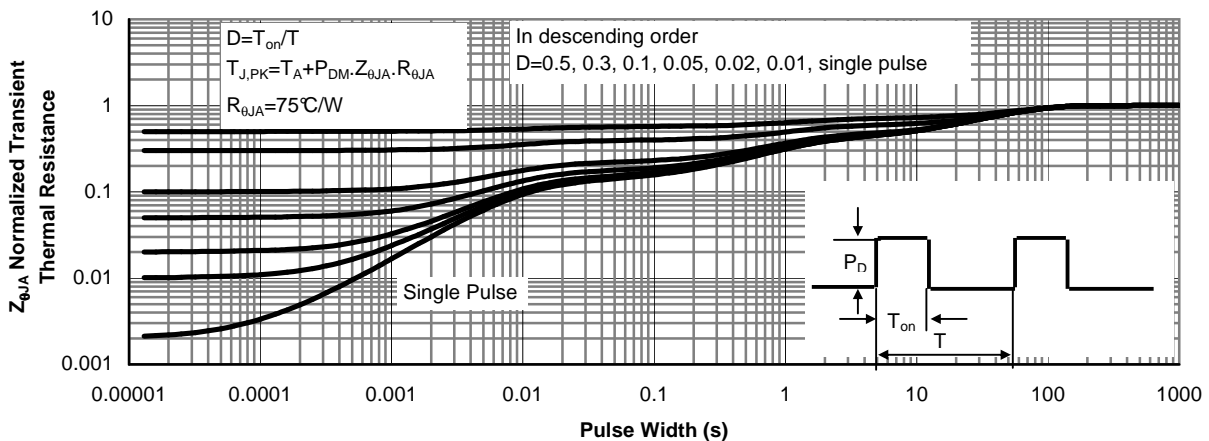
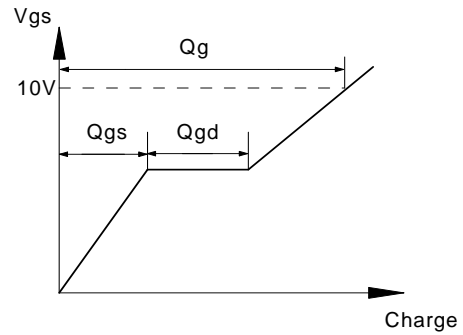
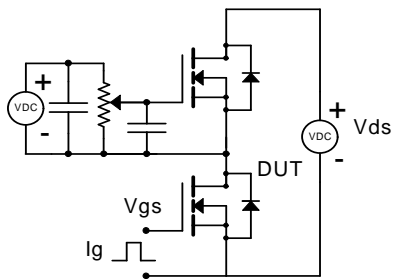
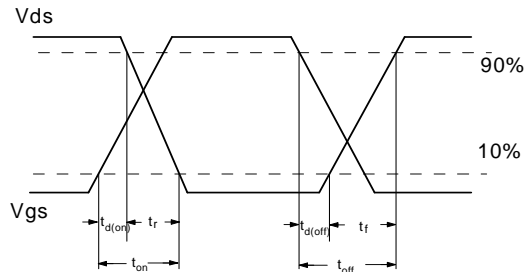
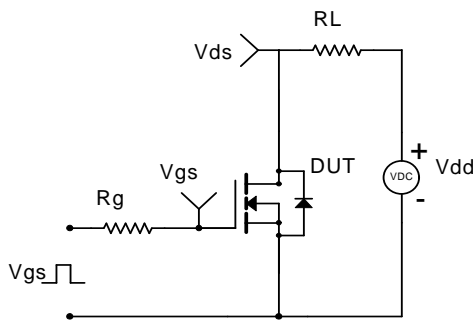


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

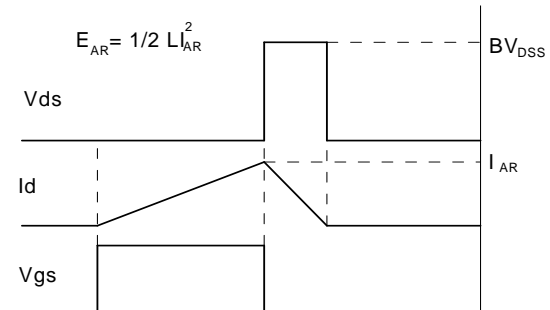
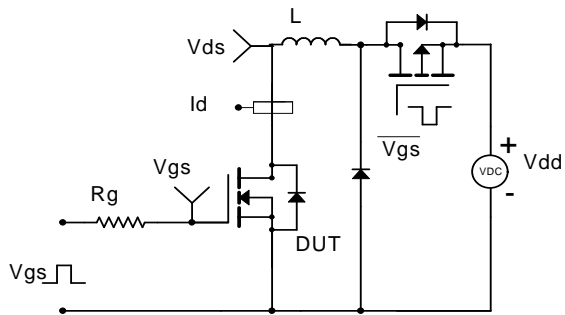
Gate Charge Test Circuit & Waveform



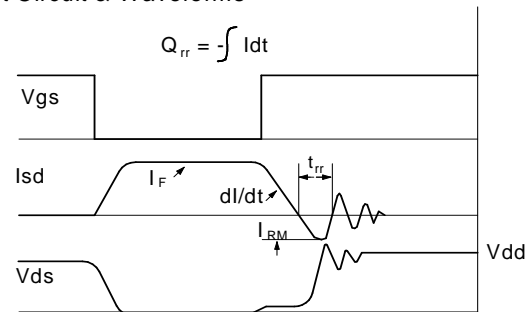
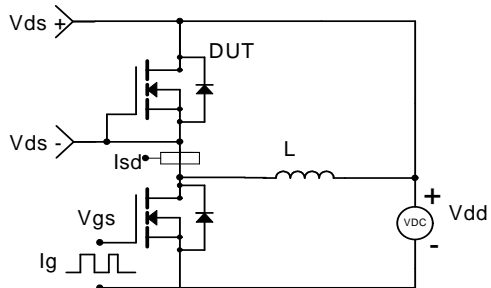
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms



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