THE DATASHEET OF

ADM8693ARU

Microprocessor Supervisory Circuits

Data Sheet

ADM8690/ADM8691/ADM8695

FEATURES

- **Upgrade for the ADM690, ADM691, ADM695 and for the MAX690, MAX691, MAX695**
- **Specified over temperature**
- **Low power consumption: 0.7 mW**
- **Precision voltage monitor**
- **Reset assertion down to 1 V V_{CC}**
- **Low switch on resistance: 0.7 Ω normal, 7 Ω in backup**
- **High current drive: 100 mA**
- **Watchdog timer: 100 ms, 1.6 sec, or adjustable**
- **Standby current: 400 nA**
- **Automatic battery backup power switching**
- **Extremely fast gating of chip enable signals (3 ns)**
- **Voltage monitor for power fail**
- **Available in TSSOP package**

APPLICATIONS

- **Microprocessor systems**
- **Computers**
- **Controllers**
- **Intelligent instruments**
- **Automotive systems**

PRODUCT HIGHLIGHTS

The ADM8690 is available in 8-lead PDIP and SOIC packages and provides the following functions:

1. Power-on reset output during power-up, power-down, and brownout conditions. The $\overline{\text{RESET}}$ output remains operational with V_{CC} as low as 1 V.
2. Battery backup switching for CMOS RAM, CMOS microprocessor, or other low power logic.
3. Reset pulse if the optional watchdog timer is not toggled within a specified time.
4. 1.3 V threshold detector for power-fail warning, low battery detection, or to monitor a power supply other than 5 V.

The ADM8691 and ADM8695 are available in 16-lead PDIP and small outline packages (including TSSOP) and provide three additional functions:

1. Write protection of CMOS RAM or EEPROM.
2. Adjustable reset and watchdog timeout periods.
3. Separate watchdog timeout, backup battery switchover, and low V_{CC} status outputs.

FUNCTIONAL BLOCK DIAGRAMS

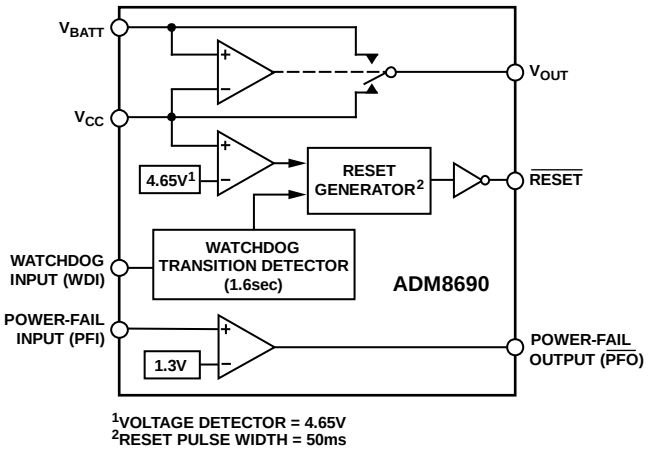

Figure 1. ADM8690

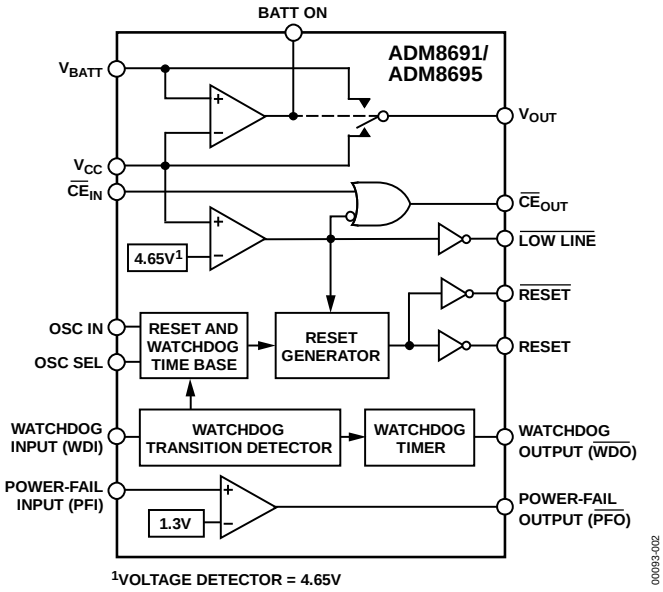

Figure 2. ADM8691/ADM8695

Rev. C

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REVISION HISTORY

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6/11—Rev. A to Rev. B

Deleted ADM8694 ... Throughout
Updated Figure 11, Figure 12, and Figure 13 ... 9
Updated Outline Dimensions ... 18

9/06—Rev. 0 to Rev. A

Updated Format ... Universal
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2/97—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM8690/ADM8691/ADM8695 supervisory circuits offer complete single-chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include microprocessor reset, backup battery switchover, watchdog timer, CMOS RAM write protection, and power failure warning. The complete family provides a variety of configurations to satisfy most microprocessor system requirements.

The ADM8690/ADM8691/ADM8695 are fabricated using an advanced epitaxial CMOS process that combines low power consumption (0.7 mW), extremely fast chip enable gating (3 ns), and high reliability. $\overline{\text{RESET}}$ assertion is guaranteed with V_{CC} as low as 1 V. In addition, the power switching circuitry is designed for minimal voltage drop, thereby permitting increased output current drive of up to 100 mA without the need for an external pass transistor.

See Table 1 for a product selection guide listing the characteristics of each device. To place an order, see the Ordering Guide.

Table 1. Product Selection Guide

Part No.	Nominal Reset Time	Nominal V_{CC} Reset Threshold	Nominal Watchdog Timeout Period	Battery Backup Switching	Base Drive, Ext PNP	Chip Enable Signals
ADM8690	50 ms	4.65 V	1.6 sec	Yes	No	No
ADM8691	50 ms or ADJ	4.65 V	100 ms, 1.6 sec, ADJ	Yes	Yes	Yes
ADM8695	200 ms or ADJ	4.65 V	100 ms, 1.6 sec, ADJ	Yes	Yes	Yes

SPECIFICATIONS

V_{CC} = full operating range, V_{BATT} = 2.8 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BATTERY BACKUP SWITCHING					
V_{CC} Operating Voltage Range	4.75		5.5	V	
V_{BATT} Operating Voltage Range	2.0		4.25	V	
V_{OUT} Output Voltage	V_{CC} − 0.005	V_{CC} − 0.0025		V	I_{OUT} = 1 mA
	V_{CC} − 0.2	V_{CC} − 0.125		V	I_{OUT} ≤ 100 mA
V_{OUT} in Battery Backup Mode	V_{BATT} − 0.005	V_{BATT} − 0.002		V	I_{OUT} = 250 µA, V_{CC} < V_{BATT} − 0.2 V
Supply Current (Excludes I_{OUT})		140	200	µA	I_{OUT} = 100 µA
Supply Current in Battery Backup Mode		0.4	1	µA	V_{CC} = 0 V, V_{BATT} = 2.8 V
Battery Standby Current					5.5 V > V_{CC} > V_{BATT} + 0.2 V
+ = Discharge, − = Charge	−0.1		+0.02	µA	T_A = 25°C
Battery Switchover Threshold		70		mV	Power-up
V_{CC} − V_{BATT}		50		mV	Power-down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.3	V	I_{SINK} = 3.2 mA
BATT ON Output Short-Circuit Current		55		mA	BATT ON = V_{OUT} = 4.5 V, sink current
	0.5	2.5	25	µA	BATT ON = 0 V, source current
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold	4.5	4.65	4.73	V	
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay					
ADM8690 and ADM8691	35	50	70	ms	OSC SEL = high
ADM8695	140	200	280	ms	OSC SEL = high
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	Seconds	Long period
	70	100	140	ms	Short period
Watchdog Timeout Period, External Clock	3840	4064	4097	Cycles	Long period
	768	1011	1025	Cycles	Short period
Minimum WDI Input Pulse Width	50			ns	V_{IL} = 0.4 V, V_{IH} = 3.5 V
$\overline{\text{RESET}}$ Output Voltage at V_{CC} = 1 V		4	20	mV	I_{SINK} = 10 µA, V_{CC} = 1 V
$\overline{\text{RESET}}$, $\overline{\text{LOW LINE}}$ Output Voltage		0.05	0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 4.25 V
	3.5			V	I_{SOURCE} = 1 µA
$\overline{\text{RESET}}$, $\overline{\text{WDO}}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA
	3.5			V	I_{SOURCE} = 1 µA
Output Short-Circuit Source Current	1	10	25	µA	
Output Short-Circuit Sink Current		25		mA	
WDI Input Threshold[1]					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		1	10	µA	WDI = V_{OUT}
	−10	−1		µA	WDI = 0 V
POWER-FAIL DETECTOR					
PFI Input Threshold	1.25	1.3	1.35	V	V_{CC} = 5 V
PFI Input Current	−25	±0.01	+25	nA	
$\overline{\text{PFO}}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	3.5			V	I_{SOURCE} = 1 µA
$\overline{\text{PFO}}$ Short-Circuit Source Current	1	3	25	µA	PFI = low, $\overline{\text{PFO}}$ = 0 V
$\overline{\text{PFO}}$ Short-Circuit Sink Current		25		mA	PFI = high, $\overline{\text{PFO}}$ = V_{OUT}

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CHIP ENABLE GATING					
$\overline{CE}_{IN}$ Threshold			0.8	V	V_{IL}
	3.0			V	V_{IH}
$\overline{CE}_{IN}$ Pull-Up Current		3		µA	
$\overline{CE}_{OUT}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	V_{OUT} − 1.5			V	I_{SOURCE} = 3.0 mA
	V_{OUT} − 0.05			V	I_{SOURCE} = 1 µA, V_{CC} = 0 V
$\overline{CE}$ Propagation Delay		3	7	ns	
OSCILLATOR					
OSC IN Input Current		±2		µA	
OSC SEL Input Pull-Up Current		5		µA	
OSC IN Frequency Range	0		500	kHz	OSC SEL = 0 V
OSC IN Frequency with External Capacitor		4		kHz	OSC SEL = 0 V, C_{OSC} = 47 pF

[1] WDI is a three-level input that is internally biased to 38% of V_{CC} and has an input impedance of approximately 5 MΩ.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
V_{BATT}	−0.3 V to +6 V
All Other Inputs	−0.3 V to V_{OUT} + 0.5 V
Input Current	
V_{CC}	200 mA
V_{BATT}	50 mA
GND	20 mA
Digital Output Current	20 mA
Power Dissipation, 8-Lead PDIP	400 mW
θ_{JA} Thermal Impedance	120°C/W
Power Dissipation, 8-Lead SOIC	400 mW
θ_{JA} Thermal Impedance	120°C/W
Power Dissipation, 16-Lead PDIP	600 mW
θ_{JA} Thermal Impedance	135°C/W
Power Dissipation, 16-Lead TSSOP	600 mW
θ_{JA} Thermal Impedance	158°C/W
Power Dissipation, 16-Lead SOIC_N	600 mW
θ_{JA} Thermal Impedance	110°C/W
Power Dissipation, 16-Lead SOIC_W	600 mW
θ_{JA} Thermal Impedance	73°C/W
Operating Temperature Range	
Industrial (A Version)	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

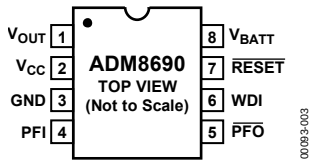


Figure 3. ADM8690 Pin Configuration, 8-Lead PDIP and 8-Lead SOIC_N

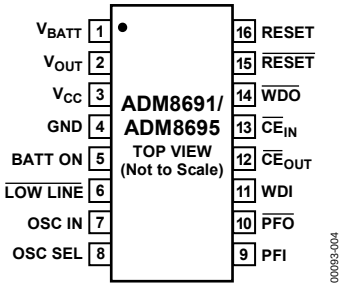


Figure 4. ADM8691/ADM8695 Pin Configuration, 16-Lead PDIP, 16-Lead SOIC_N, 16-Lead SOIC_W, and 16-Lead TSSOP

Table 4. Pin Function Descriptions

Pin No.			
8-Lead	**16-Lead**	**Mnemonic**	**Description**
8	1	V_{BATT}	Backup Battery Input. V_{BATT} or V_{CC} is internally switched to V_{OUT}, depending on which is at the highest potential.
1	2	V_{OUT}	Output Voltage. V_{CC} or V_{BATT} is internally switched to V_{OUT}, depending on which is at the highest potential. V_{OUT} can supply up to 100 mA to power CMOS RAM. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
2	3	V_{CC}	Power Supply Input. 5 V nominal. V_{CC} or V_{BATT} is internally switched to V_{OUT}, depending on which is at the highest potential.
3	4	GND	Ground. This is the 0 V ground reference for all signals.
N/A	5	BATT ON	Logic Output. BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 35 mA and can directly drive the base of an external PNP transistor to increase the output current above the 100 mA rating of V_{OUT}.
N/A	6	$\overline{\text{LOW LINE}}$	Logic Output. $\overline{\text{LOW LINE}}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold.
N/A	7	OSC IN	Oscillator Logic Input. When OSC SEL is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. This sets both the reset active pulse timing and the watchdog timeout period (see Table 5 and Figure 17 through Figure 20). When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 50 ms typical (ADM8691) or 200 ms typical (ADM8695). In this mode, the OSC IN pin selects either the fast (100 ms) or slow (1.6 sec) watchdog timeout period. In both modes, the timeout period immediately after a reset is 1.6 sec typical.
N/A	8	OSC SEL	Logic Oscillator Select Input. When OSC SEL is unconnected (floating) or driven high, the internal oscillator sets the reset active time and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled (see Table 5). OSC SEL has a 5 µA internal pull-up.
4	9	PFI	Power-Fail Input. PFI is the noninverting input to the power-fail comparator. When PFI is less than 1.3 V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND or V_{OUT} when not used.
5	10	$\overline{\text{PFO}}$	Power-Fail Output. $\overline{\text{PFO}}$ is the output of the power-fail comparator. It goes low when PFI is less than 1.3 V. The comparator is turned off and $\overline{\text{PFO}}$ goes low when V_{CC} is below V_{BATT}.
6	11	WDI	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ pulses low and $\overline{\text{WDO}}$ goes low. The timer is reset with each transition on the WDI line. The watchdog timer can be disabled if WDI is left floating or is driven to midsupply.
N/A	12	$\overline{\text{CE}}_{OUT}$	Logic Output. $\overline{\text{CE}}_{OUT}$ is a gated version of the $\overline{\text{CE}}_{IN}$ signal. $\overline{\text{CE}}_{OUT}$ tracks $\overline{\text{CE}}_{IN}$ when V_{CC} is above the reset threshold. If V_{CC} is below the reset threshold, $\overline{\text{CE}}_{OUT}$ is forced high. See Figure 21 and Figure 22.
N/A	13	$\overline{\text{CE}}_{IN}$	Logic Input. Input to the $\overline{\text{CE}}$ gating circuit. When not in use, connect this pin to GND or V_{OUT}.
N/A	14	$\overline{\text{WDO}}$	Logic Output. The watchdog output, $\overline{\text{WDO}}$, goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{\text{WDO}}$ is set high by the next transition at WDI. If WDI is unconnected or at midsupply, the watchdog timer is disabled and $\overline{\text{WDO}}$ remains high. $\overline{\text{WDO}}$ also goes high when $\overline{\text{LOW LINE}}$ goes low.

Pin No.			
8-Lead	16-Lead	Mnemonic	Description
7	15	$\overline{\text{RESET}}$	Logic Output. $\overline{\text{RESET}}$ goes low if V_{CC} falls below the reset threshold or if the watchdog timer is not serviced within its timeout period. The reset threshold is typically 4.65 V. $\overline{\text{RESET}}$ remains low for 50 ms (ADM8690/ADM8691) or 200 ms (ADM8695) after V_{CC} returns above the threshold. $\overline{\text{RESET}}$ also goes low for 50 ms (ADM8690/ADM8691) or 200 ms (ADM8695) if the watchdog timer is enabled but not serviced within its timeout period. The $\overline{\text{RESET}}$ pulse width can be adjusted on the ADM8691/ADM8695, as shown in Table 5. The $\overline{\text{RESET}}$ output has an internal 3 µA pull-up and can either connect to an open-collector reset bus or directly drive a CMOS gate without an external pull-up resistor.
N/A	16	RESET	Logic Output. RESET is an active high output. It is the inverse of $\overline{\text{RESET}}$.

TYPICAL PERFORMANCE CHARACTERISTICS

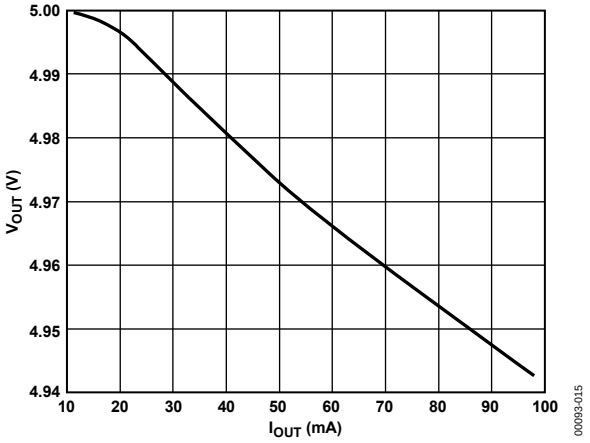


Figure 5. V_{OUT} vs. I_{OUT}, Normal Operation

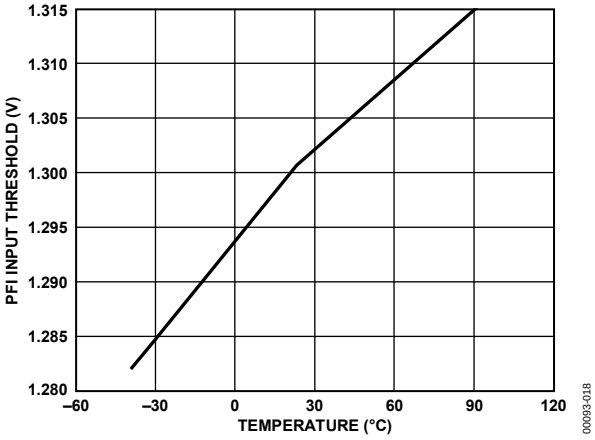


Figure 8. PFI Input Threshold vs. Temperature

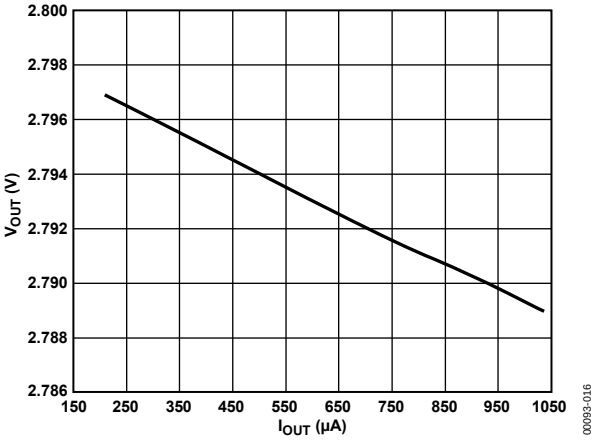


Figure 6. V_{OUT} vs. I_{OUT}, Battery Backup

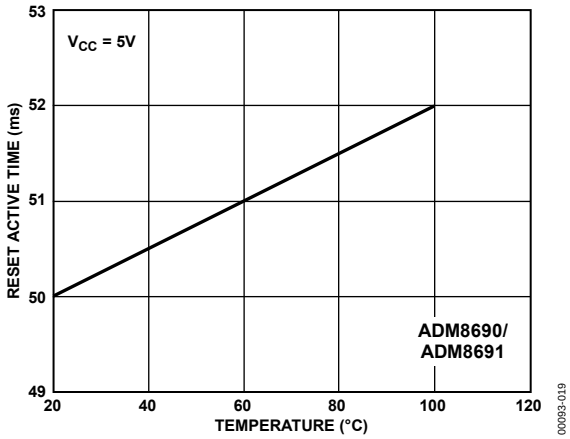


Figure 9. Reset Active Time vs. Temperature

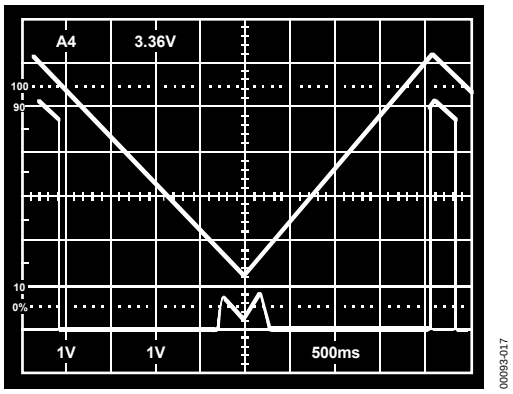


Figure 7. Reset Output Voltage vs. Supply Voltage

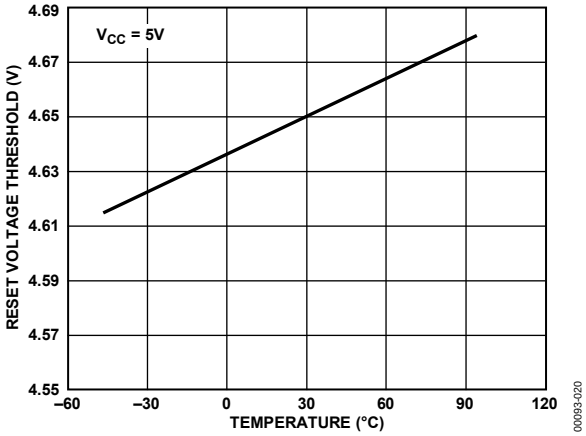


Figure 10. Reset Voltage Threshold vs. Temperature

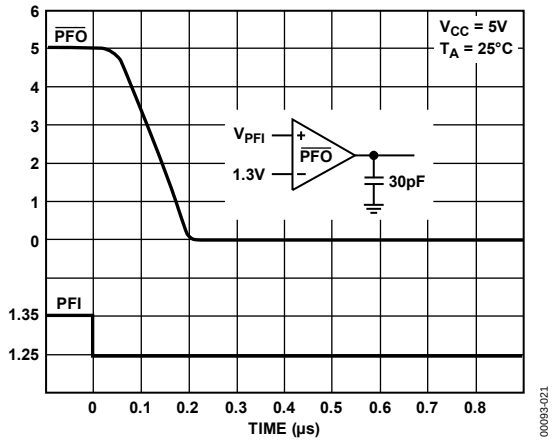


Figure 11. Power-Fail Comparator Response Time, Falling

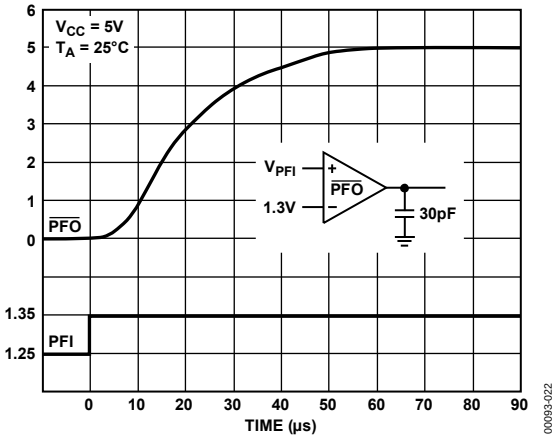


Figure 12. Power-Fail Comparator Response Time, Rising

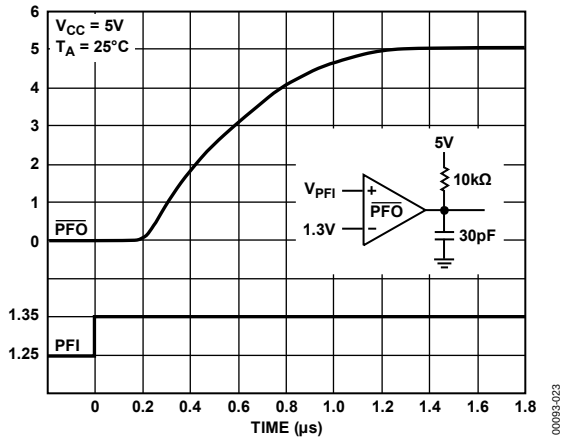


Figure 13. Power-Fail Comparator Response Time with Pull-Up Resistor

CIRCUIT INFORMATION

BATTERY SWITCHOVER SECTION

The battery switchover circuit compares V_{CC} to the V_{BATT} input and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50 mV higher than V_{BATT} as V_{CC} falls, and when V_{CC} is 70 mV greater than V_{BATT} as V_{CC} rises. This 20 mV hysteresis prevents repeated rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

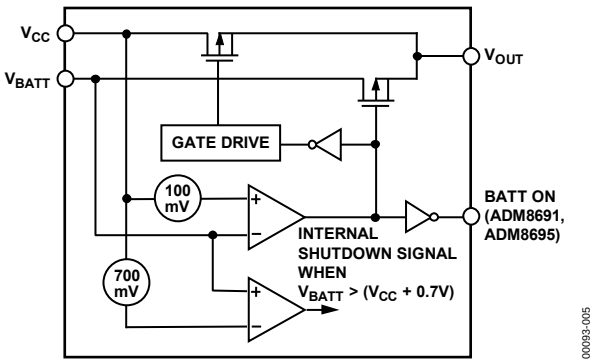


Figure 14. Battery Switchover Schematic

During normal operation, with V_{CC} higher than V_{BATT}, V_{CC} is internally switched to V_{OUT} through an internal PMOS transistor switch. This switch has a typical on resistance of 0.7 Ω and can supply up to 100 mA at the V_{OUT} terminal. V_{OUT} is normally used to drive a RAM memory bank, requiring instantaneous currents of greater than 100 mA. If this is the case, a bypass capacitor should be connected to V_{OUT}. The capacitor provides the peak current transients to the RAM. A capacitance value of 0.1 µF or greater can be used.

If the continuous output current requirements at V_{OUT} exceed 100 mA or if a lower $V_{CC} - V_{OUT}$ voltage differential is desired, an external PNP pass transistor can be connected in parallel with the internal transistor. The BATT ON output (ADM8691/ADM8695) can directly drive the base of the external transistor (see Figure 24).

A 7 Ω MOSFET switch connects the V_{BATT} input to V_{OUT} during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. The supply current in battery backup is typically 0.4 µA.

The ADM8690/ADM8691/ADM8695 operate with battery voltages from 2.0 V to 4.25 V. High value capacitors, either standard electrolytic or the farad-size, double-layer capacitors, can also be used for short-term memory backup. A small charging current of typically 10 nA (0.1 µA maximum) flows out of the V_{BATT} terminal. This current is useful for maintaining rechargeable batteries in a fully charged condition. This extends the life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup because the maximum charging current (0.1 µA) is safe for even the smallest lithium cells.

If the battery switchover section is not used, V_{BATT} should be connected to GND and V_{OUT} should be connected to V_{CC}.

POWER-FAIL $\overline{\text{RESET}}$ OUTPUT

$\overline{\text{RESET}}$ is an active low output that provides a $\overline{\text{RESET}}$ signal to the microprocessor whenever V_{CC} is at an invalid level. When V_{CC} falls below the reset threshold, the $\overline{\text{RESET}}$ output is forced low. The nominal reset voltage threshold is 4.65 V.

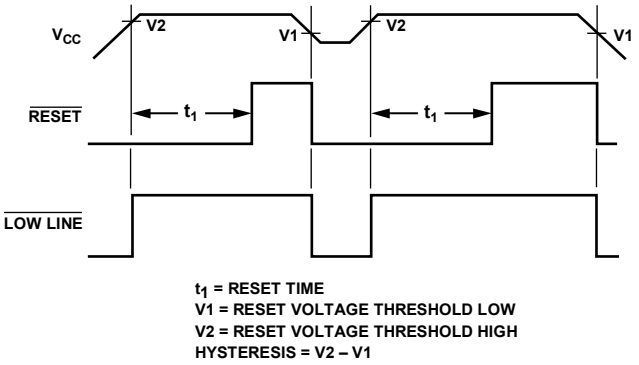


Figure 15. Power-Fail Reset Timing

On power-up, $\overline{\text{RESET}}$ remains low for 50 ms (200 ms for the ADM8695) after V_{CC} rises above the appropriate reset threshold. This allows time for the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ output remains low with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition.

The $\overline{\text{RESET}}$ active time is adjustable on the ADM8691/ADM8695 by using an external oscillator or by connecting an external capacitor to the OSC IN pin. See Table 5 and Figure 17 through Figure 20.

The guaranteed minimum and maximum reset thresholds for the ADM8690/ADM8691/ADM8695 are 4.5 V and 4.73 V. The ADM8690/ADM8691/ADM8695 are, therefore, compatible with 5 V supplies with a +10%, −5% tolerance. The reset threshold comparator typically has 40 mV of hysteresis. The response time of the reset voltage comparator is less than 1 µs. If glitches are present on the V_{CC} line that could cause spurious reset pulses, V_{CC} should be decoupled close to the device.

In addition to $\overline{\text{RESET}}$, the ADM8691/ADM8695 provide an active high RESET output. This output is the complement of $\overline{\text{RESET}}$ and is intended for processors that require an active high reset signal.

WATCHDOG TIMER $\overline{\text{RESET}}$

The watchdog timer circuit monitors the activity of the microprocessor to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the watchdog input (WDI) line. If this line is not toggled within the selected timeout period, a $\overline{\text{RESET}}$ pulse is generated.

The nominal watchdog timeout period is preset at 1.6 sec on the ADM8690. The ADM8691/ADM8695 can be configured for a fixed timeout period—short (100 ms) or long (1.6 sec)—or for an adjustable timeout period. Some systems are unable to service the watchdog timer immediately after a reset; in this case, if the short period is selected for the ADM8691/ADM8695, the device automatically selects the long timeout period directly after a reset is issued. The watchdog timer is restarted at the end of a reset, regardless of whether the reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold.

The normal (short) timeout period becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ has gone inactive. The watchdog timeout period restarts with each transition on the WDI pin. To ensure that the watchdog timer does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur by the end of the minimum timeout period. If WDI remains permanently high or low, reset pulses are issued after each long (1.6 sec) timeout period. The watchdog monitor can be deactivated by allowing the watchdog input (WDI) to float or by connecting it to midsupply.

On the ADM8690 the watchdog timeout period is fixed at 1.6 sec, and the reset pulse width is fixed at 50 ms. The ADM8691/ADM8695 allow these times to be adjusted, as shown in Table 5. Figure 17, Figure 18, Figure 19, and Figure 20 show the various oscillator configurations that can be used to adjust the reset pulse width and watchdog timeout period.

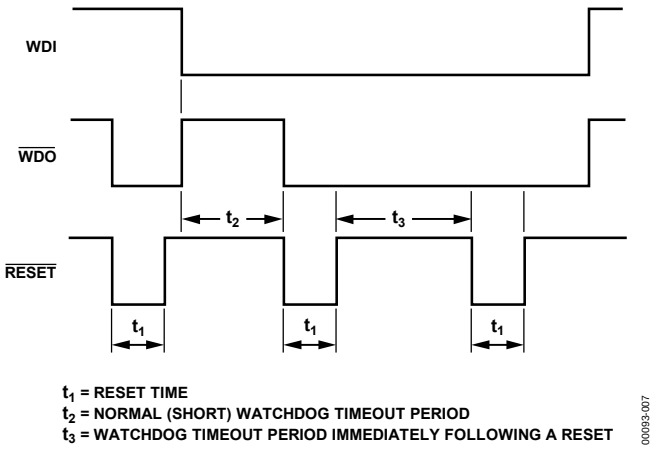


Figure 16. Watchdog Timeout Period and Reset Active Time

The internal oscillator is enabled when OSC SEL is high or floating. In this mode, OSC IN selects either the 1.6 sec watchdog timeout period or the 100 ms watchdog timeout period. When OSC IN is connected high or left floating, the 1.6 sec timeout period is selected; when OSC IN is connected low, the 100 ms timeout period is selected. In either case, the timeout period is 1.6 sec immediately after a reset. This gives the microprocessor time to reinitialize the system. If OSC IN is low, the 100 ms watchdog timeout period becomes effective after the first transition of WDI. The software should be written such that the input/output port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70 ms.

Table 5. ADM8691 and ADM8695 Reset Pulse Width and Watchdog Timeout Selections

		Watchdog Timeout Period		Reset Active Period	
OSC SEL	**OSC IN**	**Normal**	**Immediately After Reset**	**ADM8691**	**ADM8695**
Low[1]	External clock input	1024 CLKs	4096 CLKs	512 CLKs	2048 CLKs
Low[1]	External capacitor	400 ms × C/47 pF	1.6 sec × C/47 pF	200 ms × C/47 pF	520 ms × C/47 pF
Floating or high	Low	100 ms	1.6 sec	50 ms	200 ms
Floating or high	Floating or high	1.6 sec	1.6 sec	50 ms	200 ms

[1] When the OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor (C) can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24 kHz. The nominal oscillator frequency with an external capacitor is f_{OSC} (Hz) = 184,000/C (pF).

WATCHDOG OUTPUT ($\overline{WDO}$) (ADM8691/ADM8695)

The watchdog output ($\overline{WDO}$ pin on the ADM8691/ADM8695) provides a status output that goes low if the watchdog timer times out and remains low until set high by the next transition on the watchdog input. $\overline{WDO}$ is also set high when V_{CC} goes below the reset threshold.

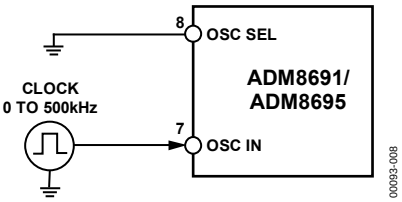


Figure 17. External Clock Source

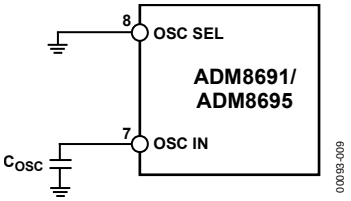


Figure 18. External Capacitor

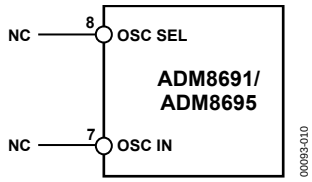


Figure 19. Internal Oscillator (1.6 Second Watchdog)

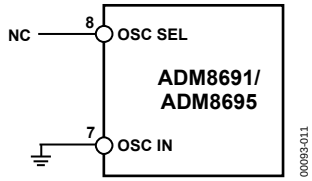


Figure 20. Internal Oscillator (100 ms Watchdog)

$\overline{CE}$ GATING AND RAM WRITE PROTECTION (ADM8691/ADM8695)

The ADM8691/ADM8695 include memory protection circuitry that ensures the integrity of data in memory by preventing write operations when V_{CC} is at an invalid level. Two additional pins ($\overline{CE}_{IN}$ and $\overline{CE}_{OUT}$) can be used to control the chip enable or write inputs of CMOS RAM. When V_{CC} is present, $\overline{CE}_{OUT}$ is a buffered replica of $\overline{CE}_{IN}$, with a 3 ns propagation delay. When V_{CC} falls below the reset voltage threshold or V_{BATT}, an internal gate forces $\overline{CE}_{OUT}$ high, independent of $\overline{CE}_{IN}$.

$\overline{CE}_{OUT}$ typically drives the $\overline{CE}$, $\overline{CS}$, or write input of battery backed-up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved using the $\overline{CE}_{OUT}$ pin to drive the store or write inputs.

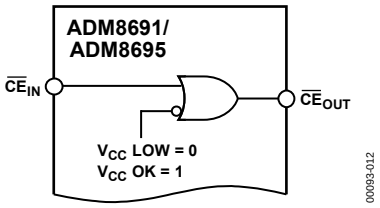


Figure 21. Chip Enable Gating

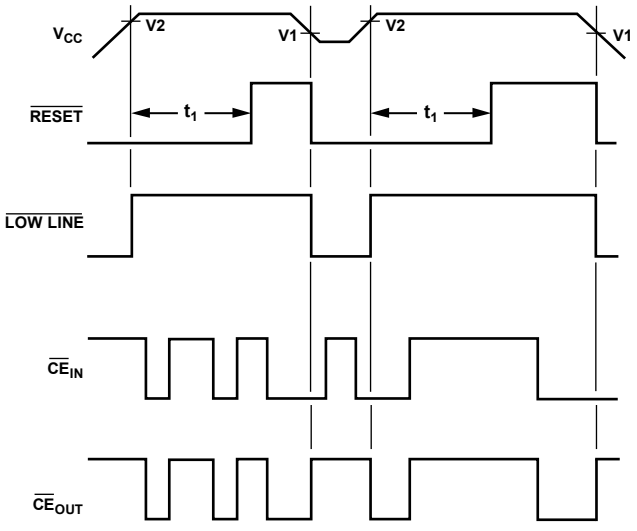


Figure 22. Chip Enable Timing

POWER-FAIL WARNING COMPARATOR

An additional comparator is provided for early warning of failure in the microprocessor power supply. The power-fail input (PFI) is compared to an internal 1.3 V reference. The power-fail output ($\overline{PFO}$) goes low when the voltage at PFI is less than 1.3 V.

Typically, PFI is driven by an external voltage divider that senses either the unregulated dc input to the system 5 V regulator or the regulated 5 V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3 V several milliseconds before the 5 V power supply falls below the reset threshold.

$\overline{PFO}$ is normally used to interrupt the microprocessor so that data can be stored in RAM and the shutdown procedure executed before power is lost.

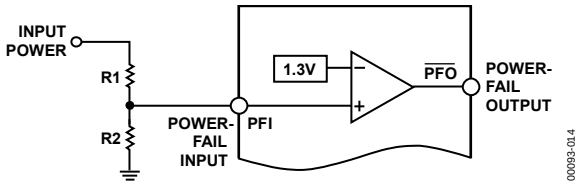


Figure 23. Power-Fail Comparator

Table 6. Input and Output Status in Battery Backup Mode

Signal	Status
V_{OUT}	V_{OUT} is connected to V_{BATT} via an internal PMOS switch.
$\overline{RESET}$	Logic low.
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{LOW\ LINE}$	Logic low.
BATT ON	Logic high. The open circuit voltage is equal to V_{OUT}.
WDI	WDI is ignored. It is internally disconnected from its internal pull-up resistor and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{WDO}$	Logic high. The open circuit voltage is equal to V_{OUT}.
PFI	The power-fail comparator is turned off and has no effect on the power-fail output.
$\overline{PFO}$	Logic low.
$\overline{CE_{IN}}$	$\overline{CE_{IN}}$ is ignored. It is internally disconnected from its internal pull-up resistor and does not source or sink current as long as its input voltage is between GND and V_{OUT}. The input voltage does not affect supply current.
$\overline{CE_{OUT}}$	Logic high. The open circuit voltage is equal to V_{OUT}.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

APPLICATIONS INFORMATION

INCREASING THE DRIVE CURRENT

If the continuous output current requirements at V_{OUT} exceed 100 mA, or if a lower $V_{CC} - V_{OUT}$ voltage differential is desired, an external PNP pass transistor can be connected in parallel with the internal transistor. The BATT ON output (ADM8691/ADM8695) can directly drive the base of the external transistor.

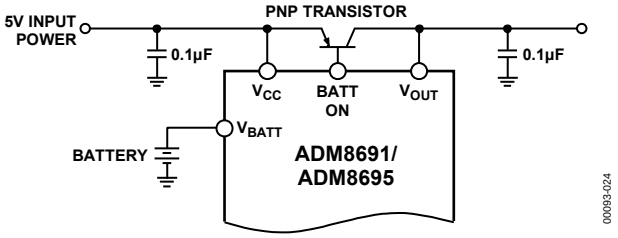


Figure 24. Increasing the Drive Current

USING A RECHARGEABLE BATTERY FOR BACKUP

If a capacitor or a rechargeable battery is used for backup, the charging resistor should be connected to V_{OUT} to eliminate the discharge path that would exist during power-down if the resistor were connected to V_{CC}.

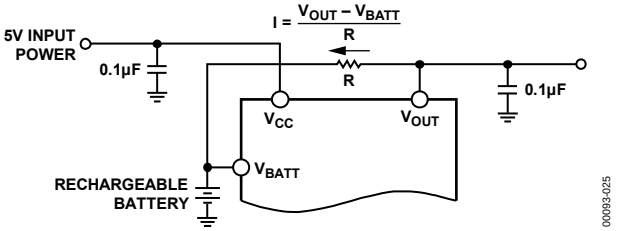


Figure 25. Rechargeable Battery

ADDING HYSTERESIS TO THE POWER-FAIL COMPARATOR

For increased noise immunity, hysteresis can be added to the power-fail comparator. Because the comparator circuit is noninverting, hysteresis can be added simply by connecting a resistor between the $\overline{PFO}$ output and the PFI input, as shown in Figure 26. When $\overline{PFO}$ is low, Resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, the series combination of R3 and R4 sources current into the PFI summing junction. This results in differing trip levels for the comparator.

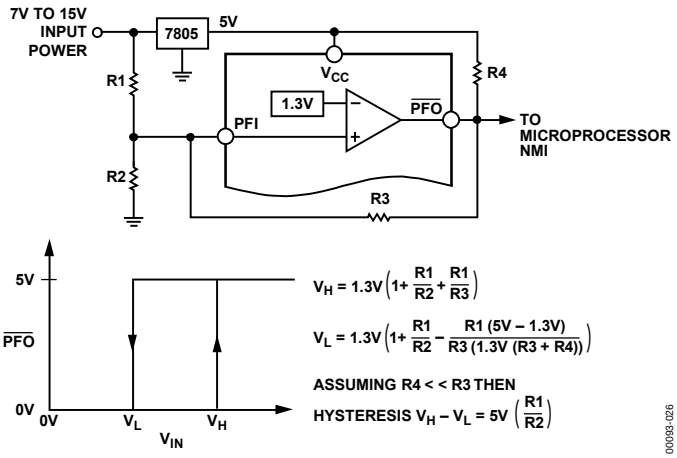


Figure 26. Adding Hysteresis to the Power-Fail Comparator

MONITORING THE STATUS OF THE BATTERY

The power-fail comparator can be used to monitor the status of the backup battery instead of the power supply, if desired (see Figure 27). The PFI input samples the battery voltage and generates an active low $\overline{PFO}$ signal when the battery voltage drops below a selected threshold. It may be necessary to apply a test load to determine the loaded battery voltage. This is done under processor control using $\overline{CE}_{OUT}$. Because $\overline{CE}_{OUT}$ is forced high during the battery backup mode, the test load is not applied to the battery while it is in use, even if the microprocessor is not powered.

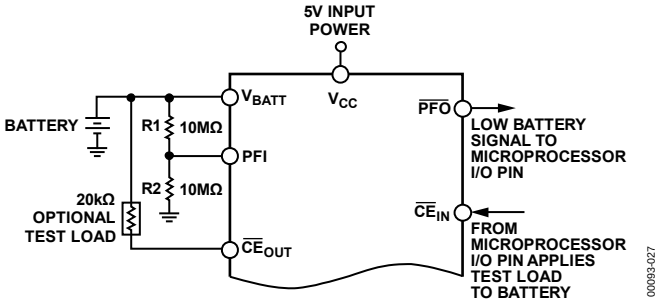


Figure 27. Monitoring the Battery Status

ALTERNATE WATCHDOG INPUT DRIVE CIRCUITS

The watchdog feature can be enabled and disabled under program control by driving WDI with a three-state buffer (see Figure 28). When three-stated, the WDI input floats, thereby disabling the watchdog timer.

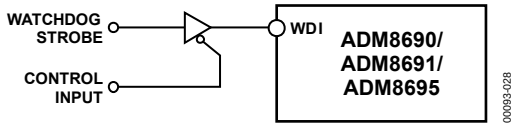


Figure 28. Enabling and Disabling the Watchdog Input

This circuit is not entirely foolproof, and it is possible for a software fault to erroneously three-state the buffer, preventing the ADM8690/ADM8691/ADM8695 from detecting that the microprocessor is no longer operating correctly. In most cases, a better method is to extend the watchdog period rather than disable the watchdog.

For the ADM8691/ADM8695, the watchdog period can be extended under program control using the circuit shown in Figure 29. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01 µF capacitor sets a watchdog timeout delay of 100 sec. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100 ms or the 1.6 sec period is chosen, depending on which diode is used, as shown in Figure 29. With D1 inserted, the internal timeout is set to 100 ms; with D2 inserted, the timeout is set to 1.6 sec.

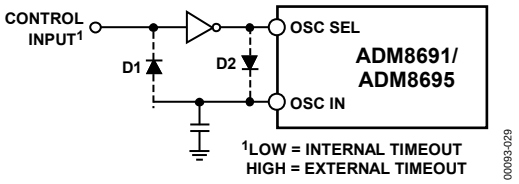


Figure 29. Extending the Watchdog Period

TYPICAL APPLICATIONS

ADM8690 APPLICATIONS

Figure 30 shows the ADM8690 in a typical power monitoring, battery backup application. V_{OUT} powers the CMOS RAM. Under normal operating conditions with V_{CC} present, V_{OUT} is internally connected to V_{CC}. If a power failure occurs, V_{CC} decays and V_{OUT} is switched to V_{BATT}, thereby maintaining power for the CMOS RAM. A $\overline{\text{RESET}}$ pulse is also generated when V_{CC} falls below 4.65 V for the ADM8690. $\overline{\text{RESET}}$ remains low for 50 ms after V_{CC} returns to 5 V.

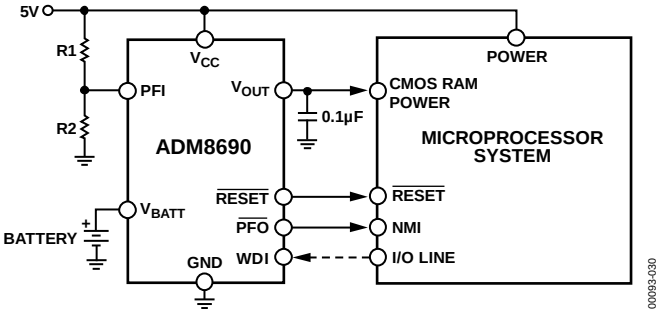


Figure 30. ADM8690 Typical Application, Circuit A

The watchdog timer input (WDI) monitors an input/output line from the microprocessor system. This line must be toggled once every 1.6 sec to verify correct software execution. Failure to toggle the line indicates that the microprocessor system is not correctly executing its program and may be tied up in an endless loop. If this happens, a reset pulse is generated to initialize the microprocessor.

If the watchdog timer is not needed, the WDI input should be left floating.

The power-fail input, PFI, monitors the input power supply via a resistive divider network. The voltage on the PFI input is compared with a precision 1.3 V internal reference. If the input voltage drops below 1.3 V, a power-fail output ($\overline{\text{PFO}}$) signal is generated. This signal warns of an impending power failure and can be used to interrupt the processor so that the system can be shut down in an orderly fashion. The resistors in the sensing network are ratioed to give the desired power-fail threshold voltage (V_T).

$$V_T = (1.3\ R1/R2) + 1.3\ \text{V}$$

$$R1/R2 = (V_T/1.3) - 1$$

Figure 31 shows a similar application, but in this case the PFI input monitors the unregulated input to the 7805 voltage regulator. This circuit provides an earlier warning of an impending power failure. It is useful with processors that operate at low speeds or where there are a significant number of housekeeping tasks to be completed before the power is lost.

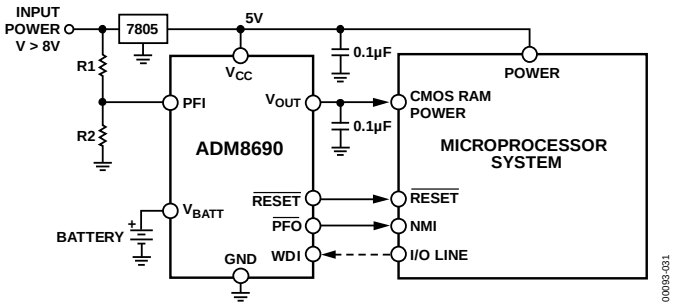


Figure 31. ADM8690 Typical Application, Circuit B

ADM8691/ADM8695 APPLICATIONS

Figure 32 shows a typical connection for the ADM8691/ADM8695. CMOS RAM is powered from V_{OUT}. When 5 V power is present, this voltage is routed to V_{OUT}. If V_{CC} fails, V_{BATT} is routed to V_{OUT}. V_{OUT} can supply up to 100 mA from V_{CC}, but if more current is required, an external PNP transistor can be added. When V_{CC} is higher than V_{BATT}, the BATT ON output goes low, providing up to 35 mA of base drive for the external transistor. A 0.1 µF capacitor is connected to V_{OUT} to supply the transient currents for CMOS RAM. When V_{CC} is lower than V_{BATT}, an internal 20 Ω MOSFET connects the backup battery to V_{OUT}.

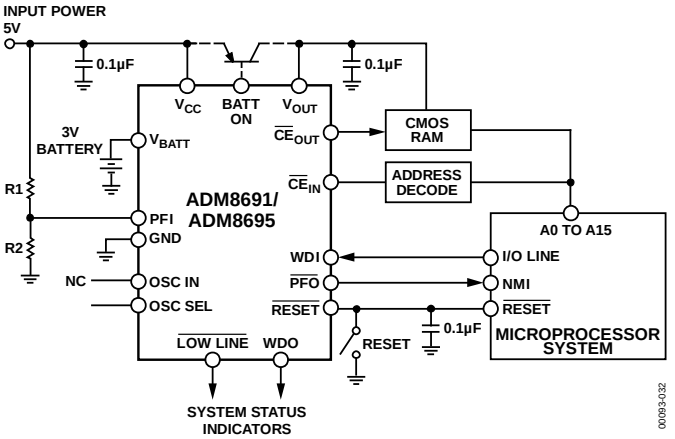


Figure 32. ADM8691/ADM8695 Typical Application

$\overline{\text{RESET}}$ OUTPUT

The internal voltage detector monitors V_{CC} and generates a $\overline{\text{RESET}}$ output to hold the microprocessor reset line low when V_{CC} is below 4.65 V. An internal timer holds $\overline{\text{RESET}}$ low for 50 ms (200 ms for the ADM8695) after V_{CC} rises above 4.65 V. This prevents repeated toggling of $\overline{\text{RESET}}$, even if the 5 V power drops out and recovers with each power line cycle.

The crystal oscillator normally used to generate the clock for microprocessors can take several milliseconds to stabilize. Because most microprocessors need several clock cycles to reset, $\overline{\text{RESET}}$ must be held low until the microprocessor clock oscillator has started. The power-up $\overline{\text{RESET}}$ pulse lasts 50 ms (200 ms for the ADM8695) to allow for this oscillator start-up time. If a different reset pulse width is required, a capacitor should be connected to OSC IN, or an external clock can be used (see Table 5 and Figure 17 through Figure 20). The manual reset switch and the 0.1 µF capacitor connected to the reset line can be omitted if a manual reset is not needed. An inverted, active high RESET output is also available on the ADM8691/ADM8695.

POWER-FAIL DETECTOR

The 5 V V_{CC} power line is monitored via a resistive potential divider connected to the power-fail input (PFI). When the voltage at PFI falls below 1.3 V, the power-fail output ($\overline{\text{PFO}}$) drives the processor's NMI input low. For example, if a power-fail threshold of 4.8 V is set with Resistor R1 and Resistor R2 and V_{CC} falls from 4.8 V to 4.65 V, the microprocessor has time to save data into RAM. An earlier power-fail warning can be generated if the unregulated dc input to the 5 V regulator is available for monitoring. This allows more time for microprocessor housekeeping tasks to be completed before power is lost.

RAM WRITE PROTECTION

The ADM8691/ADM8695 $\overline{CE}_{OUT}$ line drives the chip select inputs of the CMOS RAM. $\overline{CE}_{OUT}$ follows $\overline{CE}_{IN}$ as long as V_{CC} is above the 4.65 V reset threshold.

If V_{CC} falls below the reset threshold, $\overline{CE}_{OUT}$ goes high, independent of the logic level at $\overline{CE}_{IN}$. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions.

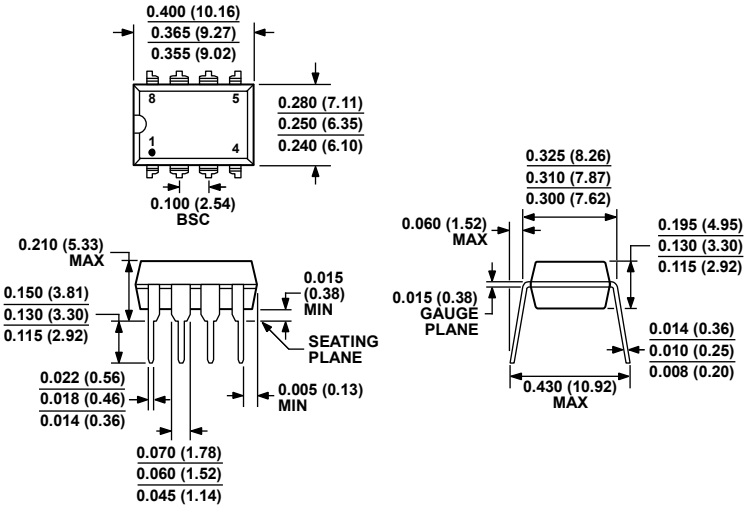
WATCHDOG TIMER

The microprocessor drives the watchdog input (WDI) with an input/output line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 sec to verify proper software execution. If a hardware or software failure occurs such that WDI is not toggled, the ADM8691 issues a 50 ms (200 ms for the ADM8695) $\overline{\text{RESET}}$ pulse after 1.6 sec. This typically restarts the microprocessor power-up routine. A new $\overline{\text{RESET}}$ pulse is issued every 1.6 sec until WDI is again strobed. If a different watchdog timeout period is required, a capacitor should be connected to OSC IN or an external clock can be used (see Table 5 and Figure 17 through Figure 20).

The watchdog output ($\overline{\text{WDO}}$) goes low if the watchdog timer is not serviced within its timeout period. After $\overline{\text{WDO}}$ goes low, it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected.

The $\overline{\text{RESET}}$ output has an internal 3 µA pull-up and can either connect to an open-collector reset bus or directly drive a CMOS gate without an external pull-up resistor.

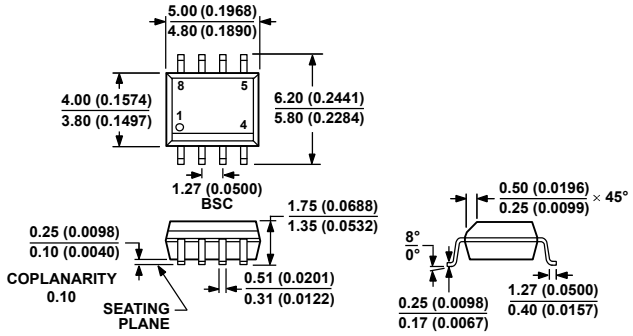
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 33. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
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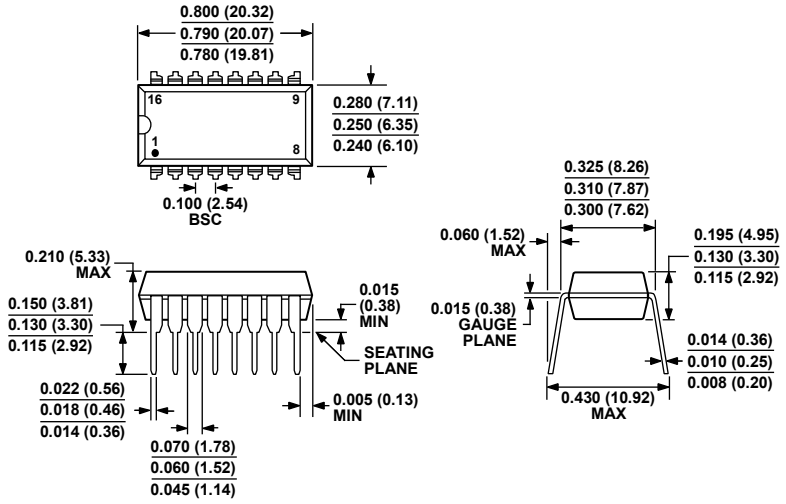
012407-A

Figure 34. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-001-AB
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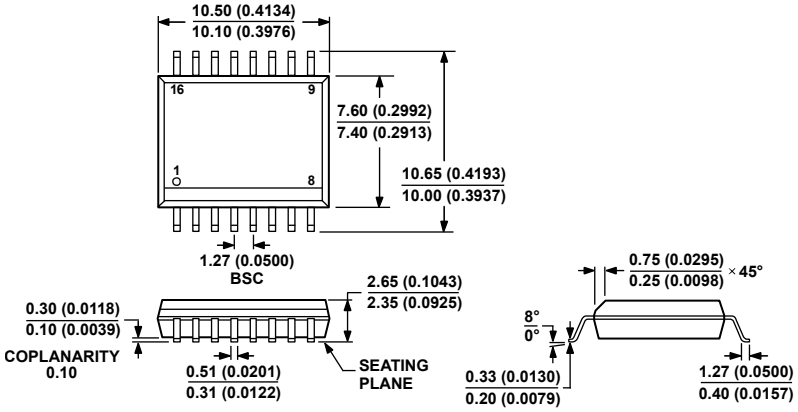
073106-B

Figure 35. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches and (millimeters)



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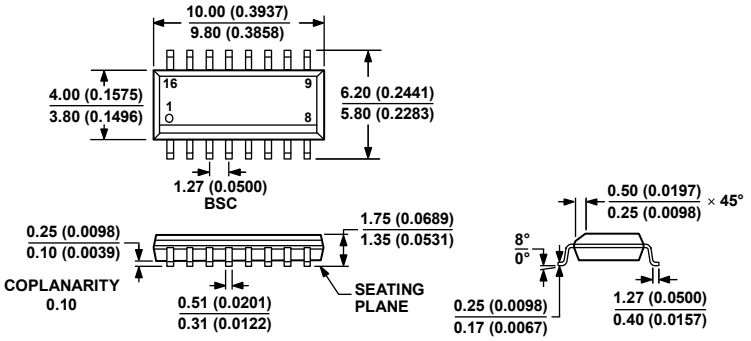
03-27-2007-B

Figure 36. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

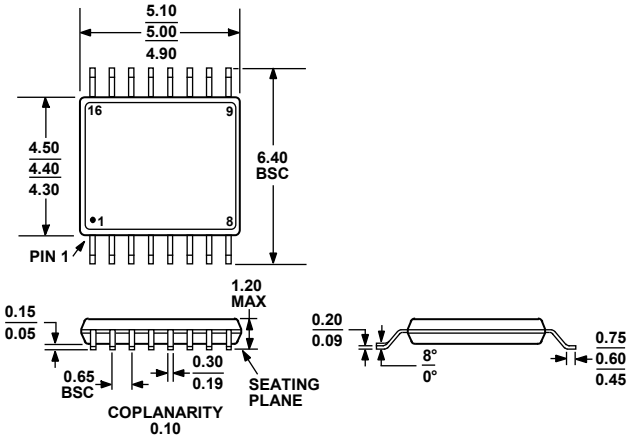


COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 37. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 38. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM8690AN	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM8690ANZ	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
ADM8690ARN	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM8690ARN-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM8690ARNZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM8691ANZ	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADM8691ARN	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADM8691ARN-REEL	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADM8691ARNZ	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADM8691ARW	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM8691ARW-REEL	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM8691ARWZ	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM8691ARU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM8691ARU-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM8691ARUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADM8695ARW	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM8695ARW-REEL	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM8695ARWZ	−40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16

[1] Z = RoHS Compliant Part.

NOTES

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