



# THE DATASHEET OF AOT264L



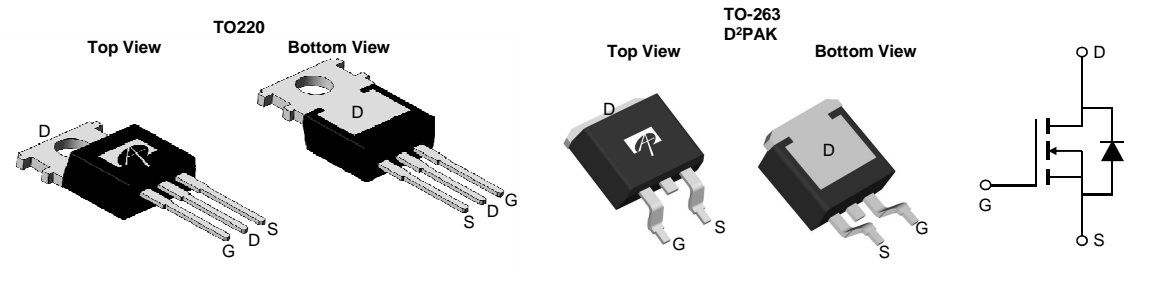
### General Description

The AOT264L/AOB264L combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

### Product Summary

$V_{DS}$	60V
$I_D$ (at $V_{GS}=10V$ )	140A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 3.2m $\Omega$ (< 3.0m $\Omega^*$ )
$R_{DS(ON)}$ (at $V_{GS} = 6V$ )	< 3.5m $\Omega$ (< 3.3m $\Omega^*$ )

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	140	A
		$T_C=25^\circ\text{C}$	
	$T_C=100^\circ\text{C}$	110	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	480	
Continuous Drain Current	$I_{DSM}$	19	A
		$T_A=25^\circ\text{C}$	
	$T_A=70^\circ\text{C}$	15	
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	100	A
Avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AS}, E_{AR}$	500	mJ
Power Dissipation <sup>B</sup>	$P_D$	333	W
		$T_C=25^\circ\text{C}$	
	$T_C=100^\circ\text{C}$	167	
Power Dissipation <sup>A</sup>	$P_{DSM}$	2.1	W
		$T_A=25^\circ\text{C}$	
	$T_A=70^\circ\text{C}$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	12	15	$^\circ\text{C}/\text{W}$
		$t \leq 10\text{s}$		
Maximum Junction-to-Ambient <sup>A D</sup>		48	60	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{\theta JC}$	0.35	0.45	$^\circ\text{C}/\text{W}$

\* Surface mount package TO263

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.2	2.7	3.2	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	480			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A TO220 T <sub>J</sub> =125°C		2.4 4	3.2 4.8	mΩ
		V <sub>GS</sub> =6V, I <sub>D</sub> =20A TO220		2.7	3.5	
		V <sub>GS</sub> =10V, I <sub>D</sub> =20A TO263		2.3	3.0	
		V <sub>GS</sub> =6V, I <sub>D</sub> =20A TO263		2.6	3.3	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		80		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.65	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				140	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =30V, f=1MHz	5500	6960	8400	pF
C <sub>oss</sub>	Output Capacitance		840			pF
C <sub>riss</sub>	Reverse Transfer Capacitance		30			pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.4	0.9	1.4	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =20A	60	75	90	nC
Q <sub>gs</sub>	Gate Source Charge		25			nC
Q <sub>gd</sub>	Gate Drain Charge		5			nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, R <sub>L</sub> =1.5Ω, R <sub>GEN</sub> =3Ω		23		ns
t <sub>r</sub>	Turn-On Rise Time		7			ns
t <sub>D(off)</sub>	Turn-Off DelayTime		45			ns
t <sub>f</sub>	Turn-Off Fall Time		8			ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs	18	26	34	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs	105	155	202	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

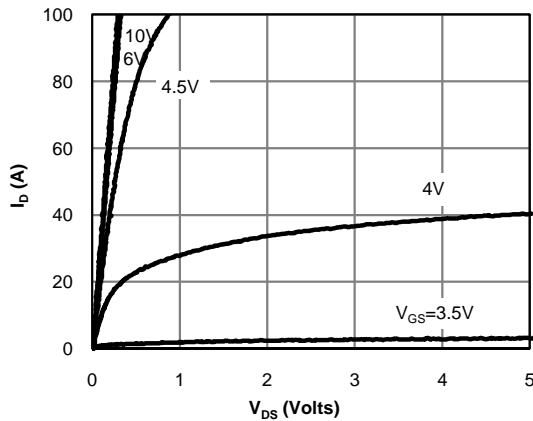
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

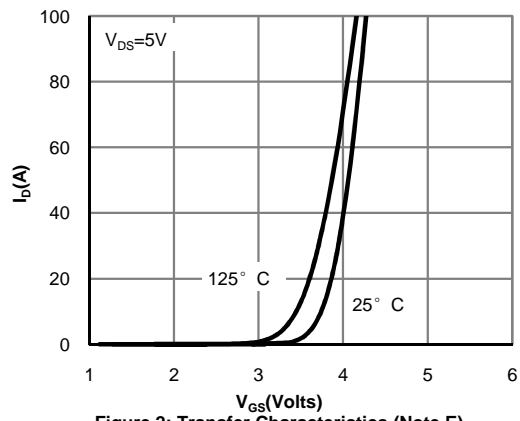
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

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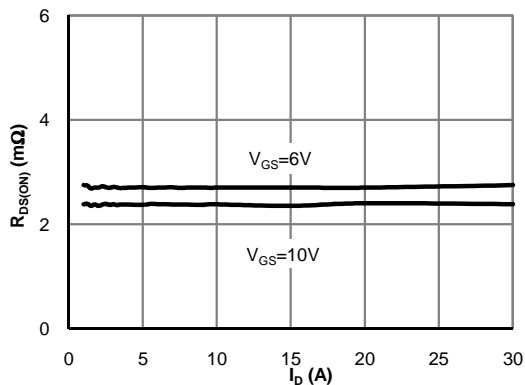
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



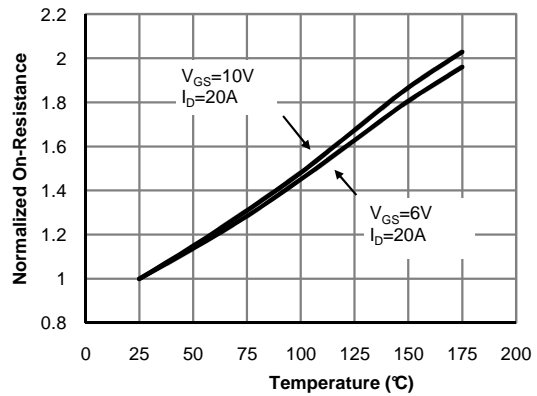
**Figure 1: On-Region Characteristics (Note E)**



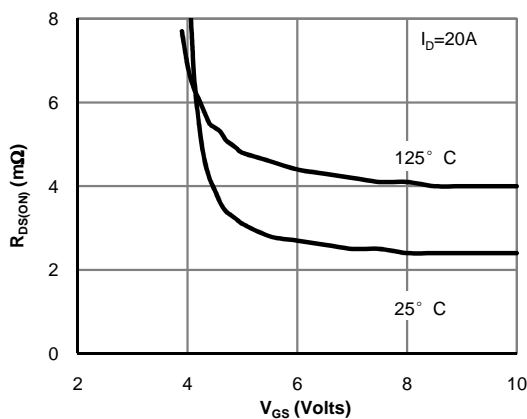
**Figure 2: Transfer Characteristics (Note E)**



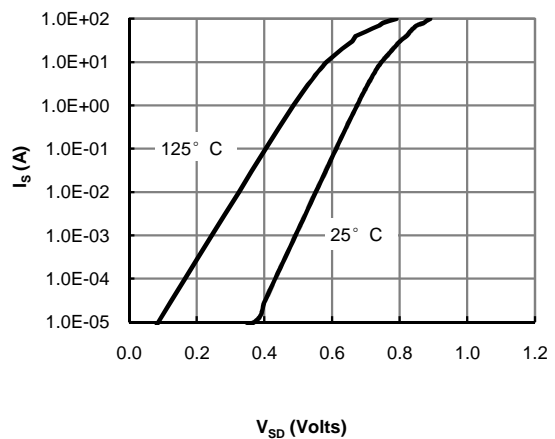
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

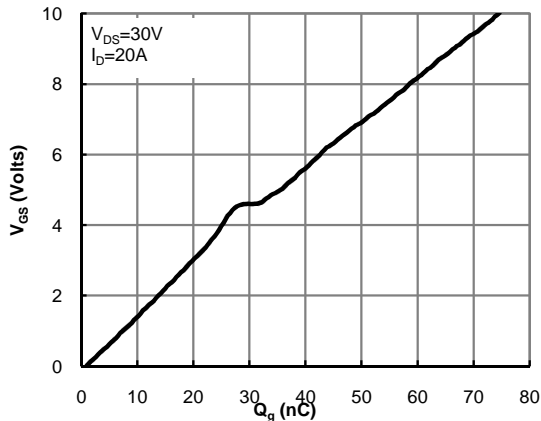


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

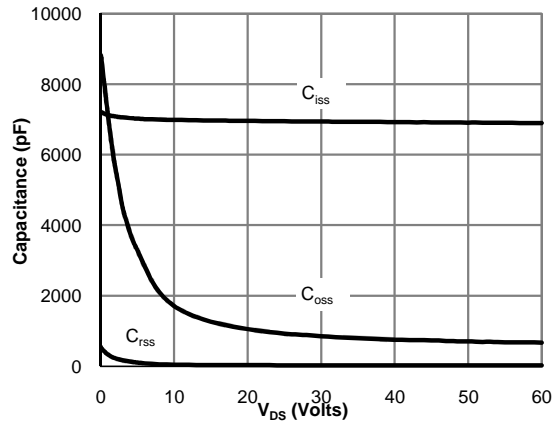


**Figure 6: Body-Diode Characteristics (Note E)**

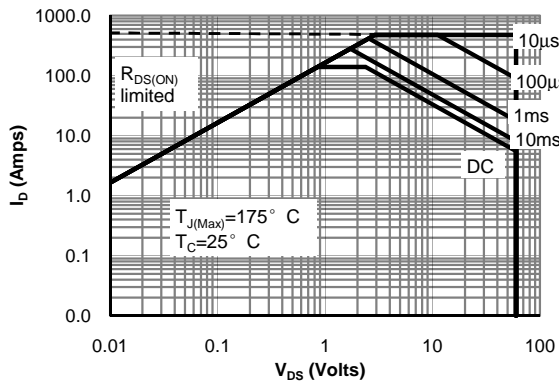
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



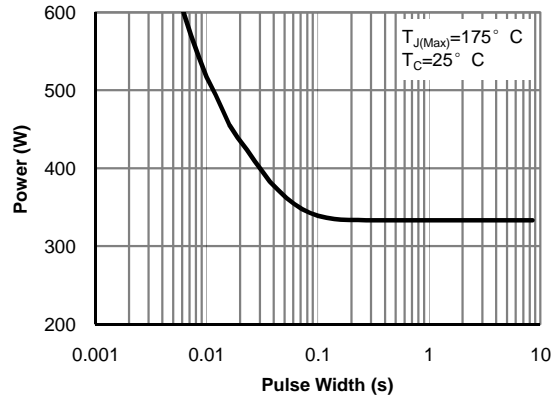
**Figure 7: Gate-Charge Characteristics**



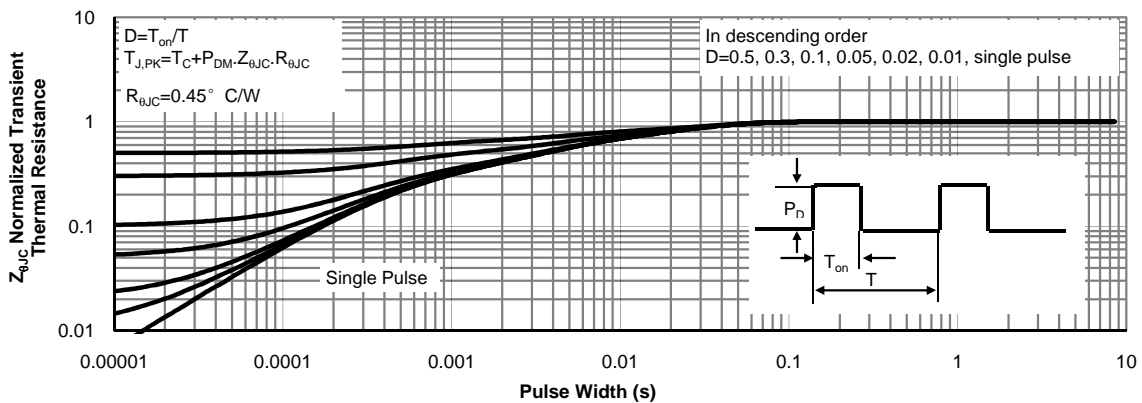
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

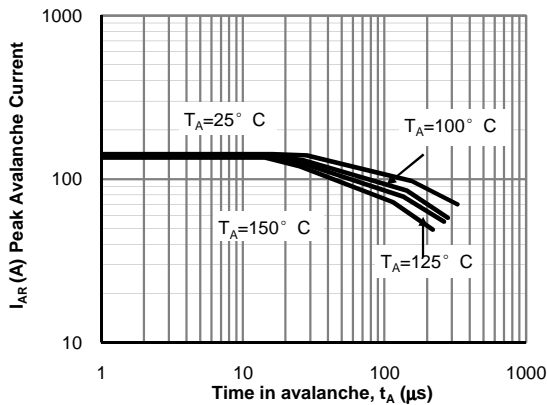


Figure 12: Single Pulse Avalanche capability (Note C)

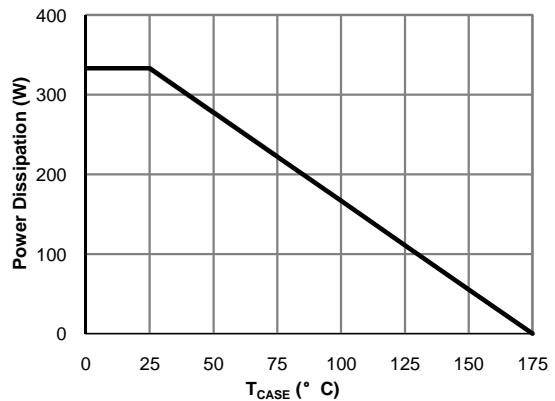


Figure 13: Power De-rating (Note F)

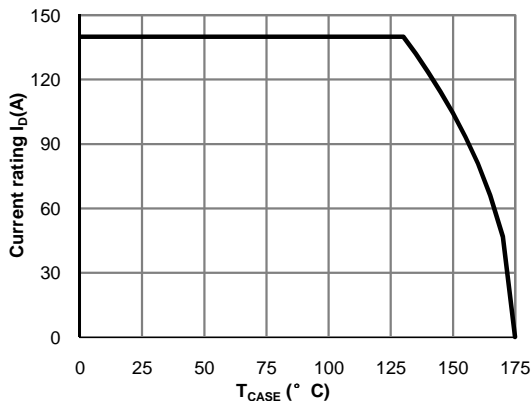


Figure 14: Current De-rating (Note F)

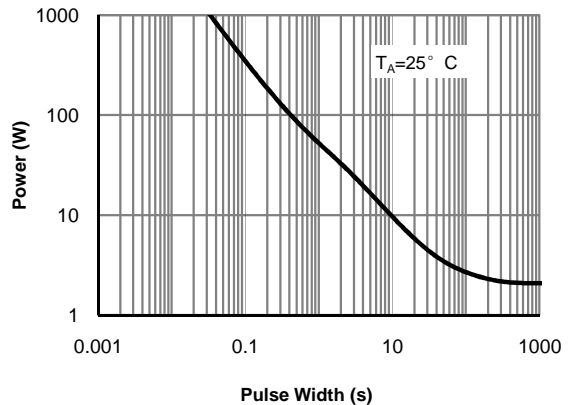


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

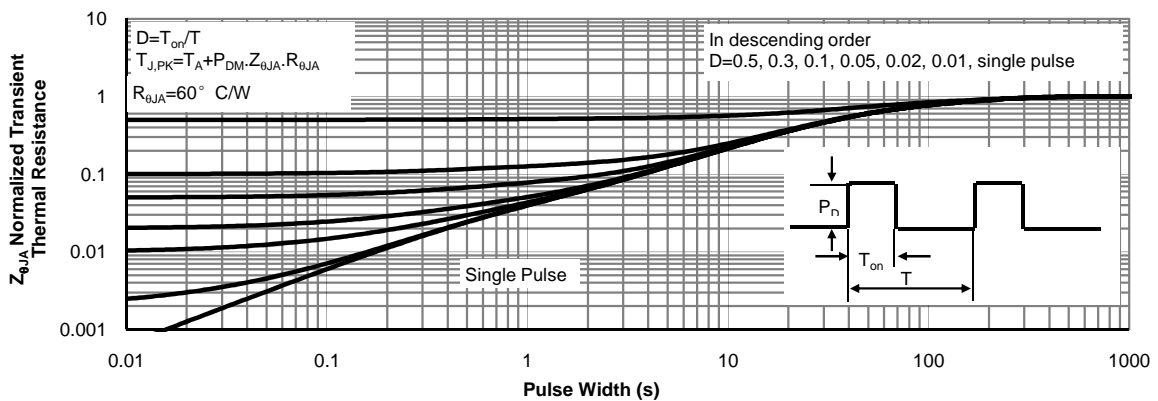


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

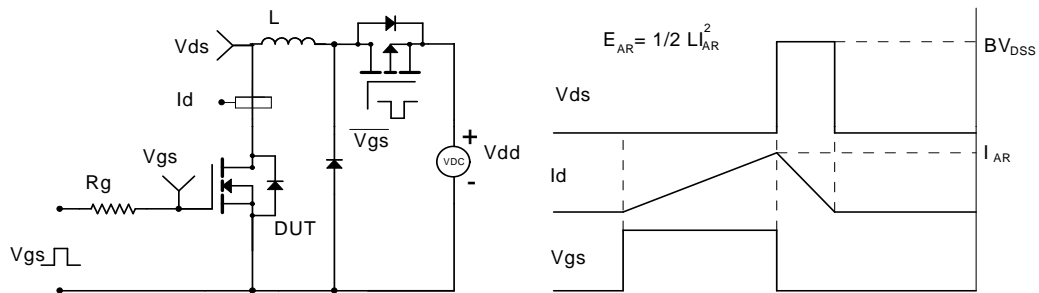
**Gate Charge Test Circuit & Waveform**



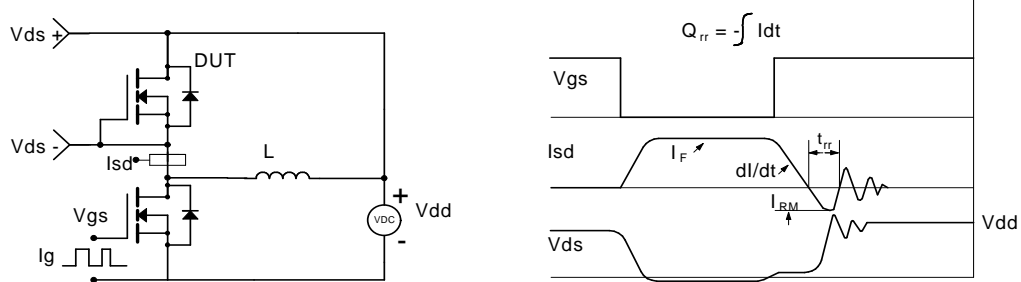
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



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