



# THE DATASHEET OF DAC8814ICDBT





## Quad, Serial Input 16-Bit Multiplying Digital-to-Analog Converter

### FEATURES

- **Relative Accuracy: 1 LSB Max**
- **Differential Nonlinearity: 1 LSB Max**
- **2-mA Full-Scale Current with  $V_{REF} = \pm 10\text{ V}$**
- **0.5- $\mu\text{s}$  Settling Time**
- **Midscale or Zero-Scale Reset**
- **Four Separate 4Q Multiplying Reference Inputs**
- **Reference Bandwidth: 10 MHz**
- **Reference Dynamics: –105 dB THD**
- **SPI™-Compatible 3-Wire Interface: 50 MHz**
- **Double Buffered Registers Enable**
- **Simultaneous Multichannel Change**
- **Internal Power-On Reset**
- **Industry-Standard Pin Configuration**

### APPLICATIONS

- **Automatic Test Equipment**
- **Instrumentation**
- **Digitally-Controlled Calibration**

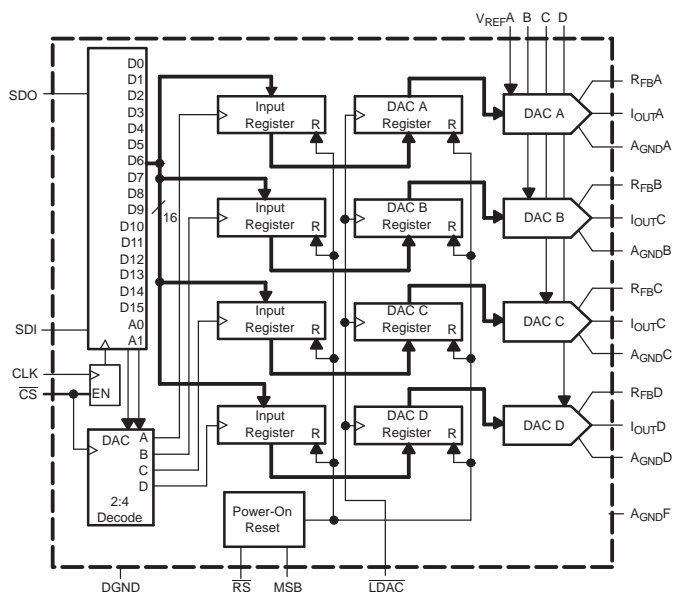
### DESCRIPTION

The DAC8814 is a quad, 16-bit, current-output digital-to-analog converter (DAC) designed to operate from a single +2.7-V to 5.0-V supply.

The applied external reference input voltage  $V_{REF}$  determines the full-scale output current. An internal feedback resistor ( $R_{FB}$ ) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier.

A doubled buffered serial data interface offers high-speed, 3-wire, SPI and microcontroller compatible inputs using serial data in (SDI), clock (CLK), and a chip-select ( $\overline{CS}$ ). In addition, a serial data out pin (SDO) allows for daisy-chaining when multiple packages are used. A common level-sensitive load DAC strobe ( $\overline{LDAC}$ ) input allows simultaneous update of all DAC outputs from previously loaded input registers. Additionally, an internal power-on reset forces the output voltage to zero at system turn on. An MSB pin allows system reset assertion ( $\overline{RS}$ ) to force all registers to zero code when MSB = 0, or to half-scale code when MSB = 1.

The DAC8814 is available in an SSOP package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**PACKAGE/ORDERING INFORMATION<sup>(1)</sup>**

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8814C	±1	±1	– 40°C to +85°C	SSOP-28	DB	DAC8814ICDBT	Tape and Reel, 250
						DAC8814ICDBR	Tape and Reel, 2500
DAC8814B	±4	±1.5	–40°C to +85°C	SSOP-28	DB	DAC8814IBDBT	Tape and Reel, 250
						DAC8814IBDBR	Tape and Reel, 2500

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

	DAC8814	UNIT
V <sub>DD</sub> to GND	–0.3 to +8	V
V <sub>REF</sub> to GND	–18 to +18	V
Logic inputs and output to GND	–0.3 to +8	V
V(I <sub>OUT</sub> ) to GND	–0.3 to V <sub>DD</sub> + 0.3	V
A <sub>GNDX</sub> to DGND	–0.3 to +0.3	V
Input current to any pin except supplies	±50	mA
Package power dissipation	(T <sub>Jmax</sub> – T <sub>A</sub> )/θ <sub>JA</sub>	W
Thermal resistance, θ <sub>JA</sub>	28-Lead shrink surface-mount (RS-28)	100
Maximum junction temperature (T <sub>Jmax</sub> )	150	°C
Operating temperature range, Model A	–40 to +85	°C
Storage temperature range	–65 to +150	°C
ESD rating, HBM	3000	V
ESD rating, CDM	500	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS**

$V_{DD} = 2.7\text{ V}$  to  $5.5\text{ V}$ ;  $I_{OUTX} = \text{Virtual GND}$ ,  $A_{GNDX} = 0\text{ V}$ ,  $V_{REFA, B, C, D} = 10\text{ V}$ ,  $T_A = \text{full operating temperature range}$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC8814			UNIT
			MIN	TYP	MAX	
<b>STATIC PERFORMANCE<sup>(1)</sup></b>						
Resolution					16	Bits
Relative accuracy	INL	DAC8814B			±4	LSB
	INL	DAC8814C			±1	LSB
Differential nonlinearity	DNL	DAC8814B			±1.5	LSB
	DNL	DAC8814C			±1	LSB
Output leakage current	$I_{OUTX}$	Data = 0000h, $T_A = 25^\circ\text{C}$			10	nA
	$I_{OUTX}$	Data = 0000h, $T_A = T_A \text{ max}$			20	nA
Full-scale gain error	$G_{FSE}$	Data = FFFFh		±0.75	±3	mV
Full-scale tempco <sup>(2)</sup>	$TCV_{FS}$			1		ppm/°C
Feedback resistor	$R_{FBX}$	$V_{DD} = 5\text{ V}$		5		kΩ
<b>REFERENCE INPUT</b>						
$V_{REFX}$ Range	$V_{REFX}$		-15		15	V
Input resistance	$R_{REFX}$		4	5	6	kΩ
Input resistance match	$R_{REFX}$	Channel-to-channel		1		%
Input capacitance <sup>(2)</sup>	$C_{REFX}$			5		pF
<b>ANALOG OUTPUT</b>						
Output current	$I_{OUTX}$	Data = FFFFh	1.6		2.5	mA
Output capacitance <sup>(2)</sup>	$C_{OUTX}$	Code-dependent		50		pF
<b>LOGIC INPUTS AND OUTPUT</b>						
Input low voltage	$V_{IL}$	$V_{DD} = +2.7\text{ V}$			0.6	V
	$V_{IL}$	$V_{DD} = +5\text{ V}$			0.8	V
Input high voltage	$V_{IH}$	$V_{DD} = +2.7\text{ V}$	2.1			V
	$V_{IH}$	$V_{DD} = +5\text{ V}$	2.4			V
Input leakage current	$I_{IL}$				1	μA
Input capacitance <sup>(2)</sup>	$C_{IL}$				10	pF
Logic output low voltage	$V_{OL}$	$I_{OL} = 1.6\text{ mA}$			0.4	V
Logic output high voltage	$V_{OH}$	$I_{OH} = 100\text{ μA}$	4			V
<b>INTERFACE TIMING<sup>(2), (3)</sup></b>						
Clock input frequency	$f_{CLK}$		50			MHz
Clock width high	$t_{CH}$		10			ns
Clock width low	$t_{CL}$		10			ns
$\overline{CS}$ to Clock setup	$t_{CSS}$		0			ns
Clock to $\overline{CS}$ hold	$t_{CSH}$		10			ns
Clock to SDO prop delay	$t_{PD}$		2		20	ns
Load DAC pulsewidth	$t_{LDAC}$		25			ns
Data setup	$t_{DS}$		5			ns
Data hold	$t_{DH}$		10			ns
Load setup	$t_{LDS}$		5			ns
Load hold	$t_{LDH}$		10			ns

(1) All static performance tests (except  $I_{OUT}$ ) are performed in a closed-loop system using an external precision OPA277 I-to-V converter amplifier. The DAC8814  $R_{FB}$  terminal is tied to the amplifier output. Typical values represent average readings measured at  $+25^\circ\text{C}$ .

(2) These parameters are specified by design and not subject to production testing.

(3) All input control signals are specified with  $t_R = t_F = 2.5\text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

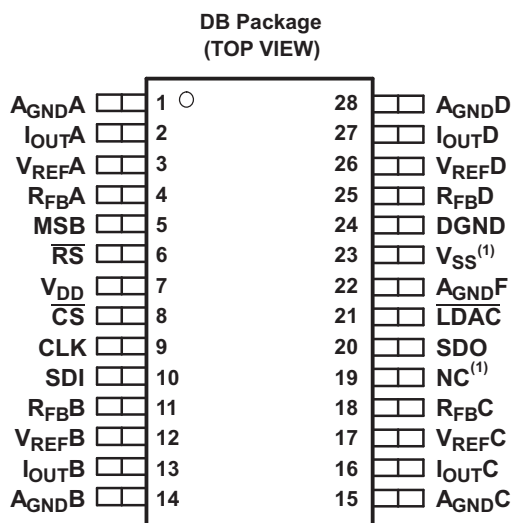
**ELECTRICAL CHARACTERISTICS (continued)**

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ;  $I_{OUTX} = \text{Virtual GND}$ ,  $A_{GNDX} = 0\text{ V}$ ,  $V_{REFA, B, C, D} = 10\text{ V}$ ,  $T_A = \text{full operating temperature range}$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC8814			UNIT
			MIN	TYP	MAX	
<b>SUPPLY CHARACTERISTICS</b>						
Power supply range	$V_{DD\text{ RANGE}}$		2.7		5.5	V
Positive supply current	$I_{DD}$	Logic inputs = 0 V, $V_{DD} = +4.5\text{ V to }+5.5\text{ V}$		2	5	$\mu\text{A}$
	$I_{DD}$	Logic inputs = 0 V, $V_{DD} = +2.7\text{ V to }+3.6\text{ V}$		1	2.5	$\mu\text{A}$
Power dissipation	$P_{DISS}$	Logic inputs = 0 V			0.0275	mW
Power supply sensitivity	$P_{SS}$	$\Delta V_{DD} = \pm 5\%$			0.006	%
<b>AC CHARACTERISTICS<sup>(4)</sup></b>						
Output voltage settling time	$t_s$	To $\pm 0.1\%$ of full-scale, Data = 0000h to FFFFh to 0000h		0.3		$\mu\text{s}$
	$t_s$	To $\pm 0.0015\%$ of full-scale, Data = 0000h to FFFFh to 0000h		0.5		$\mu\text{s}$
Reference multiplying BW	BW -3 dB	$V_{REFX} = 100\text{ mV}_{RMS}$ , Data = FFFFh, $C_{FB} = 3\text{ pF}$		10		MHz
DAC glitch impulse	Q	$V_{REFX} = 10\text{ V}$ , Data = 7FFFh to 8000h to 7FFFh		5		nV-s
Feedthrough error	$V_{OUTX}/V_{REFX}$	Data = 0000h, $V_{REFX} = 100\text{ mV}_{RMS}$ , $f = 100\text{ kHz}$		-70		dB
Crosstalk error	$V_{OUTA}/V_{REFB}$	Data = 0000h, $V_{REFB} = 100\text{ mV}_{RMS}$ , Adjacent channel, $f = 100\text{ kHz}$		-100		dB
Digital feedthrough	Q	$\overline{CS} = 1$ and $f_{CLK} = 1\text{ MHz}$		1		nV-s
Total harmonic distortion	THD	$V_{REF} = 5\text{ V}_{PP}$ , Data = FFFFh, $f = 1\text{ kHz}$		-105		dB
Output spot noise voltage	$e_n$	$f = 1\text{ kHz}$ , BW = 1 Hz		12		$\text{nV}/\sqrt{\text{Hz}}$

(4) All ac characteristic tests are performed in a closed-loop system using a THS4011 I-to-V converter amplifier.

## PIN CONFIGURATIONS



NOTE (1): No internal connection

## PIN DESCRIPTION

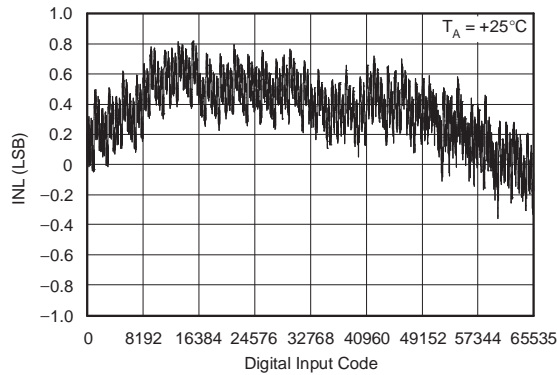
PIN	NAME	DESCRIPTION
1, 14, 15, 28	AGNDA, AGNDB, AGNDC, AGNDD	DAC A, B, C, D Analog ground.
2, 13, 16, 27	IOUTA, IOUTB, IOUTC, IOUTD	DAC A, B, C, D Current output.
3, 12, 17, 26	VREFA, VREFB, VREFC, VREFD	DAC A, B, C, D Reference voltage input terminal. Establishes DAC A, B, C, D full-scale output voltage. Can be tied to V <sub>DD</sub> .
4, 11, 18, 25	RFB A, RFB B, RFB C, RFB D	Establish voltage output for DAC A, B, C, D by connecting to external amplifier output.
5	MSB	MSB Bit set during a reset pulse (RS) or at system power-on if tied to ground or V <sub>DD</sub> .
6	$\overline{RS}$	Reset pin, active low. Input register and DAC registers are set to all zeros or half-scale code (8000h) determined by the voltage on the MSB pin. Register data = 8000h when MSB = 1.
7	V <sub>DD</sub>	Positive power-supply input. Specified range of operation +2.7 V to +5.5 V.
8	$\overline{CS}$	Chip select; active low input. Disables shift register loading when high. Transfers shift register data to input register when $\overline{CS}$ /LDAC goes high. Does not affect LDAC operation.
9	CLK	Clock input; positive edge triggered clocks data into shift register
10	SDI	Serial data input; data loads directly into the shift register.
19	NC	Not connected; leave floating.
20	SDO	Serial data output; input data loads directly into shift register. Data appears at SDO, 19 clock pulses after input at the SDI pin.
21	$\overline{LDAC}$	Load DAC register strobe; level sensitive active low. Transfers all input register data to the DAC registers. Asynchronous active low input. See <a href="#">Table 1</a> for operation.
22	AGNDF	High current analog force ground.
23	V <sub>SS</sub>	No internal connection.
24	DGND	Digital ground.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +5\text{ V}$ , unless otherwise noted.

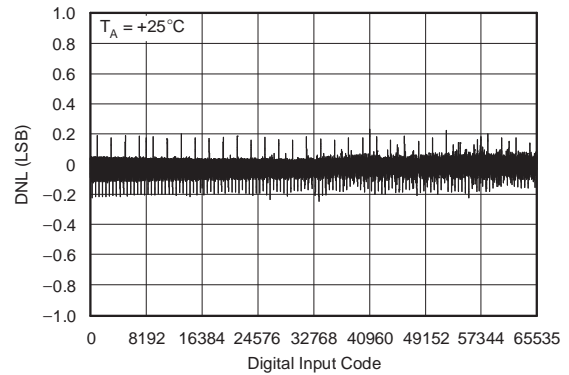
**Channel A**

**LINEARITY ERROR vs DIGITAL INPUT CODE**



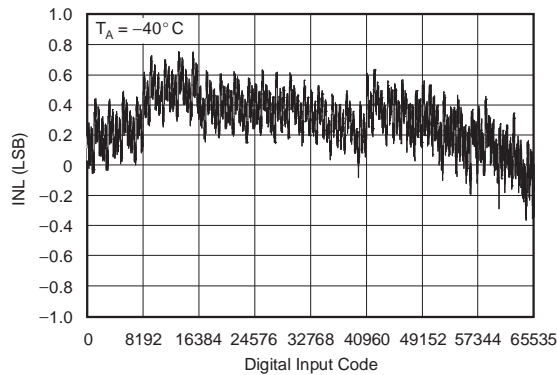
**Figure 1.**

**DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE**



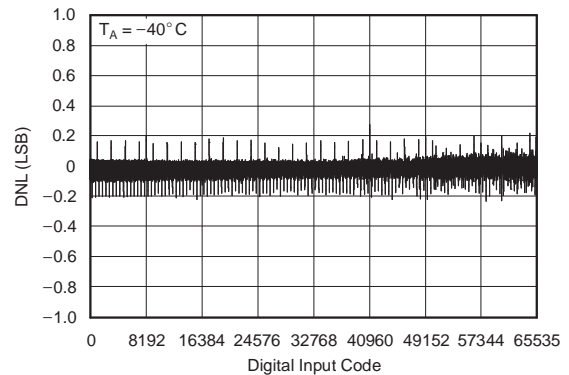
**Figure 2.**

**LINEARITY ERROR vs DIGITAL INPUT CODE**



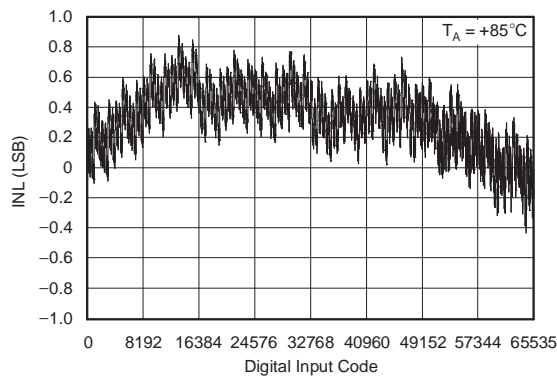
**Figure 3.**

**DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE**



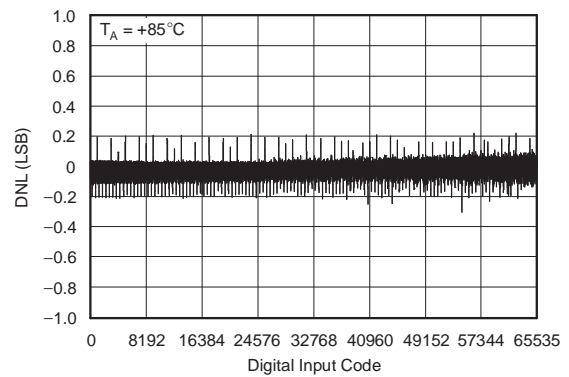
**Figure 4.**

**LINEARITY ERROR vs DIGITAL INPUT CODE**



**Figure 5.**

**DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE**



**Figure 6.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +5\text{ V}$ , unless otherwise noted.

**Channel B**

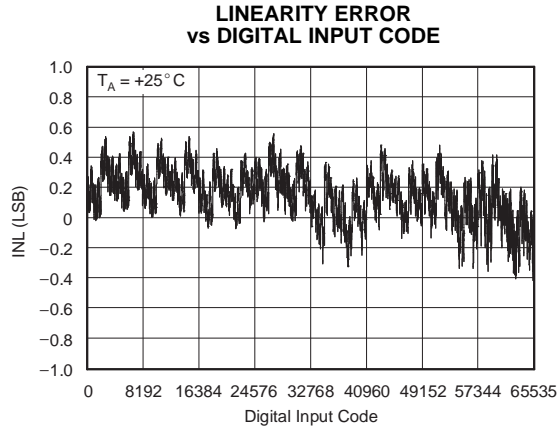


Figure 7.

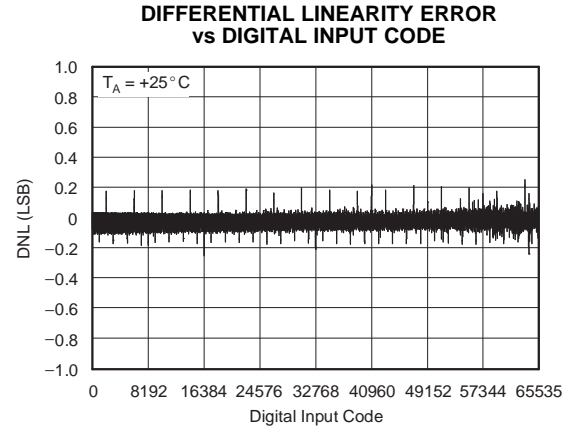


Figure 8.

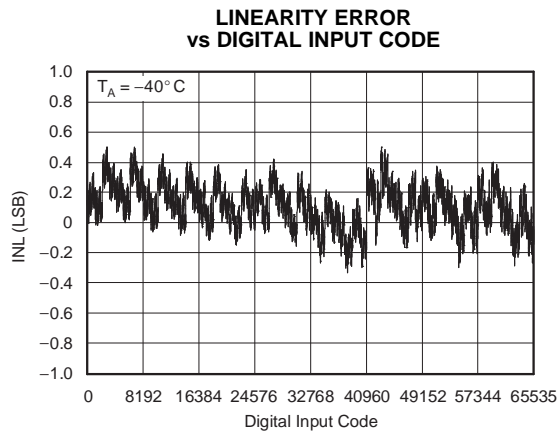


Figure 9.

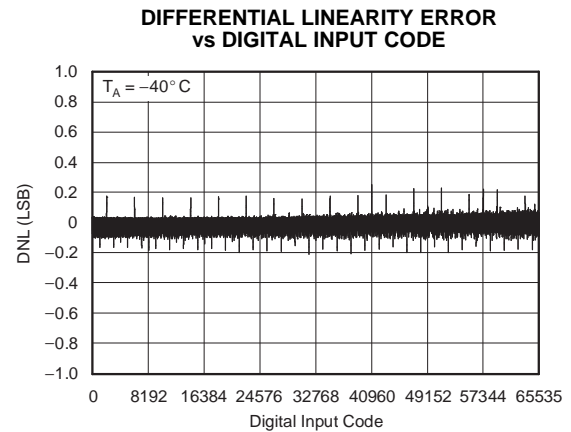


Figure 10.

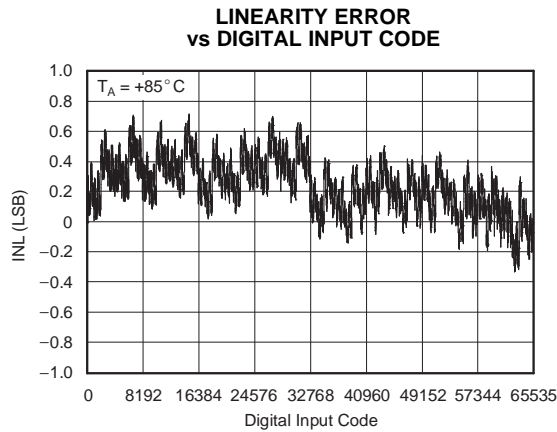


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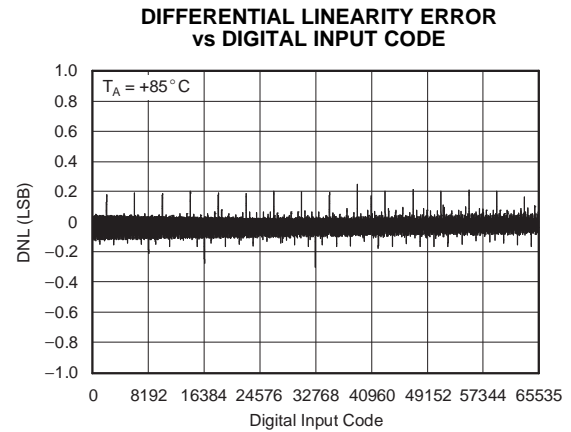


Figure 12.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +5\text{ V}$ , unless otherwise noted.

**Channel C**

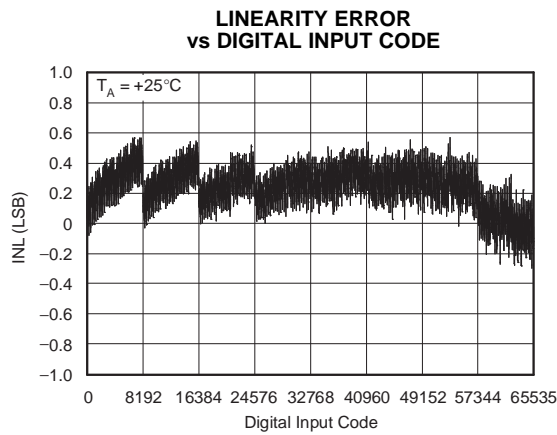


Figure 13.

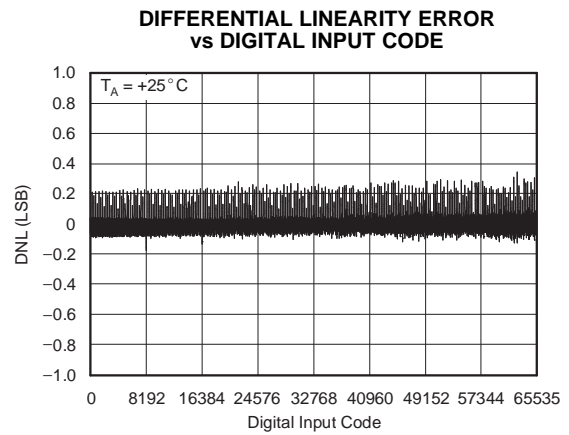


Figure 14.

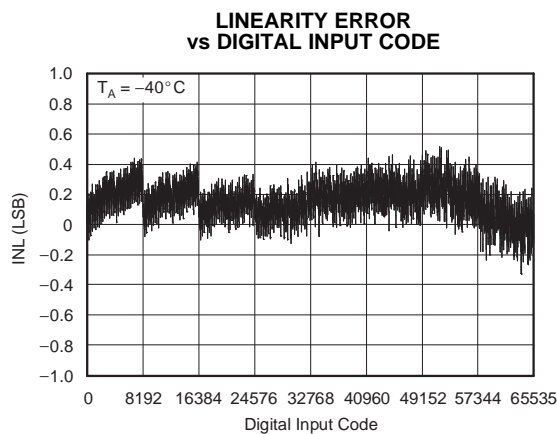


Figure 15.

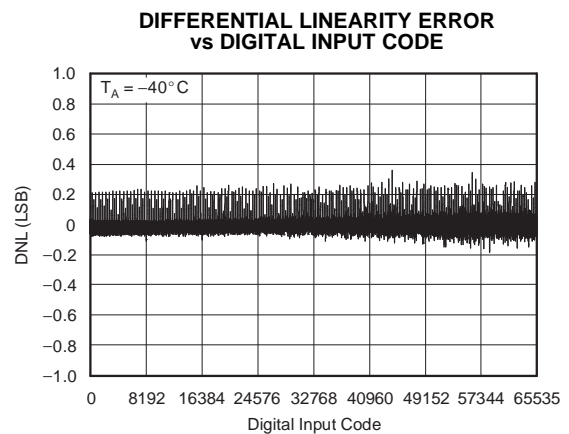


Figure 16.

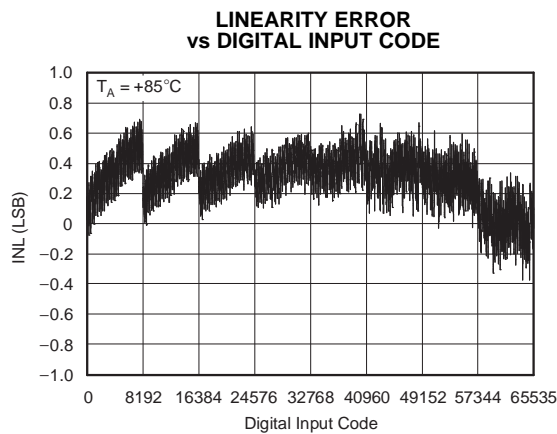


Figure 17.

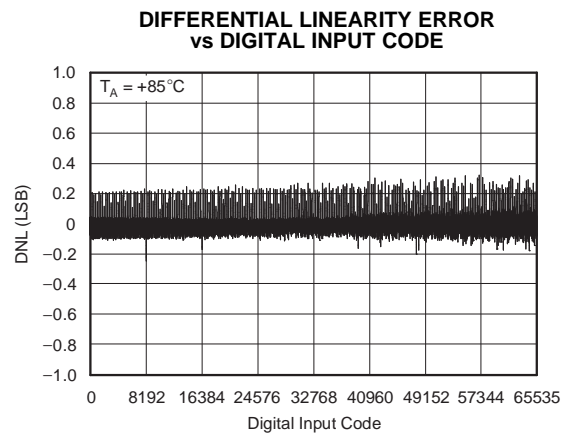


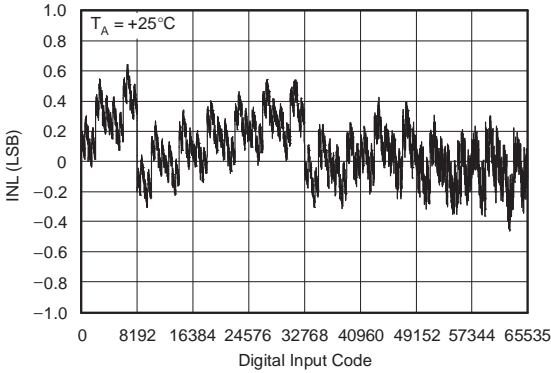
Figure 18.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +5\text{ V}$ , unless otherwise noted.

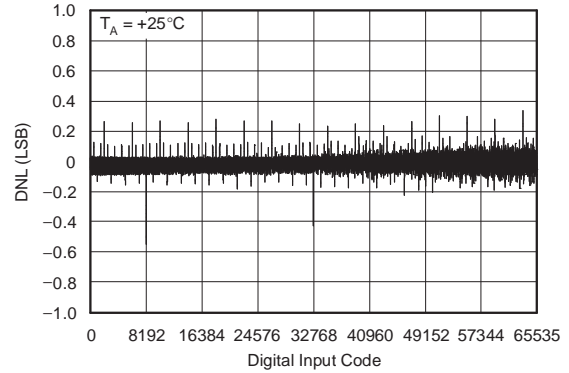
**Channel D**

**LINEARITY ERROR  
vs DIGITAL INPUT CODE**



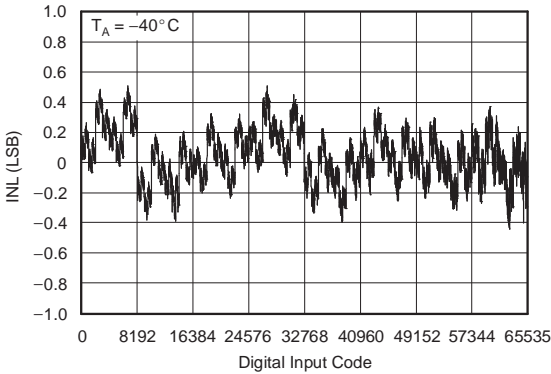
**Figure 19.**

**DIFFERENTIAL LINEARITY ERROR  
vs DIGITAL INPUT CODE**



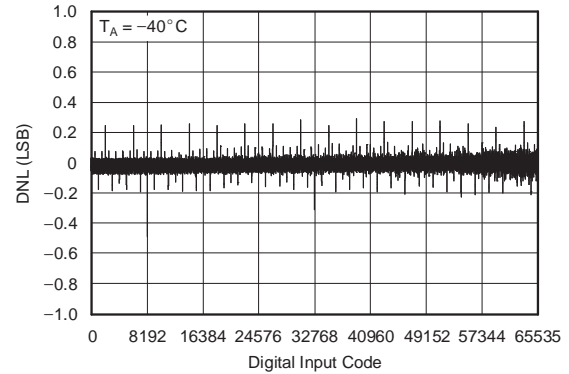
**Figure 20.**

**LINEARITY ERROR  
vs DIGITAL INPUT CODE**



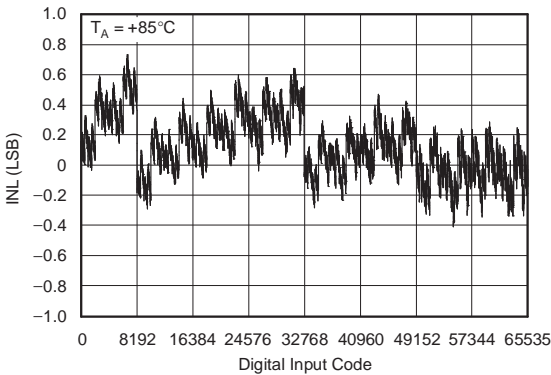
**Figure 21.**

**DIFFERENTIAL LINEARITY ERROR  
vs DIGITAL INPUT CODE**



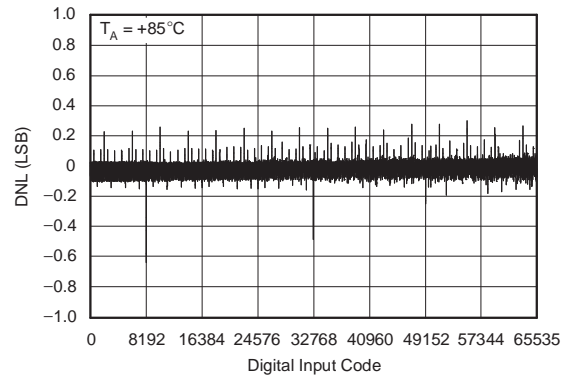
**Figure 22.**

**LINEARITY ERROR  
vs DIGITAL INPUT CODE**



**Figure 23.**

**DIFFERENTIAL LINEARITY ERROR  
vs DIGITAL INPUT CODE**



**Figure 24.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +5\text{ V}$ , unless otherwise noted.

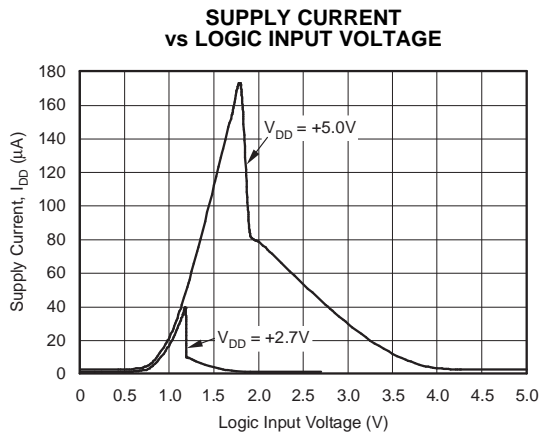


Figure 25.

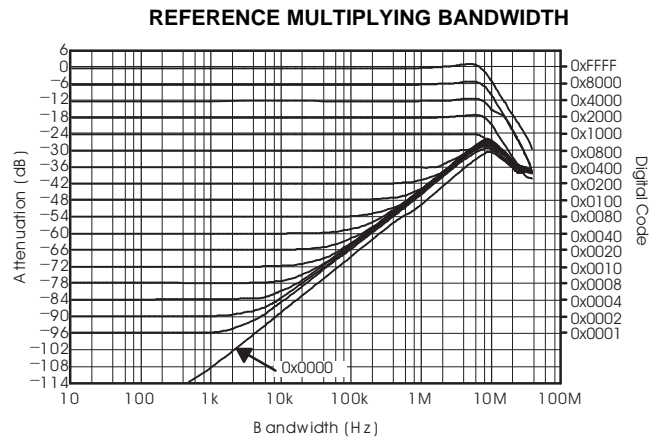


Figure 26.

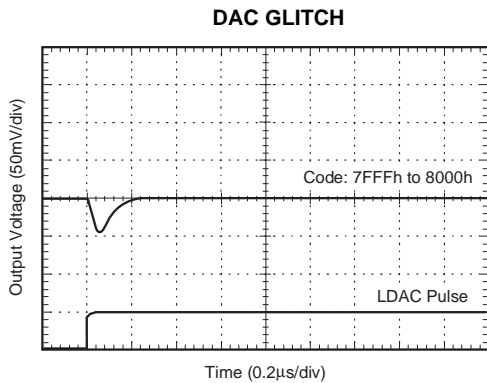


Figure 27.

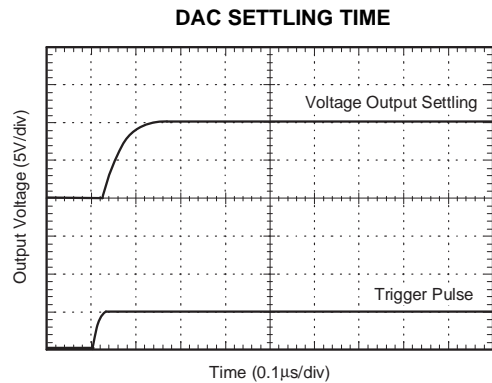


Figure 28.

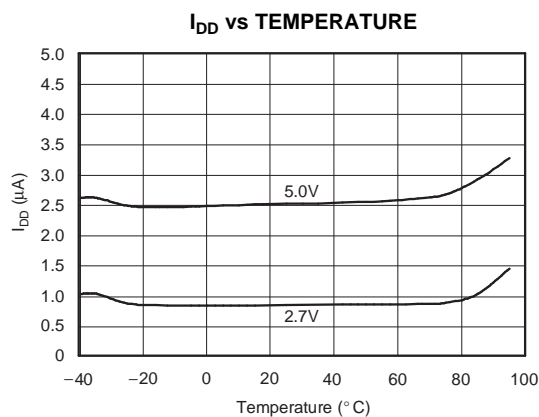


Figure 29.

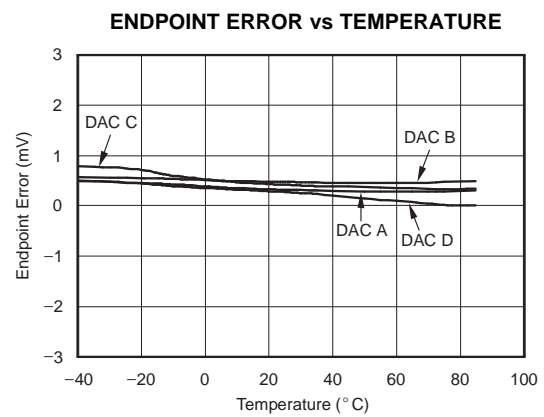


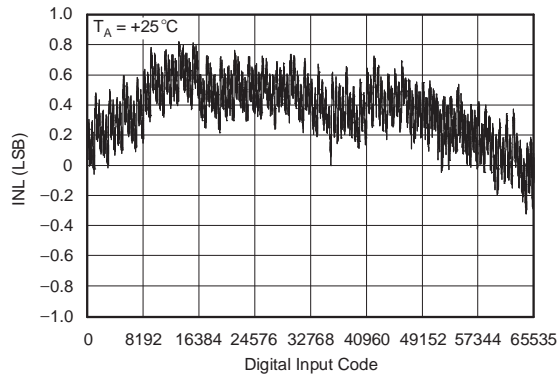
Figure 30.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.7\text{ V}$**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +2.7\text{ V}$ , unless otherwise noted.

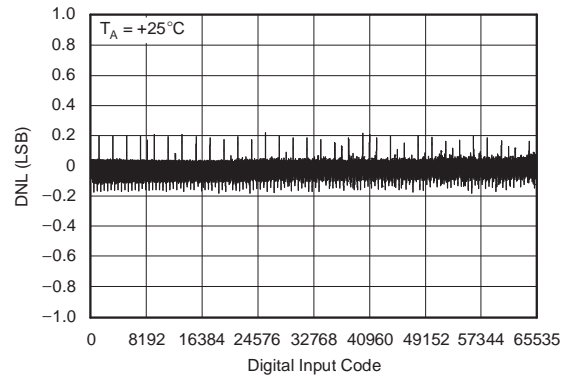
**Channel A**

**LINEARITY ERROR  
vs DIGITAL INPUT CODE**



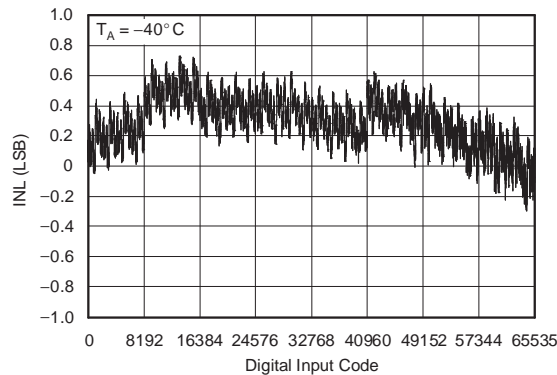
**Figure 31.**

**DIFFERENTIAL LINEARITY ERROR  
vs DIGITAL INPUT CODE**



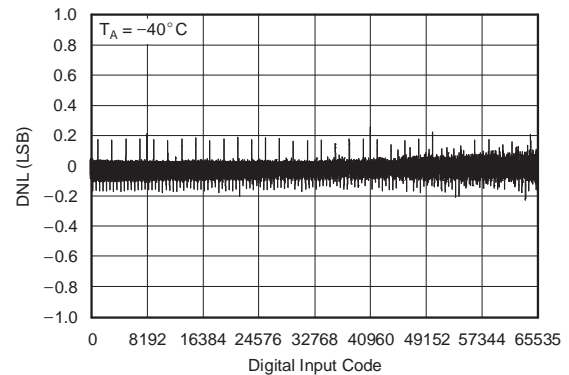
**Figure 32.**

**LINEARITY ERROR  
vs DIGITAL INPUT CODE**



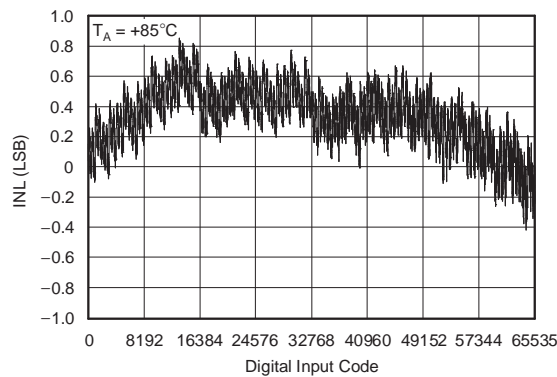
**Figure 33.**

**DIFFERENTIAL LINEARITY ERROR  
vs DIGITAL INPUT CODE**



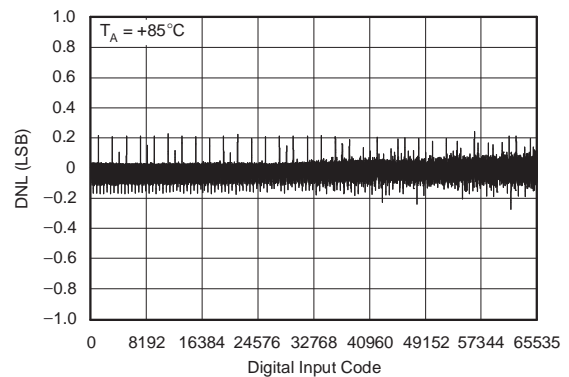
**Figure 34.**

**LINEARITY ERROR  
vs DIGITAL INPUT CODE**



**Figure 35.**

**DIFFERENTIAL LINEARITY ERROR  
vs DIGITAL INPUT CODE**



**Figure 36.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.7\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +2.7\text{ V}$ , unless otherwise noted.

**Channel B**

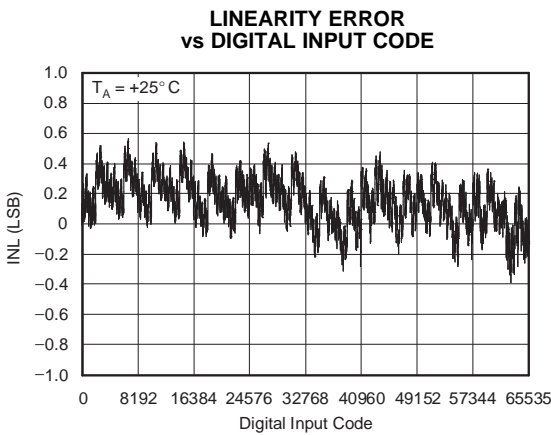


Figure 37.

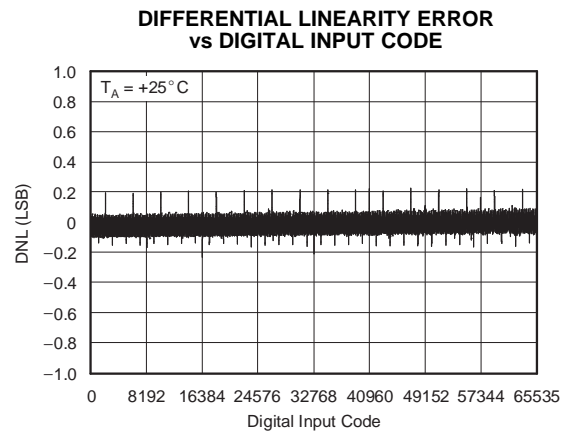


Figure 38.

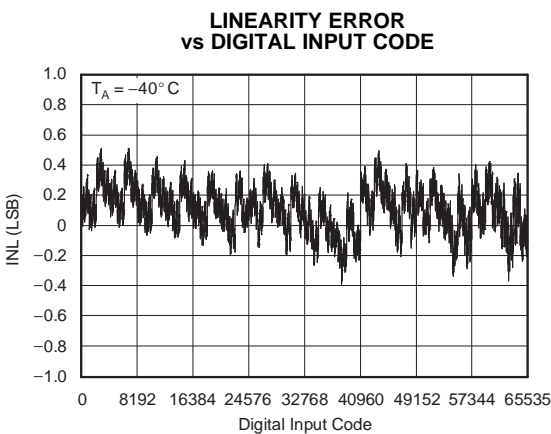


Figure 39.

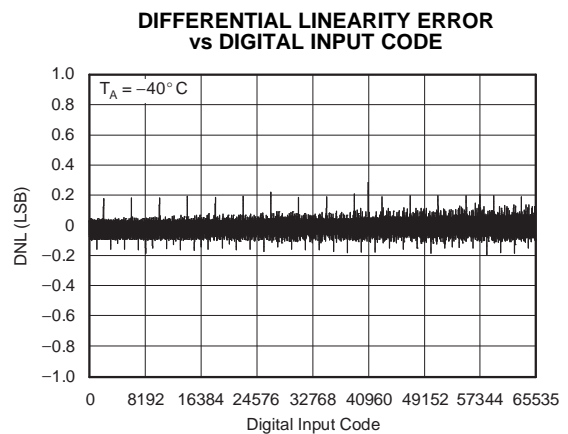


Figure 40.

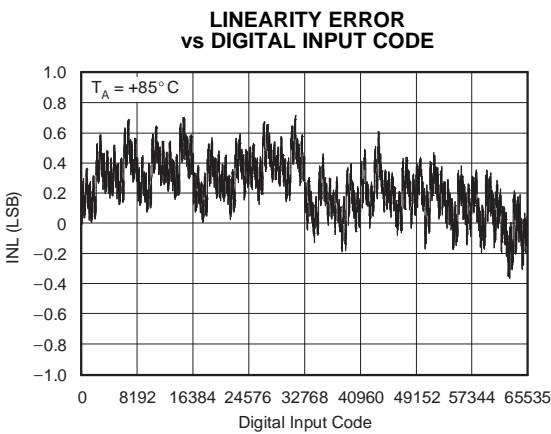


Figure 41.

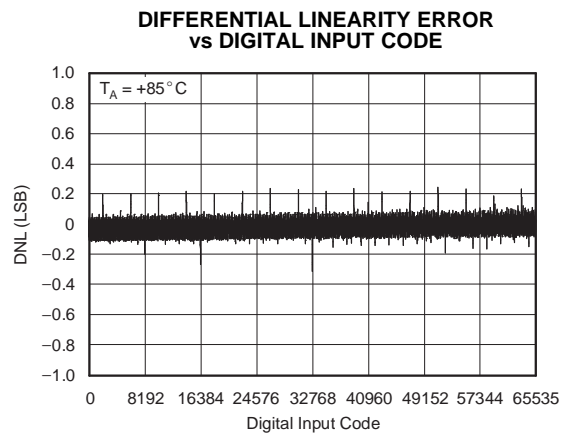
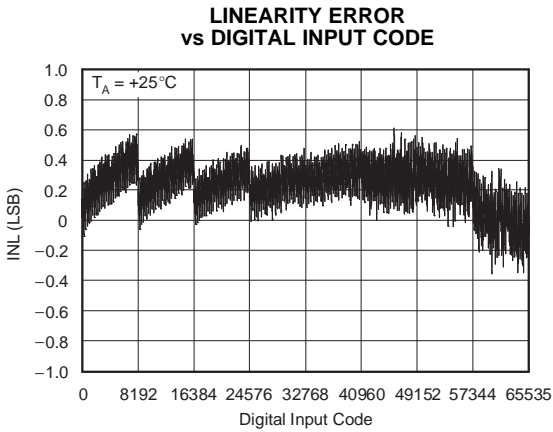


Figure 42.

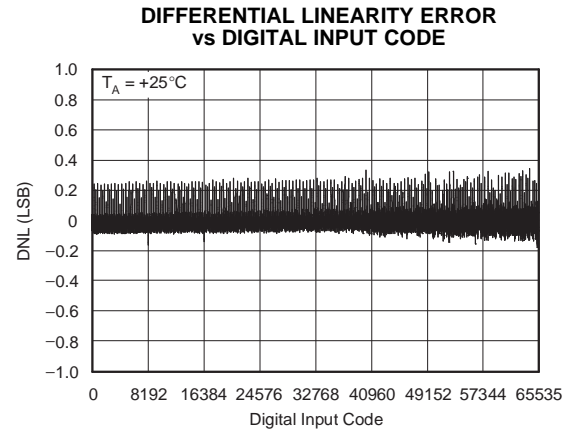
**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.7\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +2.7\text{ V}$ , unless otherwise noted.

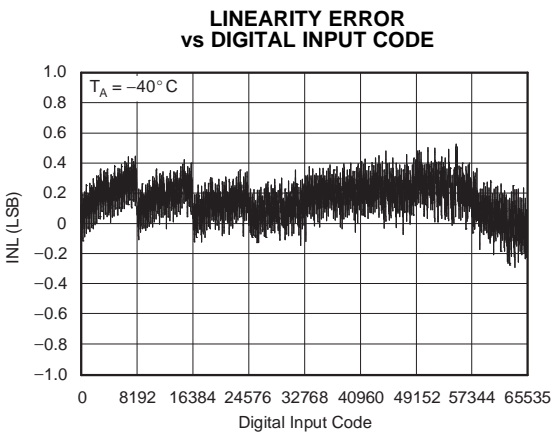
**Channel C**



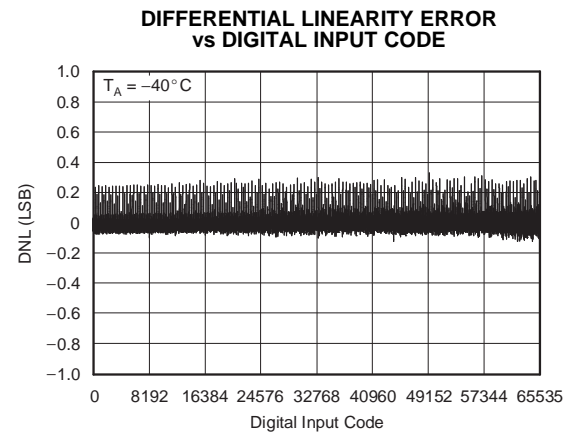
**Figure 43.**



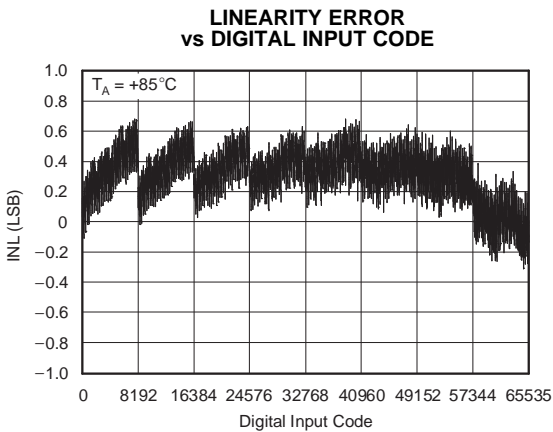
**Figure 44.**



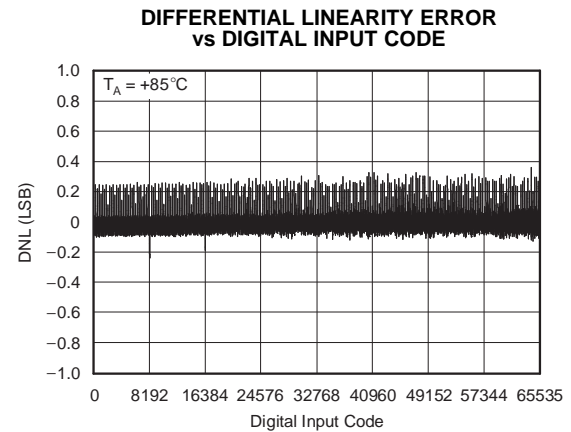
**Figure 45.**



**Figure 46.**



**Figure 47.**

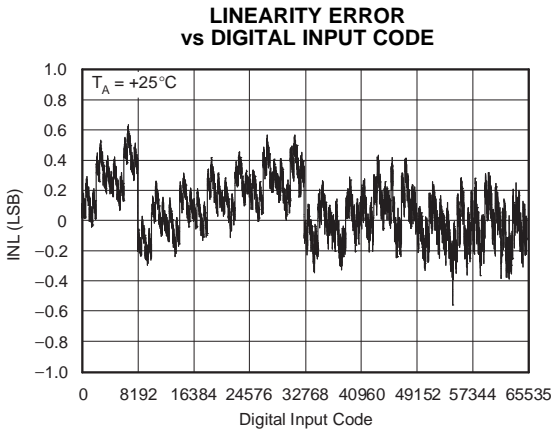


**Figure 48.**

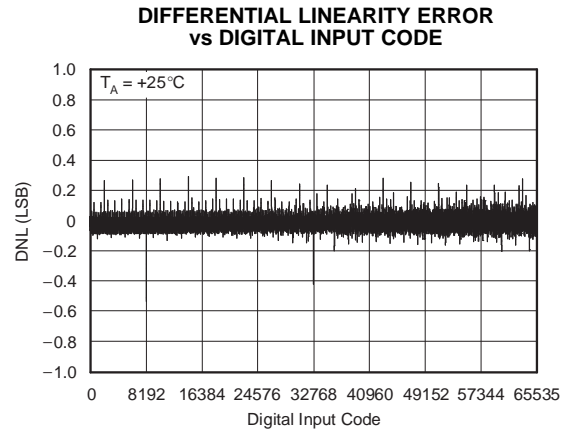
**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.7\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +2.7\text{ V}$ , unless otherwise noted.

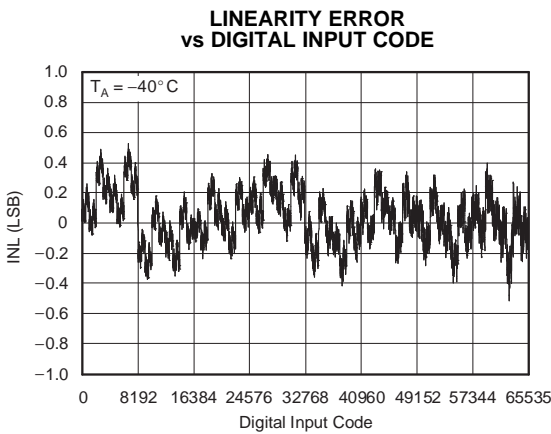
**Channel D**



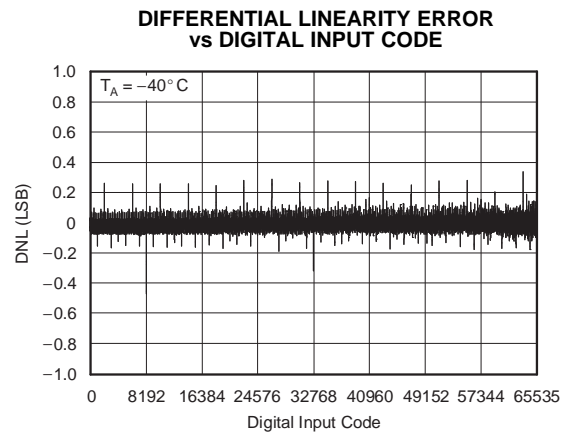
**Figure 49.**



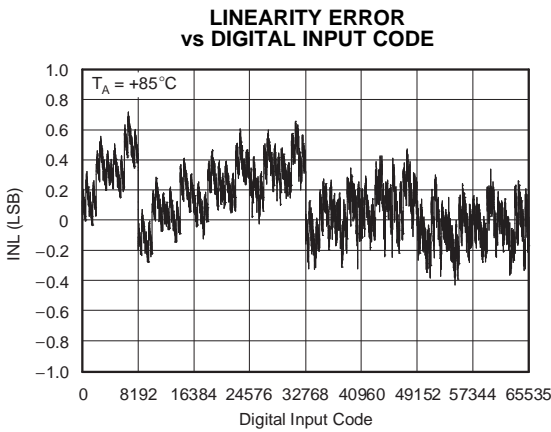
**Figure 50.**



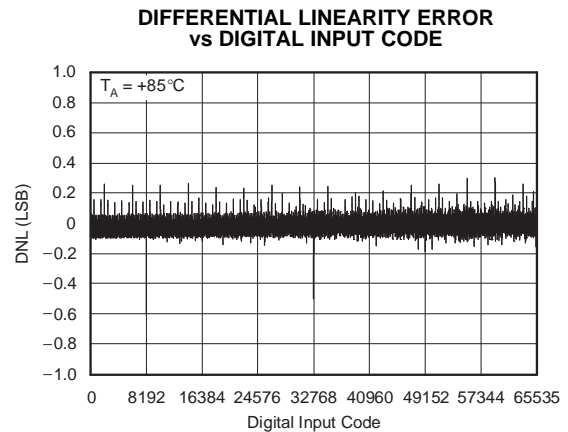
**Figure 51.**



**Figure 52.**



**Figure 53.**



**Figure 54.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.7$  V (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $+V_{DD} = +2.7$  V, unless otherwise noted.

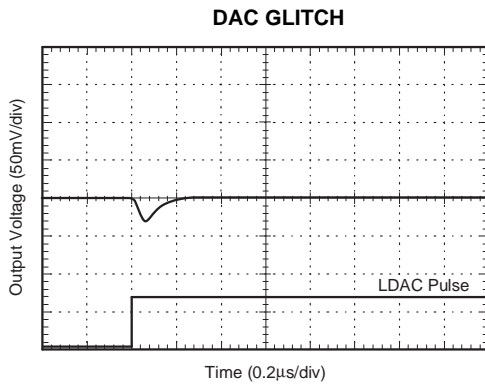


Figure 55.

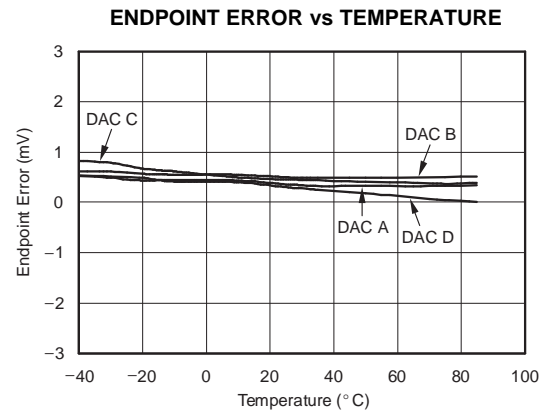


Figure 56.

**TIMING INFORMATION**

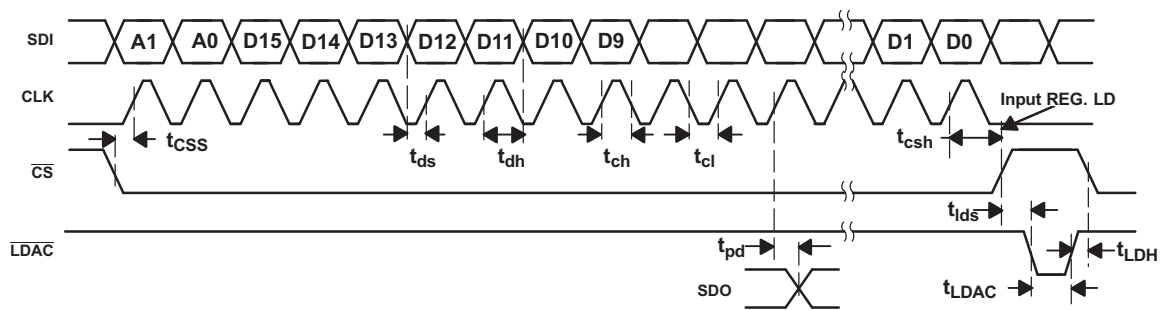


Figure 57. DAC8814 Timing Diagram

## THEORY OF OPERATION

### CIRCUIT OPERATION

The DAC8814 contains four, 16-bit, current-output, digital-to-analog converters (DACs) respectively. Each DAC has its own independent multiplying reference input. The DAC8814 uses a 3-wire SPI-compatible serial data interface, with a configurable asynchronous  $\overline{R\overline{S}}$  pin for half-scale (MSB = 1) or zero-scale (MSB = 0) preset. In addition, an  $\overline{LDAC}$  strobe enables four channel simultaneous updates for hardware-synchronized output voltage changes.

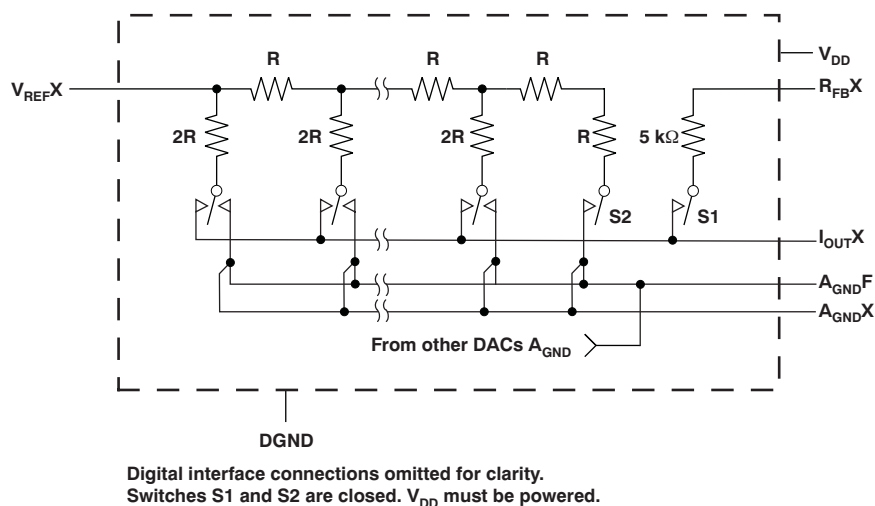
#### D/A Converter

The DAC8814 contains four current-steering R-2R ladder DACs. Figure 58 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The  $R_{FBX}$  pin is connected to the output of the external amplifier. The  $I_{OUTX}$  terminal is connected to the inverting input of the external amplifier. The  $A_{GNDX}$  pin should be Kelvin-connected to the load point in the circuit requiring the full 16-bit accuracy.

The DAC is designed to operate with both negative or positive reference voltages. The  $V_{DD}$  power pin is only used by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal 5 k $\Omega$  feedback resistor. If users are attempting to measure the value of  $R_{FB}$ , power must be applied to  $V_{DD}$  in order to achieve continuity. The DAC output voltage is determined by  $V_{REF}$  and the digital data (D) according to Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{D}{65536} \quad (1)$$

Note that the output polarity is opposite of the  $V_{REF}$  polarity for dc reference voltages.



**Figure 58. Typical Equivalent DAC Channel**

The DAC is also designed to accommodate ac reference input signals. The DAC8814 accommodates input reference voltages in the range of  $-15$  V to  $+15$  V. The reference voltage inputs exhibit a constant nominal input resistance of 5 k $\Omega$ ,  $\pm 20\%$ . On the other hand, the DAC outputs  $I_{OUTA}$ , B, C, D are code-dependent and produce various output resistances and capacitances.

The choice of external amplifier should take into account the variation in impedance generated by the DAC8814 on the amplifiers' inverting input node. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor ( $C_{FB}$ ) may be needed to provide a critically damped output response for step changes in reference input voltages.



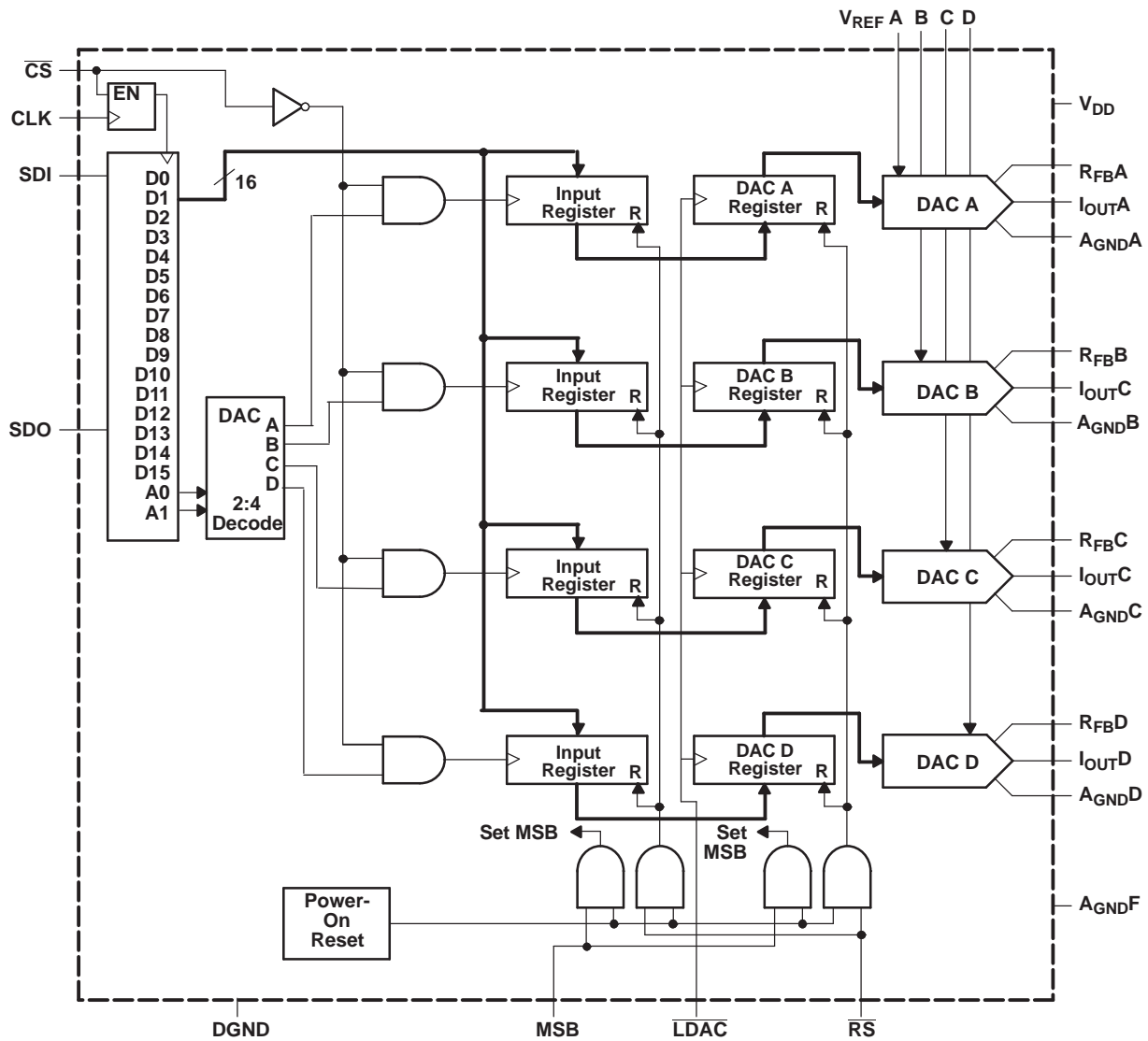


Figure 60. System Level Digital Interfacing

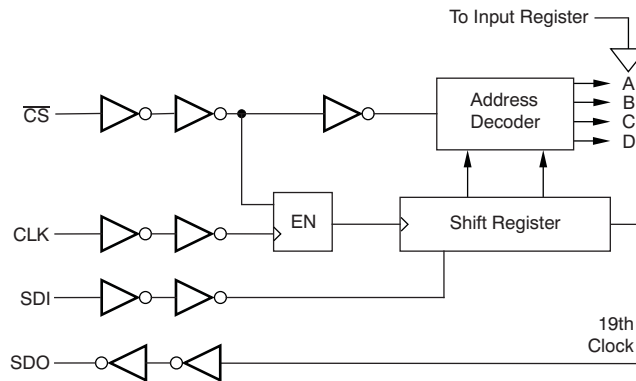
### SERIAL DATA INTERFACE

The DAC8814 uses a 3-wire ( $\overline{CS}$ , SDI, CLK) SPI-compatible serial data interface. Serial data of the DAC8814 is clocked into the serial input register in an 18-bit data-word format. MSB bits are loaded first. Table 2 defines the 18 data-word bits for the DAC8814.

Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the Interface Timing Specifications. Data can only be clocked in while the  $\overline{CS}$  chip select pin is active low. For the DAC8814, only the last 18 bits clocked into the serial register are interrogated when the  $\overline{CS}$  pin returns to the logic high state.

Since most microcontrollers output serial data in 8-bit bytes, three right-justified data bytes can be written to the DAC8814. Keeping the  $\overline{CS}$  line low between the first, second, and third byte transfers results in a successful serial register update.

Once the data is properly aligned in the shift register, the positive edge of the  $\overline{CS}$  initiates the transfer of new data to the target DAC register, determined by the decoding of address bits A1 and A0. For the DAC8814, Table 1, Table 2, Table 3 and Figure 57 define the characteristics of the software serial interface. Figure 61 shows the equivalent logic interface for the key digital control pins for the DAC8814.



**Figure 61. DAC8814 Equivalent Logic Interface**

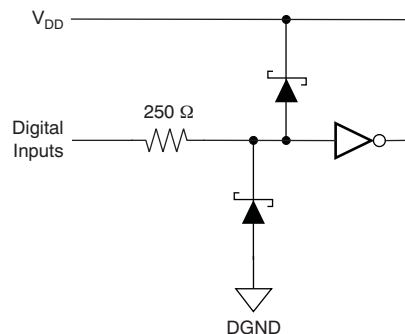
Two additional pins  $\overline{RS}$  and MSB provide hardware control over the preset function and DAC register loading. If these functions are not needed, the  $\overline{RS}$  pin can be tied to logic high. The asynchronous input  $\overline{RS}$  pin forces all input and DAC registers to either the zero-code state (MSB = 0), or the half-scale state (MSB = 1).

### POWER ON RESET

When the  $V_{DD}$  power supply is turned on, an internal reset strobe forces all the Input and DAC registers to the zero-code state or half-scale, depending on the MSB pin voltage. The  $V_{DD}$  power supply should have a smooth positive ramp without drooping in order to have consistent results, especially in the region of  $V_{DD} = 1.5$  V to 2.3 V. The DAC register data stays at zero or half-scale setting until a valid serial register data load takes place.

### ESD Protection Circuits

All logic-input pins contain back-biased ESD protection zener diodes connected to ground (DGND) and  $V_{DD}$  as shown in [Figure 62](#).



**Figure 62. Equivalent ESD Protection Circuits**

**PCB LAYOUT**

The DAC8814 is a high-accuracy DAC that can have its performance compromised by grounding and printed circuit board (PCB) lead trace resistance. The 16-bit DAC8814 with a 10-V full-scale range has an LSB value of 153  $\mu$ V. The ladder and associated reference and analog ground currents for a given channel can be as high as 2 mA. With this 2mA current level, a series wiring and connector resistance of only 76 m $\Omega$  will cause 1 LSB of voltage drop. The preferred PCB layout for the DAC8814 is to have all A<sub>GND</sub>X pins connected directly to an analog ground plane at the unit. The non-inverting input of each channel I/V converter should also either connect directly to the analog ground plane or have an individual sense trace back to the A<sub>GND</sub>X pin connection. The feedback resistor trace to the I/V converter should also be kept short and have low resistance in order to prevent IR drops from contributing to gain error. This attention to wiring ensures the optimal performance of the DAC8814.

**Table 1. Control Logic Truth Table<sup>(1)</sup>**

CS	CLK	LDAC	RS	MSB	SERIAL SHIFT REGISTER	INPUT REGISTER	DAC REGISTER
H	X	H	H	X	No effect	Latched	Latched
L	L	H	H	X	No effect	Latched	Latched
L	$\uparrow+$	H	H	X	Shift register data advanced one bit	Latched	Latched
L	H	H	H	X	No effect	Latched	Latched
$\uparrow+$	L	H	H	X	No effect	Selected DAC updated with current SR contents	Latched
H	X	L	H	X	No effect	Latched	Transparent
H	X	H	H	X	No effect	Latched	Latched
H	X	$\uparrow+$	H	X	No effect	Latched	Latched
H	X	H	L	0	No effect	Latched data = 0000h	Latched data = 0000h
H	X	H	L	H	No effect	Latched data = 8000h	Latched data = 8000h

(1)  $\uparrow+$  = Positive logic transition; X = Do not care

**Table 2. Serial Input Register Data Format, Data Loaded MSB First<sup>(1)</sup>**

Bit	B17 (MSB)	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
Data	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) Only the last 18 bits of data clocked into the serial register (address + data) are inspected when the CS line positive edge returns to logic high. At this point an internally-generated load strobe transfers the serial register data contents (bits D15-D0) to the decoded DAC-input-register address determined by bits A1 and A0. Any extra bits clocked into the DAC8814 shift register are ignored; only the last 18 bits clocked in are used. If double-buffered data is not needed, the LDAC pin can be tied logic low to disable the DAC registers.

**Table 3. Address Decode**

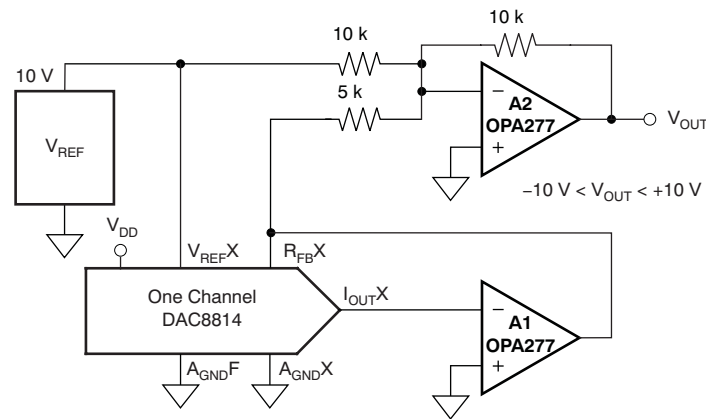
A1	A0	DAC DECODE
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

## APPLICATION INFORMATION

The DAC8814, a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output  $I_{OUT}$  is the inverse of the input reference voltage at  $V_{REF}$ .

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing, as shown in Figure 63. An additional external op amp A2 is added as a summing amp. In this circuit the first and second amps (A1 and A2) provide a gain of 2X that widens the output span to 20 V. A 4-quadrant multiplying circuit is implemented by using a 10-V offset of the reference voltage to bias A2. According to the following circuit transfer equation (Equation 2), input data (D) from code 0 to full scale produces output voltages of  $V_{OUT} = -10\text{ V}$  to  $V_{OUT} = 10\text{ V}$ .

$$V_{OUT} = \left( \frac{D}{32,768} - 1 \right) \times V_{REF} \quad (2)$$



Digital interface connections omitted for clarity.

**Figure 63. Four-Quadrant Multiplying Application Circuit**

### Cross-Reference

The DAC8814 has an industry-standard pinout. Table 4 provides the cross-reference information.

**Table 4. Cross-Reference**

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC8814ICDB	±1	±1	–40°C to +85°C	28-Lead MicroSOIC	SSOP-28	N/A
DAC8814IBDB	±4	±1.5	–40°C to +85°C	28-Lead MicroSOIC	SSOP-28	AD5544RS

### Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (September 2005) to B Revision	Page
• Changed Equation 2 .....	21

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8814IBDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8814	<a href="#">Samples</a>
DAC8814IBDBT	ACTIVE	SSOP	DB	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8814	<a href="#">Samples</a>
DAC8814ICDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8814	<a href="#">Samples</a>
DAC8814ICDBT	ACTIVE	SSOP	DB	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8814	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

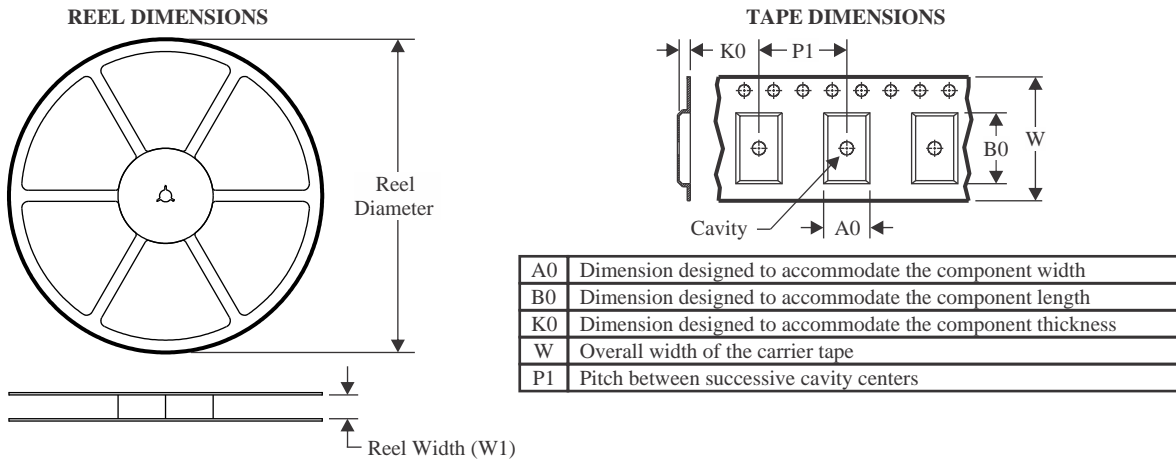
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8814IBDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
DAC8814ICDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8814IBDBR	SSOP	DB	28	2000	350.0	350.0	43.0
DAC8814ICDBR	SSOP	DB	28	2000	350.0	350.0	43.0

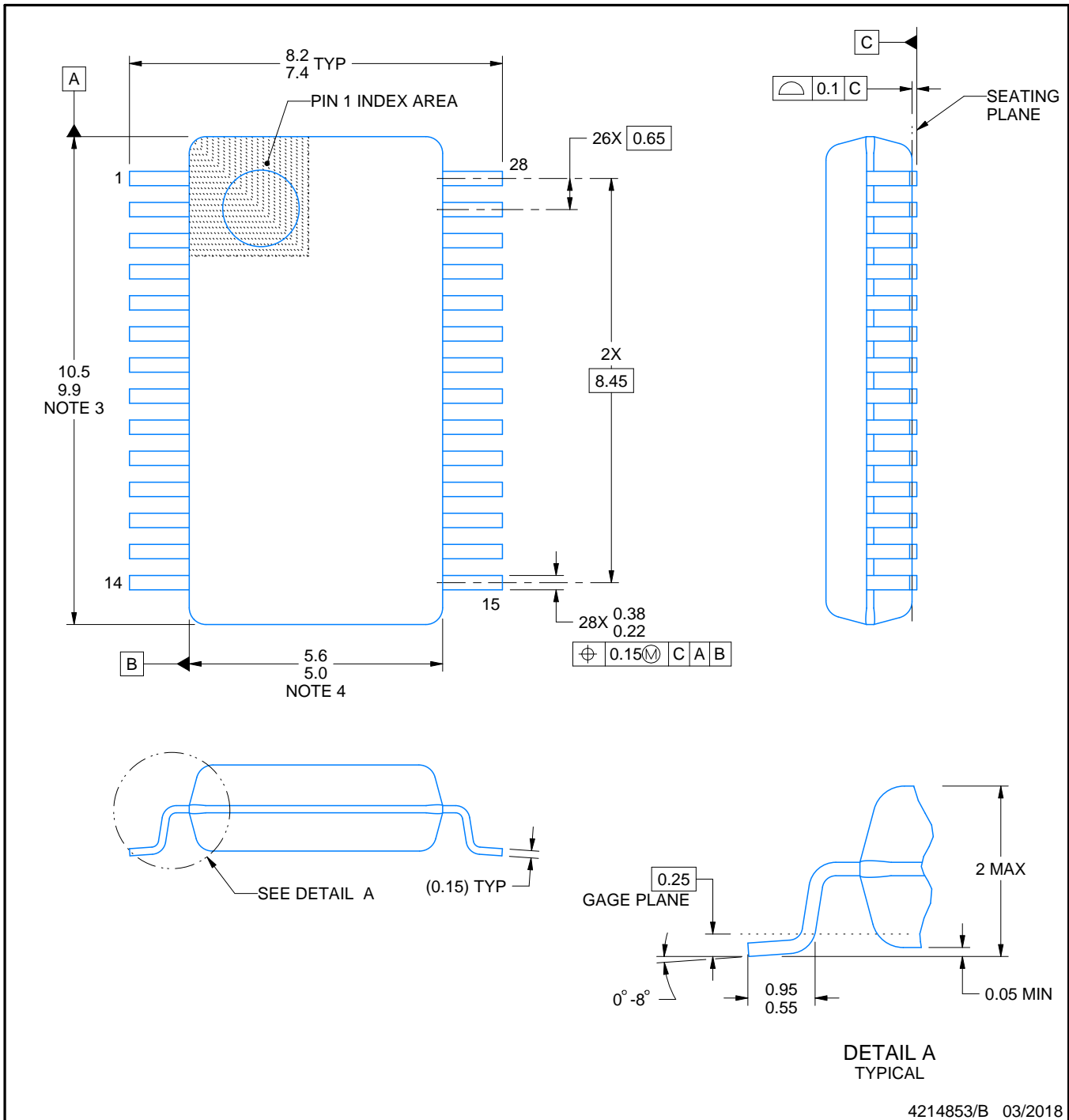
# DB0028A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

### NOTES:

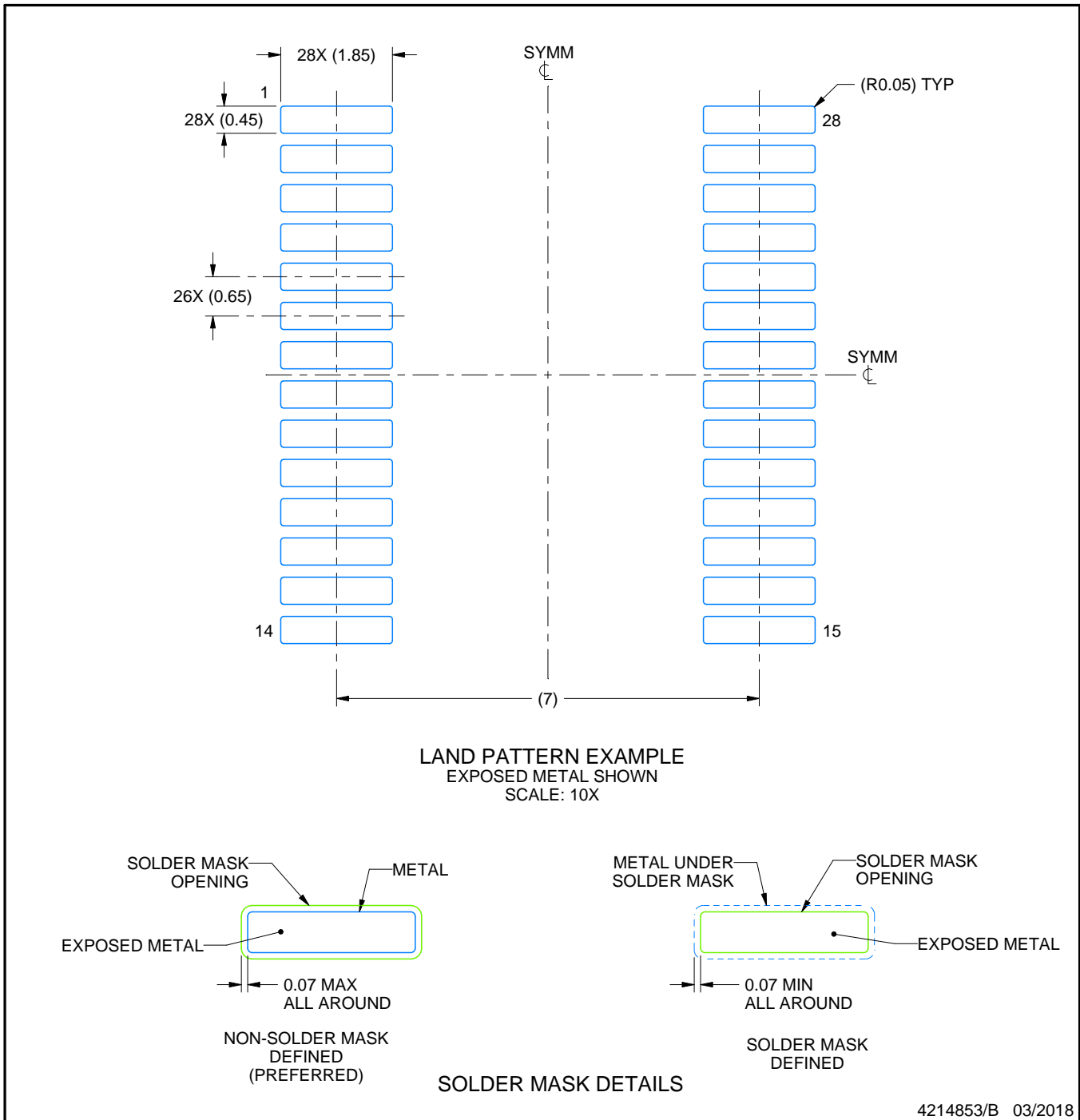
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

NOTES: (continued)

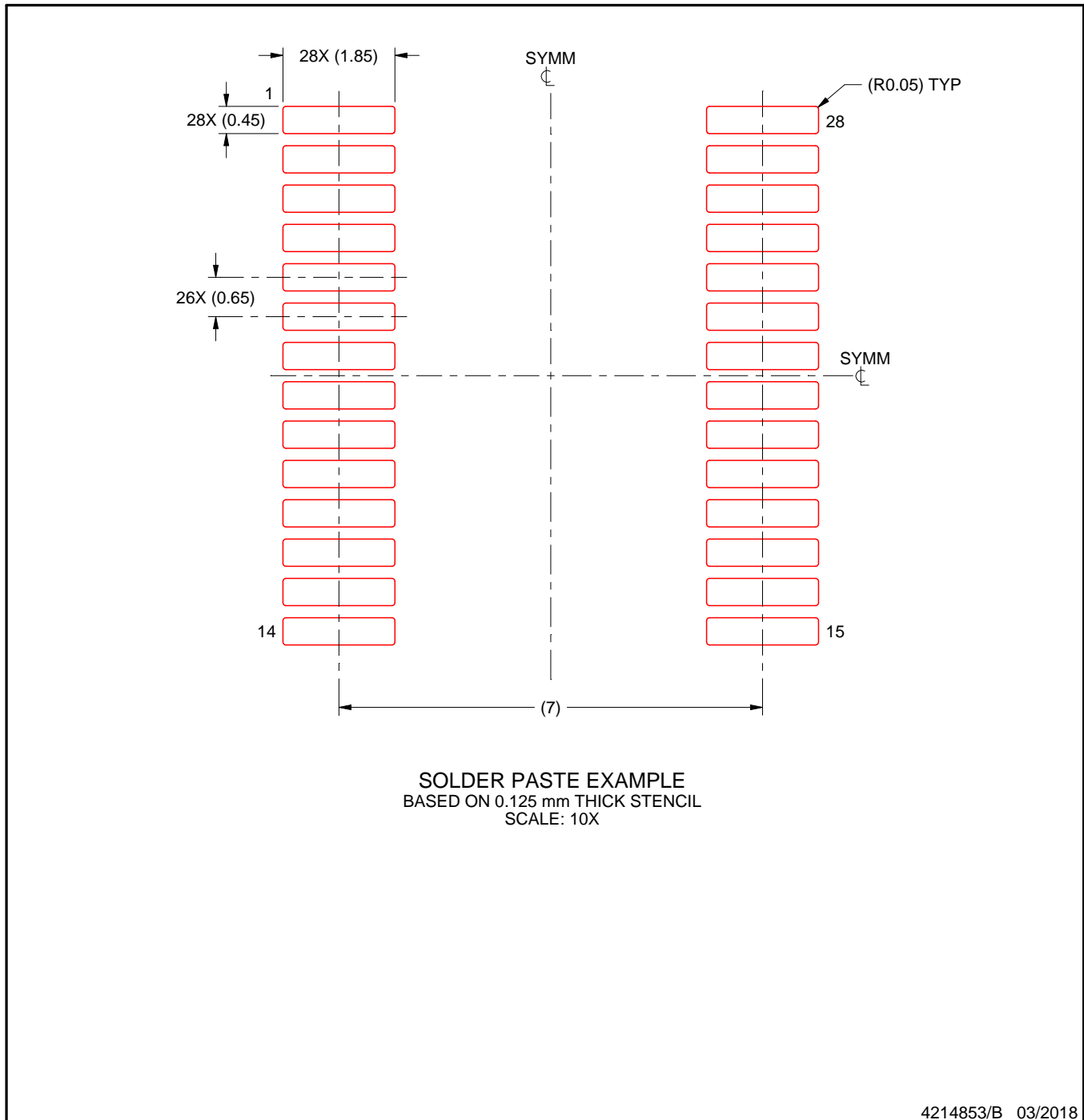
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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