



# THE DATASHEET OF AOTF5N50



### General Description

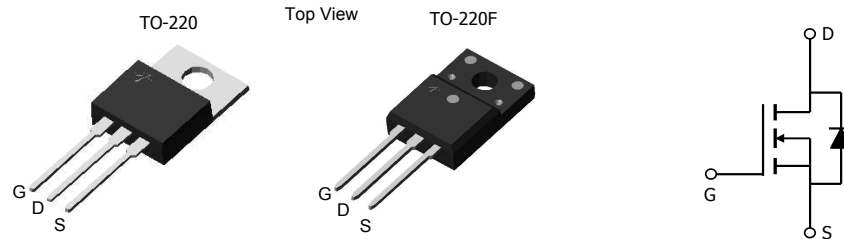
The AOT5N50 & AOTF5N50 have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low  $R_{DS(on)}$ ,  $C_{iss}$  and  $C_{rss}$  along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

For Halogen Free add "L" suffix to part number:  
AOT5N50L & AOTF5N50L

### Product Summary

$V_{DS}$	600V@150°C
$I_D$ (at $V_{GS}=10V$ )	5A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 1.5Ω

100% UIS Tested  
100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	AOT5N50	AOTF5N50	Units
Drain-Source Voltage	$V_{DS}$	500		V
Gate-Source Voltage	$V_{GS}$	±30		V
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	5	5*
		$T_C=100^\circ C$	3.3	3.3*
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	18		A
Avalanche Current <sup>C</sup>	$I_{AR}$	2.6		A
Repetitive avalanche energy <sup>C</sup>	$E_{AR}$	101		mJ
Single pulsed avalanche energy <sup>G</sup>	$E_{AS}$	203		mJ
Peak diode recovery dv/dt	dv/dt	5		V/ns
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	104	35.0
		Derate above 25°C	0.8	0.3
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	$T_L$	300		°C

### Thermal Characteristics

Parameter	Symbol	AOT5N50	AOTF5N50	Units
Maximum Junction-to-Ambient <sup>A,D</sup>	$R_{\theta JA}$	65	65	°C/W
Maximum Case-to-sink <sup>A</sup>	$R_{\theta CS}$	0.5	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	1.2	3.6	°C/W

\* Drain current limited by maximum junction temperature.

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	500			V
BV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V		0.55		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V V <sub>DS</sub> =400V, T <sub>J</sub> =125°C			1 10	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA	3.5	4.1	4.5	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =2.5A		1.1	1.5	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =40V, I <sub>D</sub> =2.5A		6		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.75	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				5	A
I <sub>SM</sub>	Maximum Body-Diode Pulsed Current				18	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz	414	517	620	pF
C <sub>oss</sub>	Output Capacitance		46	57	68	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		3.9	4.9	5.9	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1.9	3.8	6	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =400V, I <sub>D</sub> =5A		15.5	19	nC
Q <sub>gs</sub>	Gate Source Charge		3.4	4	nC	
Q <sub>gd</sub>	Gate Drain Charge		7.2	8.6	nC	
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =250V, I <sub>D</sub> =5A, R <sub>G</sub> =25Ω		14.5	17.4	ns
t <sub>r</sub>	Turn-On Rise Time		29	35	ns	
t <sub>D(off)</sub>	Turn-Off Delay Time		34.5	41.4	ns	
t <sub>f</sub>	Turn-Off Fall Time		24	29	ns	
t <sub>rr</sub>	Body Diode Reverse Recovery Time		I <sub>F</sub> =5A, dI/dt=100A/μs, V <sub>DS</sub> =100V		166	199
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =5A, dI/dt=100A/μs, V <sub>DS</sub> =100V		1.37	1.6	μC

A. The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C, Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

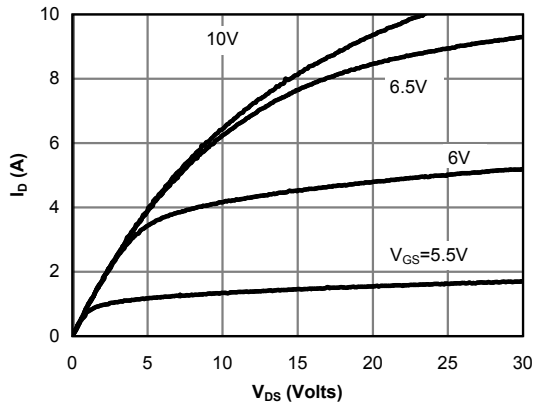
E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

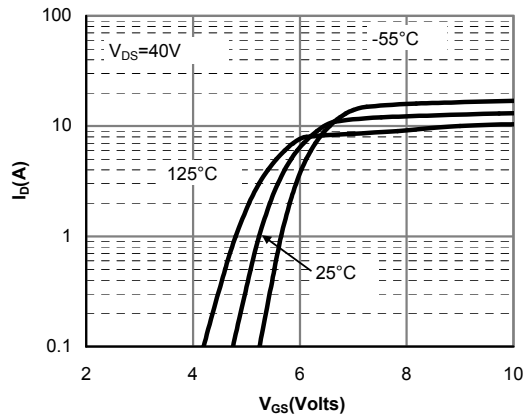
G. L=60mH, I<sub>AS</sub>=2.6A, V<sub>DD</sub>=150V, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25°C

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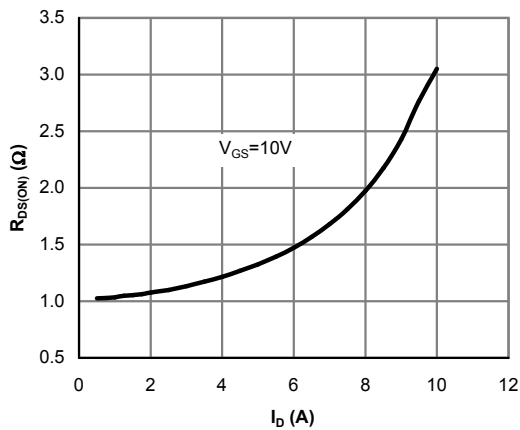
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



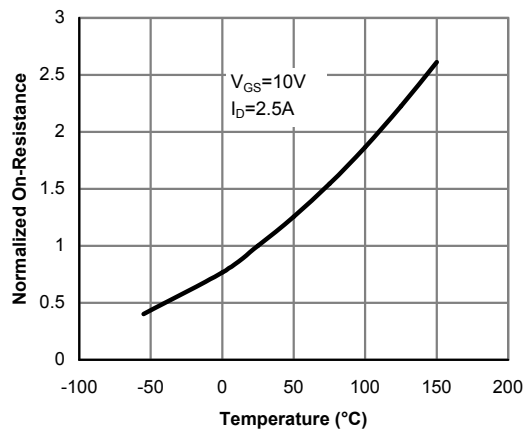
**Fig 1: On-Region Characteristics**



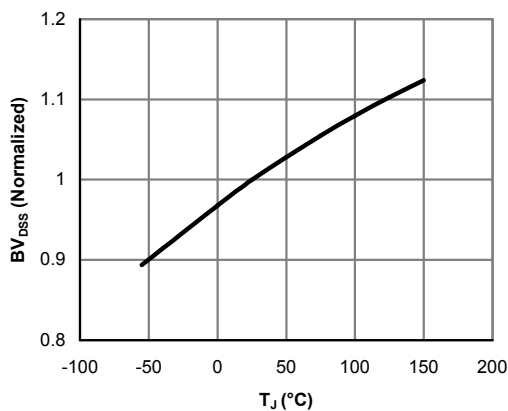
**Figure 2: Transfer Characteristics**



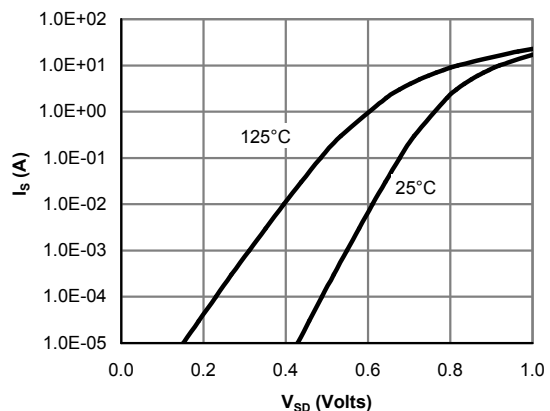
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**

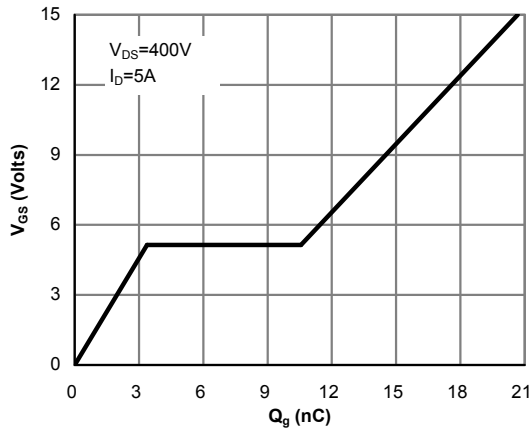


**Figure 5: Break Down vs. Junction Temperature**

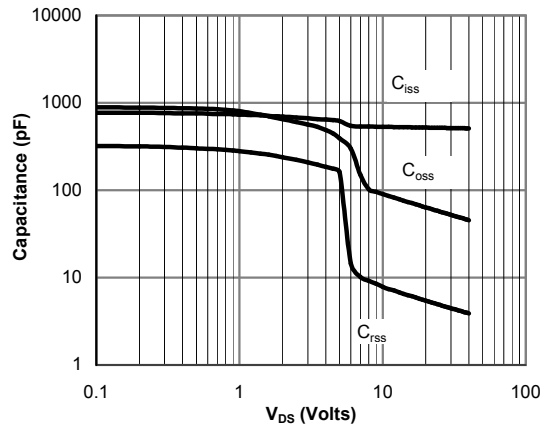


**Figure 6: Body-Diode Characteristics (Note E)**

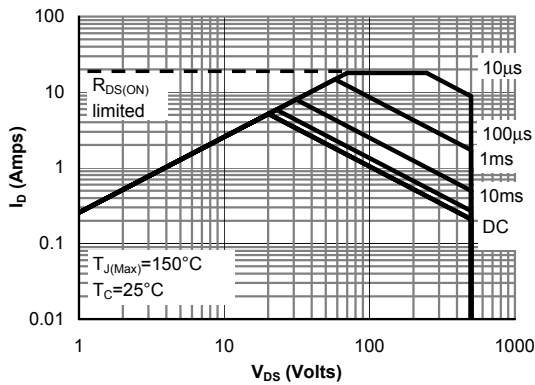
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



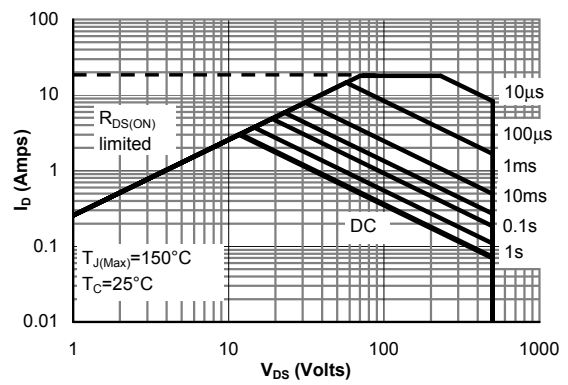
**Figure 7: Gate-Charge Characteristics**



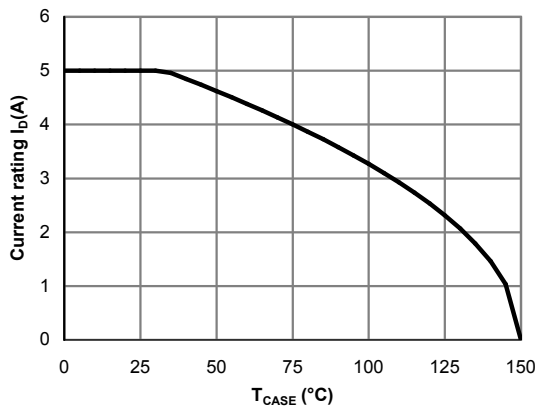
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area for AOT5N50 (Note F)**



**Figure 10: Maximum Forward Biased Safe Operating Area for AOTF5N50 (Note F)**



**Figure 11: Current De-rating (Note B)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

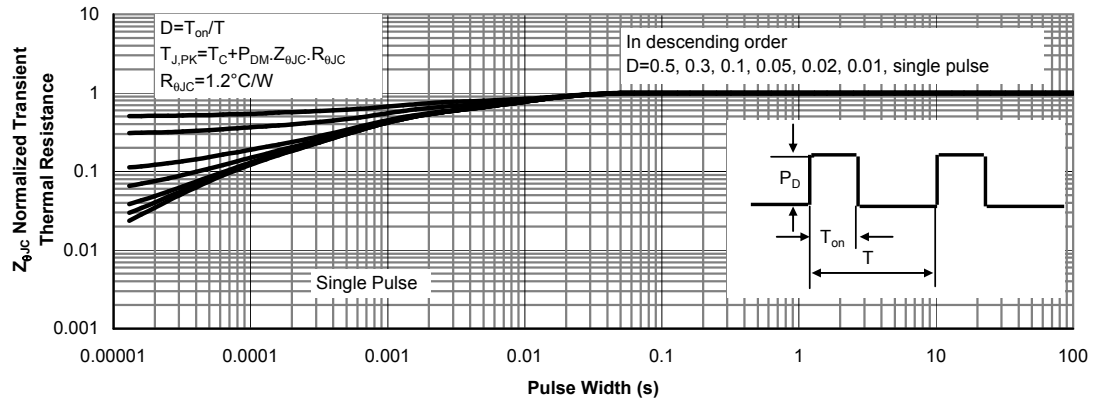


Figure 12: Normalized Maximum Transient Thermal Impedance for AOT5N50 (Note F)

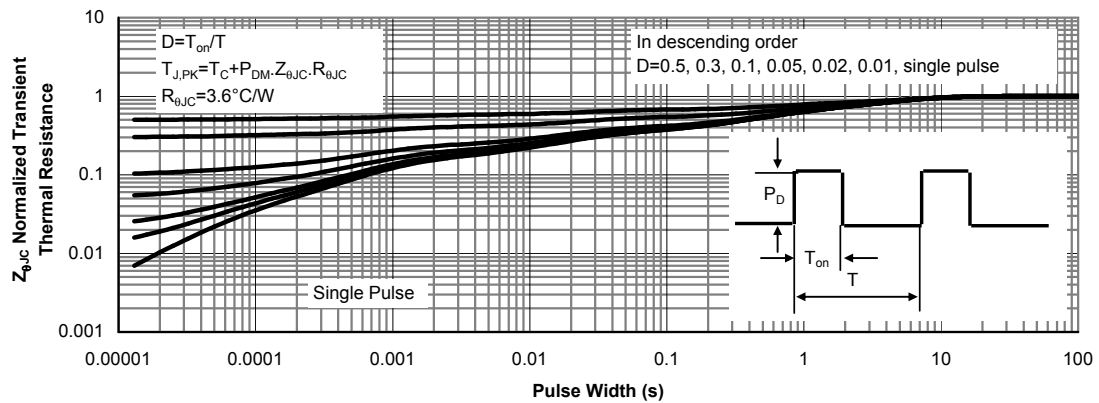
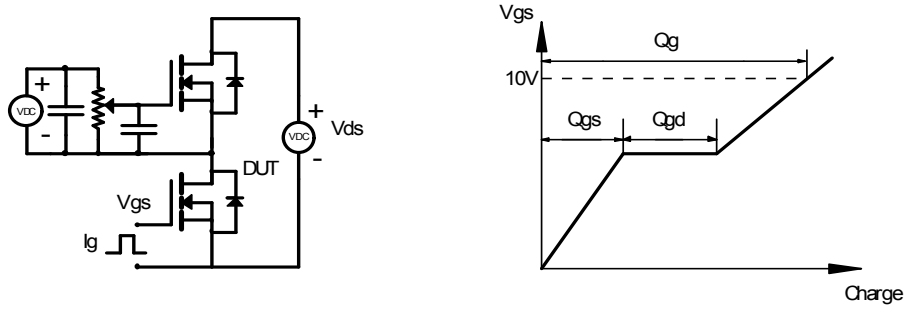
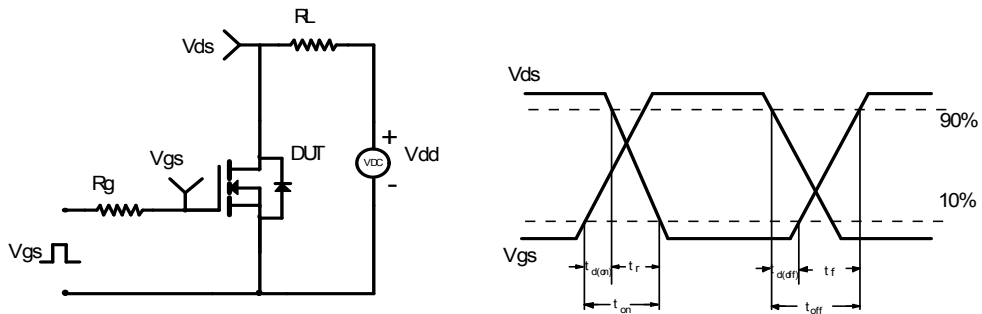


Figure 13: Normalized Maximum Transient Thermal Impedance for AOTF5N50 (Note F)

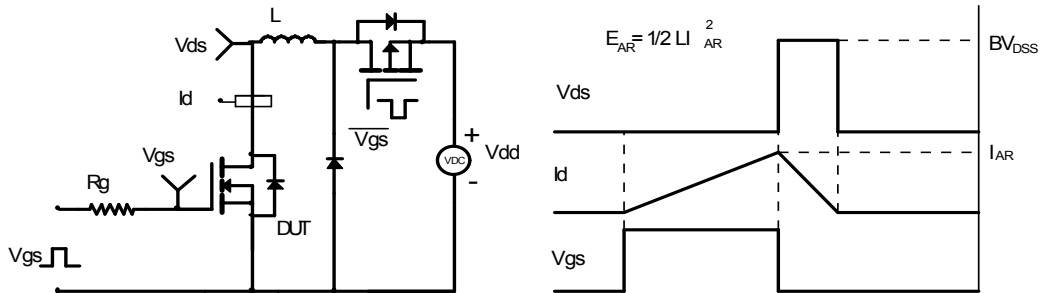
Gate Charge Test Circuit & Waveform



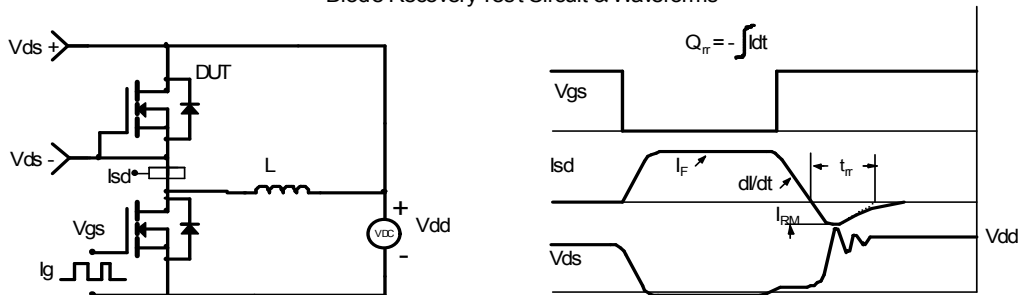
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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