



**THE DATASHEET OF  
AOZ1915DI**



### General Description

The AOZ1915 is a high-performance, current-mode, constant frequency boost regulator with internal MOSFET and internal Schottky diode. The 600kHz / 1.2MHz switching frequency allows the use of low-profile inductor and capacitors. The current-mode control ensures easy loop compensation and fast transient response. The AOZ1915 works from a 2.7V to 5.5V input voltage range and generates an output voltage as high as 22V. Other features include input under-voltage lockout, cycle-by-cycle current limit, thermal shutdown and soft-start.

The AOZ1915 is available in a tiny 4mm x 3mm 12-pin DFN package and is rated over a -40°C to +85°C

### Features

- 2.7V to 5.5V input voltage range
- Adjustable output up to 22V
- Internal Schottky diode
- 600kHz/1.2MHz constant switching frequency
- Cycle-by-cycle current limit
- Thermal overload protection
- Programmable Soft-start
- Small 4mm x 3mm DFN 12L package

### Applications

- LCD TV
- LCD Monitors
- Notebook Displays
- PCMCIA Cards
- Hand-Held Devices
- GPS power
- TV tuner



### Typical Application Circuit

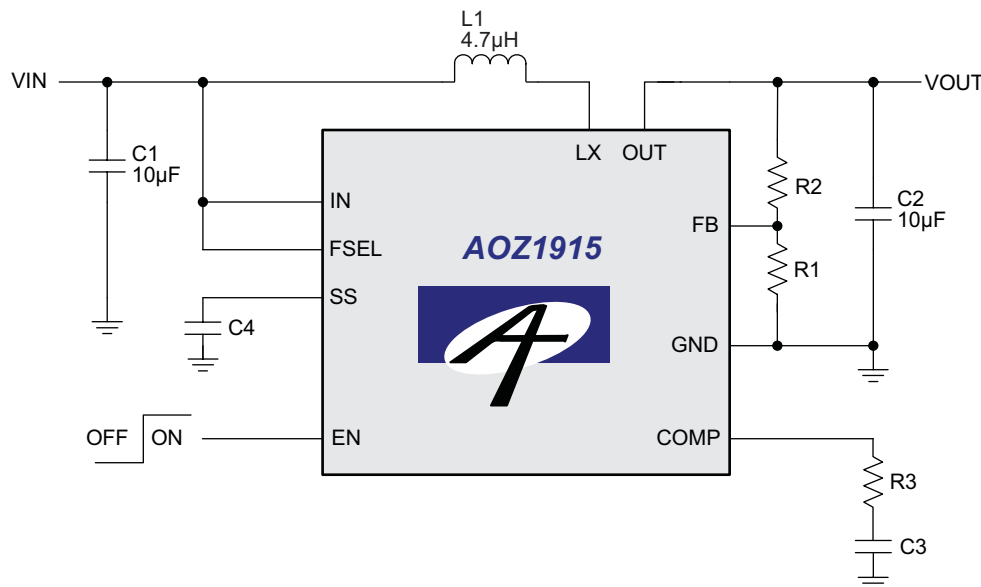


Figure 1. Typical Application Circuit

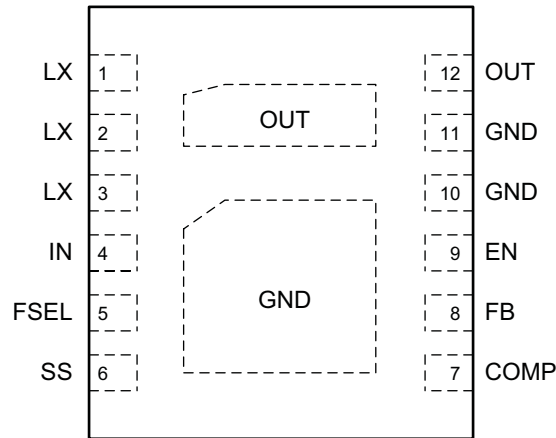
## Ordering Information

| Part Number | Operating Temperature Range | Package    | Environmental |
|-------------|-----------------------------|------------|---------------|
| AOZ1915DI   | -40°C to +85°C              | 4x3 DFN-12 | Green Product |



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant. Please visit [www.aosmd.com/web/quality/rohs\\_compliant.jsp](http://www.aosmd.com/web/quality/rohs_compliant.jsp) for additional information.

## Pin Configuration



**DFN-12**  
(Top View)

## Pin Description

| Pin Number | Pin Name | Pin Description  |
|------------|----------|--|
| 1, 2, 3    | LX       | Boost Regulator Switching Node.  |
| 4          | IN       | Input Supply Pin.  |
| 5          | FSEL     | Frequency Select Pin. The switching frequency is 1.2MHz when FSEL is connected to IN, and 600kHz when FSEL is connected to ground.                   |
| 6          | SS       | Soft-Start Pin. Connect a capacitor from SS to GND to set the soft-start period.   |
| 7          | COMP     | Compensation Pin. Connect a RC network between COMP and ground to compensate the control loop.   |
| 8          | FB       | Feedback Input. Connect a resistive divider between the boost regulator output and ground with the center tap connected to FB to set output voltage. |
| 9          | EN       | Enable Input. Pull EN high to enable the boost regulator and pull EN low to disable the regulator.   |
| 10, 11     | GND      | Ground.  |
| 12         | OUT      | Boost Regulator Output   |

### Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

| Parameter                     | Rating          |
|-------------------------------|-----------------|
| IN to GND                     | -0.3V to +6V    |
| LX, OUT to GND                | -0.3V to +26V   |
| COMP, EN, FB, FSEL, SS to GND | -0.3V to +6V    |
| Storage Temperature ( $T_S$ ) | -65°C to +150°C |
| ESD Rating <sup>(1)</sup>     | 2kV             |

**Note:**

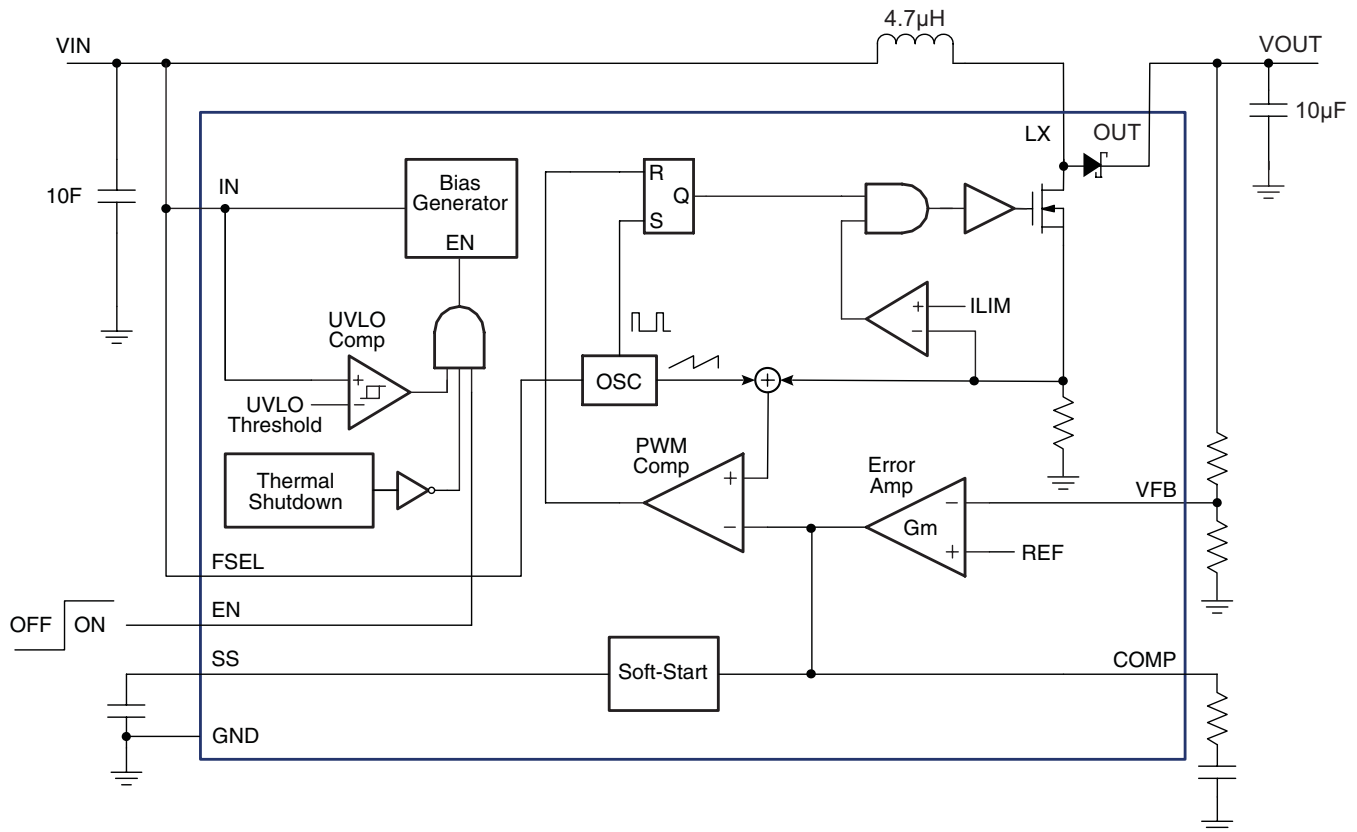
1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

### Recommend Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

| Parameter  | Rating          |
|--|-----------------|
| Supply Voltage ( $V_{IN}$ )                                  | 2.7V to 5.5V    |
| Output Voltage ( $V_{OUT}$ )                                 | $V_{IN}$ to 22V |
| Ambient Temperature ( $T_A$ )                                | -40°C to +85°C  |
| Package Thermal Resistance<br>4 x 3 DFN-10 ( $\Theta_{JA}$ ) | 48°C/W          |

### Functional Block Diagram



## Electrical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 3.3\text{V}$ , unless otherwise specified. Specifications in **BOLD** indicate an ambient temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

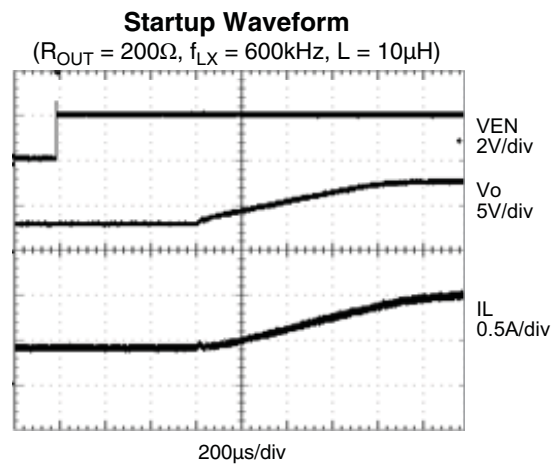
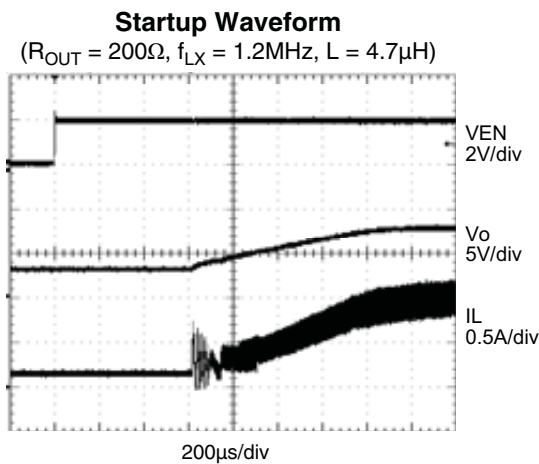
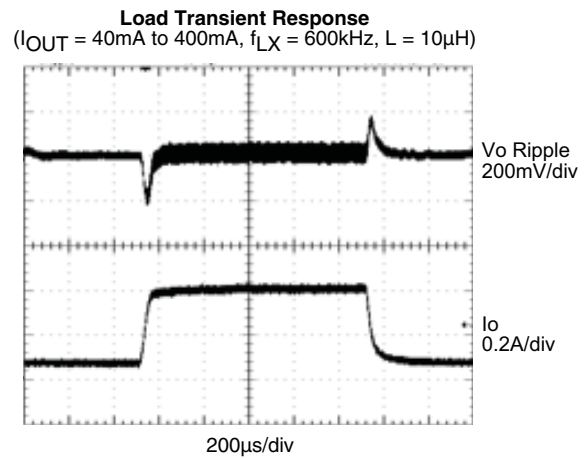
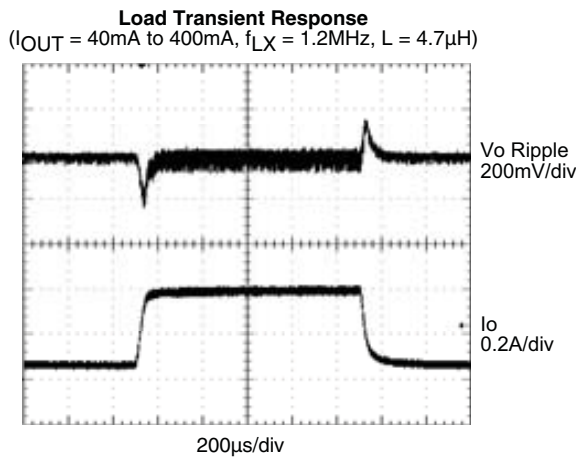
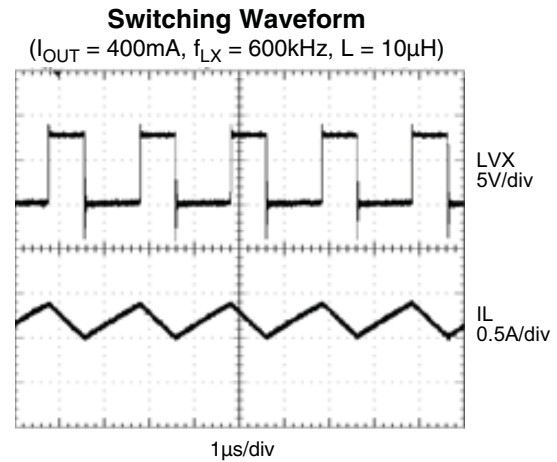
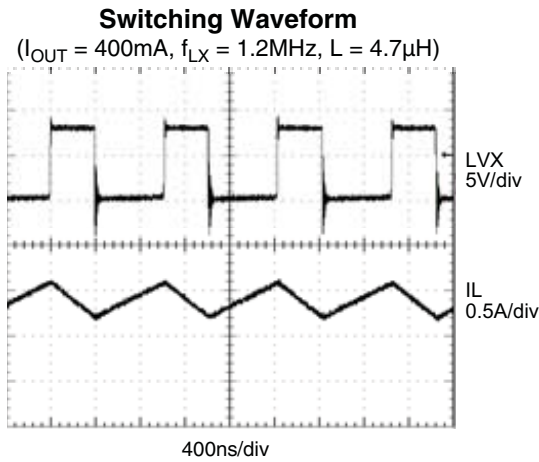
| Symbol                 | Parameter                        | Conditions  | Min.  | Typ.               | Max.  | Units                    |
|------------------------|----------------------------------|---|-------|--------------------|-------|--------------------------|
| $V_{IN}$               | IN Supply Voltage Range          |   | 2.7   |                    | 5.5   | V                        |
| $V_{IN-UVLO}$          | IN UVLO Threshold                | IN rising   |       |                    | 2.6   | V                        |
|                        | IN UVLO Hysteresis               |   |       | 200                |       | mV                       |
| $I_{IN-ON}$            | IN Quiescent Current             | EN = IN, FB = 1.4V  |       |                    | 1.2   | mA                       |
| $I_{IN-OFF}$           | IN Shutdowns Current             | EN = GND  |       |                    | 1     | $\mu\text{A}$            |
| $V_{FB}$               | FB Voltage                       |   | 1.143 | 1.17               | 1.197 | V                        |
|                        | FB Input Bias Current            | $V_{IN} = 2.7\text{V}$  |       |                    | 1     | $\mu\text{A}$            |
|                        | FB Line Regulation               | $2.7\text{V} < V_{IN} < 5.5\text{V}$  |       | 0.15               |       | % / V                    |
|                        | FB Load Regulation               | Varies load so the input DC current changes from 0.2A to 1.8A, $V_{OUT} = 16\text{V}$ |       | 1.5                |       | %                        |
| $I_{SS}$               | Soft-Start Charge Current        |   | 7     | 10                 | 13    | $\mu\text{A}$            |
| <b>ERROR AMPLIFIER</b> |                                  |   |       |                    |       |                          |
| $g_m$                  | Error Amplifier Transconductance |   |       | 200                |       | $\mu\text{A} / \text{V}$ |
| $A_V$                  | Error Amplifier Voltage Gain     |   |       | 340                |       | V / V                    |
| <b>OSCILLATOR</b>      |                                  |   |       |                    |       |                          |
| $f_{SW}$               | Switching Frequency              | FSEL = IN   | 960   | 1200               | 1440  | kHz                      |
|                        |                                  | FSEL = GND  | 480   | 600                | 720   |                          |
| $D_{MAX}^{(1)}$        | Maximum Duty Cycle               | FSEL = IN, FB = 0V  |       | 87                 |       | %                        |
|                        |                                  | FSEL = GND, FB = 0V   |       | 90                 |       |                          |
| <b>POWER SWITCH</b>    |                                  |   |       |                    |       |                          |
| $R_{ON-LX}$            | LX On Resistance                 |   |       | 0.20               | 0.25  | $\Omega$                 |
|                        | LX Leakage Current               | LX = 22V, EN = GND  |       |                    | 2     | $\mu\text{A}$            |
| <b>DIODE</b>           |                                  |   |       |                    |       |                          |
| $I_{leak}$             | Diode Leakage                    | OUT = 22V, LX = 0V  |       |                    | 10    | $\mu\text{A}$            |
|                        | Diode forward voltage            | $I_d = 100\text{mA}$  |       | 0.3                |       | V                        |
| <b>PROTECTIONS</b>     |                                  |   |       |                    |       |                          |
| $I_{LIM}$              | Current Limit                    |   | 1.5   | 2.2                | 2.9   | A                        |
| $T_{SD}$               | Thermal Shutdown Threshold       |   |       | 145                |       | $^\circ\text{C}$         |
|                        | Thermal Shutdown Hysteresis      |   |       | 35                 |       | $^\circ\text{C}$         |
| <b>LOGIC INPUTS</b>    |                                  |   |       |                    |       |                          |
|                        | EN Logic High Threshold          |   | 1.5   |                    |       | V                        |
|                        | EN Logic Low Threshold           |   |       |                    | 0.4   | V                        |
|                        | FSEL High                        |   |       | 0.9V <sub>in</sub> |       |                          |
|                        | FSEL Low                         |   |       | 0.1V <sub>in</sub> |       |                          |
|                        | EN, FSEL Input Current           |   |       |                    | 0.1   | $\mu\text{A}$            |

### Notes:

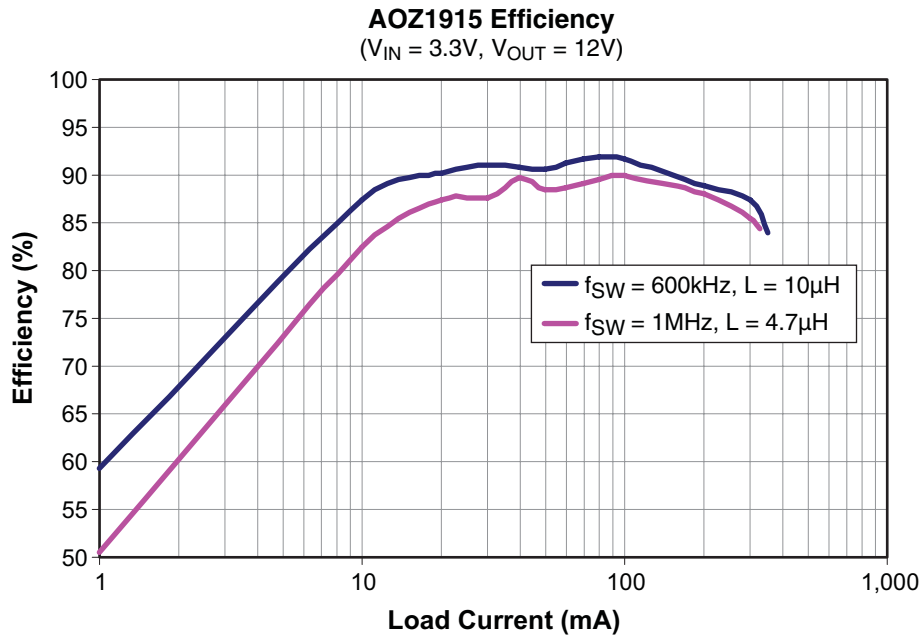
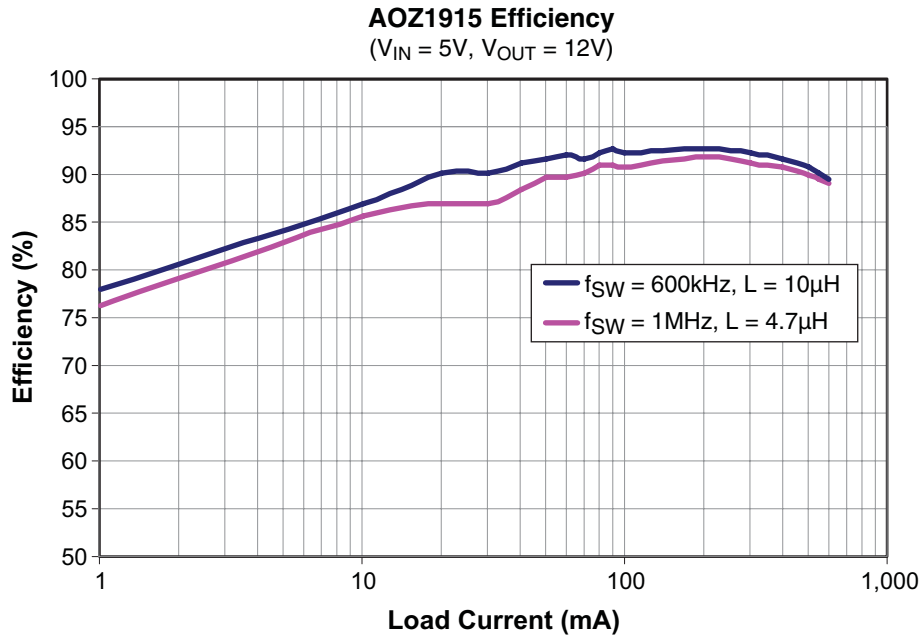
1. Guaranteed by design.

## Typical Performance Characteristics

Circuit of Figure 1.  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 3.3\text{V}$ ,  $V_{EN} = 2\text{V}$ ,  $V_{OUT} = 8\text{V}$  unless otherwise specified.



Efficiency



## Detailed Description

The AOZ1915 is a current-mode step up regulator (Boost Converter) with integrated NMOS switch. It operates from a 2.7V to 5.5V input voltage range and supplies up to 22V output voltage. The duty cycle can be adjusted to obtain a wide range of output voltage up to 22V. Features include enable control, cycle by cycle current limit, input under voltage lockout, adjustable soft-start and thermal shut down.

The AOZ1915 is available in DFN 4x3 package

### Enable and Soft Start

The AOZ1915 has the adjustable soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 2.7V and voltage on EN pin is HIGH. In soft start process, a 10μA internal current source charges the external capacitor at SS. As the SS capacitor is charged, the voltage at SS rises. The SS voltage clamps the reference voltage of the error amplifier, therefore output voltage rising time follows the SS pin voltage. With the slow ramping up output voltage, the inrush current can be prevented.

The EN pin of the AOZ1915 is active high. Connect the EN pin to VIN if enable function is not used. Pull it to ground will disable the AOZ1915. Do not leave it open. The voltage on EN pin must be above 1.5 V to enable the AOZ1915. When voltage on EN pin falls below 0.4V, the AOZ1915 is disabled. If an application circuit requires the AOZ1915 to be disabled, an open drain or open collector circuit should be used to interface to EN pin.

### Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency.

The AOZ1915 integrates an internal N-MOSFET as the control switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the control power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal NMOS switch is on. The inductor current ramps up. When the current signal exceeds the error voltage, the switch is off. The inductor current is freewheeling through the internal Schottky diode to output.

### Switching Frequency

The AOZ1915 switching frequency is fixed and set by an internal oscillator and FSEL. When the voltage of FSEL is high (connected to Vin) The switching frequency is 1.2MHz; when the voltage of FSEL is low (connected to GND), the switching frequency is 600 KHz.

### Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin with a resistor divider network. In the application circuit shown in Figure 1. The resistor divider network includes R<sub>1</sub> and R<sub>2</sub>. Usually, a design is started by picking a fixed R<sub>1</sub> value and calculating the required R<sub>2</sub> with equation below:

$$V_O = 1.2 \times \left( 1 + \frac{R_2}{R_1} \right)$$

Some standard value of R<sub>1</sub>, R<sub>2</sub> for most commonly used output voltage values are listed in Table 1.

**Table 1.**

| V <sub>O</sub> (V) | R <sub>2</sub> (kΩ) | R <sub>1</sub> (kΩ) |
|--------------------|---------------------|---------------------|
| 8                  | 170                 | 30                  |
| 12                 | 270                 | 30                  |
| 16                 | 370                 | 30                  |
| 18                 | 420                 | 30                  |
| 25                 | 595                 | 30                  |

The combination of R<sub>1</sub> and R<sub>2</sub> should be large enough to avoid drawing excessive current from the output, which will cause power loss.

### Protection Features

The AOZ1915 has multiple protection features to prevent system circuit damage under abnormal conditions.

#### Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1915 employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The peak inductor current is automatically limited cycle by cycle.

When the current of control NMOS reaches the current limit threshold, the cycle by cycle current limit circuit turns off the NMOS immediately to terminate the current duty cycle. The inductor current stop rising. The cycle by cycle current limit protection directly limits inductor peak current. The average inductor current is also limited due

to the limitation on peak inductor current. When cycle by cycle current limit circuit is triggered, the output voltage drops as the duty cycle decreasing.

### Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 2.7V, the converter starts operation. When input voltage falls below 2.2V, the converter will stop switching.

### Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and NMOS switch if the junction temperature exceeds 145°C.

## Application Information

The basic AOZ1915 application circuit is shown in Figure 1. Component selection is explained below.

### Input Capacitor

The input capacitor ( $C_1$  in Figure 1) must be connected to the  $V_{IN}$  pin and GND pin of the AOZ1915 to maintain steady input voltage. The voltage rating of input capacitor must be greater than maximum input voltage + ripple voltage. The RMS current rating should be greater than the the inductor ripple current:

$$\Delta I_L = \frac{V_{IN}}{f \times L} \times \left( 1 - \frac{V_{IN}}{V_O} \right)$$

The input capacitor value should be greater than 4.7 $\mu$ F for normal operation. The capacitor can be electrolytic, tantalum or ceramic. The input capacitor should be place as close as possible to the IC; if not possible, please put 0.1 $\mu$ F decoupling ceramics capacitor between IN pin and GND nearby.

### Inductor

The inductor is used to supply higher output voltage when the NMOS switch is off. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_{IN}}{f \times L} \times \left( 1 - \frac{V_{IN}}{V_O} \right)$$

The peak inductor current is:

$$I_{Lpeak} = I_{IN} + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor, switch and freewheeling diode, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of input current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a boost circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

### Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a boost converter circuit, output ripple voltage is determined by load current, input voltage, output voltage, switching frequency, output capacitor value and ESR. It can be calculated by the equation below::

$$\Delta V_O = I_{LOAD} \times \left( \frac{V_O}{V_{IN}} \times ESR_{CO} + \frac{\left( 1 - \frac{V_{IN}}{V_{OUT}} \right)}{f \times C_O} \right)$$

where;

$I_{LOAD}$  is the load current,

$C_O$  is the output capacitor value, and

$ESR_{CO}$  is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and load current with the fixed

frequency, input and output voltage. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = I_L \times \frac{\left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{f \times C_O}$$

Output capacitor with the range of 4.7µF to 22µF ceramic capacitor usually can meet most applications.

### Loop Compensation

The AOZ1915 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the boost power stage can be simplified to be a one-pole, one left plane zero and one right half plane (RHP) system in frequency domain. The pole is dominant pole and can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

$C_O$  is the output filter capacitor,

$R_L$  is load resistor value, and

$ESR_{CO}$  is the equivalent series resistance of output capacitor.

The RHP zero has the effect of a zero in the gain causing an imposed +20dB/decade on the roll off, but has the effect of a pole in the phase, subtracting 90° in the phase. The RHP zero can be calculated by

The RHP zero obviously can cause the instable issue if the bandwidth is higher. It is recommended to design the bandwidth to lower than the one half frequency of RHP zero.

The compensation design is actually to shape the converter close loop transfer function to get desired gain

and phase. Several different types of compensation network can be used for AOZ1915. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1915, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

$G_{EA}$  is the error amplifier transconductance, which is  $200 \times 10^{-6}$  A/V,

$G_{VEA}$  is the error amplifier voltage gain, which is 340 V/V, and  $C_C$  is compensation capacitor.

The zero given by the external compensation network, capacitor  $C_C$  ( $C_3$  in Figure 1) and resistor  $R_C$  ( $R_3$  in Figure 1), is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

Choosing the suitable  $C_C$  and  $R_C$  by trading-off stability and bandwidth.

### Thermal Management and Layout Consideration

In the AOZ1915 boost regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the filter inductor, to the LX pin, to the internal NMOS switch, to the ground and back to the input capacitor, when the switch turns on. The second loop starts from input capacitor, to the filter inductor, to the LX pin to the internal diode, to the ground and back to the input capacitor, when the switch is off.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is recommended to connect input capacitor, output capacitor, and GND pin of the AOZ1915.

In the AOZ1915 boost regulator circuit, the three major power dissipating components are the AOZ1915 and output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by input current and DCR of inductor.

$$P_{inductor\_loss} = I_{IN}^2 \times R_{inductor} \times 1.1$$

The actual AOZ1915 junction temperature can be calculated with power dissipation in the AOZ1915 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss} - P_{diode\_loss}) \times \Theta + T_{ambient}$$

The maximum junction temperature of AOZ1915 is 145°C, which limits the maximum load current capability.

The thermal performance of the AOZ1915 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electric and thermal performance.

1. Do not use thermal relief connection to the  $V_{IN}$  and the GND pin. Pour a maximized copper area to the GND pin and the  $V_{IN}$  pin to help thermal dissipation.
2. A ground plane is preferred.
3. Make the current trace from LX pins to L to Co to the GND as short as possible.
4. Pour copper plane on all unused board area and connect it to stable DC nodes, like  $V_{IN}$ , GND or  $V_{OUT}$ .
5. Keep sensitive signal trace such as trace connected with FB pin and COMP pin far away from the LX pin.
6. The output schottky diode is integrated into AOZ1915. Proper layout should incorporate thermal via connection from top to bottom layers.

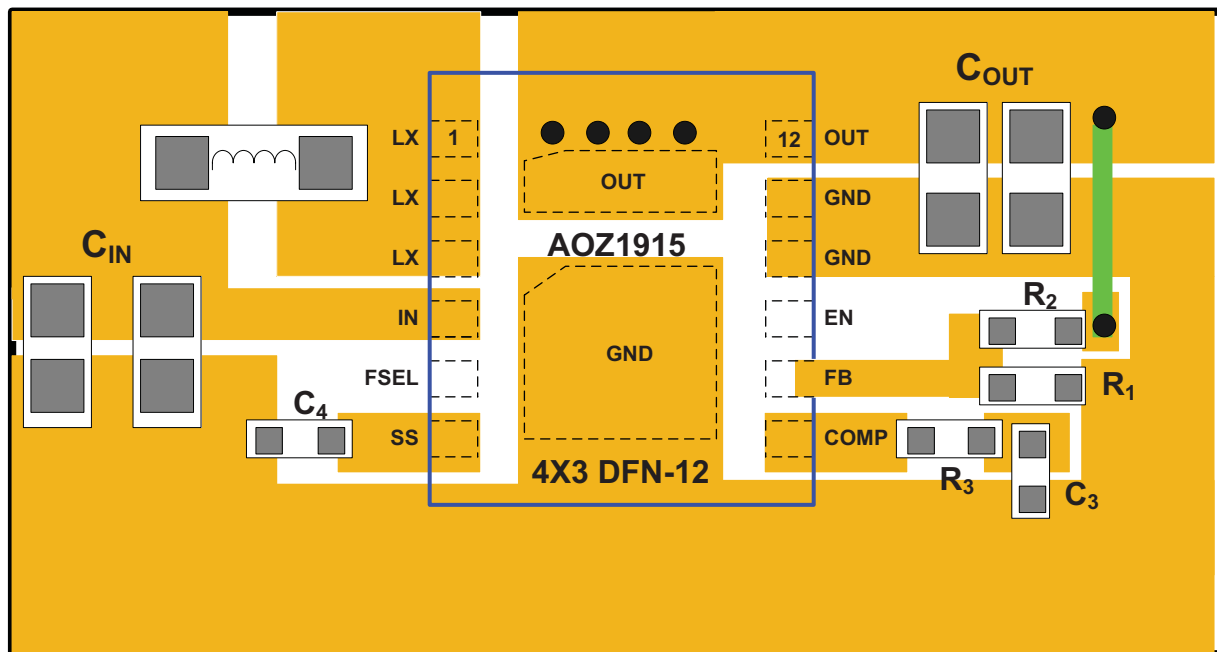
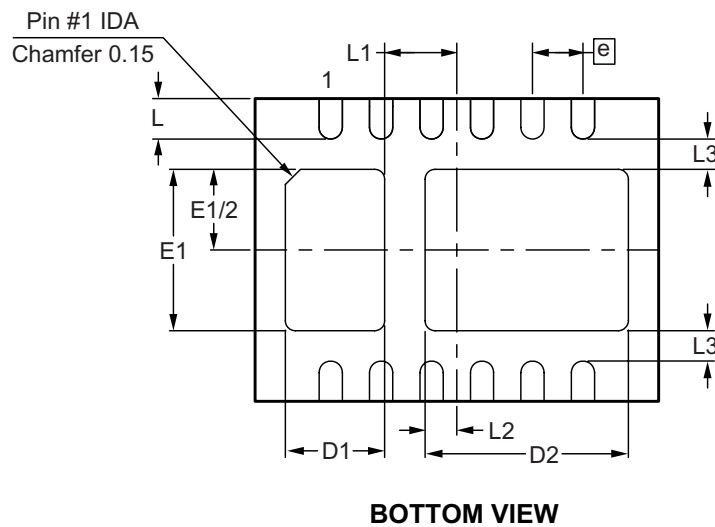
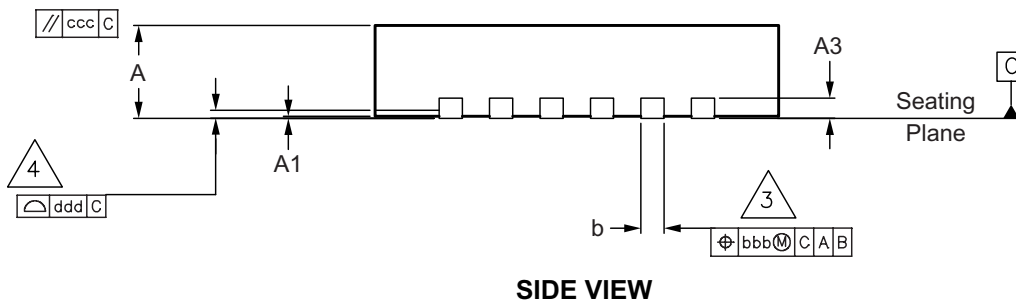
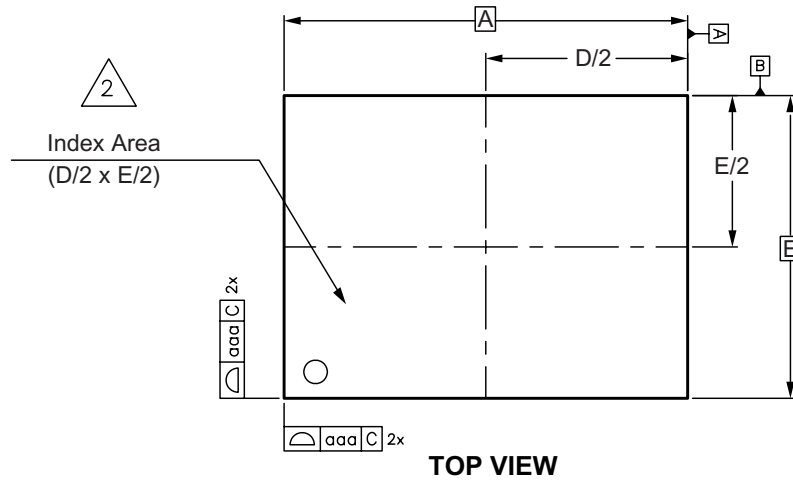


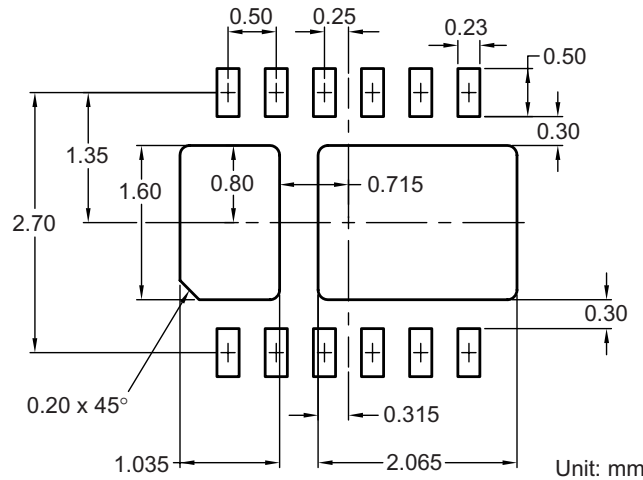
Figure 3 . AOZ1915 PCB Layout Example

Package Dimensions, DFN 4 x 3



Package Dimensions, DFN 4 x 3 (Continued)

RECOMMENDED LAND PATTERN



Dimensions in millimeters

| Symbols | Min.      | Nom.  | Max. |
|---------|-----------|-------|------|
| A       | 0.80      | 0.90  | 1.00 |
| A1      | 0.00      | 0.02  | 0.05 |
| A3      | 0.20 REF. |       |      |
| b       | 0.20      | 0.23  | 0.35 |
| D       | 4.00 BSC  |       |      |
| D1      | 0.83      | 0.985 | 1.09 |
| D2      | 1.86      | 2.015 | 2.12 |
| E       | 3.00 BSC  |       |      |
| E1      | 1.45      | 1.60  | 1.70 |
| ⓐ       | 0.50 BSC  |       |      |
| L       | 0.30      | 0.40  | 0.50 |
| L1      | 0.61      | 0.715 | 0.82 |
| L2      | 0.21      | 0.315 | 0.42 |
| L3      | 0.30 REF. |       |      |
| aaa     | 0.15      |       |      |
| bbb     | 0.10      |       |      |
| ccc     | 0.10      |       |      |
| ddd     | 0.08      |       |      |

Dimensions in inches

| Symbols | Min.       | Nom.  | Max.  |
|---------|------------|-------|-------|
| A       | 0.031      | 0.035 | 0.039 |
| A1      | 0.000      | 0.001 | 0.002 |
| A3      | 0.008 REF. |       |       |
| b       | 0.008      | 0.009 | 0.014 |
| D       | 0.157 BSC  |       |       |
| D1      | 0.033      | 0.039 | 0.043 |
| D2      | 0.073      | 0.079 | 0.083 |
| E       | 0.118 BSC  |       |       |
| E1      | 0.057      | 0.063 | 0.067 |
| ⓐ       | 0.020 BSC  |       |       |
| L       | 0.012      | 0.016 | 0.020 |
| L1      | 0.024      | 0.028 | 0.032 |
| L2      | 0.008      | 0.012 | 0.017 |
| L3      | 0.012 REF. |       |       |
| aaa     | 0.006      |       |       |
| bbb     | 0.004      |       |       |
| ccc     | 0.004      |       |       |
| ddd     | 0.003      |       |       |

Notes:

1. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

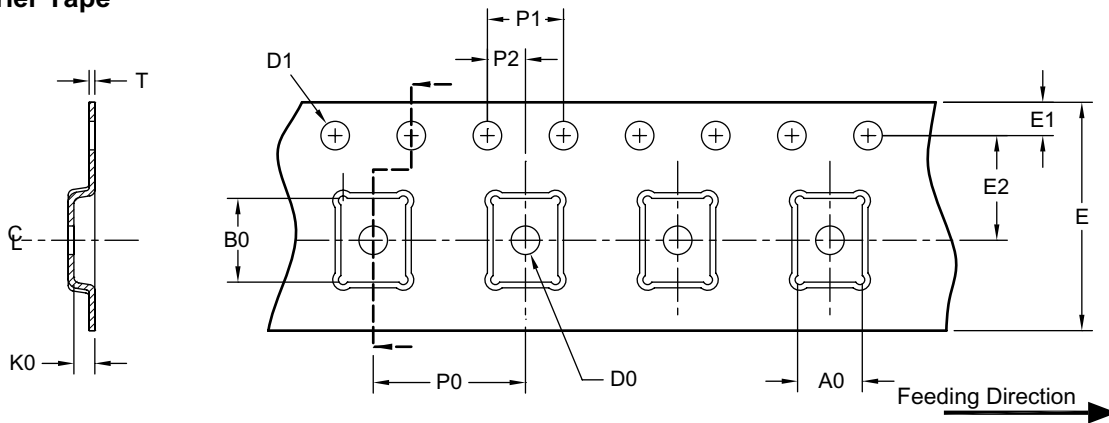
2. The location of the terminal #1 identifier and terminal numbering conforms to JEDEC publication 95 SPP-002.

3. Dimension b applied to metallized terminal and is measured between 0.20mm and 0.35mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, dimension b should not be measured in that radius area.

4. Coplanarity ddd applies to the terminals and all other bottom surface metallization.

## Tape and Reel Dimensions, DFN 4 x 3

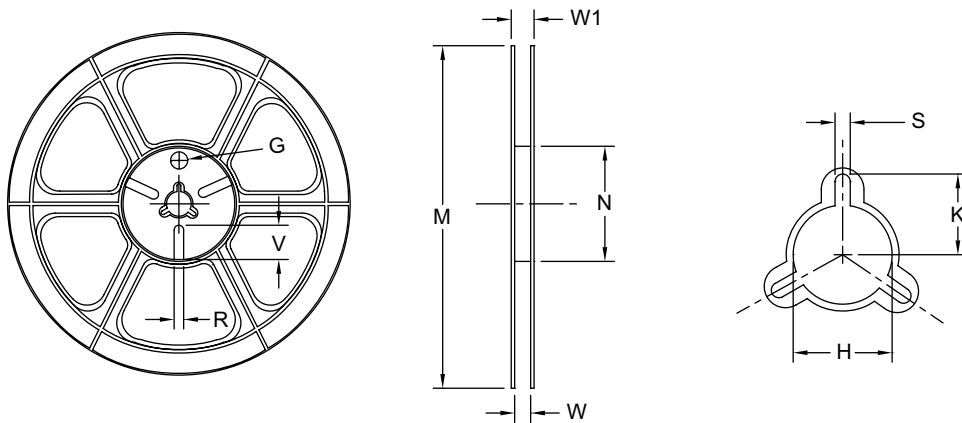
### Carrier Tape



UNIT: mm

| Package              | A0            | B0            | K0            | D0           | D1                 | E            | E1            | E2            | P0            | P1            | P2            | T             |
|----------------------|---------------|---------------|---------------|--------------|--------------------|--------------|---------------|---------------|---------------|---------------|---------------|---------------|
| DFN 4 x 3<br>(12 mm) | 3.40<br>±0.10 | 4.40<br>±0.10 | 1.10<br>±0.10 | 1.50<br>Min. | 1.50<br>+0.10/-0.0 | 12.0<br>±0.3 | 1.75<br>±0.10 | 5.50<br>±0.05 | 8.00<br>±0.10 | 4.00<br>±0.10 | 2.00<br>±0.10 | 0.30<br>±0.05 |

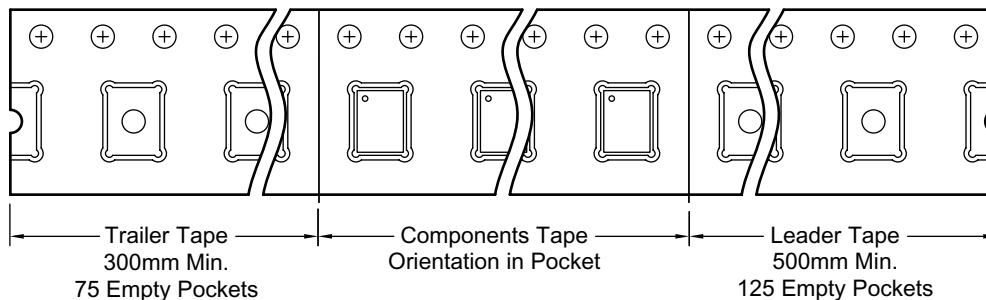
### Reel



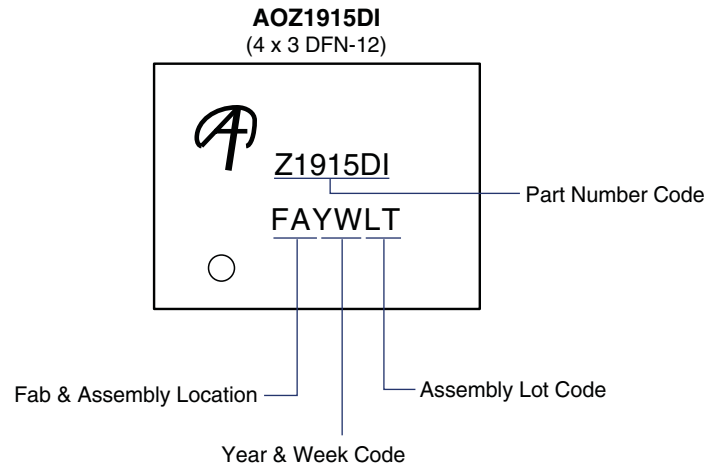
UNIT: mm

| Tape Size | Reel Size | M              | N             | W               | W1              | H             | K            | S           | G | R | V |
|-----------|-----------|----------------|---------------|-----------------|-----------------|---------------|--------------|-------------|---|---|---|
| 12mm      | ø330      | ø330.0<br>±2.0 | ø79.0<br>±1.0 | 12.4<br>+2.0/-0 | 17.0<br>+2.6/-0 | ø13.0<br>±0.5 | 10.5<br>±0.2 | 2.0<br>±0.5 | — | — | — |

### Leader / Trailer & Orientation



## Package Marking



**Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.**

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