



**THE DATASHEET OF
MP20042DG-JG-LF-Z**



DESCRIPTION

The MP20042 is a dual-channel, micropower, low noise, low dropout and high PSRR linear regulator. The output voltage of MP20042 ranges from 1.2V to 5.0V and 1% accuracy by operating from a +2.5V to +6.0V input. The MP20042 can supply up to 200mA of load current at each channel.

The MP20042 uses an internal PMOS as the pass element, which consumes 114µA supply current (both LDOs on) at no load condition. The EN1 and EN2 pins control each output respectively. When both channels shutdown simultaneously, the chip will be turned off and consume nearly zero operation current which is suitable for battery-power devices. The MP20042 features current limiting and over temperature protection.

It is available in a 2mm x 2mm QFN8 package.

FEATURES

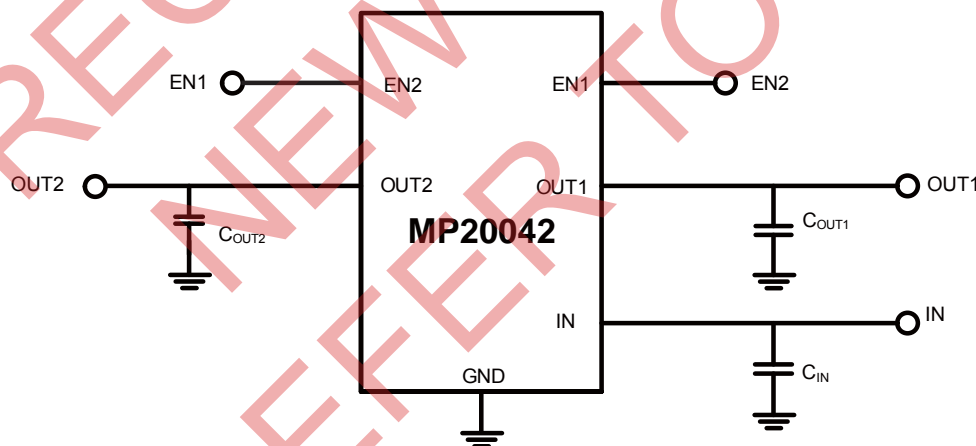
- Two LDOs in a 2mmx2mm QFN8 Package
- Up to 200mA Output Current (Per Channel)
- Dual Enable Pins Control Each Output
- 72dB PSRR at 1kHz
- 11µV_{RMS} Low Noise Output
- 110mV Dropout at 100mA Load
- Very Fast Transient Responses with Small Output Capacitor
- Current Limiting and Thermal Protection

APPLICATIONS

- Cellular Phones
- Battery-powered Equipment
- Laptop, Notebook, and Palmtop Computers
- Hand-held Equipment
- Wireless LAN

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TYPICAL APPLICATION



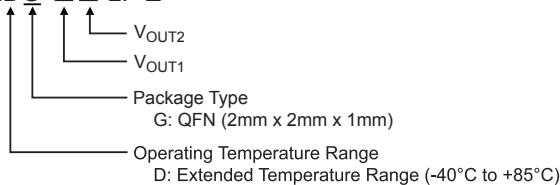
ORDERING INFORMATION*

Part Number	V _{OUT1}	V _{OUT2}	Package	Temperature	Top Marking
MP20042DG-JG-LF-Z	2.5V	1.8V	QFN8 (2mmx2mm)	-40°C to +85°C	7E
MP20042DG-ZS-LF-Z	5.0V	3.3V			7L
MP20042DG-PN-LF-Z	3.0V	2.85V			8L
MP20042DG-DD-LF-Z	1.85V	1.85V			9L
MP20042DG-SJ-LF-Z	3.3V	2.5V			2M
MP20042DG-MG-LF-Z	2.8V	1.8V			3M

* Other output voltage versions between 1.2V and 5.0V are available in 100mV increments. Contact factory for availability.

ORDERING GUIDE**

MP20042DG-□□-LF-Z

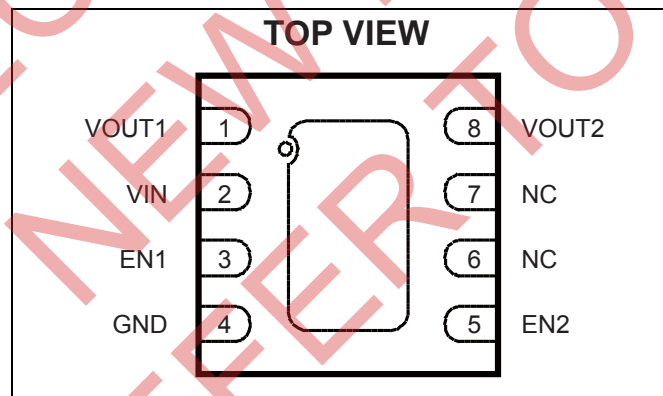


** For RoHS Compliant Packaging, add suffix - LF (e.g. MP20042DG-□□-LF); For Tape and Reel, add suffix -Z (e.g. MP20042DG-□□-LF-Z)

OUTPUT VOLTAGE SELECTOR GUIDE***

Code	V _{OUT}	Code	V _{OUT}
C	1.2	T	2.65
B	1.3	L	2.7
F	1.5	M	2.8
W	1.6	N	2.85
G	1.8	V	2.9
D	1.85	P	3.0
Y	1.9	Q	3.1
H	2.0	X	3.15
E	2.1	R	3.2
J	2.5	S	3.3
K	2.6	Z	5.0

*** Code in **Bold** are standard versions. For other output voltages between 1.2V and 5.0V contact factory for availability. Minimum order quantity on non-standard versions is 25,000 units.

PACKAGE REFERENCE


ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Input Voltage	6.5V
Continuous Power Dissipation (T _A = +25°C) ⁽²⁾	1.25W
Operation Temperature Range ...	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10sec)	260°C

Recommended Operating Conditions ⁽³⁾

Supply Input Voltage.....	2.5V to 6.0V
Enable Input Voltage	0V to 6.0V
Junction Temperature Range .	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
2x2 QFN8	80	16... °C/W

Notes:

- 1) Exceeding these ratings may cause permanent damage to the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside its operating conditions.
- 4) Measured on JESD51-7 4-layer board.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP20041

ELECTRICAL CHARACTERISTICS

$V_{IN}=3.6V$, $V_{OUT1}=2.5V$, $V_{OUT2}=1.8V$, $C_{IN}=C_{OUT1}=C_{OUT2}=2.2\mu F$, $EN1=EN2=V_{IN}$, Typical Value at $T_A=25^\circ C$ for each LDO unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Voltage Accuracy (Load regulation) ⁽⁵⁾	ΔV_{OUT}	$I_{LOAD} = 1mA$ to 200mA	-1		+1	%
Maximum Output Current	I_{MAX}	Continuous	200			mA
Current Limit	I_{LIM}	$R_{Load}=1\Omega$		450		mA
Quiescent Current	I_G	No Load		114		μA
Dropout Voltage ⁽⁶⁾	V_{DROP}	$I_{OUT} = 100mA$		110		mV
		$I_{OUT} = 200mA$		250		mV
Line Regulation ⁽⁷⁾	ΔV_{LINE}	$V_{IN}=(V_{OUT}+0.4V$ or $2.5V)$ to 6V, $I_{OUT}=1mA$	-0.05		+0.05	%/V
EN Input High Threshold	V_{IH}	$V_{IN} = 2.5V$ to 6.0V	1.6			V
EN Input Low Threshold	V_{IL}	$V_{IN} = 2.5V$ to 6.0V			0.45	V
EN Input Bias Current	I_{SD}	$EN = V_{IN}=6.5V$			300	nA
Shutdown Supply Current	I_{GSD}	$EN1 = EN2 = GND$		0.03	1	μA
Thermal Shutdown Temperature	T_{SD}			140		$^\circ C$
Thermal Shutdown Hysteresis	ΔT_{SD}			10		$^\circ C$
Output Voltage Noise		10Hz to 100kHz, $C_{OUT}=4.7\mu F$, $I_{LOAD}=1mA$		11		μV_{RMS}
Output Voltage AC PSRR		100Hz, $C_{OUT} = 2.2\mu F$, $I_{LOAD} = 100mA$		72		dB
		1kHz, $C_{OUT} = 2.2\mu F$, $I_{LOAD} = 100mA$		72		dB
		100kHz, $C_{OUT} = 2.2\mu F$, $I_{LOAD} = 100mA$		47		dB

Notes:

$$5) \text{ Load Regulation} = \frac{V_{OUT}[I_{OUT(MAX)}] - V_{OUT}[I_{OUT(MIN)}]}{V_{OUT(NOM)}} \times (\%)$$

6) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

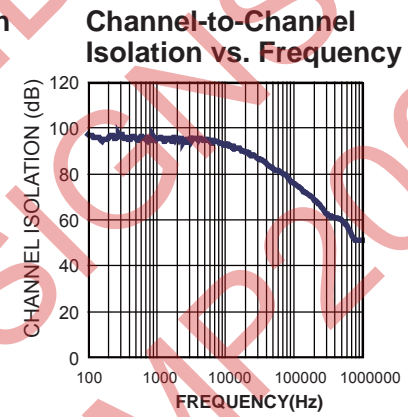
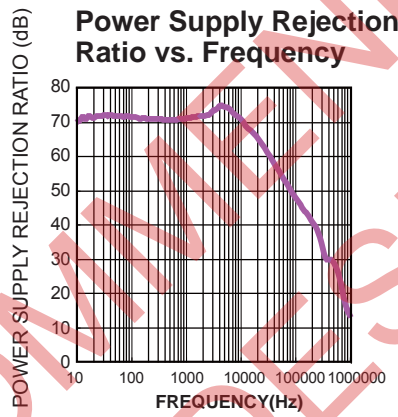
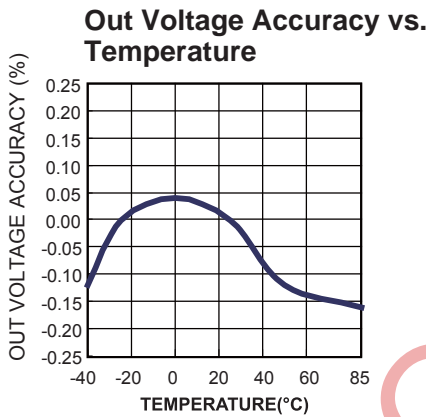
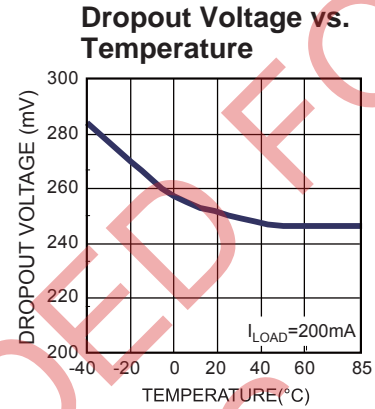
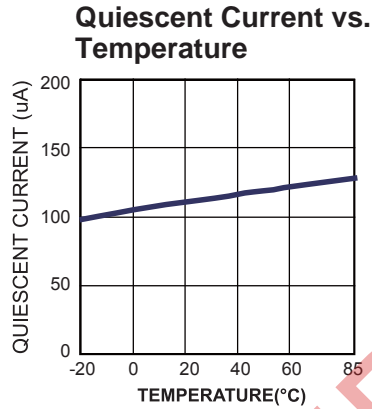
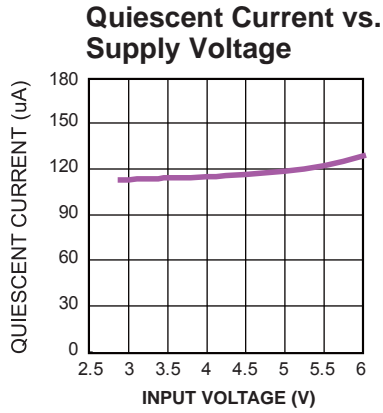
$$7) \text{ Line Regulation} = \frac{V_{OUT}[V_{IN(MAX)}] - V_{OUT}[V_{IN(MIN)}]}{[V_{IN(MAX)} - V_{IN(MIN)}] \times V_{OUT(NOM)}} \times (\% / V)$$

PIN FUNCTIONS

Pin #	Name	Description
1	VOUT1	Channel 1 Output Voltage
2	VIN	Supply Input Pin
3	EN1	Channel 1 Enable (Active High). Do Not Float This Pin.
4	GND	Common Ground
5	EN2	Channel 2 Enable (Active High). Do Not Float This Pin.
6, 7	NC	
8	VOUT2	Channel 2 Output Voltage

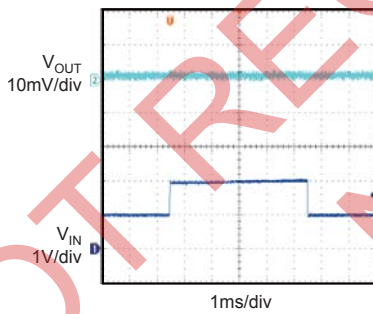
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=3.6V$, $V_{OUT1}=2.5V$, $V_{OUT2}=1.8V$, $C_{IN}=C_{OUT1}=C_{OUT2}=2.2\mu F$, $EN1=EN2=V_{IN}$, Typical Value at $T_A = 25^\circ C$ for Both Channel Enabled.



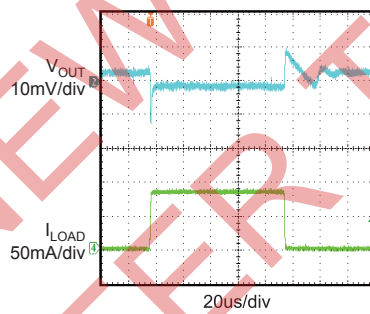
Line Transient Response

$V_{OUT}=3.5V$ to $4.5V$, $C_{IN}=0\mu F$, $C_{OUT}=2.2\mu F$
No Load



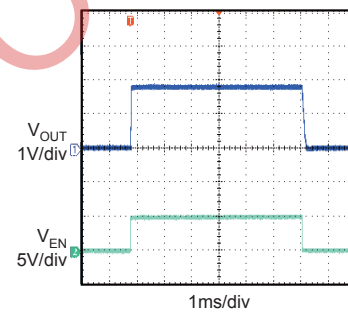
Load Transient Response

$V_{IN}=3.6V$, $V_{OUT}=1.8V$
 $I_{LOAD}=0$ to $80mA$, with Resistor Load



EN Pin Shut Down Response

$V_{IN}=3.6V$, $V_{OUT}=1.8V$, $V_{EN}=0$ to $5V$
 $I_{LOAD}=50mA$, with Resistor Load



APPLICATION INFORMATION

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature difference between the junction and ambient air, and the rate of airflow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where $(T_{Junction} - T_{Ambient})$ is the temperature difference between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connect the GND pin of MP20042 to ground using a large pad or ground plane helps to channel heat away.

Input Capacitor Selection

Using a capacitor whose value is $>0.47\mu F$ on the MP20042 input and the amount of capacitance can be increased without limit. Larger values will help improve line transient response with the drawback of increased size. Ceramic capacitors are preferred, but tantalum capacitors may also suffice.

Output Capacitor Selection

The MP20042 is designed specifically to work with very low ESR ceramic output capacitor in space-saving and performance consideration. A ceramic capacitor in the range of $0.47\mu F$ and $10\mu F$, and with ESR lower than 1.2Ω is suitable for the MP20042 application circuit. Output capacitor of larger values will help to improve load transient response and reduce noise with the drawback of increased size.

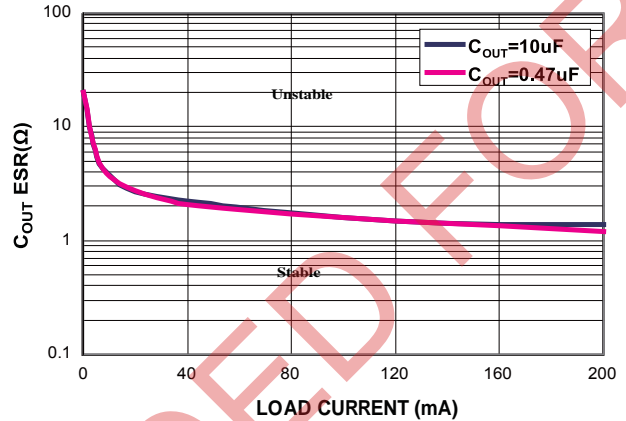


Figure 2—Relationship between ESR and LDO Stability

Reverse Current Path

The PMOS used in the MP20042 has an inherent diode connected between input and output (see Figure 3). If $V_{OUT} - V_{IN}$ is more than a diode-drop, this diode gets forward biased and starts to conduct. To avoid misoperation, an external Schottky connected in parallel with the internal parasitic diode prevents it from being turned on by limiting the voltage drop across it to about 0.3V (see Figure 4).

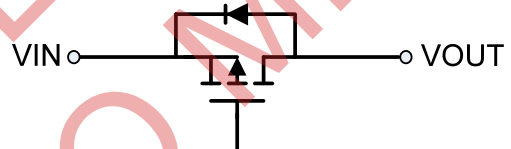


Figure 3—Inherent Diode Connected between Each Regulator Input and Output

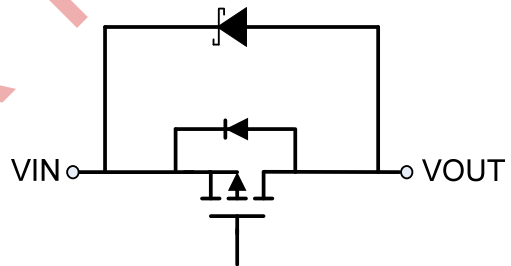
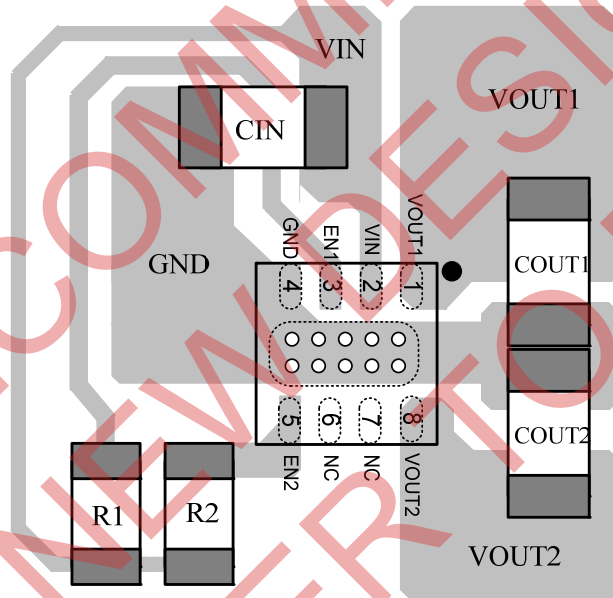
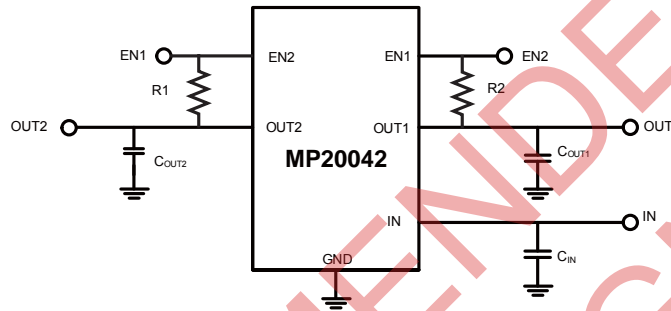


Figure 4—External Schottky Diode Connected in Parallel with the Internal Parasitic Diode

PCB layout guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take figure ? for reference.

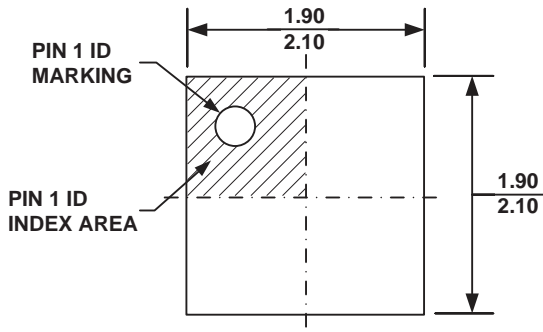
- 1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
- 2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 3) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



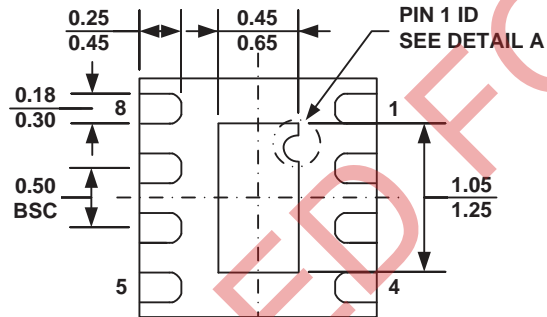
Top Layer
Figure 5—PCB Layout

PACKAGE INFORMATION

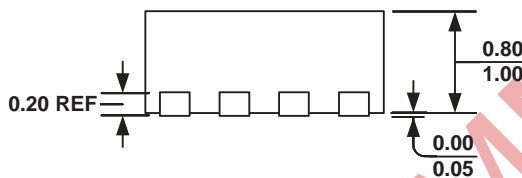
2mm x 2mm QFN8



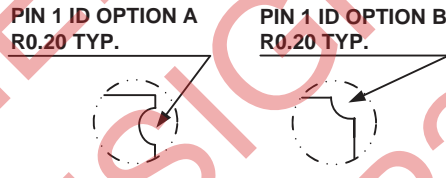
TOP VIEW



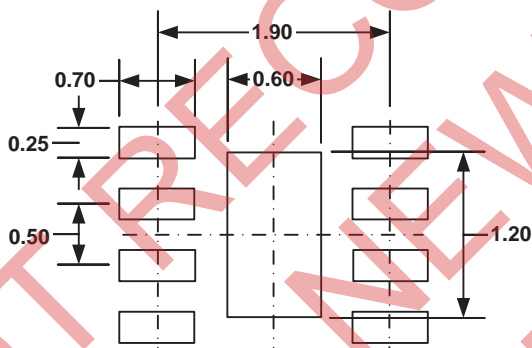
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCCD-3.
- 5) DRAWING IS NOT TO SCALE.

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