



**THE DATASHEET OF
NTMD5836NLR2G**



NTMD5836NL

Power MOSFET

40 V, Dual N-Channel, SOIC-8

Features

- Asymmetrical N Channels
- Low $R_{DS(on)}$
- Low Capacitance
- Optimized Gate Charge
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

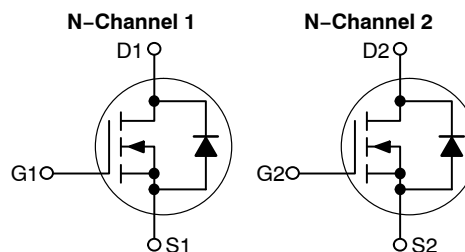
	$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max (Notes 1 and 2)
Channel 1	40 V	12 m Ω @ 10 V	11 A
		16 m Ω @ 4.5 V	
Channel 2	40 V	20 m Ω @ 10 V	6.5 A
		36.5 m Ω @ 4.5 V	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Only selected channel is been powered
1W applied on channel 1: $T_J = 1 W * 85^{\circ}C/W + 25^{\circ}C = 110^{\circ}C$

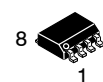


ON Semiconductor®

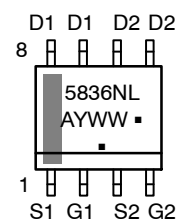
<http://onsemi.com>



MARKING DIAGRAM* AND PIN ASSIGNMENT



SOIC-8
CASE 751



- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMD5836NLR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

NTMD5836NL

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Ch 1	Ch 2	Unit	
Drain-to-Source Voltage		V_{DSS}	40	40	V	
Gate-to-Source Voltage		V_{GS}	± 20	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Notes 3 and 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D	9.0	5.7	A
		$T_A = 70^\circ\text{C}$		7.2	4.6	
Power Dissipation $R_{\theta JA}$ (Notes 3 and 4)		$T_A = 25^\circ\text{C}$	P_D	1.5	1.5	W
		$T_A = 70^\circ\text{C}$		0.9	0.9	
Continuous Drain Current $R_{\theta JA}$ (Notes 3 and 4)	$t \leq 10\text{s}$	$T_A = 25^\circ\text{C}$	I_D	11	6.5	A
		$T_A = 70^\circ\text{C}$		8.6	4.6	
Power Dissipation $R_{\theta JA}$ (Notes 3 and 4)		$T_A = 25^\circ\text{C}$	P_D	2.1	1.9	W
		$T_A = 70^\circ\text{C}$		1.3	1.2	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	43	26	A	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to +150		$^\circ\text{C}$	
Source Current (Body Diode)		I_S	10	7.0	A	
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 40\text{V}$, $V_{GS} = 10\text{V}$, $L = 0.1\text{mH}$)		E_{AS}	76	22	mJ	
		I_{AS}	39	21	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10s)		T_L	260		$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
- Only selected channel is been powered
1W applied on channel 1: $T_J = 1\text{W} * 85^\circ\text{C}/\text{W} + 25^\circ\text{C} = 110^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Ch 1	Ch 2	Unit
Junction-to-Ambient Steady State (Notes 5 and 7)	$R_{\theta JA}$	85	86	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t \leq 10\text{s}$ (Notes 5 and 7)	$R_{\theta JA}$	60	65	
Junction-to-Ambient Steady State (Notes 5 and 8)	$R_{\theta JA}$	59		
Junction-to-Ambient Steady State (Notes 6 and 7)	$R_{\theta JA}$	136	136	

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
- Surface-mounted on FR4 board using 0.155 in sq (100 mm²) pad size
- Only selected channel is been powered
1W applied on channel 1: $T_J = 1\text{W} * 85^\circ\text{C}/\text{W} + 25^\circ\text{C} = 110^\circ\text{C}$
- Both channels receive equivalent power dissipation
1 W applied on each channel: $T_J = 2\text{W} * 59^\circ\text{C}/\text{W} + 25^\circ\text{C} = 143^\circ\text{C}$

NTMD5836NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Ch	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	Ch 1	40			V
			Ch 2				
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$		Ch 1		146		mV/ $^\circ\text{C}$
			Ch 2		25		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$				μA
			Ch 1	1.0			
			Ch 2				
			$T_J = 125^\circ\text{C}$				
Ch 1							
Ch 2							
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch 1			± 100	nA
			Ch 2				

ON CHARACTERISTICS (Note 9)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	Ch 1	1.0	1.8	3.0	V	
			Ch 2	1.0	1.8	3.0		
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$		Ch 1		6.0		mV/ $^\circ\text{C}$	
			Ch 2		6.0			
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch 1		9.5	12	m Ω	
			Ch 2		16.2	20		
			$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch 1		13	16	m Ω
				Ch 2		25.0	36.5	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	Ch 1		10.5		S	
			Ch 2		6.0			

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$	Ch 1		2120		pF
			Ch 2		730		
Output Capacitance	C_{OSS}		Ch 1		315		
			Ch 2		123		
Reverse Transfer Capacitance	C_{RSS}		Ch 1		225		
			Ch 2		84		

9. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

10. Switching characteristics are independent of operating junction temperatures

NTMD5836NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Ch	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE							
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10V, V _{DS} = 20V, I _D = 10A	Ch 1		36	50	nC
		V _{GS} = 10 V, V _{DS} = 20 V, I _D = 7 A	Ch 2		16		
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 4.5 V, V _{DS} = 20 V, CH1: I _D = 10 A, CH2: I _D = 7 A	Ch 1		15	23	V
			Ch 2		8.5	11	
Gate-to-Source Charge	Q _{GS}		Ch 1		2.4		
			Ch 2		1.0		
Gate-to-Drain Charge	Q _{GD}		Ch 1		6.9		
			Ch 2		2.8		
Plateau Voltage	V _{GP}		Ch 1		7.2		
			Ch 2		4.0		
Gate Resistance	R _G	Ch 1		3.2			
		Ch 2		3.3			
Gate Resistance	R _G	Ch 1		1.2		Ω	
		Ch 2		2.1			

SWITCHING CHARACTERISTICS (Note 10)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DD} = 20 V, CH1: I _D = 10 A, CH2: I _D = 7 A, R _G = 2.5 Ω	Ch 1		16		ns
			Ch 2		11.5		
Rise Time	t _r		Ch 1		22		
			Ch 2		14		
Turn-Off Delay Time	t _{d(OFF)}		Ch 1		26		
			Ch 2		15.5		
Fall Time	t _f		Ch 1		8.5		
			Ch 2		3.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, CH1: I _D = 10 A, CH2: I _D = 7 A	T _J = 25°C	Ch 1		0.9	1.2	V
				Ch 2		0.85	1.2	
			T _J = 125°C	Ch 1		0.65		
				Ch 2		0.73		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _{SD} /dt = 100 A/μs, CH1: I _D = 10 A, CH2: I _D = 7 A	Ch 1		27		ns	
Charge Time	T _a		Ch 2		17			
			Ch 1		14			
Ch 2			11					
Discharge Time	T _b		Ch 1		13			
			Ch 2		6.0			
Reverse Recovery Charge	Q _{RR}		Ch 1		19		nC	
			Ch 2		9.0			

9. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

10. Switching characteristics are independent of operating junction temperatures

TYPICAL PERFORMANCE CURVES

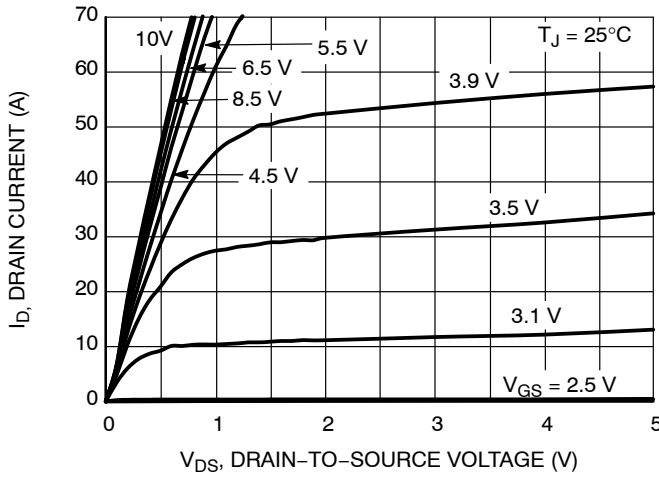


Figure 1. On-Region Characteristics - Channel 1

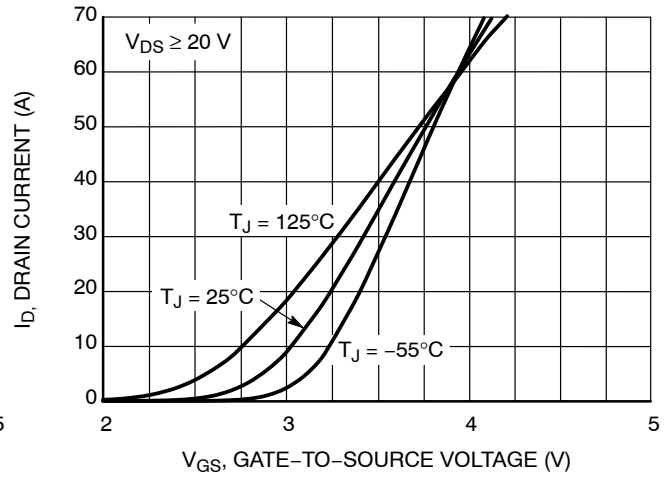


Figure 2. Transfer Characteristics - Channel 1

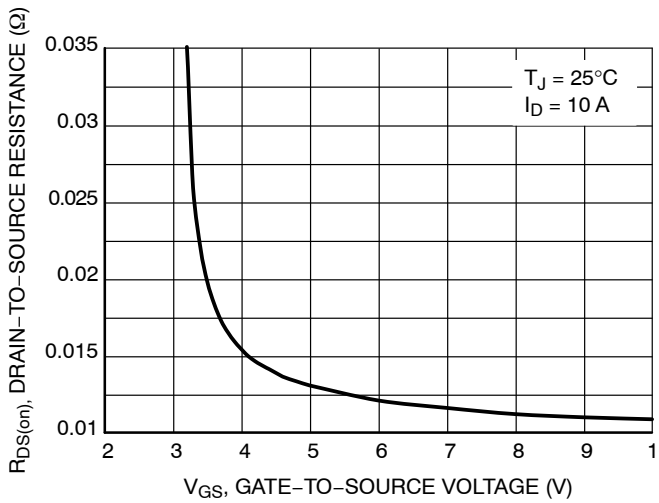


Figure 3. On-Resistance vs. Gate-to-Source Voltage - Channel 1

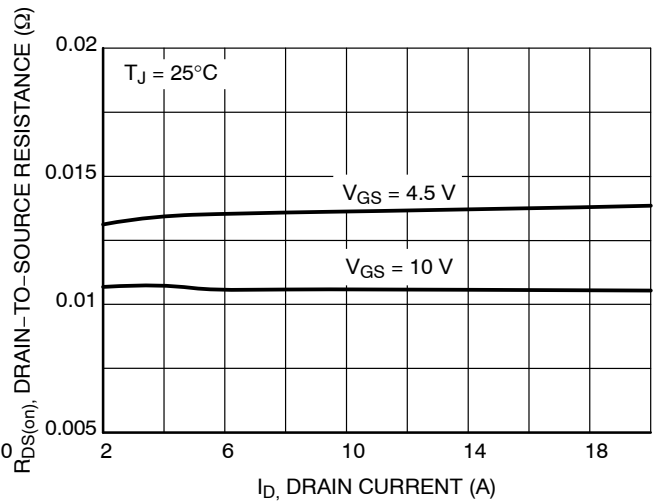


Figure 4. On-Resistance vs. Drain Current and Gate Voltage - Channel 1

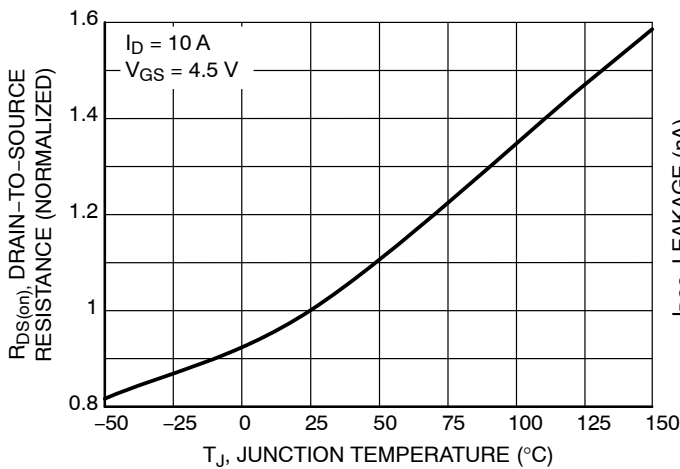


Figure 5. On-Resistance Variation with Temperature - Channel 1

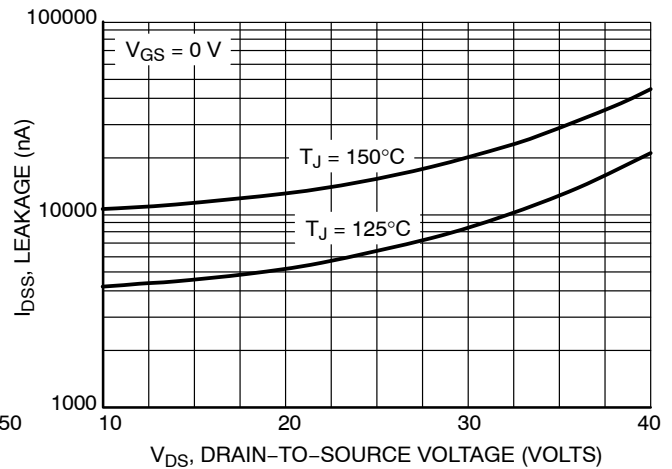


Figure 6. Drain-to-Source Leakage Current vs. Voltage - Channel 1

TYPICAL PERFORMANCE CURVES

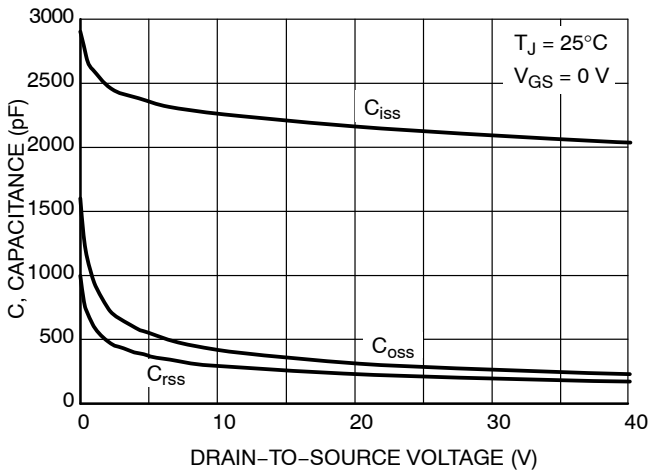


Figure 7. Capacitance Variation - Channel 1

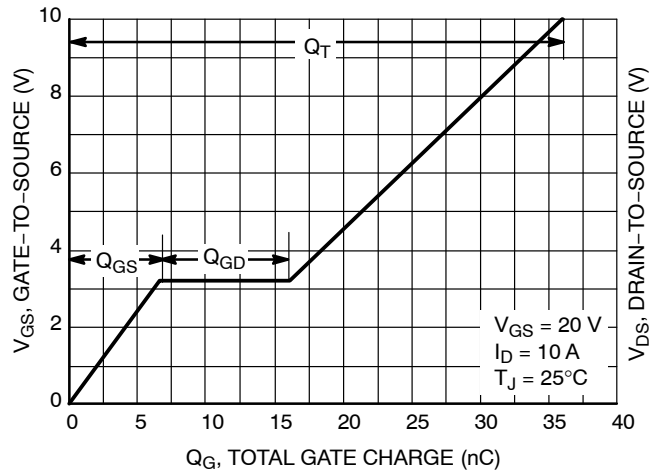


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge - Channel 1

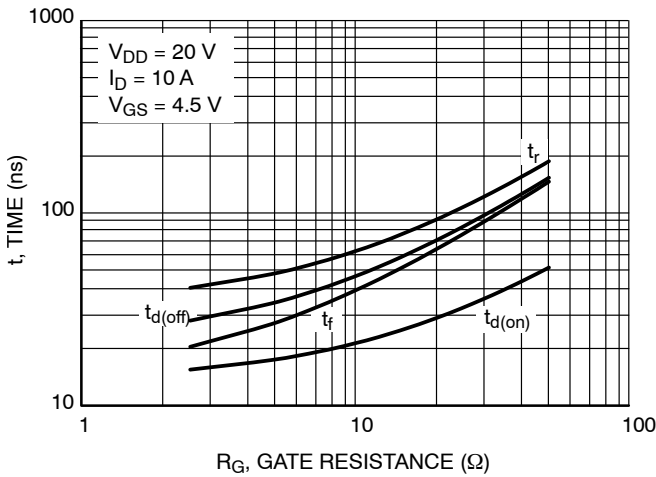


Figure 9. Resistive Switching Time Variation vs. Gate Resistance - Channel 1

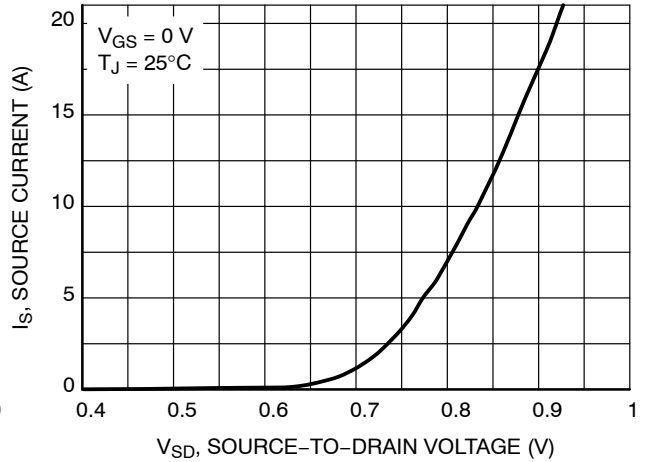


Figure 10. Diode Forward Voltage vs. Current - Channel 1

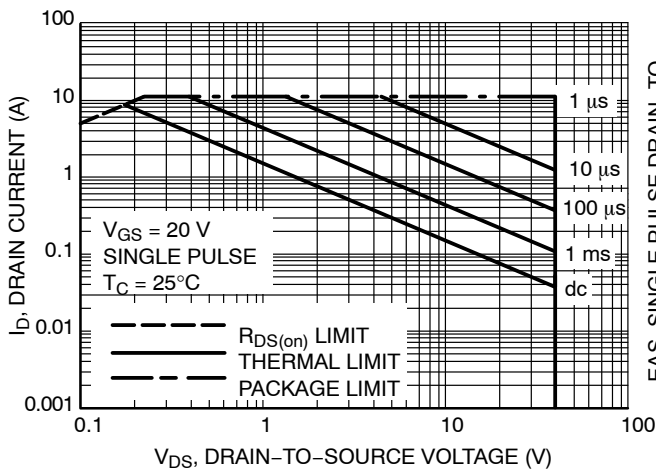


Figure 11. Maximum Rated Forward Biased Safe Operating Area - Channel 1

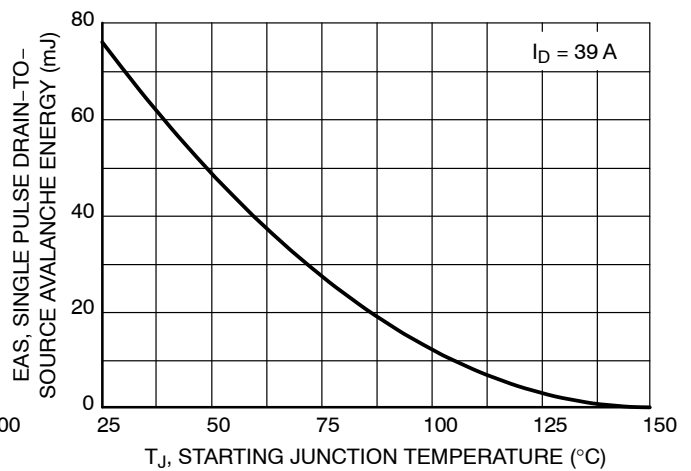


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature - Channel 1

TYPICAL PERFORMANCE CURVES

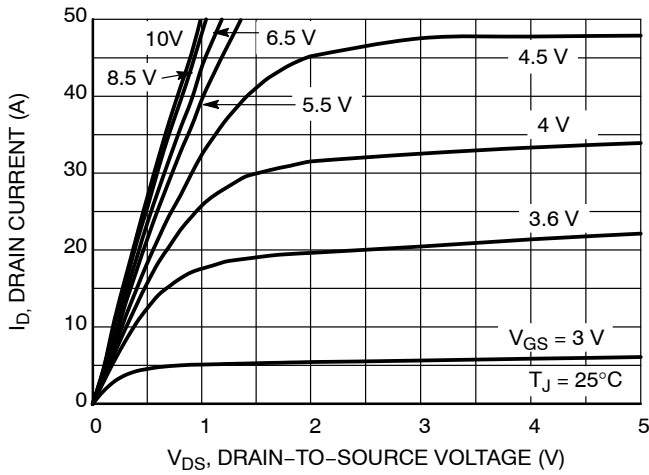


Figure 1. On-Region Characteristics - Channel 2

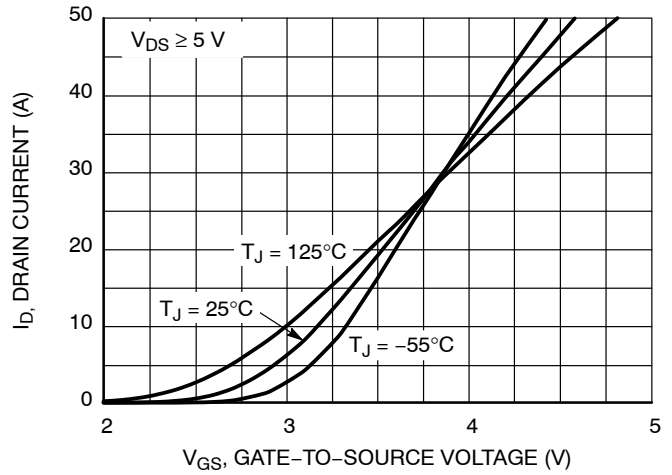


Figure 2. Transfer Characteristics - Channel 2

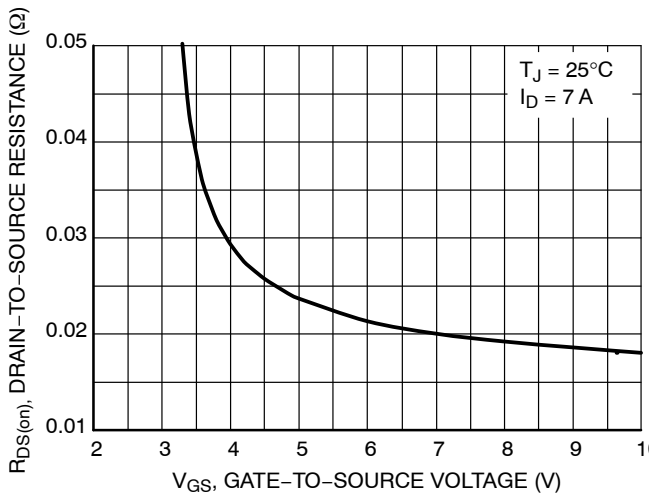


Figure 3. On-Resistance vs. Gate-to-Source Voltage - Channel 2

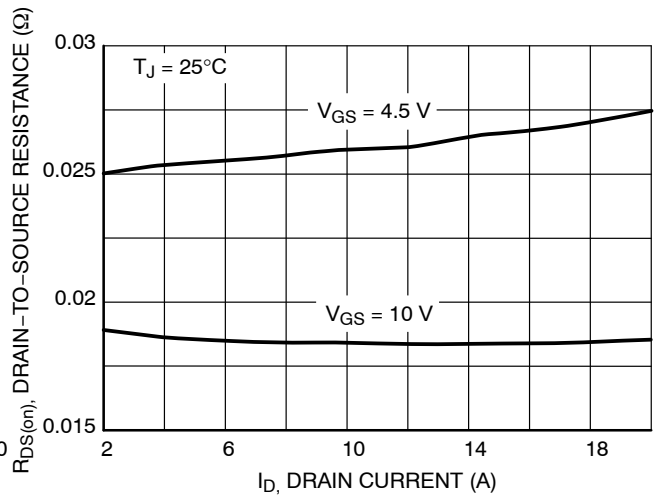


Figure 4. On-Resistance vs. Drain Current and Gate Voltage - Channel 2

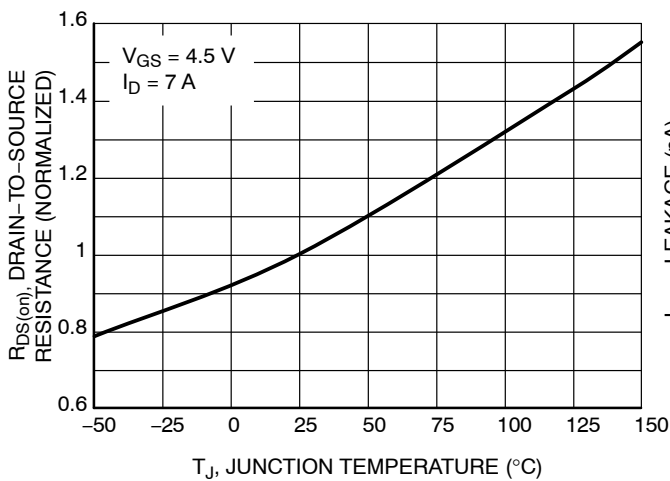


Figure 5. On-Resistance Variation with Temperature - Channel 2

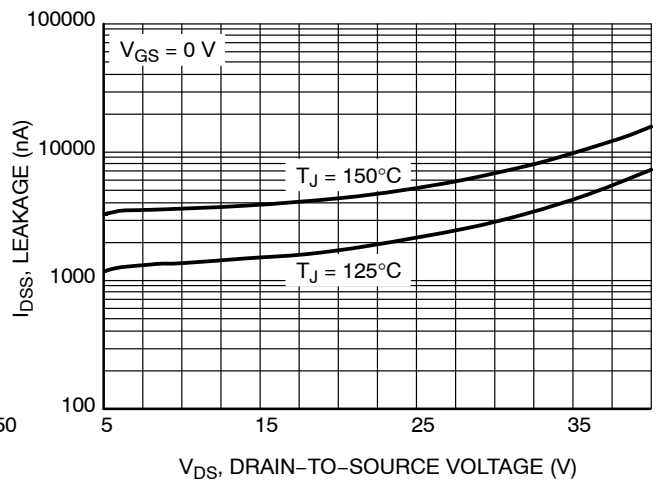


Figure 6. Drain-to-Source Leakage Current vs. Voltage - Channel 2

TYPICAL PERFORMANCE CURVES

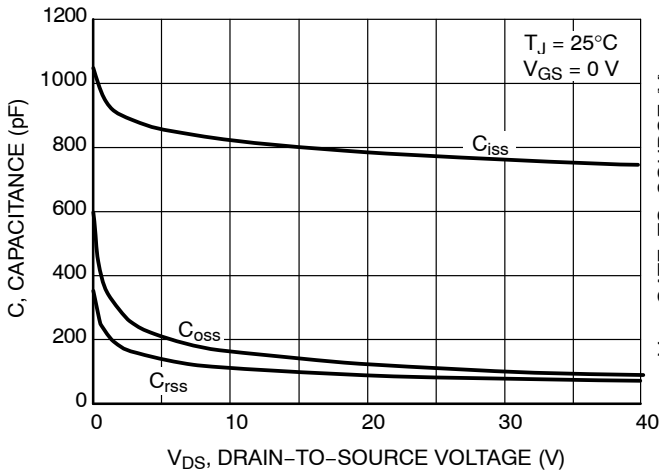


Figure 7. Capacitance Variation - Channel 2

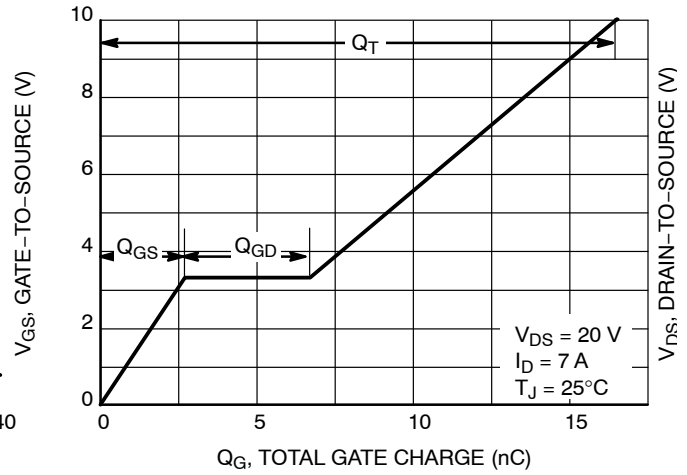


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

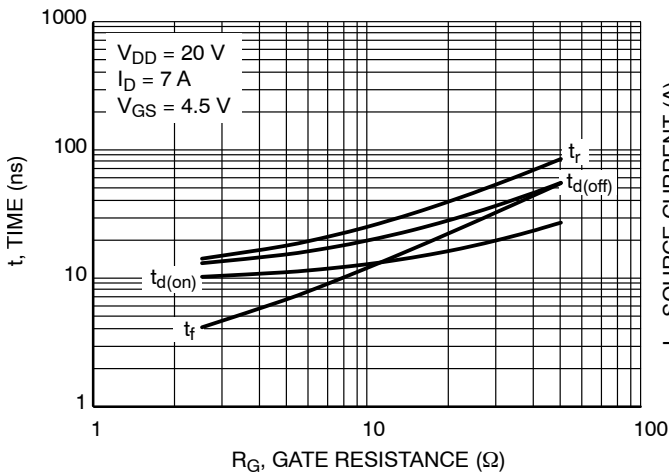


Figure 9. Resistive Switching Time Variation vs. Gate Resistance - Channel 2

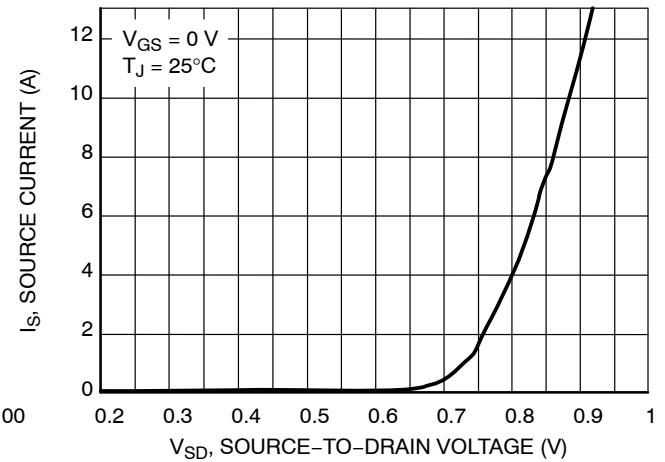


Figure 10. Diode Forward Voltage vs. Current - Channel 2

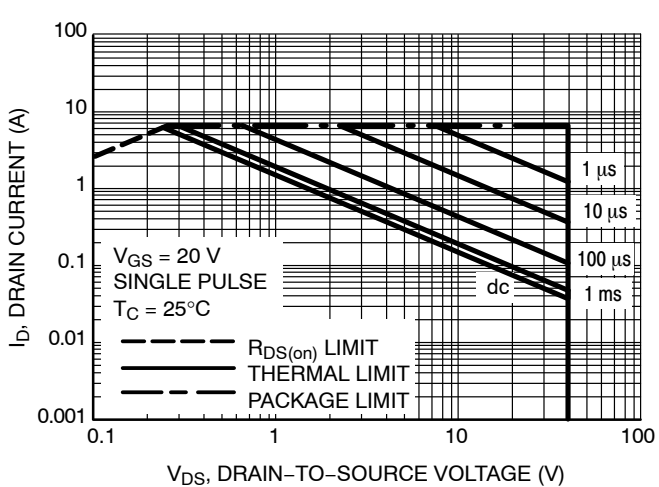


Figure 11. Maximum Rated Forward Biased Safe Operating Area - Channel 2

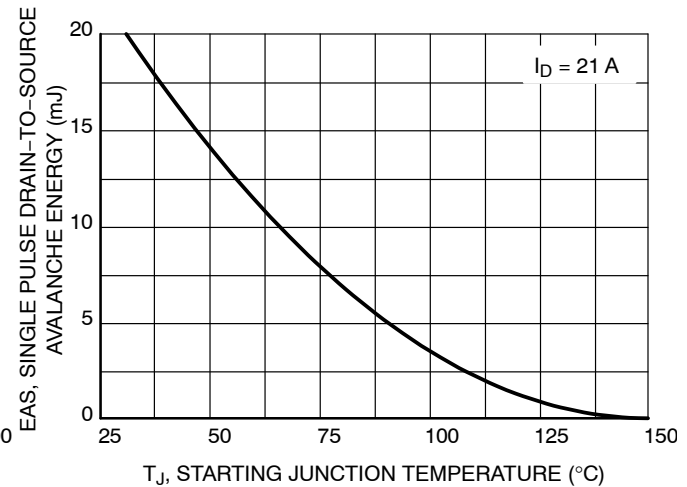


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTMD5836NL

TYPICAL PERFORMANCE CURVES

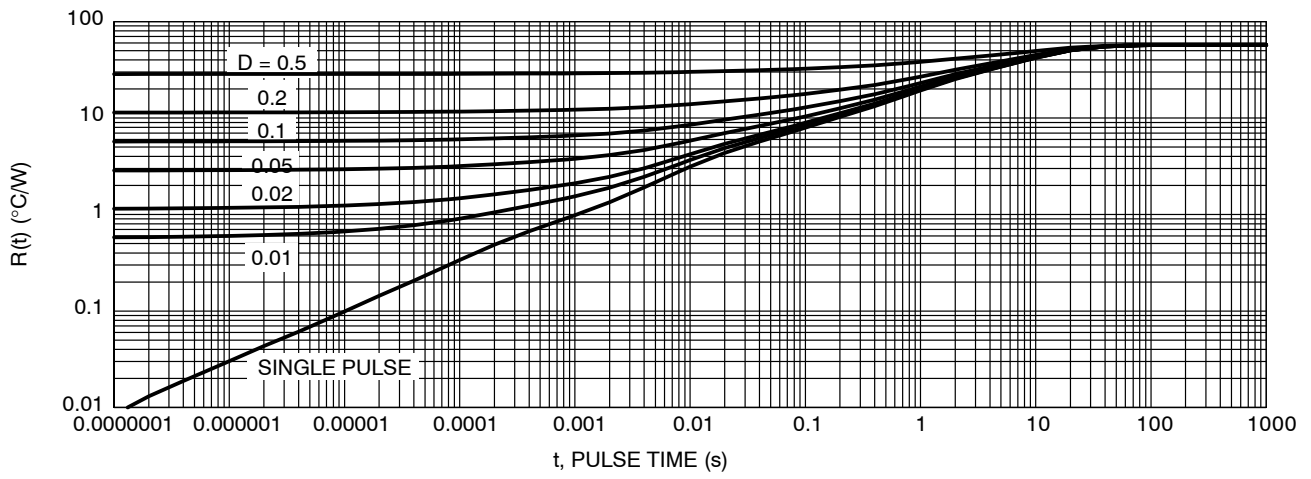
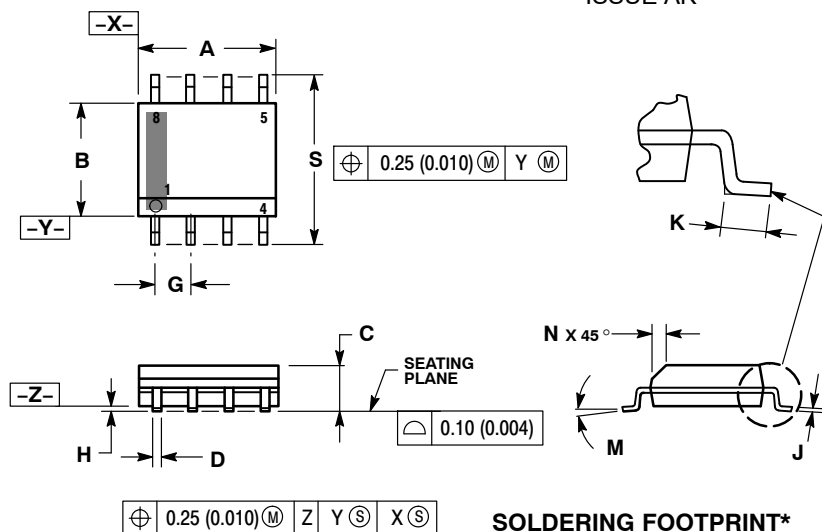


Figure 13. Thermal Response

NTMD5836NL

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

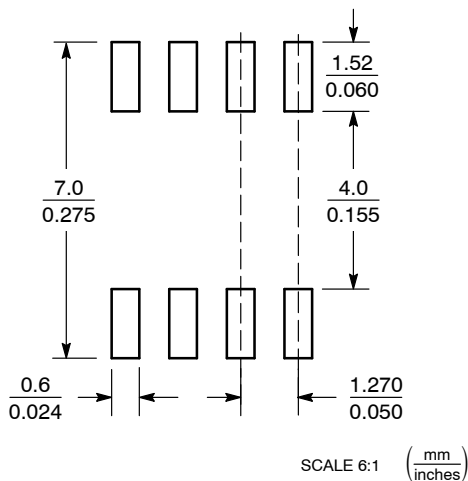


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910
Japan Customer Focus Center Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View NTMD5836NLR2G on WIN SOURCE](#)

 [ON Semiconductor](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management