



**THE DATASHEET OF
AD1868N-J**



FEATURES

Dual Serial Input, Voltage Output DACs
 Single +5 V Supply
 0.004% THD+N (typ)
 Low Power: 50 mW (typ)
 108 dB Channel Separation (min)
 Operates at 8× Oversampling
 16-Pin Plastic DIP or SOIC Package

APPLICATIONS

Portable Compact Disc Players
 Portable DAT Players and Recorders
 Automotive Compact Disc Players
 Automotive DAT Players
 Multimedia Workstations

PRODUCT DESCRIPTION

The AD1868 is a complete dual 18-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements, and laser-trimmed thin-film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation, and low power dissipation.

The DACs on the AD1868 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into seven elements. The 15 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. The AD1868 requires no deglitcher or trimming circuitry. Low noise is achieved through the use of two noise-reduction capacitors.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ± 1 V signals at load currents up to ± 1 mA. The buffered output signal range is 1.5 V to 3.5 V. Reference voltages of 2.5 V are provided, eliminating the need for "False Ground" networks.

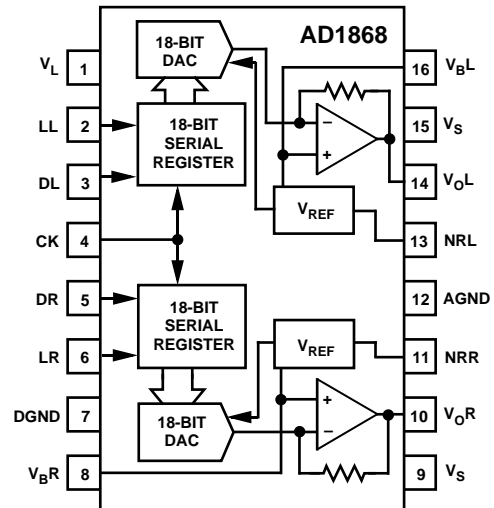
A versatile digital interface allows the AD1868 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 13.5 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency for each channel. The digital input pins of the AD1868 are TTL and +5 V CMOS compatible.

*Protected by U.S. Patent Numbers: 3,961,326; 4,141,004; 4,349,811; 4,857,862; and patents pending.

REV. A

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FUNCTIONAL BLOCK DIAGRAM



The AD1868 operates on +5 V power supplies. The digital supply, V_L , can be separated from the analog supply, V_S , for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery operated systems, operation will continue even with reduced supply voltage. Typically, the AD1868 dissipates 50 mW.

The AD1868 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of -35°C to $+85^\circ\text{C}$ and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single-supply operation @ +5 V.
2. 50 mW power dissipation (typical).
3. THD+N is 0.004% (typical).
4. Signal-to-Noise Ratio is 97.5 dB (typical).
5. 108 dB channel separation (minimum).
6. Compatible with all digital filter chips.
7. 16-pin DIP and 16-pin SOIC packages.
8. No deglitcher required.
9. No external adjustments required.

AD1868—SPECIFICATIONS (typical at $T_A = +25^\circ\text{C}$ and +5 V supplies unless otherwise noted)

| | Min | Typ | Max | Units |
|--|--|------------|--------------|--|
| RESOLUTION | | 18 | | Bit |
| DIGITAL INPUTS | V_{IH} V_{IL} $I_{IH}, V_{IH} = V_L$ $I_{IL}, V_{IL} = \text{DGND}$ | | 0.8 | V V μA μA |
| Maximum Clock Input Frequency | 13.5 | 1.0 1.0 | | MHz |
| ACCURACY | | | | |
| Gain Error | | ± 1 | | % of FSR |
| Gain Matching | | ± 1 | | % of FSR |
| Midscale Error | | ± 15 | | mV |
| Midscale Error Matching | | ± 10 | | mV |
| Gain Linearity Error | | ± 3 | | dB |
| DRIFT (0°C to $+70^\circ\text{C}$) | | | | |
| Gain Drift | | ± 100 | | ppm/ $^\circ\text{C}$ |
| Midscale Drift | | ± 100 | | $\mu\text{V}/^\circ\text{C}$ |
| TOTAL HARMONIC DISTORTION + NOISE | | | | |
| 0 dB, 990.5 Hz | AD1868N | 0.004 | 0.008 | % |
| | AD1868N-J | 0.004 | 0.006 | % |
| -20 dB, 990.5 Hz | AD1868N | 0.020 | 0.08 | % |
| | AD1868N-J | 0.020 | 0.08 | % |
| -60 dB, 990.5 Hz | AD1868N | 2.0 | 5.0 | % |
| | AD1868N-J | 2.0 | 5.0 | % |
| CHANNEL SEPARATION 1 kHz, 0 dB | 108 | NIL* | | dB |
| SIGNAL-TO-NOISE RATIO (with A-Weight Filter) | 95 | 97.5 | | dB |
| D-RANGE (with A-Weight Filter) | 86 | 92 | | dB |
| OUTPUT | | | | |
| Voltage Output Pins (V_{OL}, V_{OR}) | | | | |
| Output Range ($\pm 3\%$) | | ± 1 | | V |
| Output Impedance | | 0.1 | | Ω |
| Load Current | | ± 1 | | mA |
| Bias Voltage Pins (V_{BL}, V_{BR}) | | | | |
| Output Voltage | | +2.5 | | V |
| Output Impedance | | 350 | | Ω |
| POWER SUPPLY | | | | |
| Specification, V_L and V_S | 4.75 | 5 | 5.25 | V |
| Operation, V_L and V_S | 3.5 | | 5.25 | V |
| +I, V_L and $V_S = 5$ V | | 10 | 14 | mA |
| POWER DISSIPATION | | 50 | 70 | mW |
| TEMPERATURE RANGE | | | | |
| Specification | 0 | 25 | 70 | $^\circ\text{C}$ |
| Operation | -35 | | 85 | $^\circ\text{C}$ |
| Storage | -60 | | 100 | $^\circ\text{C}$ |

*Above 115 dB.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

| | |
|------------------------|--------------------------------|
| V_L to DGND | 0 V to 6 V |
| V_S to AGND | 0 V to 6 V |
| AGND to DGND | ± 0.3 V |
| Digital Inputs to DGND | -0.3 to V_L |
| Soldering | +300 $^\circ\text{C}$, 10 sec |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1868 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Typical Performance of the AD1868

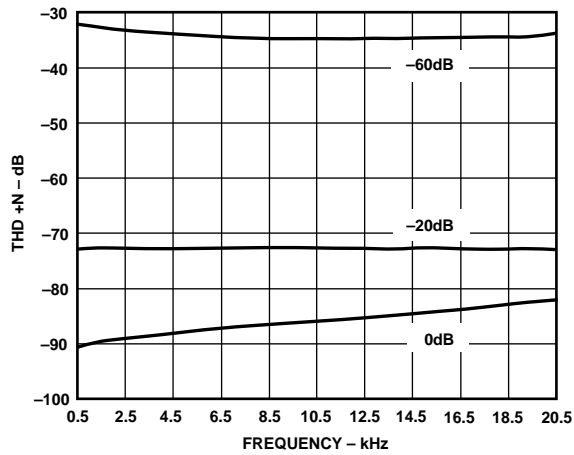


Figure 1. THD+N vs. Frequency

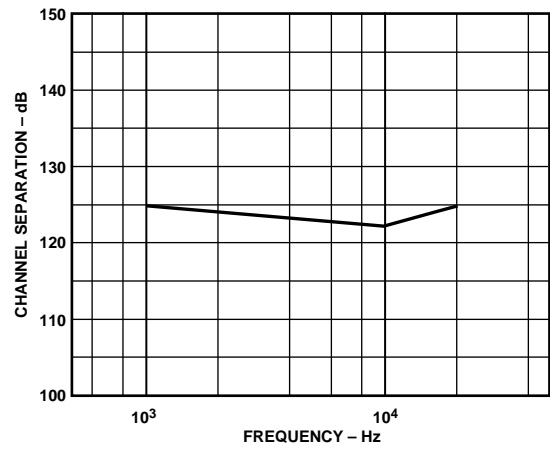


Figure 2. Channel Separation vs. Frequency

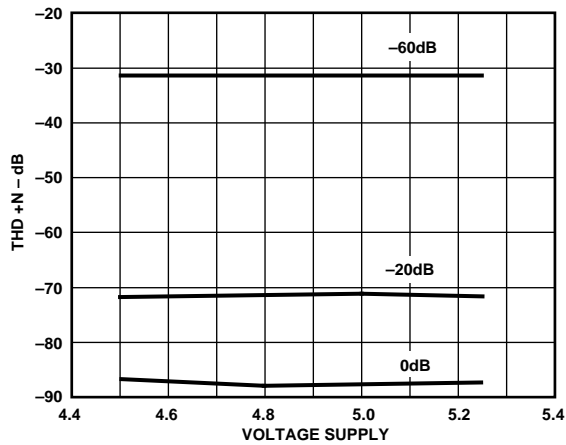


Figure 3. THD+N vs. Supply Voltage

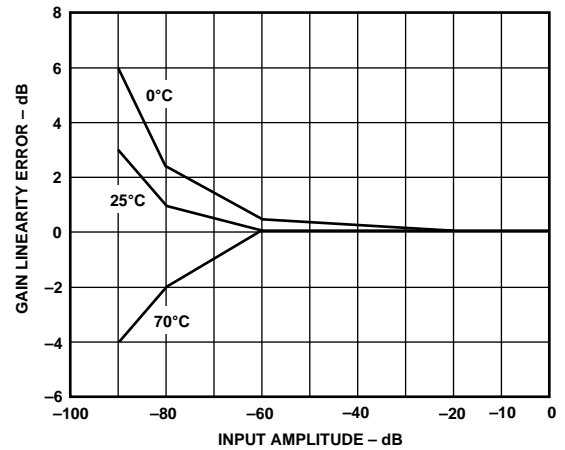


Figure 4. Gain Linearity Error vs. Input Amplitude

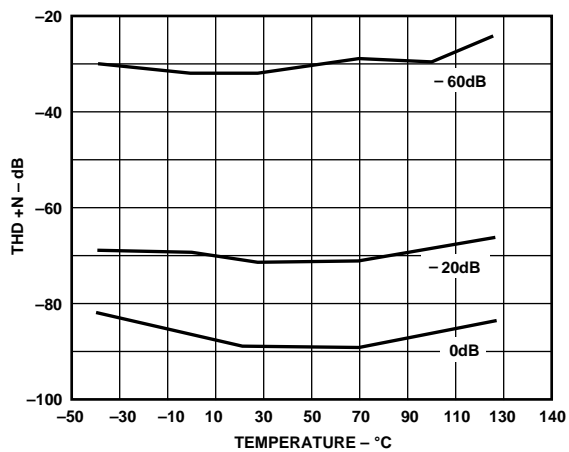


Figure 5. THD+N vs. Temperature

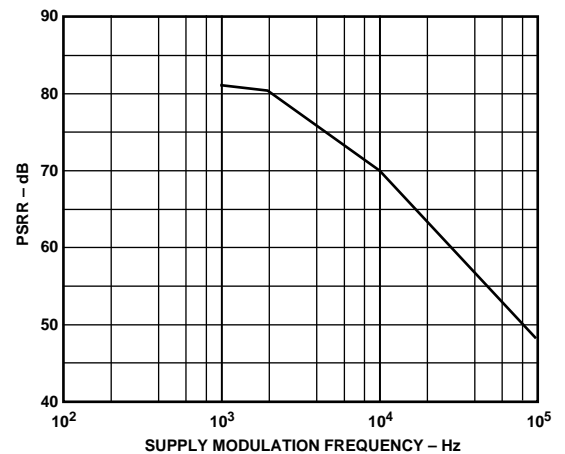
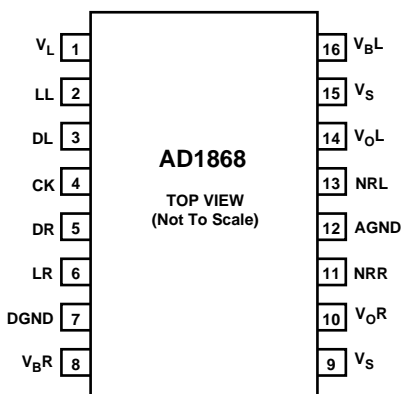


Figure 6. Power Supply Rejection Ratio vs. Frequency

AD1868

PIN CONFIGURATION



PIN DESIGNATIONS

| | | |
|----|------------------|-------------------------------|
| 1 | V _L | Digital Supply (+5 Volts) |
| 2 | LL | Left Channel Latch Enable |
| 3 | DL | Left Channel Data Input |
| 4 | CK | Clock Input |
| 5 | DR | Right Channel Data Input |
| 6 | LR | Right Channel Latch Enable |
| 7 | DGND | Digital Common |
| 8 | V _B R | Right Channel Bias |
| 9 | V _S | Analog Supply (+5 Volts) |
| 10 | V _O R | Right Channel Output |
| 11 | NRR | Right Channel Noise Reduction |
| 12 | AGND | Analog Common |
| 13 | NRL | Left Channel Noise Reduction |
| 14 | V _O L | Left Channel Output |
| 15 | V _S | Analog Supply (+5 Volts) |
| 16 | V _B L | Left Channel Bias |

DEFINITION OF SPECIFICATIONS

Total Harmonic Distortion + Noise

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the amplitude of the fundamental input frequency. It is usually expressed in percent (%) or decibels (dB).

D-Range Distortion

D-range distortion is the ratio of the amplitude of the signal at an amplitude of -60 dB to the amplitude of the distortion plus noise. In this case, an A-weight filter is used. The value specified for D-range performance is the ratio measured plus 60 dB.

Signal-to-Noise Ratio

The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale output is present to the amplitude of the output with no signal present. It is expressed in decibels (dB) and measured using an A-weight filter.

Gain Linearity

Gain linearity is a measure of the deviation of the actual output amplitude from the ideal output amplitude. It is determined by measuring the amplitude of the output signal as the amplitude of that output signal is digitally reduced to a lower level. A perfect D/A converter exhibits no difference between the ideal and actual amplitudes. Gain linearity is expressed in decibels (dB).

Midscale Error

Midscale error is the difference between the analog output and the bias when the twos complement input code representing midscale is loaded in the input register. Midscale error is expressed in mV.

ORDERING GUIDE

| Model | THD + N @ F _S | SNR | Package Option* |
|-----------|--------------------------|-------|-----------------|
| AD1868N | 0.008% | 95 dB | N-16 |
| AD1868R | 0.008% | 95 dB | R-16 |
| AD1868N-J | 0.006% | 95 dB | N-16 |
| AD1868R-J | 0.006% | 95 dB | R-16 |

*N = Plastic DIP; R = SOIC.

FUNCTIONAL DESCRIPTION

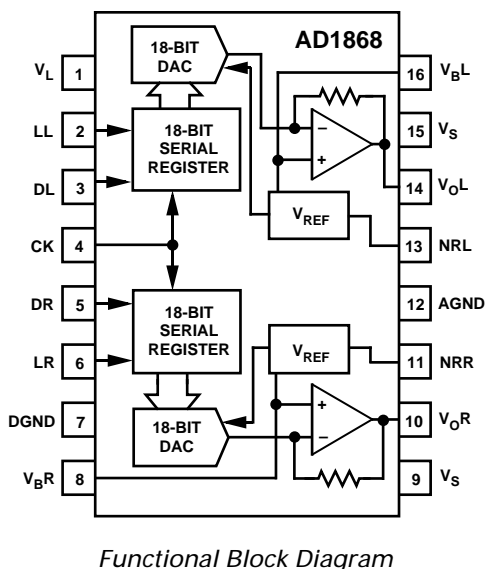
The AD1868 is a complete, voltage output dual 18-bit digital audio DAC which operates with a single +5 volt supply. As shown in the block diagram, each channel contains a voltage reference, an 18-bit DAC, an output amplifier, an 18-bit input latch, and an 18-bit serial-to-parallel input register.

The voltage reference section provides a reference voltage and a false ground voltage for each channel. The low noise bandgap circuits produce reference voltages that are unaffected by changes in temperature, time, and power supply.

The output amplifier uses both MOS and bipolar devices and incorporates an NPN class-A output stage. It is designed to produce high slew rate, low noise, low distortion, and optimal frequency response.

Each 18-bit DAC uses a combination of segmented decoder and R-2R architecture to achieve good integral and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser trimming of these resistors further reduces linearity error, resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow fast switching speeds and low power consumption, contributing to the fast digital timing, low glitch, and low power dissipation of the AD1868.



ANALOG CIRCUIT CONSIDERATIONS GROUNDING RECOMMENDATIONS

The AD1868 has two ground pins, designated as AGND (Pin 12) and DGND (Pin 7). The analog ground, AGND, serves as the “high quality” reference ground for analog signals and as a return path for the supply current from the analog portion of the device. The system analog common should be located as close as possible to Pin 12 to minimize any voltage drop which may develop between these two points, although the internal circuit is designed to minimize signal dependence of the analog return current.

The digital ground, DGND, returns ground current from the digital logic portion of the device. This pin should be connected to the digital common node in the system. As shown in Figure 7, the analog and digital grounds should be joined at one point in the system. When these two grounds are remotely connected such as at the power supply ground, care should be taken to minimize the voltage difference between the DGND and AGND pins in order to ensure the specified performance.

POWER SUPPLIES AND DECOUPLING

The AD1868 has three power supply input pins. V_S (Pins 9 and 15) provides the supply voltages which operate the analog portion of the device including the 18-bit DACs, the voltage references, and the output amplifiers. The V_S supplies are designed to operate with a +5 V supply. These pins should be decoupled to analog common using a 0.1 μF capacitor. Good engineering practice suggests that the bypass capacitors be placed as close as possible to the package pins. This minimizes the inherent inductive effects of printed circuit board traces.

V_L (Pin 1) operates the digital portions of the chip including the input shift registers and the input latching circuitry. V_L is also designed to operate with a +5 V supply. This pin should be bypassed to digital common using a 0.1 μF capacitor, again placed as close as possible to the package pin. Figure 7 illustrates the correct connection of the digital and analog supply bypass capacitors.

An important feature of the AD1868 audio DAC is its ability to operate at reduced power supply voltages. This feature is very important in portable battery operated systems. As the batteries discharge, the supply voltage drops. Unlike any other audio

DAC, the AD1868 can continue to function at supply voltages as low as 3.5 V. Because of its unique design, the power requirements of the AD1868 diminish as the battery voltage drops, further extending the operating time of the system.

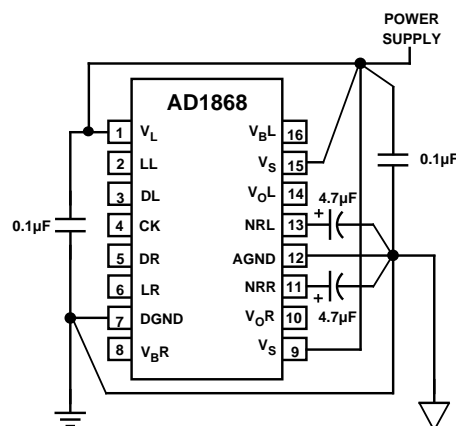


Figure 7. Recommended Circuit Schematic

NOISE REDUCTION CAPACITORS

The AD1868 has two noise reduction pins designated as NRL (Pin 13) and NRR (Pin 11). It is recommended that external noise reduction capacitors be connected from these pins to AGND to reduce the output noise contributed by the voltage reference circuitry. As shown in Figure 7, each of these pins should be bypassed to AGND with a 4.7 μF or larger capacitor. The connections between the capacitors, package pins and AGND should be as short as possible to achieve the lowest noise.

USING V_{B_L} AND V_{B_R}

The AD1868 has two bias voltage reference pins, designated as V_{B_R} (Pin 8) and V_{B_L} (Pin 16). These pins supply a dc reference voltage equal to the center of the output voltage swing. These bias voltages replace “False Ground” networks previously required in single-supply audio systems. At the same time, they allow dc-coupled systems, improving audio performance.

Figure 8a illustrates the traditional approach used to generate False Ground voltages in single-supply audio systems. This circuit requires additional power and circuit board space.

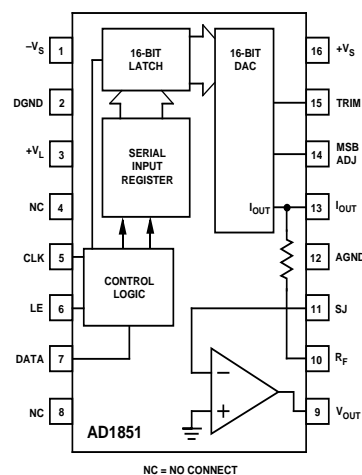


Figure 8a. Schematic Using False Ground

AD1868

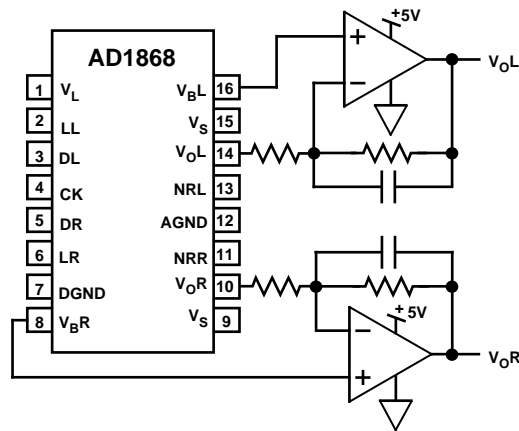


Figure 8b. Circuitry Using Voltage Biases

The AD1868 eliminates the need for “False Ground” circuitry. V_{BR} and V_{BL} generate the required bias voltages previously generated by the “False Ground.” As shown in Figure 8b, V_{BR} and V_{BL} may be used as the reference point in each output channel. This permits a dc-coupled output signal path. This eliminates ac-coupling capacitors and improves low frequency performance. It should be noted that these bias outputs have relatively high output impedance and will not drive output currents larger than 100 μ A without degrading the specified performance.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. Therefore, the THD+N specification provides a direct method to classify and choose an audio DAC for a desired level of performance.

Figure 1 illustrates the typical THD+N versus frequency performance of the AD1868. It is evident that the THD+N performance of the AD1868 remains stable at all three levels through a wide range of frequencies. A load impedance of at least 2 k Ω is recommended for best THD+N performance.

Analog Devices tests and grades all AD1868s on the basis of THD+N performance. During the distortion test, a high speed digital pattern generator transmits digital data to each channel of the device under test. Eighteen-bit data is latched into the DAC at 352.8 kHz ($8 \times F_S$). The test waveform is a 990.5 Hz sine wave with 0 dB, -20 dB, and -60 dB amplitudes. A 4096-point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, and D-range. No deglitchers or external adjustments are used.

DIGITAL CIRCUIT CONSIDERATIONS

INPUT DATA

The AD1868 digital input port employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial inputs for the left and right DACs, respectively. Input data bits are clocked into the input register on the rising edge of CLK. The falling edges of LL and LR cause the last 18 bits which were clocked into the serial registers to be shifted into the DACs, thereby updating the respective DAC outputs. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together. Data is transmitted to the AD1868 in a bit stream composed of 18-bit words with a serial, two's complement, MSB first format. Left and right channels share the Clock (CLK) signal.

Figure 9 illustrates the general signal requirements for data transfer for the AD1868.

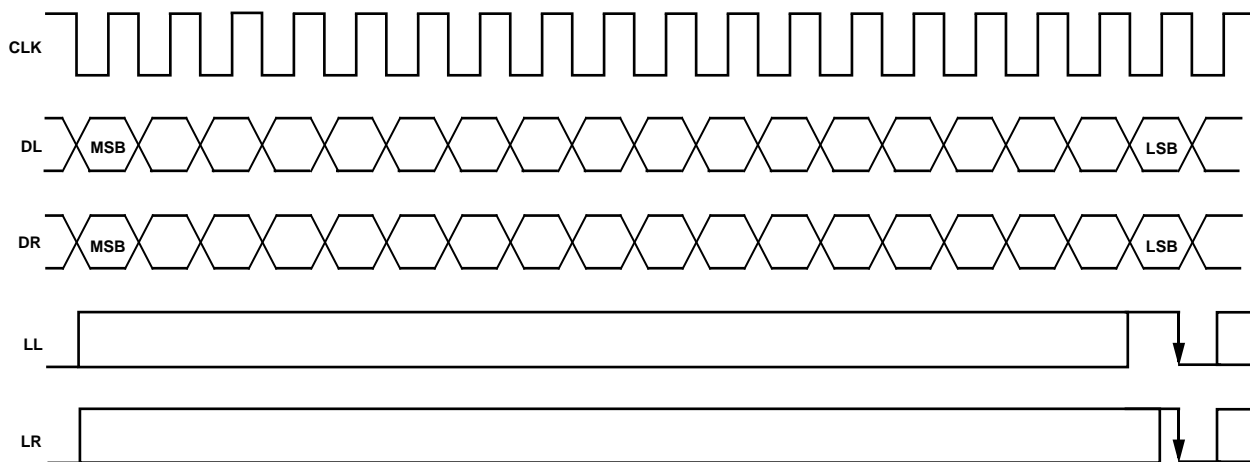


Figure 9. Control Signals

TIMING

Figure 10 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1868 are TTL and 5 V CMOS compatible.

The maximum clock rate of the AD1868 is specified to be at least 13.5 MHz. This clock rate allows data transfer rates of $2\times$, $4\times$, $8\times$, and $16\times F_S$ (where F_S equals 44.1 kHz). The applications section of this data sheet contains additional guidelines for using the AD1868.

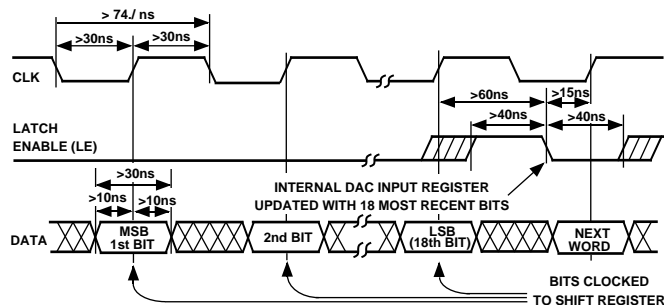


Figure 10. Input Signal Timing

APPLICATIONS OF THE AD1868

The AD1868 is a high performance audio DAC specifically designed for portable and automotive digital audio applications. These market segments have technical requirements fundamentally different than those found in the high-end or home-use market segments. Portable equipment must rely on components which require low amounts of power to offer reasonable playing times. Also, battery voltages drop as the end of the discharge cycle is approached. The AD1868's ability to operate from a single +5 V supply makes it a good choice for battery-operated gear. As the battery voltage drops, the power dissipation of the

AD1868 drops. This extends the usable battery life. Finally, as the battery supply voltage drops, the bias voltages and signal swings also drop, preventing signal clipping and abrupt degradation of distortion. Figure 3 illustrates that THD+N performance of the AD1868 remains constant through a wide range of supply voltages.

Automotive equipment rely on components which are able to consistently perform in a wide range of temperatures. In addition, due to the limited space available in automotive applications, small size is essential. The AD1868 is able to satisfy both of these requirements. The device has guaranteed specified performance between 0°C and $+70^\circ\text{C}$, and the 16-pin DIP or 16-pin SOIC package is particularly attractive where overall size is important.

Since the AD1868 provides dc bias voltages, the entire signal chain can be dc-coupled. This eliminates ac-coupling capacitors from the signal path, improving low frequency performance and lowering system cost and size.

In summary, the AD1868 is an excellent choice for battery operated portable or automotive digital audio systems. In the following sections, some examples of high performance audio applications featuring the AD1868 are described.

AD1868 with Sony CXD2550P Digital Filter

Figure 11 illustrates an 18-bit CD player design incorporating an AD1868 DAC, a Sony CXD2550P digital filter and 2-pole antialias filters. This high performance, single supply design operates at $8\times F_S$ and is suitable for portable and automotive applications. In this design, the CXD2550P filter transmits left and right channel digital data to the AD1868. The left and right latch signals, LL and LR, are both provided by the word clock signal (LRCKO) of the digital filter. The digital data is converted to low distortion output voltages by the output amplifiers on the AD1868. Also, no deglitching circuitry or external adjustments are required. Bypass capacitors, noise reduction capacitors and the antialias filter details are omitted for clarity.

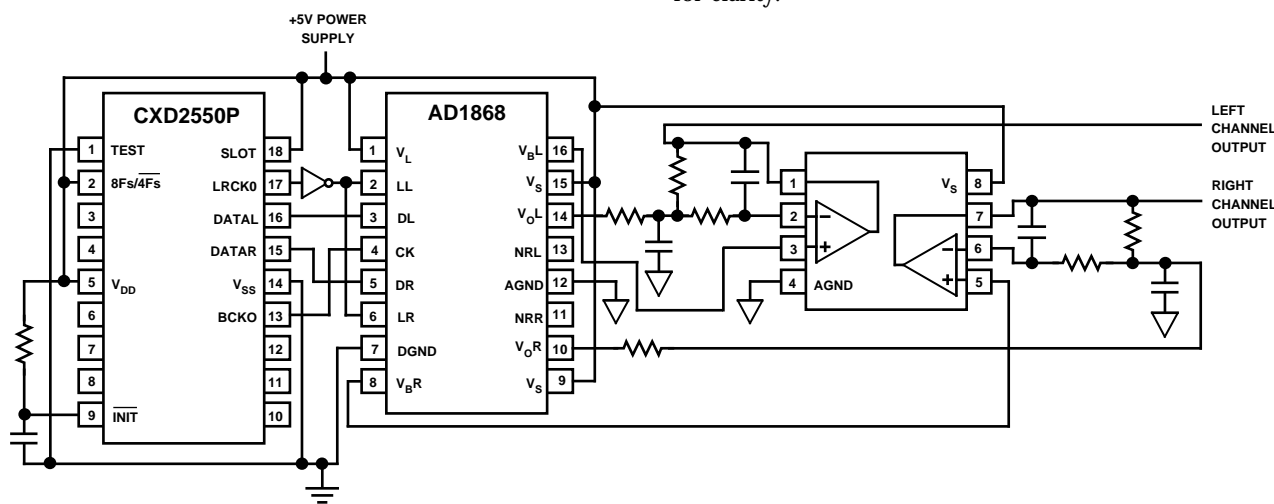


Figure 11. AD1868 with Sony CXD2550P Digital Filter

AD1868

ADDITIONAL APPLICATIONS

In addition to CD player designs, the AD1868 is suitable for similar applications such as DAT, portable musical instruments, Laptop and Notebook personal computers, and PC audio I/O boards. The circuit techniques illustrated are directly applicable in those applications.

Figures 12, 13, and 14 show connection diagrams for the AD1868 with popular digital filter chips from NPC and Yamaha. Each application operates at $8 \times F_S$ operation. Please refer to the appropriate sections of this data sheet for additional information.

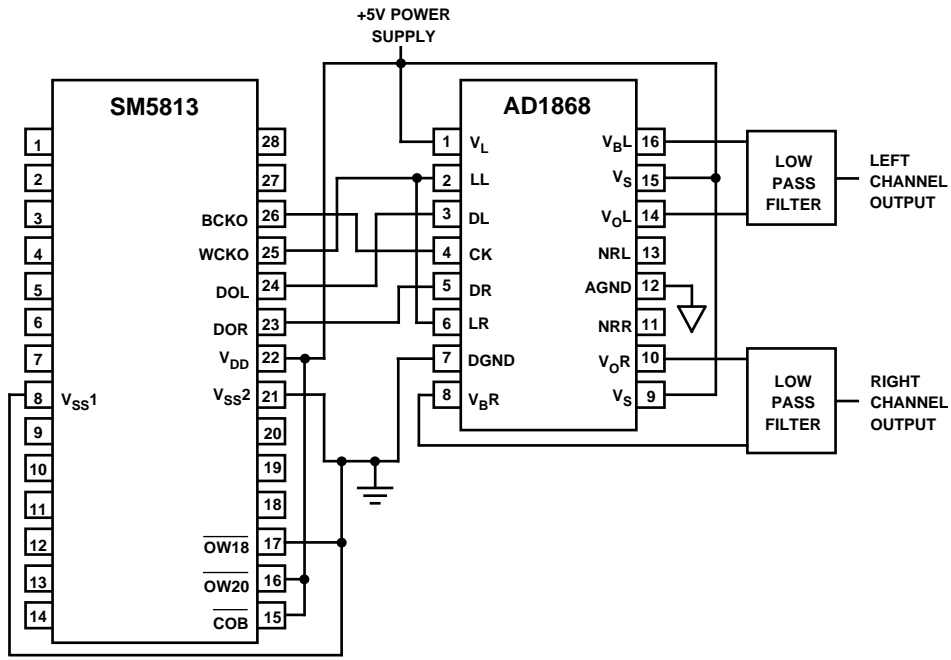


Figure 12. AD1868 with NPC SM5813 Digital Filter

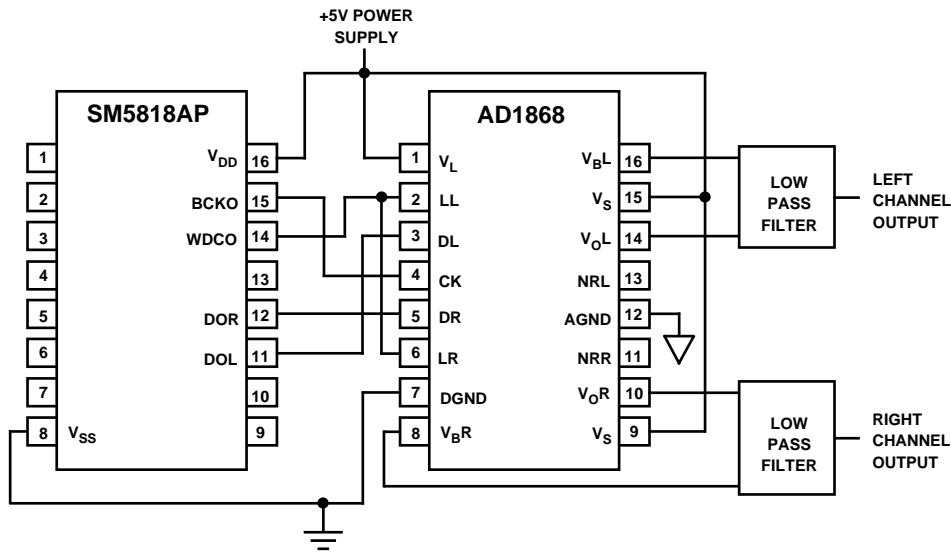


Figure 13. AD1868 with NPC SM5818AP Digital Filter

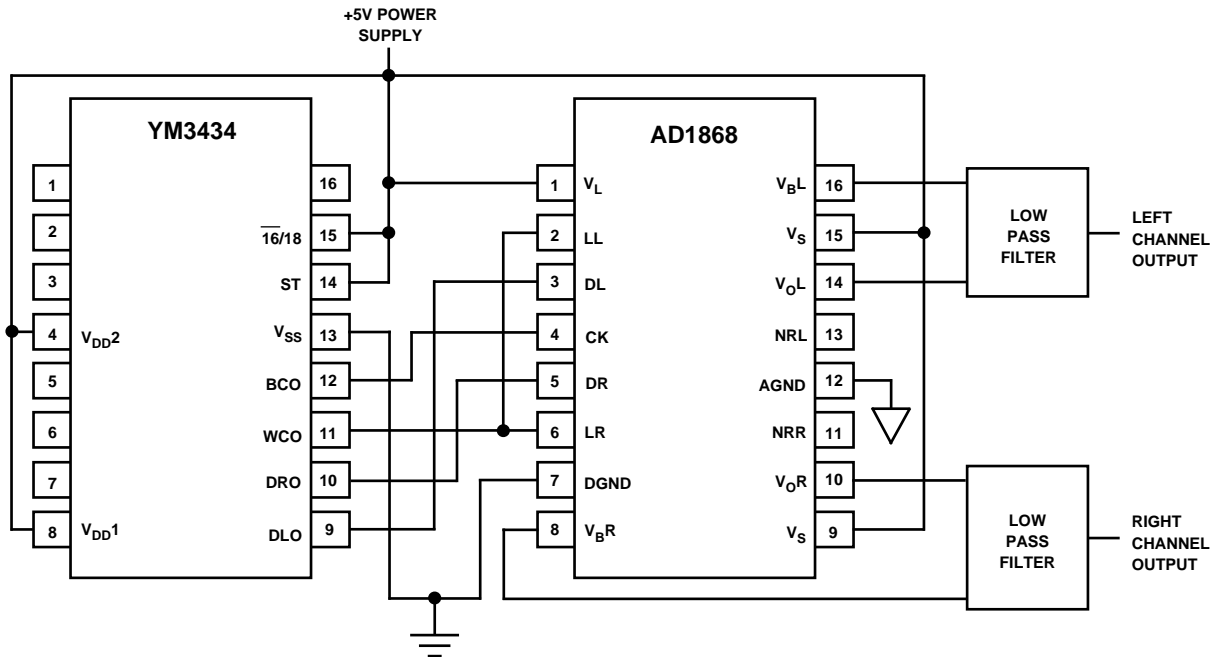
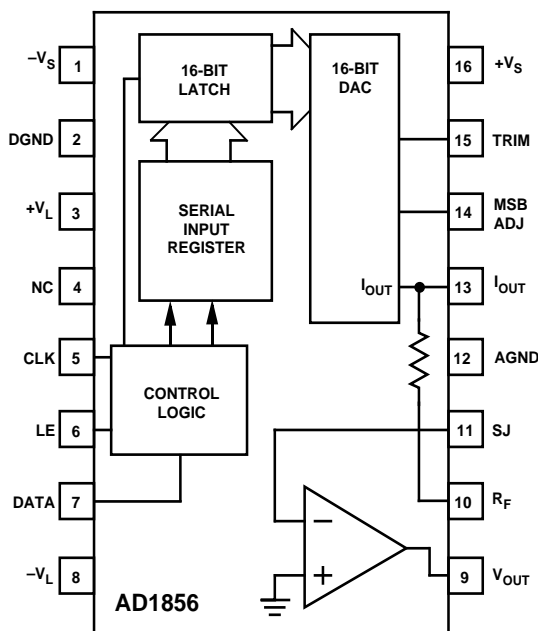


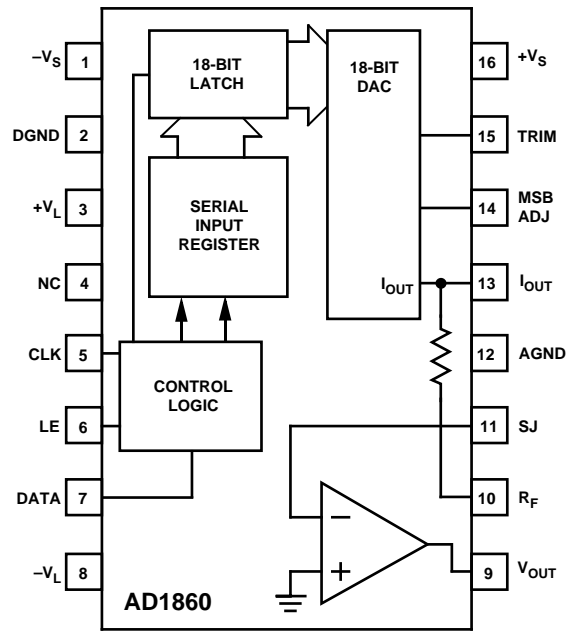
Figure 14. AD1868 with Yamaha YM3434 Digital Filter

OTHER DIGITAL AUDIO COMPONENTS AVAILABLE FROM ANALOG DEVICES



NC = NO CONNECT

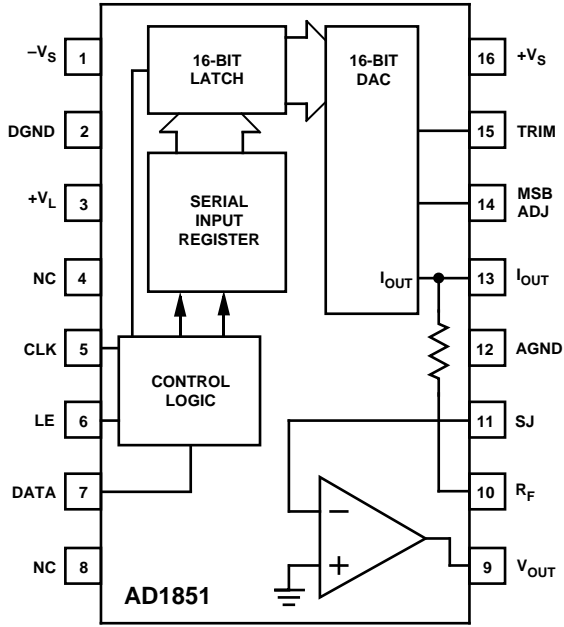
AD1856 16-Bit Audio DAC
 Complete, No External Components Required
 16-Pin DIP or SOIC Package
 Standard Pinout
 Low Cost



NC = NO CONNECT

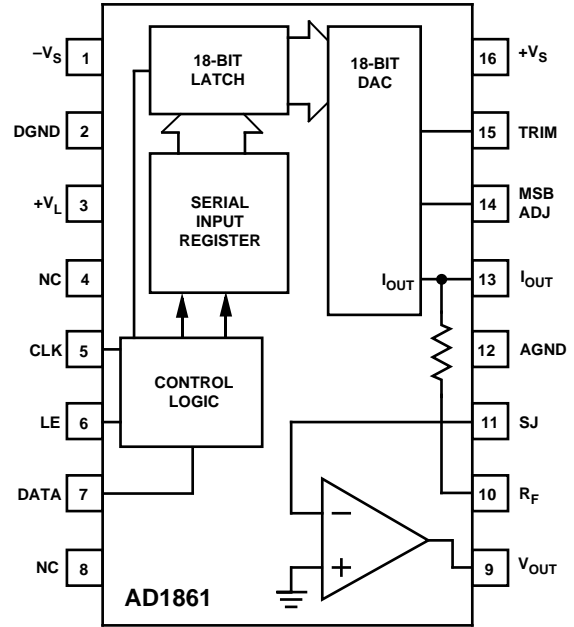
AD1860 18-Bit Audio DAC
 Complete, No External Components Required
 102 dB SNR Minimum
 16-Pin DIP or SOIC Package
 Standard Pinout

AD1868



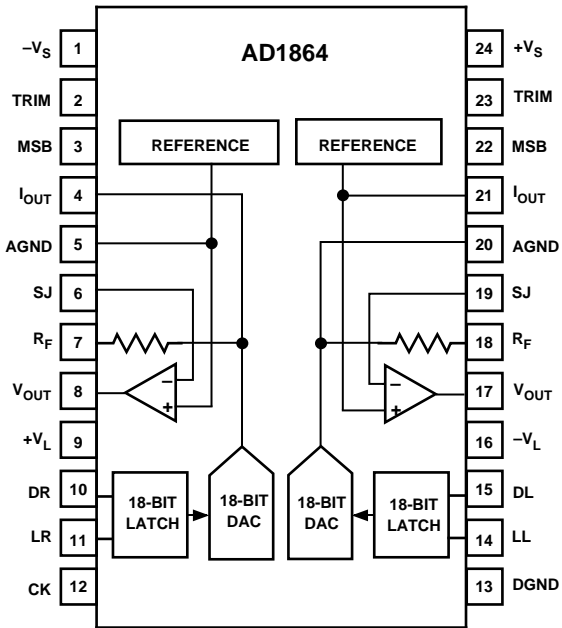
NC = NO CONNECT

AD1851 16-Bit PCM Audio DAC
 107 dB SNR Minimum
 $16 \times F_S$ Capability
 ± 5 V Supply

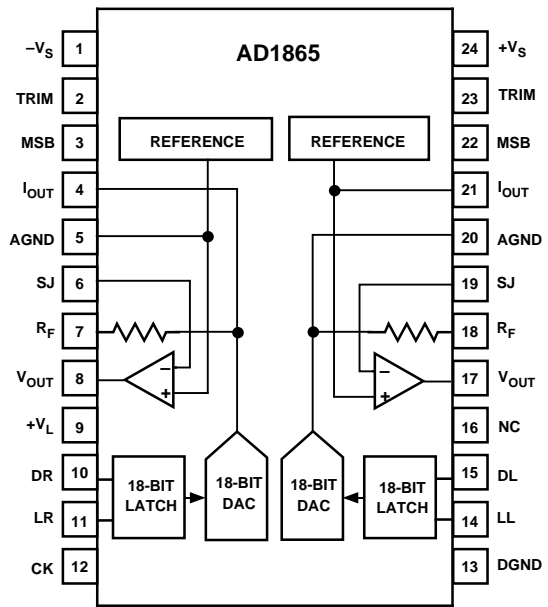


NC = NO CONNECT

AD1861 18-Bit PCM Audio DAC
 107 dB SNR Minimum
 $16 \times F_S$ Capability
 ± 5 V Supply

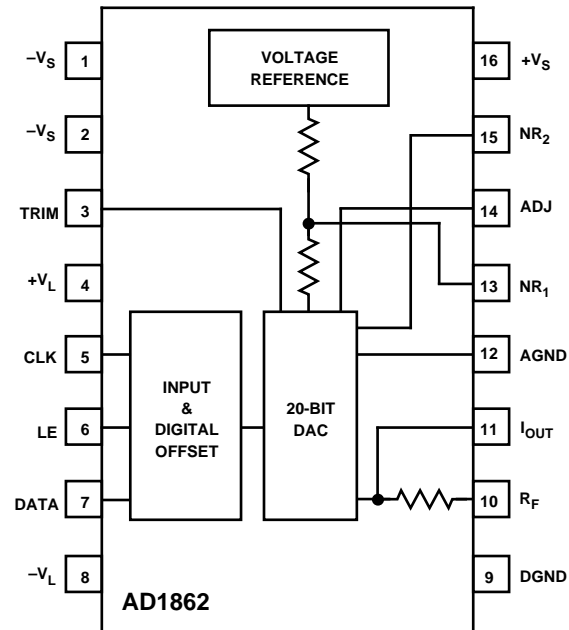


AD1864 Dual 18-Bit Audio DAC
 Complete, No External Components
 High Performance
 Low Crosstalk
 24-Pin DIP
 THD+N = 0.004% (typical)



NC = NO CONNECT

AD1865 Dual 18-Bit Audio DAC
 107 dB SNR Minimum
 $16 \times F_S$ Capability
 THD+N = 0.004% (typical)
 ± 5 V Supply

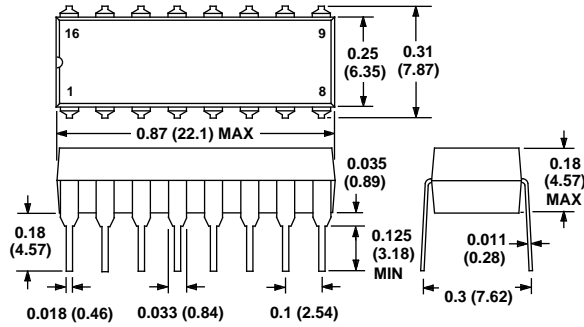


AD1862 20-Bit, Low Noise Audio DAC

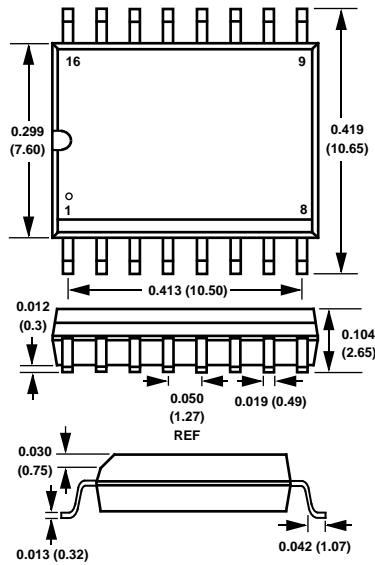
110 dB SNR Minimum
 THD+N = 0.0019% (typical)
 ±1 dB Gain Linearity
 16-Pin Plastic DIP

OUTLINE DIMENSIONS
 Dimensions shown in inches and (mm).

Plastic DIP (N) Package





Plastic SOIC (R) Package



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