



# THE DATASHEET OF STF20N95K5



N-channel 950 V, 0.275  $\Omega$  typ., 17.5 A MDmesh™ K5  
Power MOSFETs in D<sup>2</sup>PAK, TO-220FP, TO-220 and TO-247

Datasheet - production data

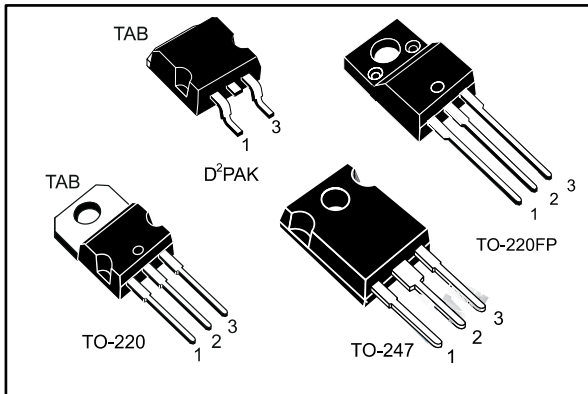
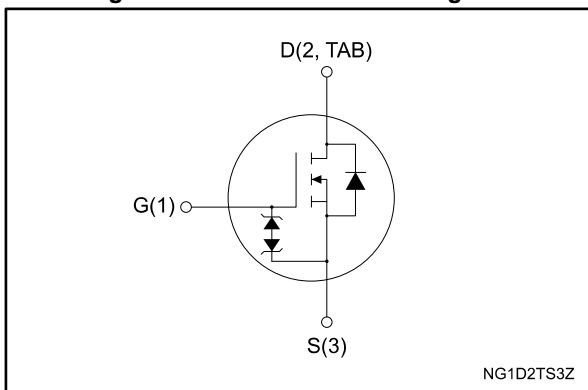


Figure 1: Internal schematic diagram



## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STB20N95K5	950 V	0.330 $\Omega$	17.5 A	250 W
STF20N95K5				40 W
STP20N95K5				250 W
STW20N95K5				

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STB20N95K5	20N95K5	D <sup>2</sup> PAK	Tape and reel
STF20N95K5		TO-220FP	Tube
STP20N95K5		TO-220	
STW20N95K5		TO-247	

---

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits .....</b>	<b>9</b>
<b>4</b>	<b>Package information .....</b>	<b>10</b>
	4.1 D <sup>2</sup> PAK package information .....	10
	4.2 TO-220FP package information .....	13
	4.3 TO-220 type A package information .....	15
	4.4 TO-247 package information .....	17
	4.5 D <sup>2</sup> PAK packing information .....	19
<b>5</b>	<b>Revision history .....</b>	<b>21</b>

# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK TO-220 TO-247	TO-220FP	
V <sub>GS</sub>	Gate-source voltage	±30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	17.5		A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	11		A
I <sub>D</sub> <sup>(1)</sup>	Drain current (pulsed)	70		A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	250	40	W
ESD	Gate-source human body model (R= 1,5 kΩ, C = 100 pF)	2		kV
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)	2500		V
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	6		V/ns
dv/dt <sup>(3)</sup>	MOSFET dv/dt ruggedness	50		
T <sub>j</sub>	Operating junction temperature range	-55 to 150		°C
T <sub>stg</sub>	Storage temperature range			

**Notes:**

- (1) Pulse width limited by safe operating area.
- (2) I<sub>SD</sub> ≤ 17.5 A, di/dt ≤ 100 A/μs; V<sub>DS</sub> peak ≤ V<sub>(BR)DSS</sub>
- (3) V<sub>DS</sub> ≤ 760 V

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		D <sup>2</sup> PAK	TO-220	TO-247	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case	0.5			3.1	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient		62.5	50	62.5	
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb	30				

**Notes:**

- (1) When mounted on 1 inch<sup>2</sup> FR-4 board, 2 Oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>jmax</sub> )	6	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	200	mJ

## 2 Electrical characteristics

T<sub>C</sub> = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	950			V
I <sub>DSS</sub>	Zero-gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 950 V			1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 950 V T <sub>C</sub> = 125 °C <sup>(1)</sup>			50	μA
I <sub>GSS</sub>	Gate body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9 A		0.275	0.330	Ω

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iSS</sub>	Input capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	1550	-	pF
C <sub>oSS</sub>	Output capacitance		-	140	-	pF
C <sub>rSS</sub>	Reverse transfer capacitance		-	1	-	pF
C <sub>o(er)</sub> <sup>(1)</sup>	Equivalent capacitance energy related	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 760 V	-	65	-	pF
C <sub>o(tr)</sub> <sup>(2)</sup>	Equivalent capacitance time related			178	-	pF
R <sub>g</sub>	Intrinsic gate resistance	f = 1 MHz, I <sub>D</sub> = 0 A	-	3.5	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 760 V, I <sub>D</sub> = 17.5 A V <sub>GS</sub> = 10 V (see Figure 20: "Test circuit for gate charge behavior")	-	48	-	nC
Q <sub>gs</sub>	Gate-source charge		-	9	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	32.5	-	nC

**Notes:**

<sup>(1)</sup>C<sub>o(er)</sub> is a constant capacitance value that gives the same stored energy as C<sub>oSS</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.

<sup>(2)</sup>C<sub>o(tr)</sub> is a constant capacitance value that gives the same charging time as C<sub>oSS</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$ , $I_D = 9\text{ A}$ , $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 19</a> : "Test circuit for resistive load switching times" and <a href="#">Figure 24</a> : "Switching time waveform")	-	18	-	ns
$t_r$	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	65	-	ns
$t_f$	Fall time		-	18	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		17.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		70	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17.5\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 21</a> : "Test circuit for inductive load switching and diode recovery times")	-	513		ns
$Q_{rr}$	Reverse recovery charge		-	12		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	46		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 21</a> : "Test circuit for inductive load switching and diode recovery times")	-	670		ns
$Q_{rr}$	Reverse recovery charge		-	15		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	44		A

**Notes:**

(1)Pulse width limited by safe operating area

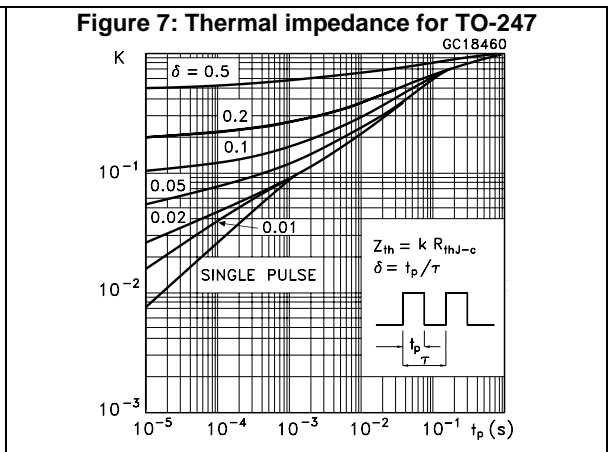
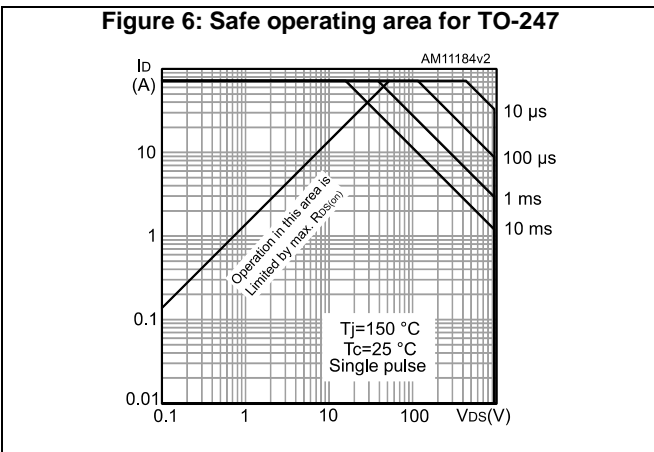
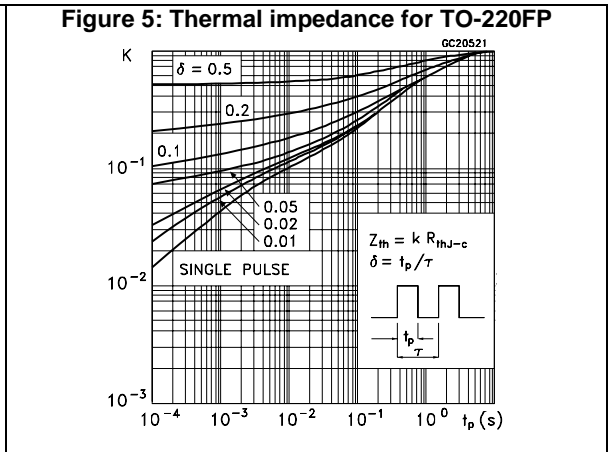
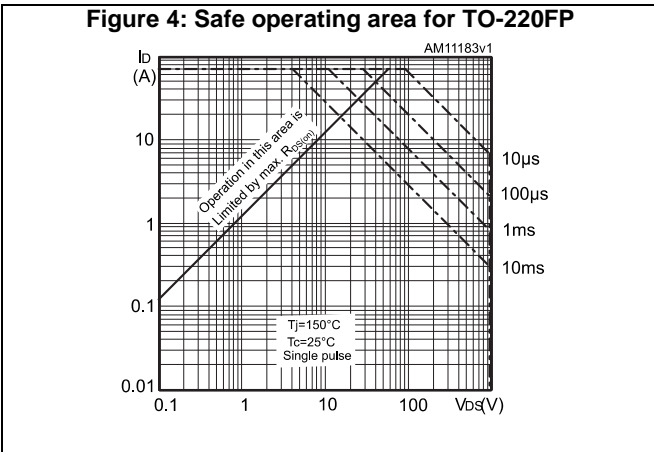
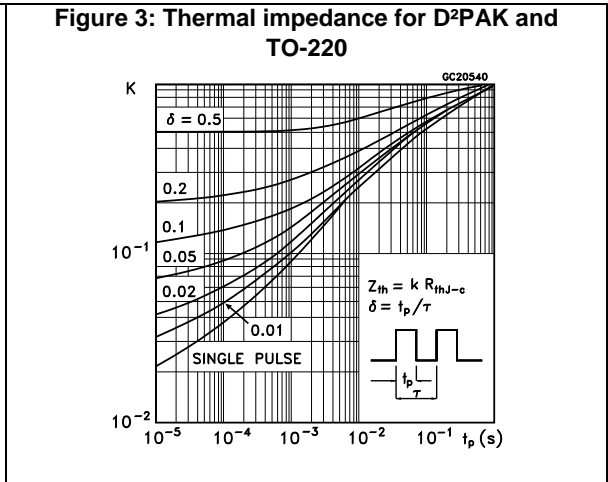
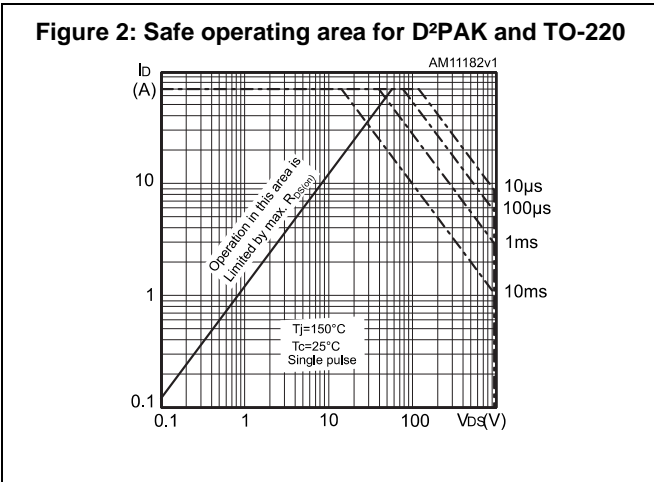
(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

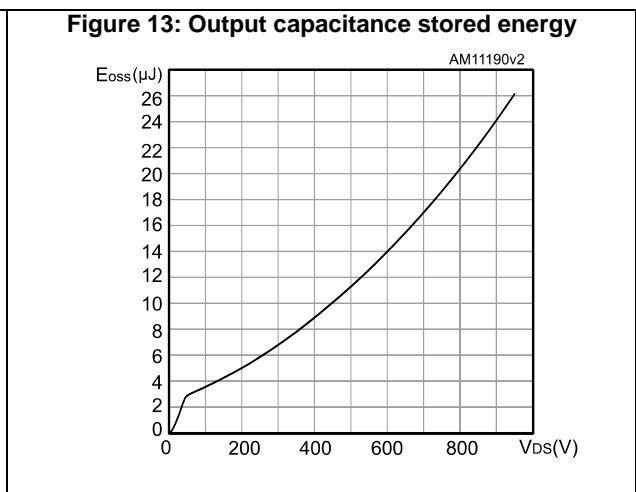
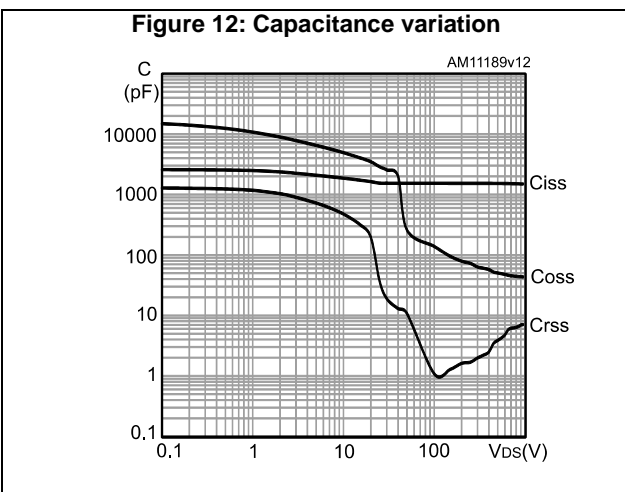
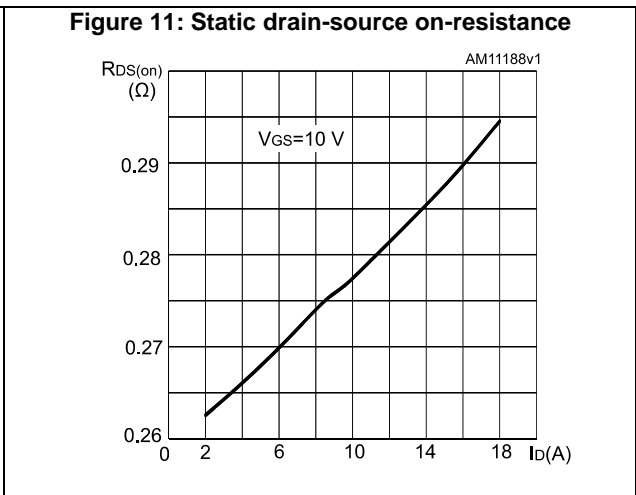
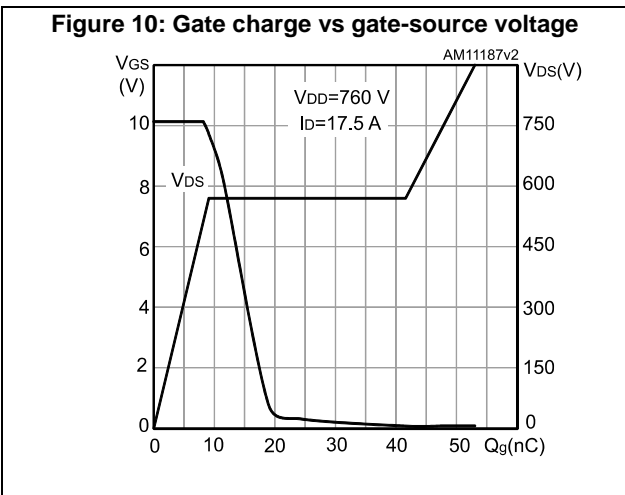
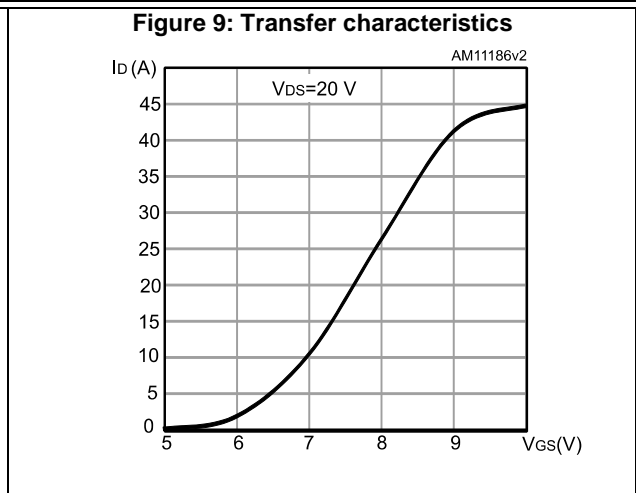
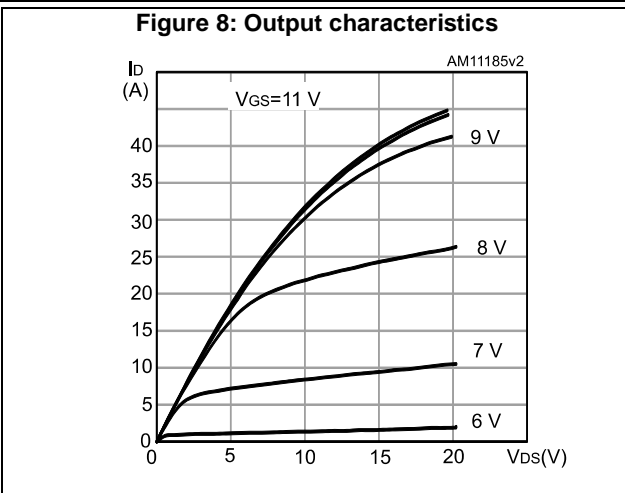
Table 9: Gate-source Zener diode

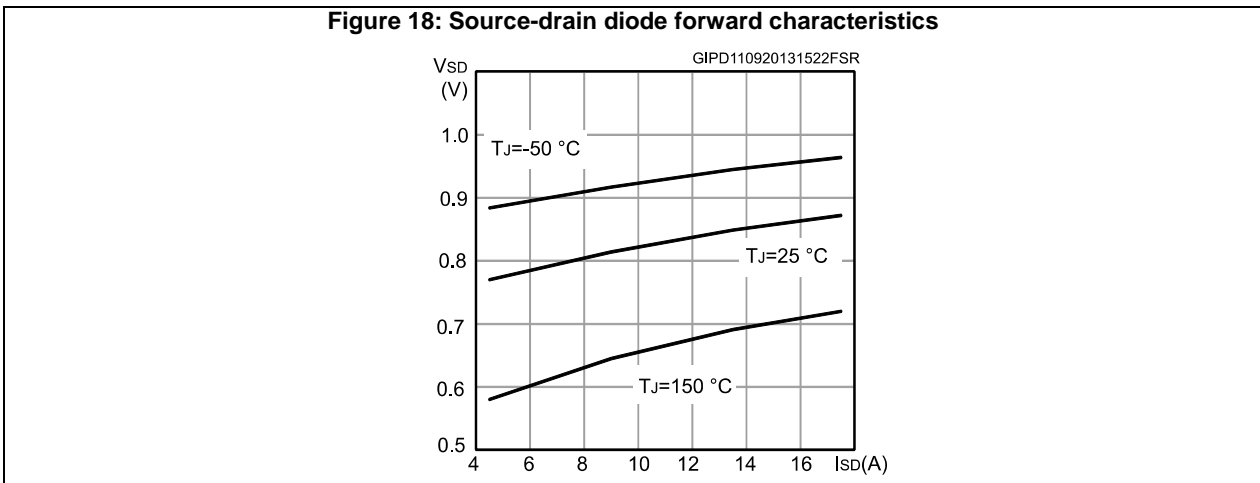
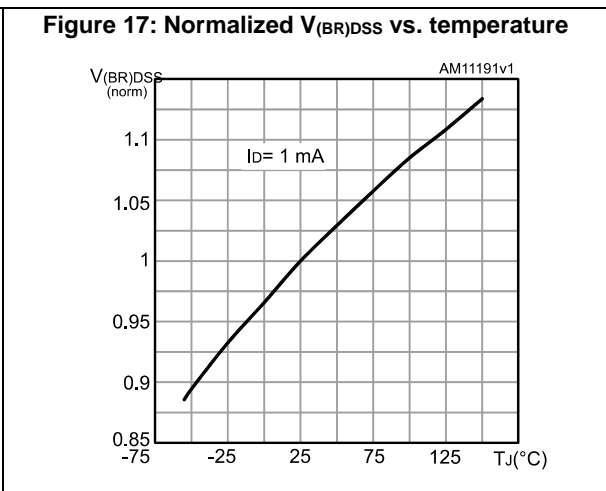
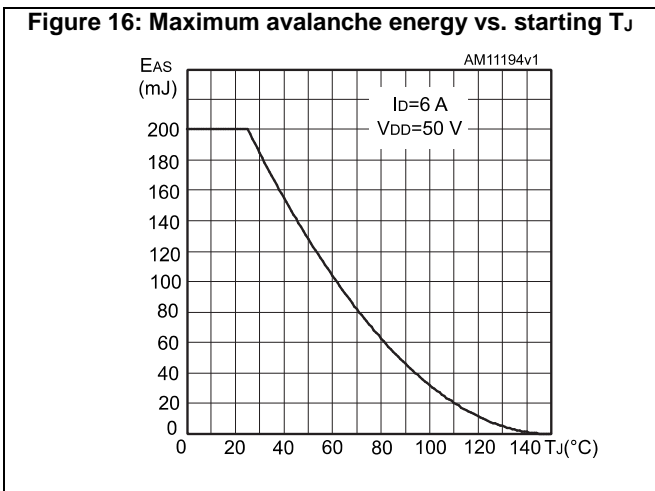
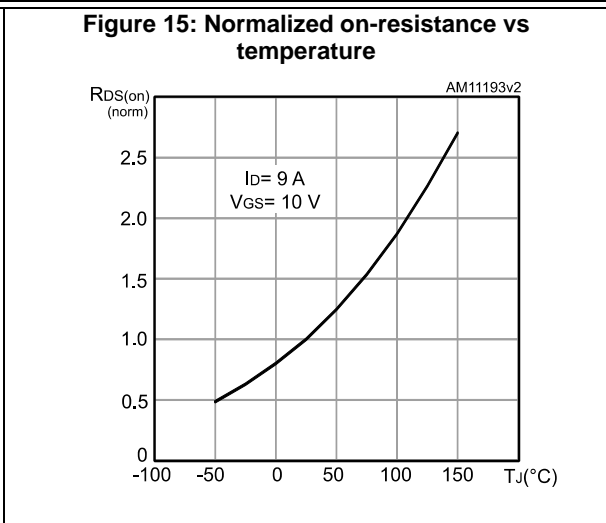
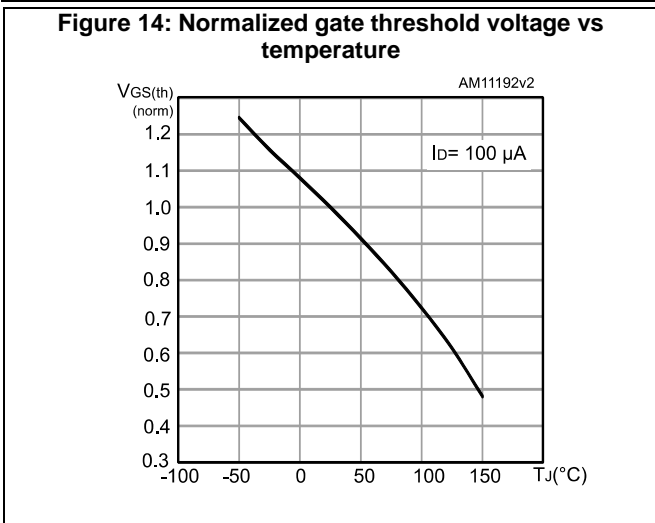
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

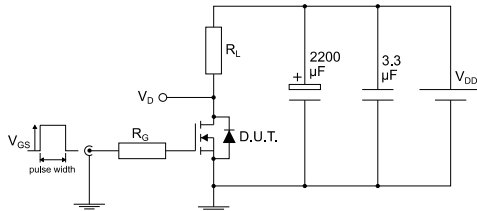






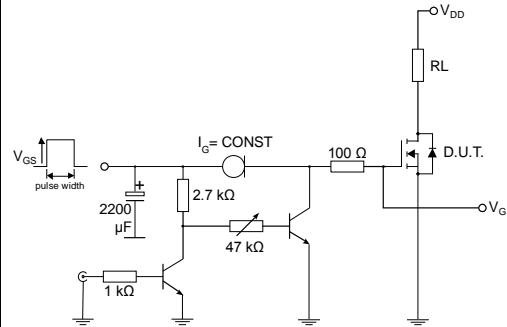
### 3 Test circuits

**Figure 19: Test circuit for resistive load switching times**



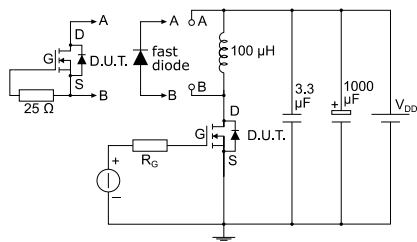
AM01468v1

**Figure 20: Test circuit for gate charge behavior**



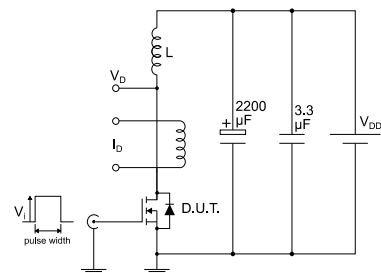
AM01469v10

**Figure 21: Test circuit for inductive load switching and diode recovery times**



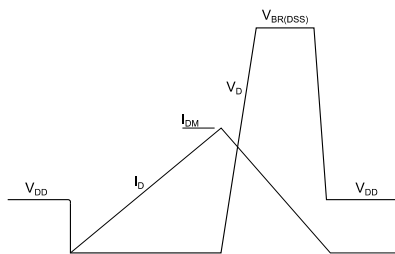
AM01470v1

**Figure 22: Unclamped inductive load test circuit**



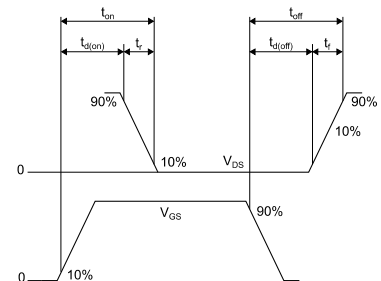
AM01471v1

**Figure 23: Unclamped inductive waveform**



AM01472v1

**Figure 24: Switching time waveform**



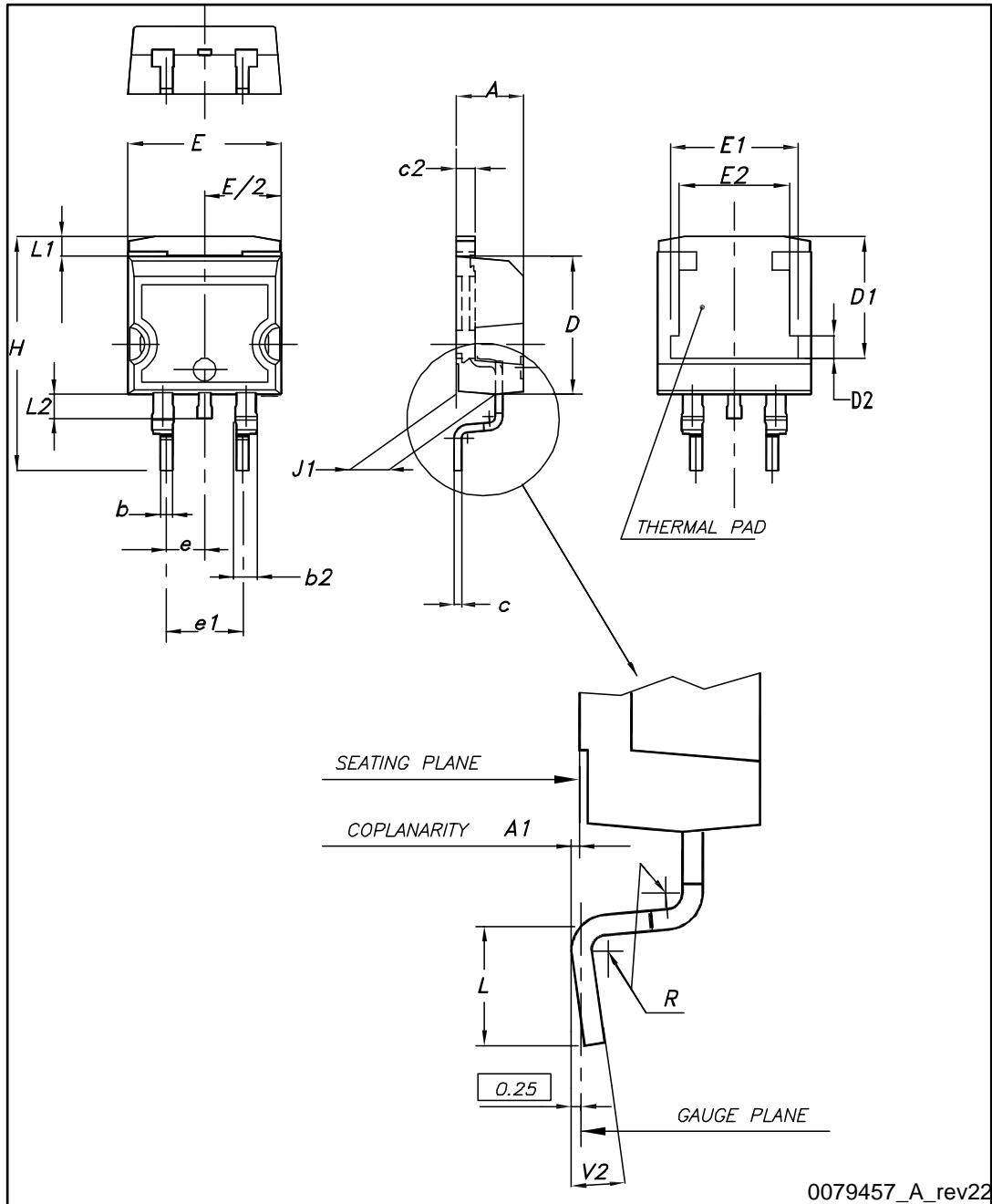
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 D<sup>2</sup>PAK package information

Figure 25: D<sup>2</sup>PAK (TO-263) type A package outline

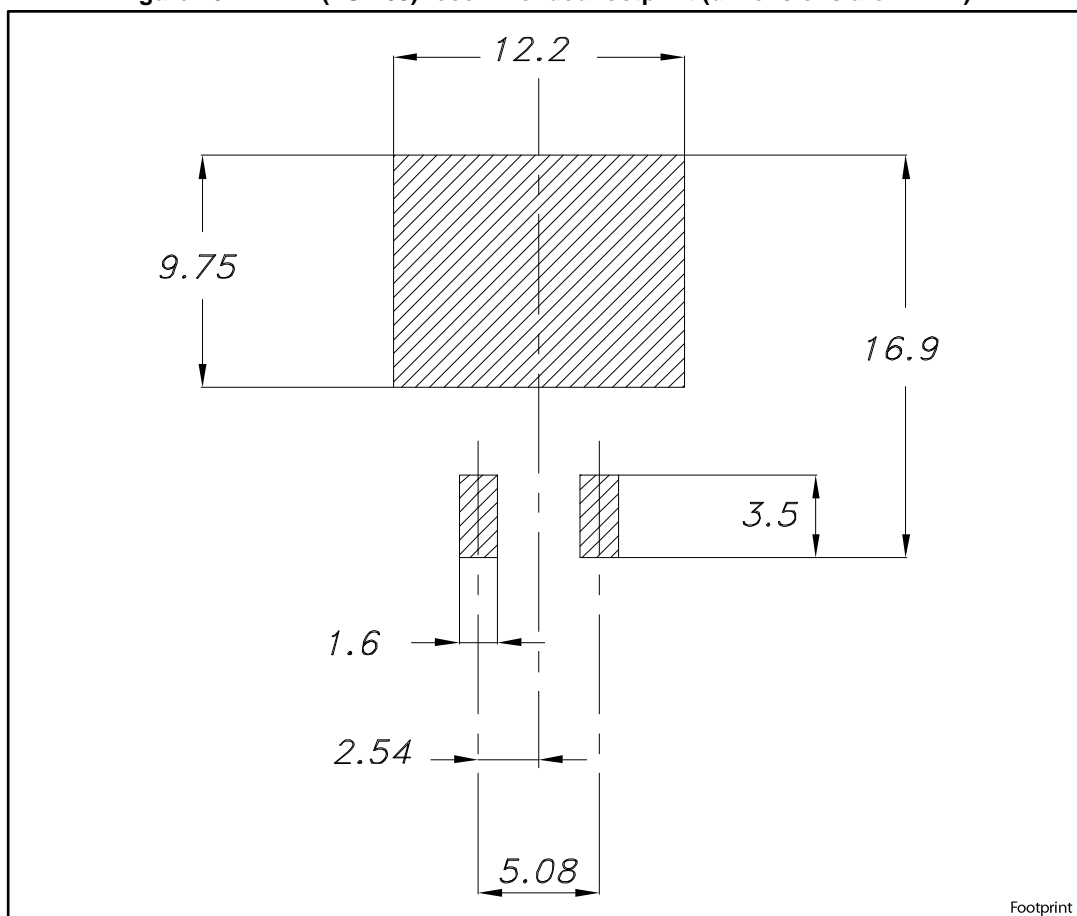


0079457\_A\_rev22

Table 10: D<sup>2</sup>PAK (TO-263) type A package mechanical data

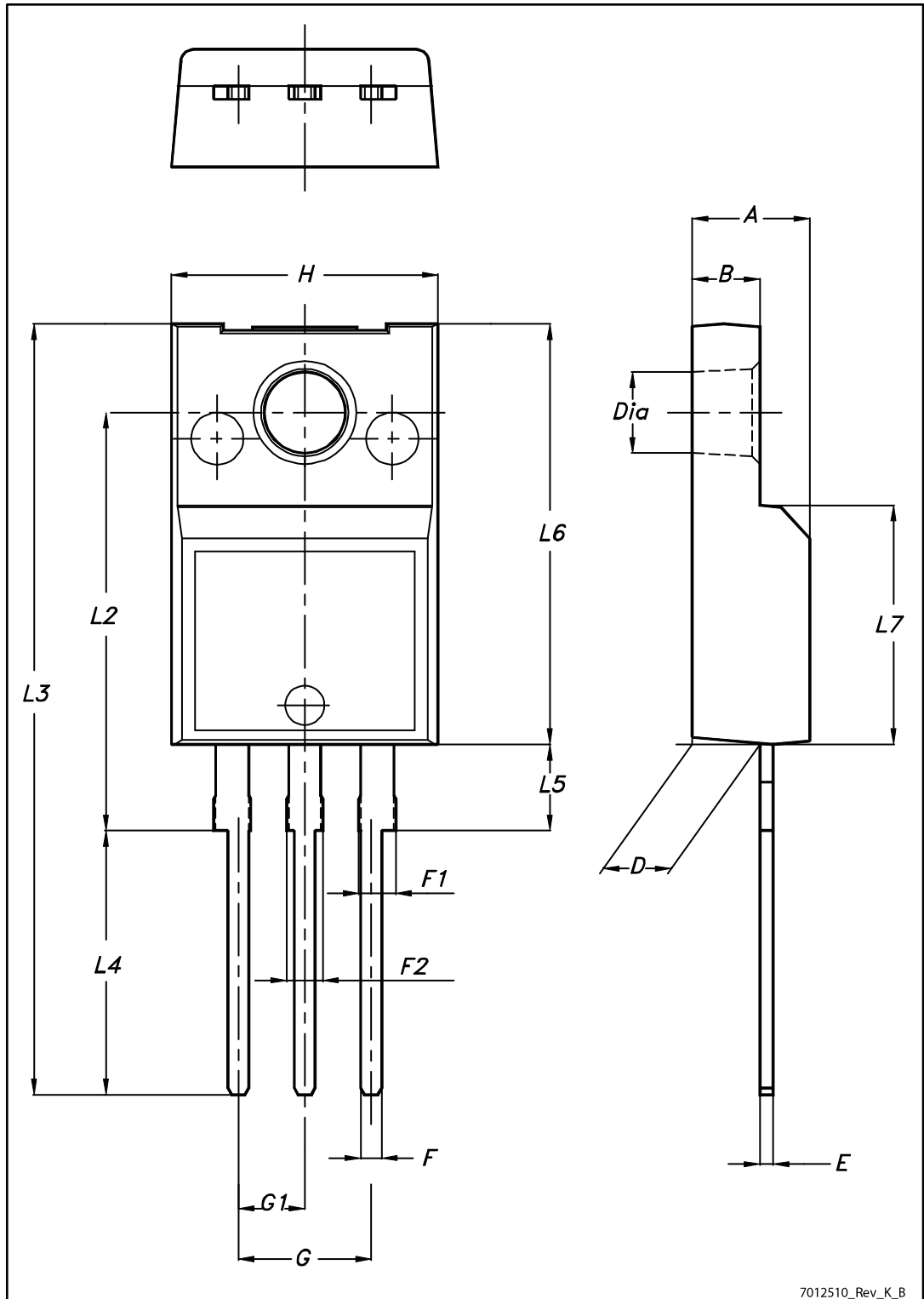
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 26: D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)



### 4.2 TO-220FP package information

Figure 27: TO-220FP package outline



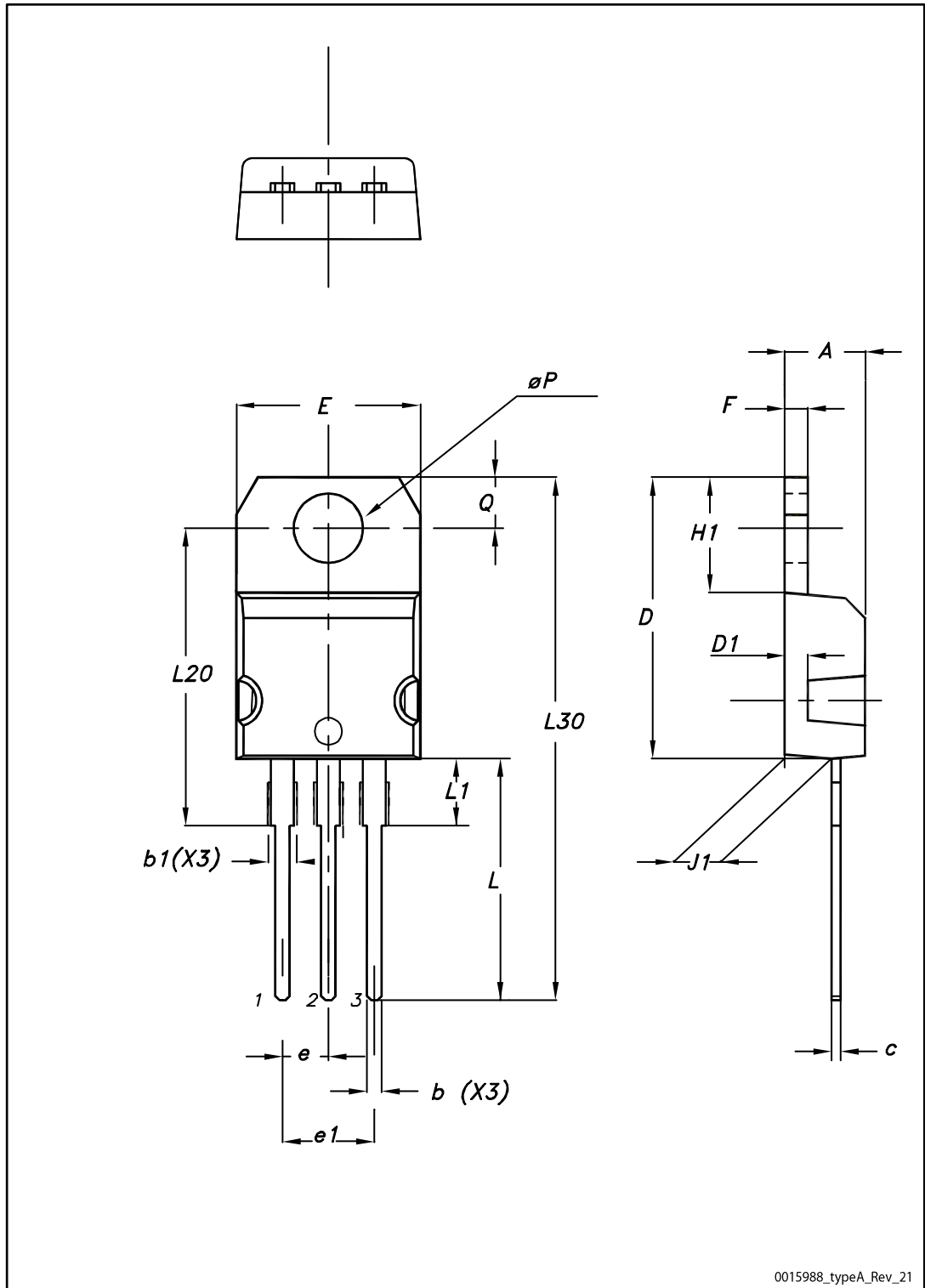
7012510\_Rev\_K\_B

Table 11: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

### 4.3 TO-220 type A package information

Figure 28: TO-220 type A package outline



0015988\_typeA\_Rev\_21

Table 12: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

### 4.4 TO-247 package information

Figure 29: TO-247 package outline

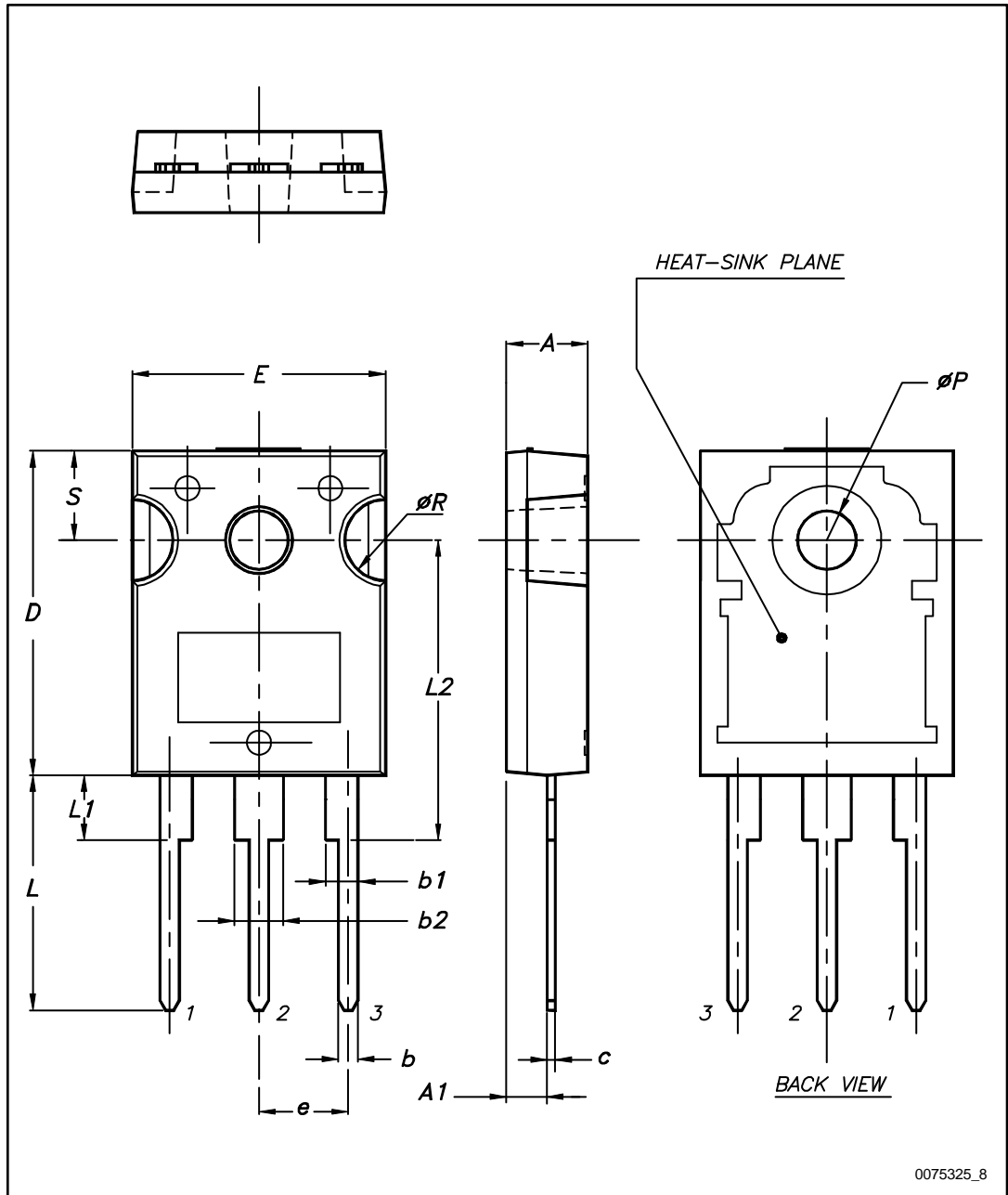


Table 13: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

### 4.5 D<sup>2</sup>PAK packing information

Figure 30: Tape outline

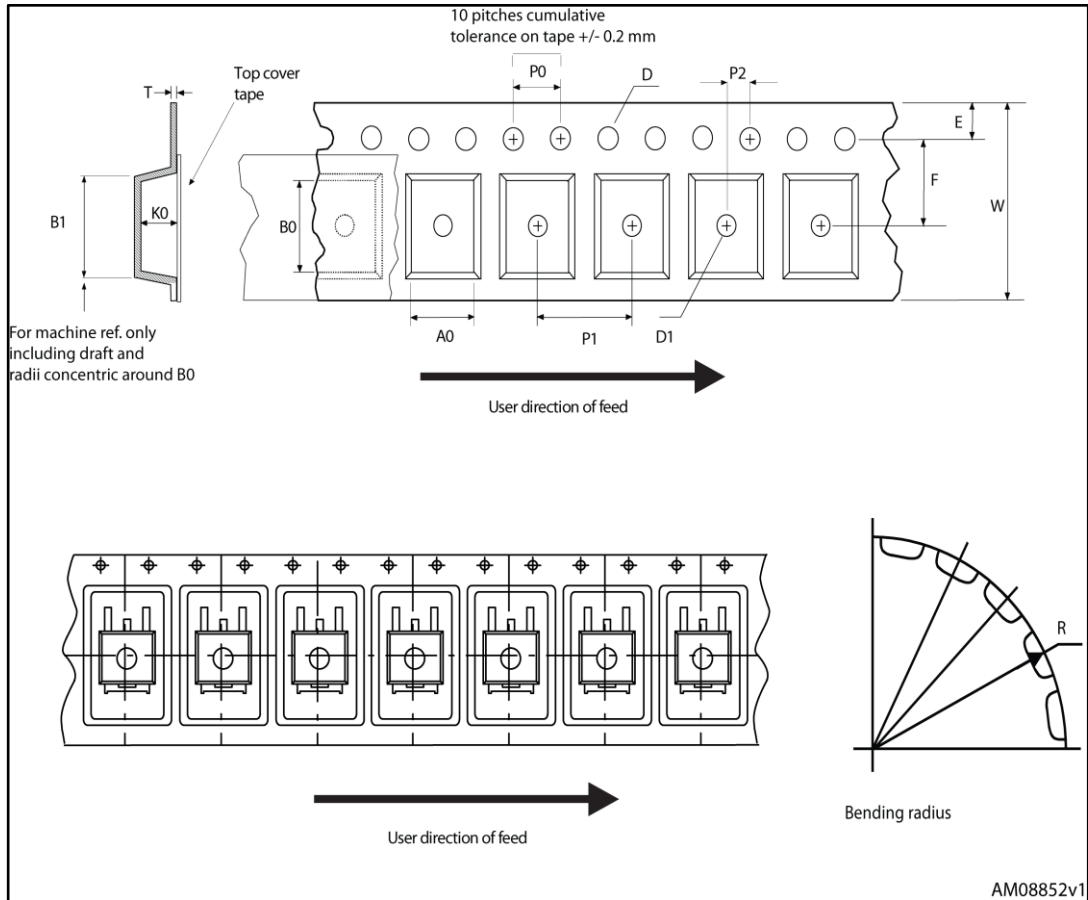


Figure 31: Reel outline

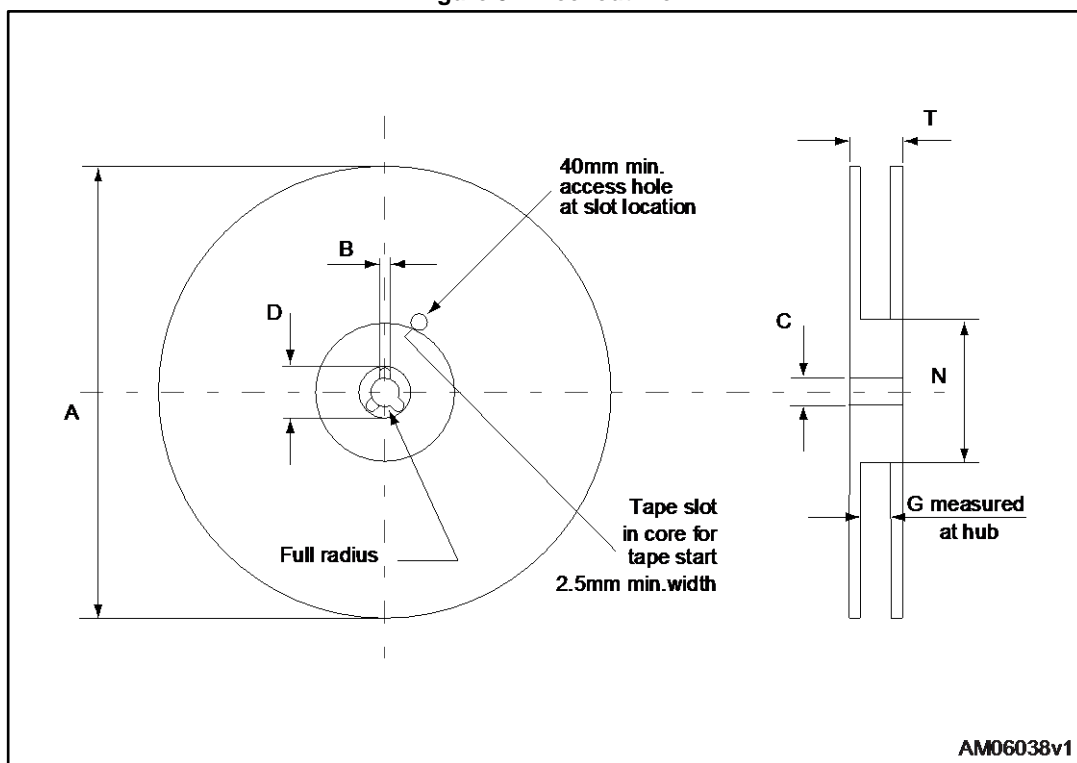


Table 14: D<sup>2</sup>PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 5 Revision history

Table 15: Document revision history

Date	Revision	Changes
25-Nov-2009	1	First release.
12-Jan-2010	2	Corrected $V_{GS}$ value in <i>Table 2: Absolute maximum ratings</i> .
22-Dec-2011	3	Inserted device in D <sup>2</sup> PAK. Document status promoted from preliminary data to datasheet. Added: <i>Section 2.1: Electrical characteristics (curves)</i> Updated <i>Section 4: Package mechanical data</i> . Added <i>Section 5: Packaging mechanical data</i> . Minor text changes.
06-Jun-2012	4	<i>Figure 9: Transfer characteristics</i> has been updated.
16-Jan-2017	5	Updated title, features, description and schematic diagram in cover page. Minor text changes in <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Updated <i>Section 2.1: "Electrical characteristics (curves)"</i> Updated package information section.

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved






## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View STF20N95K5 on WIN SOURCE](#)

 [STMicroelectronics](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management