



# THE DATASHEET OF A6595KA



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## *8-Bit Serial Input DMOS Power Driver*

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### **Discontinued Product**

These parts are no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: May 3, 2010

#### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, refer to your Allegro sales representative.*

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NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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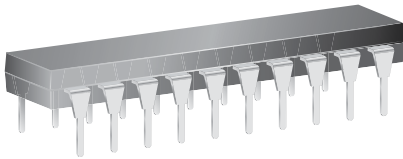
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## 8-Bit Serial Input DMOS Power Driver

### Features and Benefits

- 50 V minimum output clamp voltage
- 250 mA output current (all outputs simultaneously)
- 1.3  $\Omega$  typical  $r_{DS(on)}$
- Low power consumption
- Replacements for TPIC6595N and TPIC6595DW

### Package: 20-pin DIP (suffix A)



Not to scale

### Description

The A6595 combines an 8-bit CMOS shift register and accompanying data latches, control circuitry, and DMOS power driver outputs. Power driver applications include relays, solenoids, and other medium-current or high-voltage peripheral power loads.

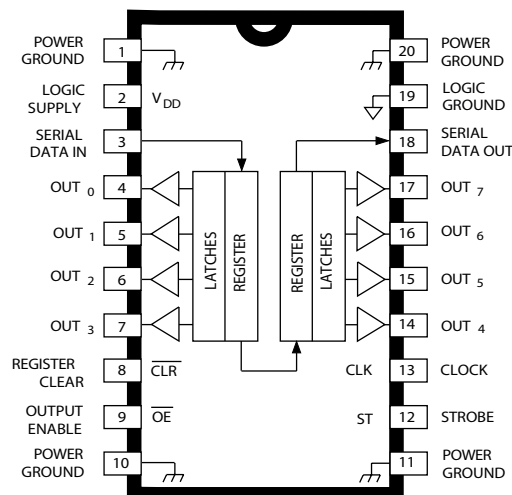
The serial-data input, CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Serial-data input rates are over 5 MHz. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial-data output enables cascade connections in applications requiring additional drive lines.

The A6595 DMOS open-drain outputs are capable of sinking up to 750 mA. All of the output drivers are disabled (the DMOS sink drivers turned off) by the OUTPUT ENABLE input high.

The A6595 is furnished in a 20-pin dual in-line plastic package that is lead (Pb) free, with 100% matte tin leadframe plating. Copper leadframe base material, reduced supply current requirements, and low on-state resistance allow the device to sink 150 mA from all outputs continuously, to ambient temperatures to 125°C.

### Pin-out Diagram



## Selection Guide

Part Number	Packing
A6595KA-T	18 pieces per tube

## Absolute Maximum Ratings\*

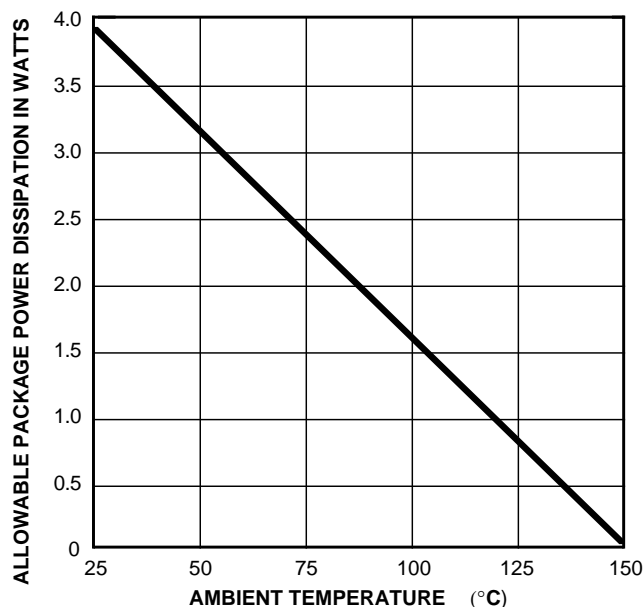
Characteristic	Symbol	Notes	Rating	Units
Logic Supply Voltage	$V_{DD}$		7.0	V
Input Voltage Range	$V_I$		-0.3 to 7.0	V
Output Voltage	$V_O$		50	V
Output Drain Current	$I_O$	Continuous, each output, all outputs on	250	mA
	$I_{OM}$	Pulsed $t_w \leq 100 \mu s$ , duty cycle $\leq 2\%$ ; each output, all outputs on	750	mA
		Pulsed $t_w \leq 100 \mu s$ , duty cycle $\leq 2\%$ ;	2.0	A
Single-Pulse Avalanche Energy	$E_{AS}$		75	mJ
Operating Ambient Temperature	$T_A$	Range K	-40 to 125	$^{\circ}C$
Maximum Junction Temperature	$T_J(max)$		150	$^{\circ}C$
Storage Temperature	$T_{stg}$		-55 to 150	$^{\circ}C$

\*These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.

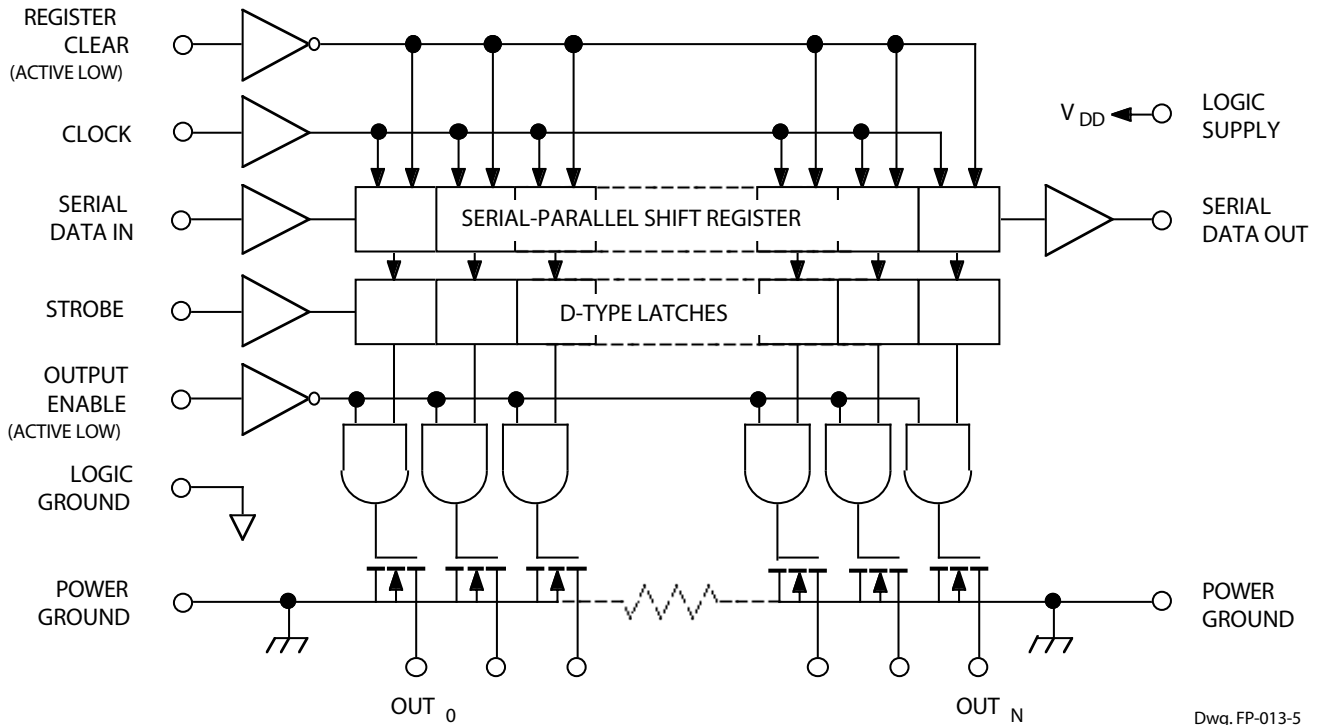
**Thermal Characteristics** may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	32	$^{\circ}C/W$

\*Additional thermal information available on the Allegro website.

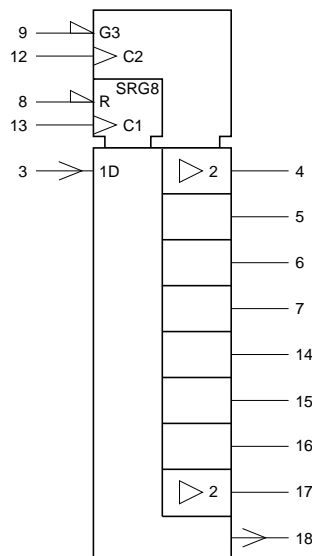


**Functional Block Diagram**



Grounds (terminals 1, 10, 11, 19, and 20) must be connected together externally.

**Device Logic Diagram**





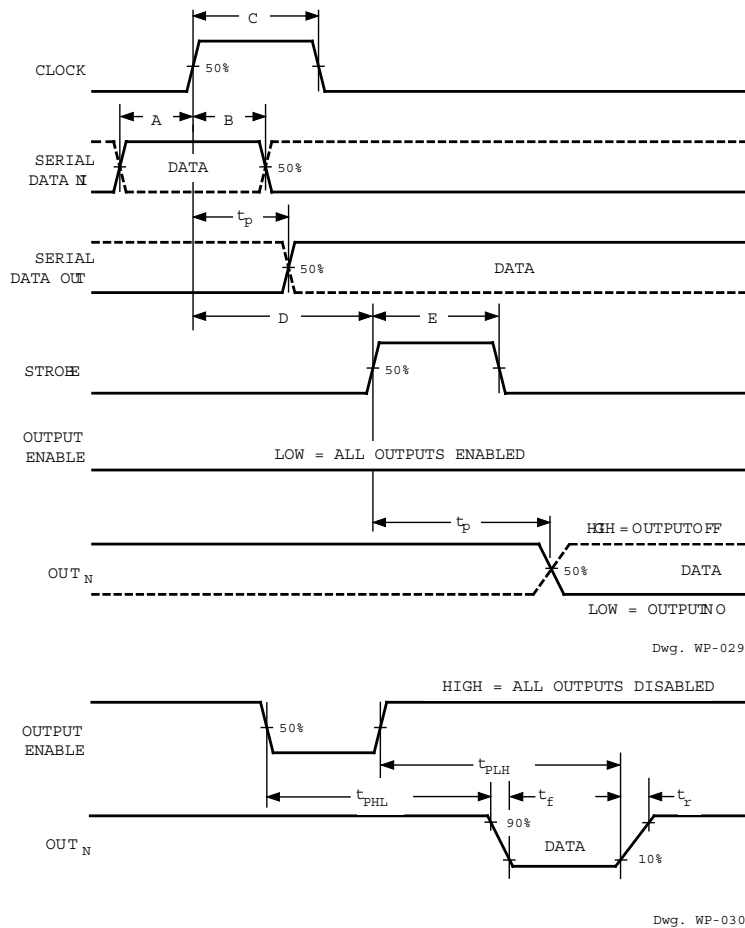
**ELECTRICAL CHARACTERISTICS at  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$ ,  $t_{ir} = t_{if} \leq 10\text{ ns}$  (unless otherwise specified).**

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Breakdown Voltage	$V_{(BR)DSX}$	$I_O = 1\text{ mA}$	50	—	—	V
Off-State Output Current	$I_{DSX}$	$V_O = 40\text{ V}$	—	0.05	1.0	$\mu\text{A}$
		$V_O = 40\text{ V}$ , $T_A = 125^\circ\text{C}$	—	0.15	5.0	$\mu\text{A}$
Static Drain-Source On-State Resistance	$r_{DS(on)}$	$I_O = 250\text{ mA}$ , $V_{DD} = 4.5\text{ V}$	—	1.3	2.0	$\Omega$
		$I_O = 250\text{ mA}$ , $V_{DD} = 4.5\text{ V}$ , $T_A = 125^\circ\text{C}$	—	2.0	3.2	$\Omega$
		$I_O = 500\text{ mA}$ , $V_{DD} = 4.5\text{ V}$ (see note)	—	1.3	2.0	$\Omega$
Nominal Output Current	$I_{ON}$	$V_{DS(on)} = 0.5\text{ V}$ , $T_A = 85^\circ\text{C}$	—	250	—	mA
Logic Input Current	$I_{IH}$	$V_I = V_{DD} = 5.5\text{ V}$	—	—	1.0	$\mu\text{A}$
	$I_{IL}$	$V_I = 0$ , $V_{DD} = 5.5\text{ V}$	—	—	-1.0	$\mu\text{A}$
Logic Input Hysteresis	$V_{I(hys)}$		—	1.3	—	V
SERIAL-DATA Output Voltage	$V_{OH}$	$I_{OH} = -20\text{ }\mu\text{A}$ , $V_{DD} = 4.5\text{ V}$	4.4	4.49	—	V
		$I_{OH} = -4\text{ mA}$ , $V_{DD} = 4.5\text{ V}$	4.1	4.3	—	V
	$V_{OL}$	$I_{OL} = 20\text{ }\mu\text{A}$ , $V_{DD} = 4.5\text{ V}$	—	0.002	0.1	V
		$I_{OL} = 4\text{ mA}$ , $V_{DD} = 4.5\text{ V}$	—	0.2	0.4	V
Prop. Delay Time	$t_{PLH}$	$I_O = 250\text{ mA}$ , $C_L = 30\text{ pF}$	—	650	—	ns
	$t_{PHL}$	$I_O = 250\text{ mA}$ , $C_L = 30\text{ pF}$	—	150	—	ns
Output Rise Time	$t_r$	$I_O = 250\text{ mA}$ , $C_L = 30\text{ pF}$	—	7500	—	ns
Output Fall Time	$t_f$	$I_O = 250\text{ mA}$ , $C_L = 30\text{ pF}$	—	425	—	ns
Supply Current	$I_{DD(OFF)}$	All inputs low	—	15	100	$\mu\text{A}$
	$I_{DD(ON)}$	$V_{DD} = 5.5\text{ V}$ , Outputs on	—	150	300	$\mu\text{A}$
	$I_{DD(fclk)}$	$f_{clk} = 5\text{ MHz}$ , $C_L = 30\text{ pF}$ , Outputs off	—	0.6	5.0	mA

Typical Data is at  $V_{DD} = 5\text{ V}$  and is for design information only.

NOTE — Pulse test, duration  $\leq 100\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

**TIMING REQUIREMENTS and SPECIFICATIONS**  
(Logic Levels are  $V_{DD}$  and Ground)



- A.** Data Active Time Before Clock Pulse  
(Data Set-Up Time),  $t_{su(D)}$  ..... **10 ns**
- B.** Data Active Time After Clock Pulse  
(Data Hold Time),  $t_{h(D)}$  ..... **10 ns**
- C.** Clock Pulse Width,  $t_{w(CLK)}$  ..... **20 ns**
- D.** Time Between Clock Activation  
and Strobe,  $t_{su(ST)}$  ..... **50 ns**
- E.** Strobe Pulse Width,  $t_{w(ST)}$  ..... **50 ns**
- F.** Output Enable Pulse Width,  $t_{w(OE)}$  ..... **4.5  $\mu$ s**

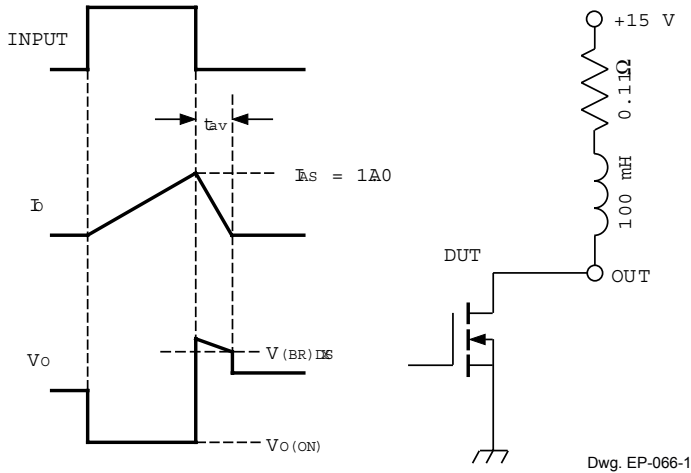
NOTE – Timing is representative of a 12.5 MHz clock.  
Higher speeds are attainable.

Serial data present at the input is transferred to the shift register on the rising edge of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT.

Information present at any register is transferred to the respective latch on the rising edge of the STROBE input pulse (serial-to-parallel conversion).

When the OUTPUT ENABLE input is high, the output source drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

**TEST CIRCUITS**



$$E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{AV}/2$$

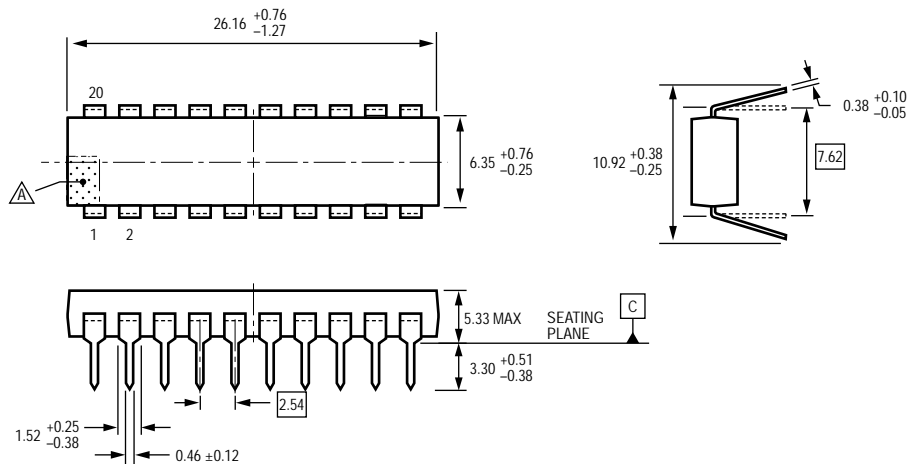
**Single-Pulse Avalanche Energy Test Circuit and Waveforms**

**TERMINAL DESCRIPTIONS**

<b>Terminal No.</b>	<b>Terminal Name</b>	<b>Function</b>
1	POWER GROUND	Reference terminal for output voltage measurements (OUT <sub>0,3</sub> ).
2	LOGIC SUPPLY	(V <sub>DD</sub> ) The logic supply voltage (typically 5 V).
3	SERIAL DATA IN	Serial-data input to the shift-register.
4-7	OUT <sub>0,3</sub>	Current-sinking, open-drain DMOS output terminals.
8	CLEAR	When (active) low, the registers are cleared (set low).
9	OUTPUT ENABLE	When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
10	POWER GROUND	Reference terminal for output voltage measurements (OUT <sub>0,3</sub> ).
11	POWER GROUND	Reference terminal for output voltage measurements (OUT <sub>0,7</sub> ).
12	STROBE	Data strobe input terminal; shift register data is latched on rising edge.
13	CLOCK	Clock input terminal for data shift on rising edge.
14-17	OUT <sub>4,7</sub>	Current-sinking, open-drain DMOS output terminals.
18	SERIAL DATA OUT	CMOS serial-data output to the following shift register.
19	LOGIC GROUND	Reference terminal for input voltage measurements.
20	POWER GROUND	Reference terminal for output voltage measurements (OUT <sub>4,7</sub> ).

NOTE — Grounds (terminals 1, 10, 11, 19, and 20) must be connected together externally.

Package A, 20-Pin DIP



Preliminary dimensions, for reference only  
 Dimensions in inches  
 Metric dimensions (mm) in brackets, for reference only  
 (reference JEDEC MS-001 AD)  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown  
 ⚠ Terminal #1 mark area

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