



**THE DATASHEET OF  
NTQD4154ZR2**



# NTQD4154Z

## Power MOSFET

20 V, 7.5 A, Common-Drain,  
Dual N-Channel TSSOP-8



ON Semiconductor®

<http://onsemi.com>

### Features

- Common Drain for Ease of Circuit Connection
- Low  $R_{DS(on)}$  Extending Battery Life
- ESD Protected Gate
- Pb-Free Package is Available

### Applications

- Li-Ion Battery Protection Circuit
- Power Management in Portable and Battery-Powered Products

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ Max
20 V	15 mΩ @ 4.5 V	7.5 A
	21 mΩ @ 2.5 V	

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

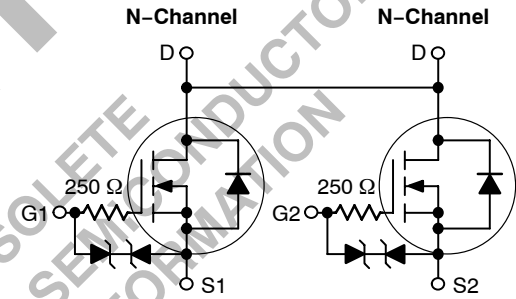
Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		$V_{DSS}$	20	V	
Gate-to-Source Voltage		$V_{GS}$	±12	V	
Continuous Drain Current (Note 1)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	7.5	A
			$T_A = 75^\circ\text{C}$	5.8	
Power Dissipation (Note 1)	$T_A = 25^\circ\text{C}$	$P_D$	1.52	W	
Continuous Drain Current (Note 2)	$t \leq 10$ s	$I_D$	$T_A = 25^\circ\text{C}$	9.8	A
			$T_A = 75^\circ\text{C}$	7.6	
Power Dissipation (Note 2)	$t \leq 10$ s	$P_D$	2.6	W	
Pulsed Drain Current	$t_p = 10$ μs	$I_{DM}$	30	A	
Operating Junction and Storage Temperature		$T_J, T_{STG}$	-55 to 150	°C	
Source Current (Body Diode)		$I_S$	2.2	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	°C	

### THERMAL RESISTANCE RATINGS

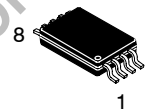
Parameter	Symbol	Max	Units
Junction-to-Ambient – Steady State	$R_{\theta JA}$	82	°C/W
Junction-to-Ambient – $t \leq 10$ s	$R_{\theta JA}$	48	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

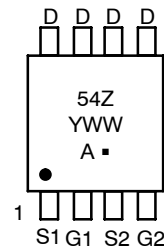
1. Mounted onto a 2" square FR-4 board (1 in sq, 2 oz. cu. 0.06" thick single-sided), steady state.
2. Mounted onto a 2" square FR-4 board (1 in sq, 2 oz. cu. 0.06" thick single-sided),  $t \leq 10$  s.



### MARKING DIAGRAM & PIN ASSIGNMENT



TSSOP-8  
CASE 948S  
PLASTIC



- 54Z = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NTQD4154ZR2	TSSOP-8	4000 / Tape & Reel
NTQD4154ZR2G	TSSOP-8 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTQD4154Z

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			12		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 16 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 125°C		25	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±4.5 V			±1.0	μA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	0.6		1.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			4.1		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7.5 A		15	19	mΩ
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 5.5 A		21	26	
Forward Transconductance	g <sub>FS</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.5 A		46		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 16 V		1485		pF
Output Capacitance	C <sub>OSS</sub>			220		
Reverse Transfer Capacitance	C <sub>RSS</sub>			175		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7.5 A		21.5		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			4.0		
Gate-to-Source Charge	Q <sub>GS</sub>			6.0		
Gate-to-Drain Charge	Q <sub>GD</sub>			5.5		

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 10 V, I <sub>D</sub> = 7.5 A, R <sub>G</sub> = 6.0 Ω		0.2		μs
Rise Time	t <sub>r</sub>			0.5		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			1.12		
Fall Time	t <sub>f</sub>			0.86		

### DRAIN-SOURCE DIODE CHARACTERISTICS (Note 3)

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 6.5 A	T <sub>J</sub> = 25°C		0.8	1.2	V
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>SD</sub> /dt = 100 A/μs, I <sub>S</sub> = 6.5 A			1.02		μs
	t <sub>a</sub>			0.32			
	t <sub>b</sub>			0.7			
	Q <sub>RR</sub>				11.6		μC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

# NTQD4154Z

## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

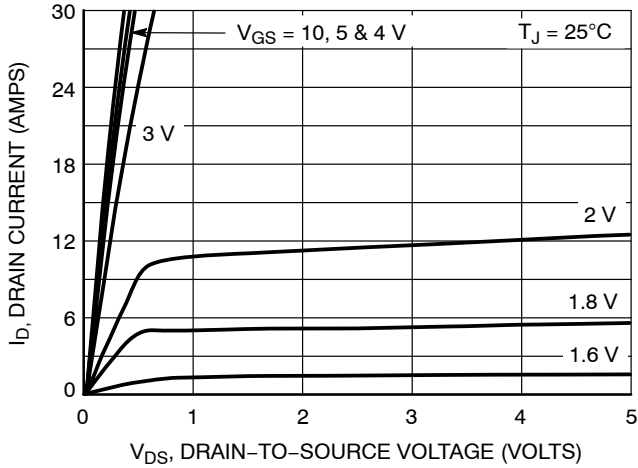


Figure 1. On-Region Characteristics

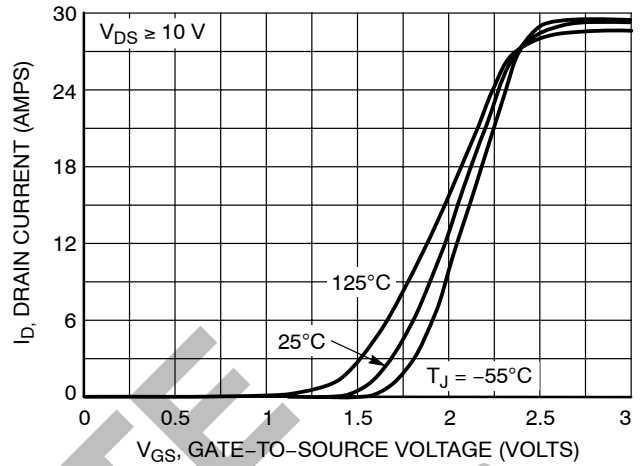


Figure 2. Transfer Characteristics

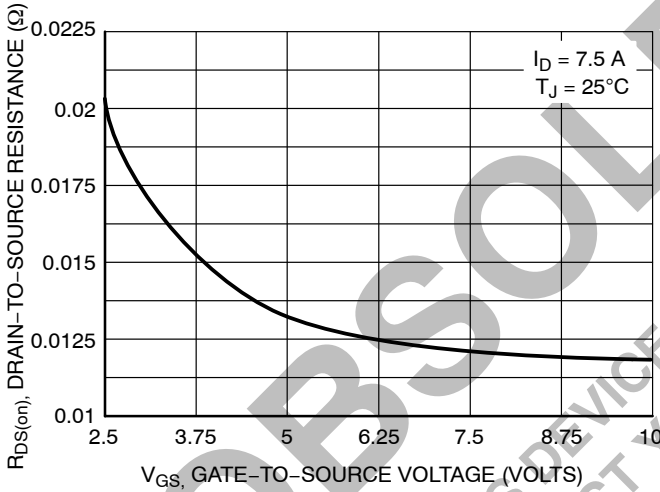


Figure 3. On-Resistance vs. Gate-to-Source Voltage

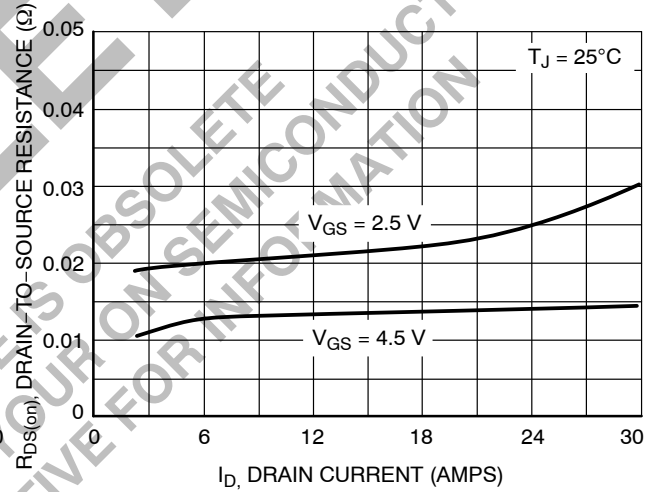


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

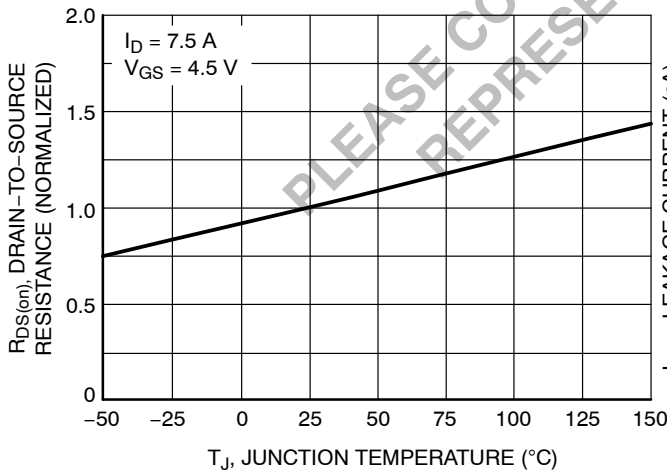


Figure 5. On-Resistance Variation with Temperature

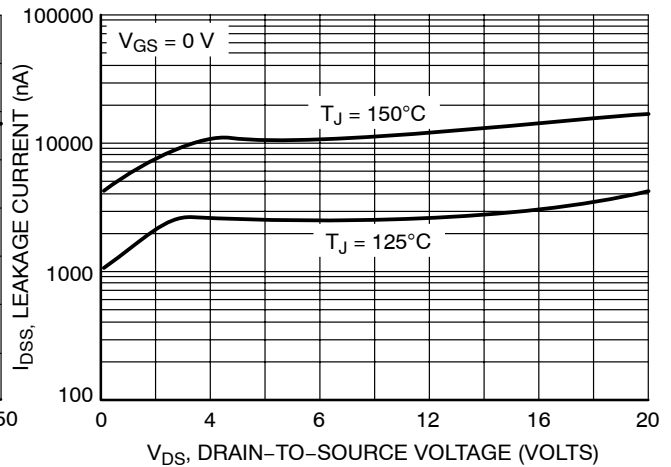


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

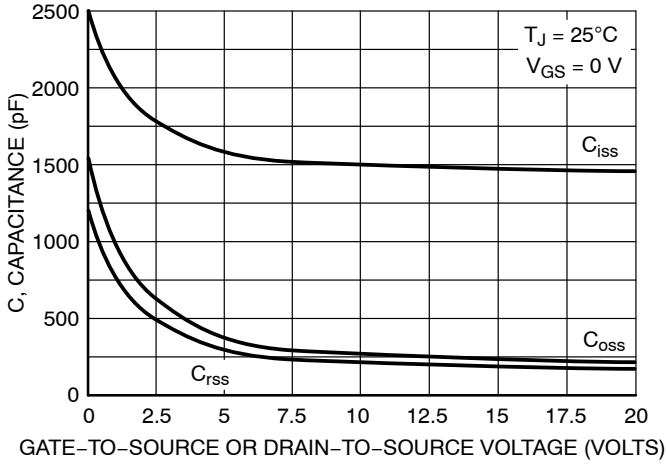


Figure 7. Capacitance Variation

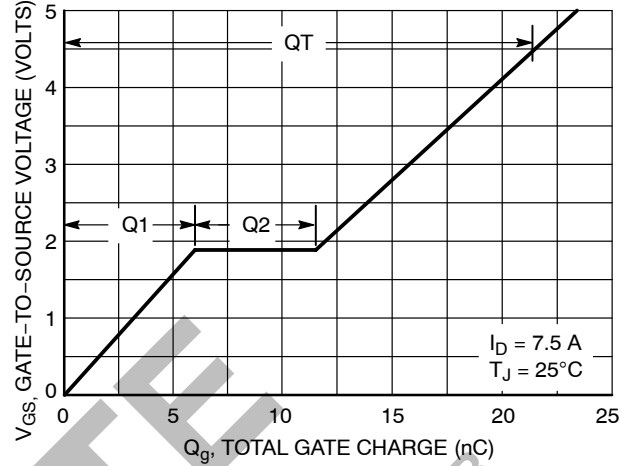


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

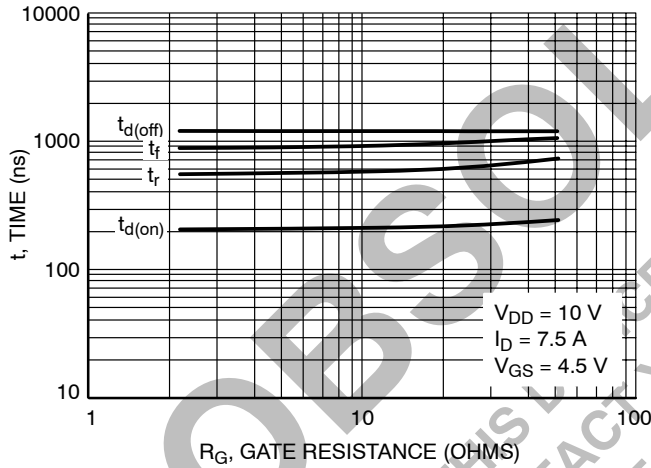


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

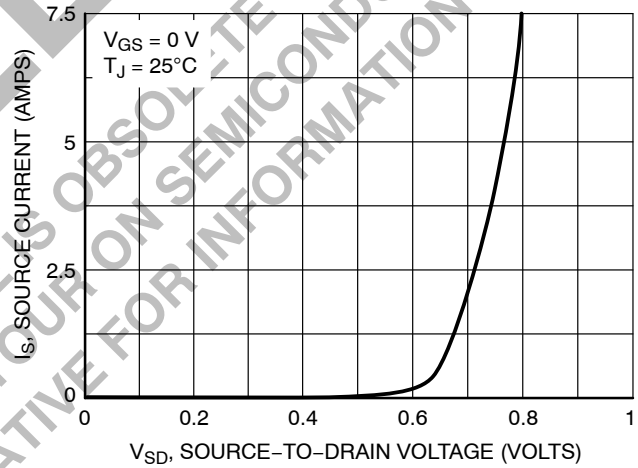


Figure 10. Diode Forward Voltage vs. Current

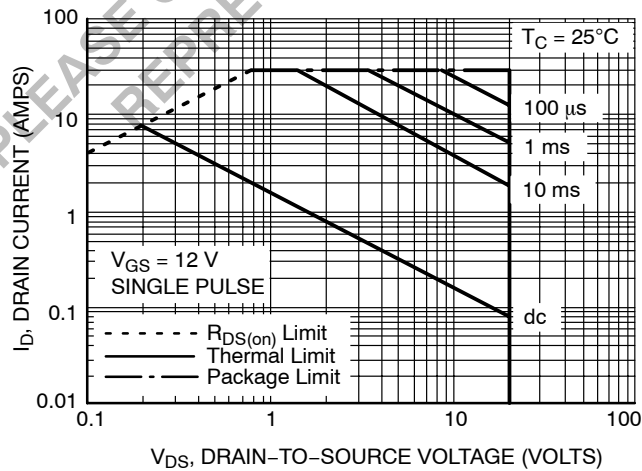
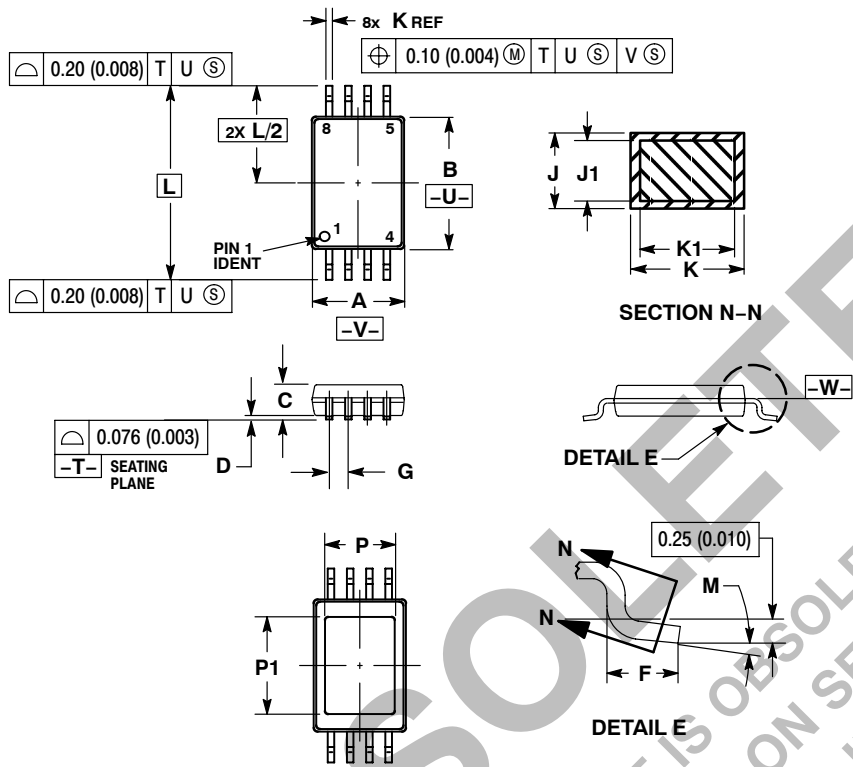


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTQD4154Z

## PACKAGE DIMENSIONS

TSSOP-8  
CASE 948S-01  
ISSUE A

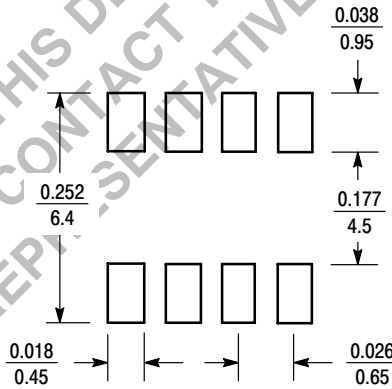


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°
P	---	2.20	---	0.087
P1	---	3.20	---	0.126


### SOLDERING FOOTPRINT\*



(inches)  
mm

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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