



**THE DATASHEET OF
SNJ5428J**



SN5428, SN54LS28, SN7428, SN74LS28 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

SDLS094 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input NOR buffer gates.

The SN5428, and SN54LS28 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7428, and SN74LS28 are characterized for operation from 0°C to 70°C .

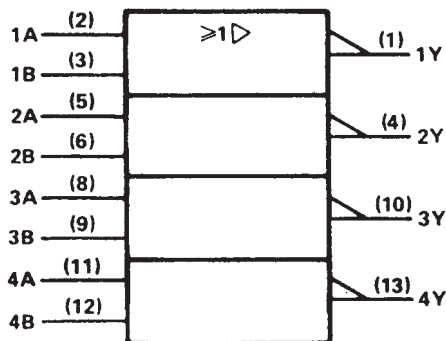
FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

positive logic

$$Y = \overline{A + B} \text{ or } Y = \overline{A} \cdot \overline{B}$$

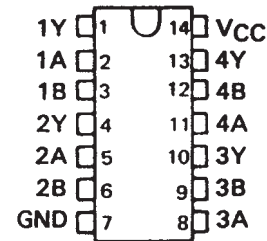
logic symbol†



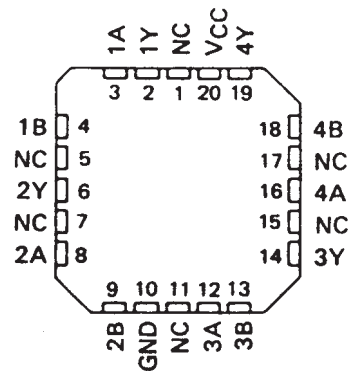
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN5428, SN54LS28 . . . J OR W PACKAGE
SN7428 . . . N PACKAGE
SN74LS28 . . . D OR N PACKAGE
(TOP VIEW)

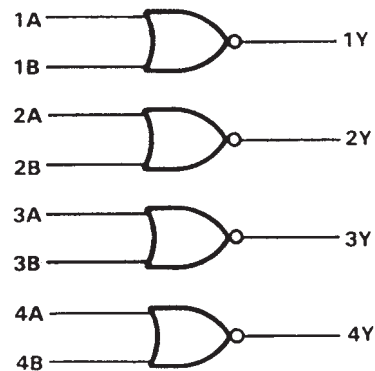


SN54LS28 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

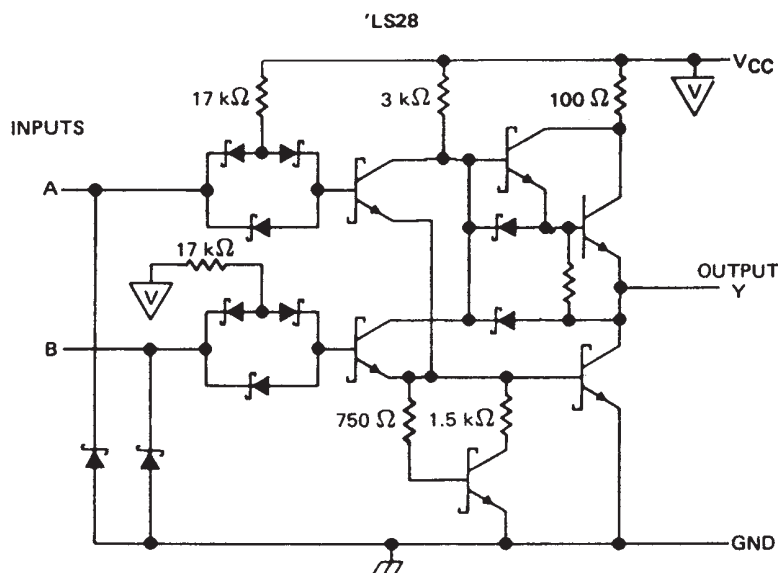
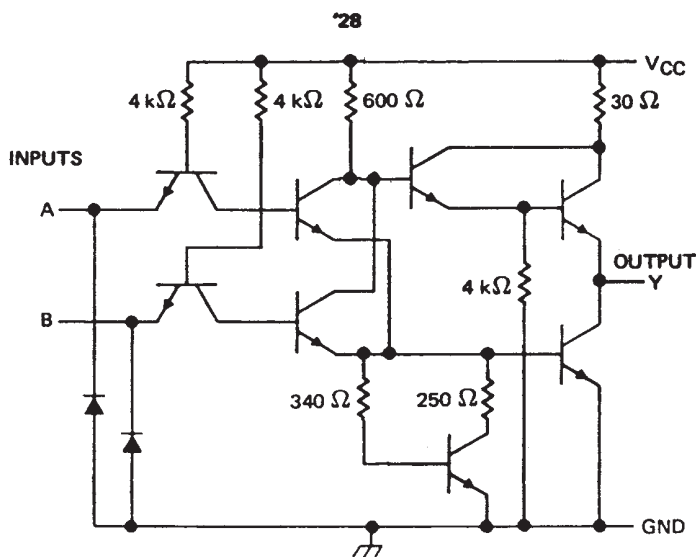
logic diagram



SN5428, SN54LS28, SN7428, SN74LS28 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

SDLS094 – DECEMBER 1983 – REVISED MARCH 1988

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '28	5.5 V
'LS28	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



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SN5428, SN54LS28, SN7428, SN74LS28 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

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recommended operating conditions

	SN5428			SN7428			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			-2.4			-2.4	mA
I _{OL} Low-level output current			48			48	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
V _{IK}	V _{CC} = MIN, I _I = -12mA			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -2.4 mA	2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 48 mA		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-1.6	mA
I _{OS} §	V _{CC} = MAX	-70		-180	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		12	21	mA
I _{CCL}	V _{CC} = MAX, See Note 2		33	57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 133 Ω, C _L = 50 pF	6	9		ns
t _{PHL}				8	12		ns
t _{PLH}			R _L = 133 Ω, C _L = 150 pF	10	15		ns
t _{PHL}				12	18		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN5428, SN54LS28, SN7428, SN74LS28 QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

SDLS094 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

	SN54LS28			SN74LS28			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.7			0.8	V
I _{OH} High-level output current			-1.2			-1.2	mA
I _{OL} Low-level output current			12			24	mA
T _A Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS28			SN74LS28			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = -1.2 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 12 mA		0.25	0.4		0.24	0.4	V
	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 24 mA					0.35	0.5	
I _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA
I _{OS} §	V _{CC} = MAX	-30		-130	-30		-130	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		1.8	3.6		1.8	3.6	mA
I _{CCL}	V _{CC} = MAX, See Note 2		6.9	13.8		6.9	13.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	Y	R _L = 667 Ω, C _L = 45 pF		12	24	ns
t _{PHL}					12	24	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN5428J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN5428J	Samples
SNJ5428J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ5428J	Samples
SNJ5428J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ5428J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

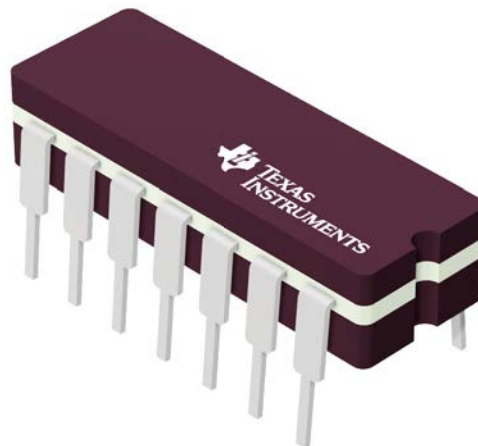
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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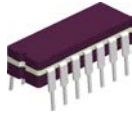
GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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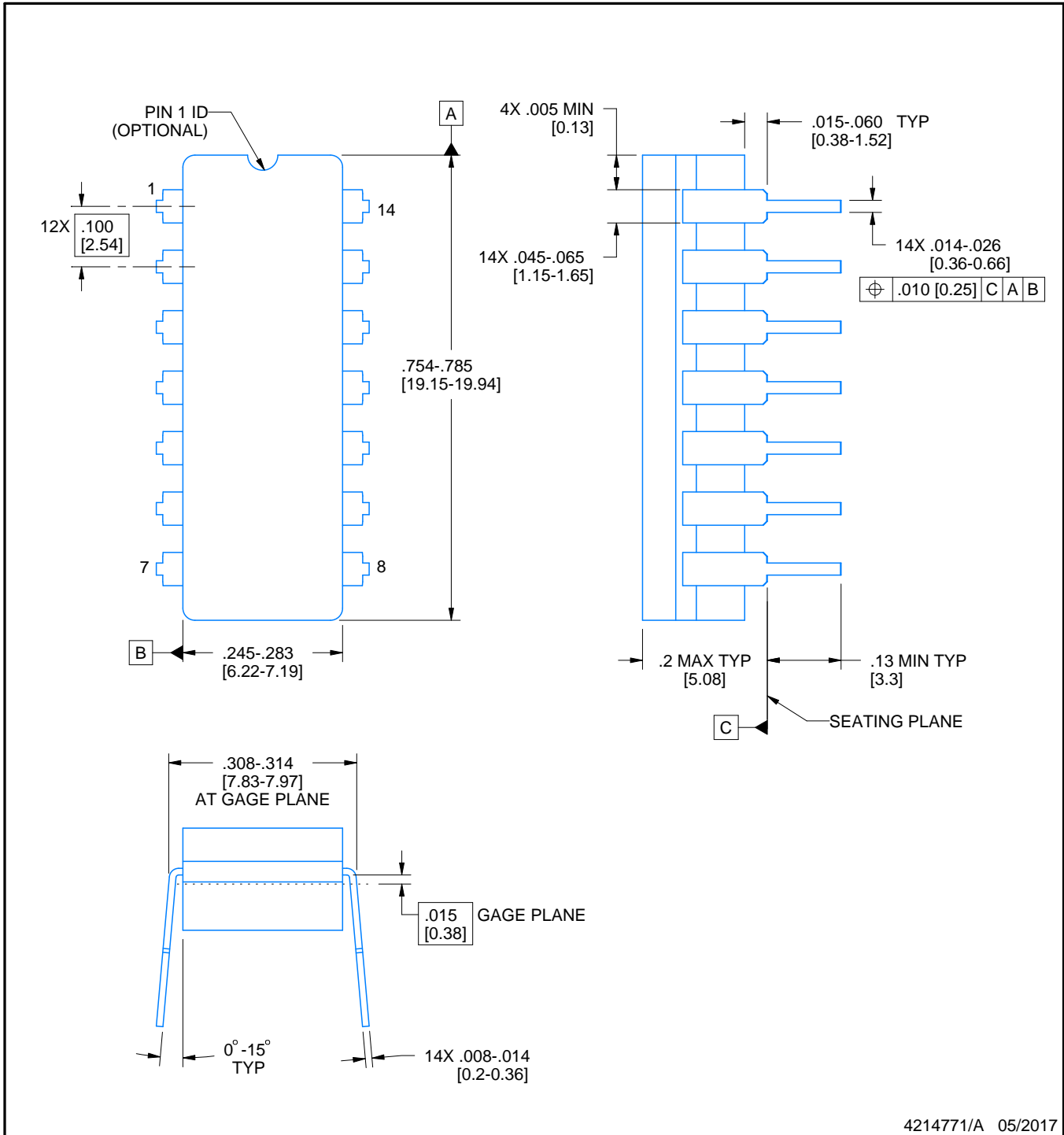
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PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

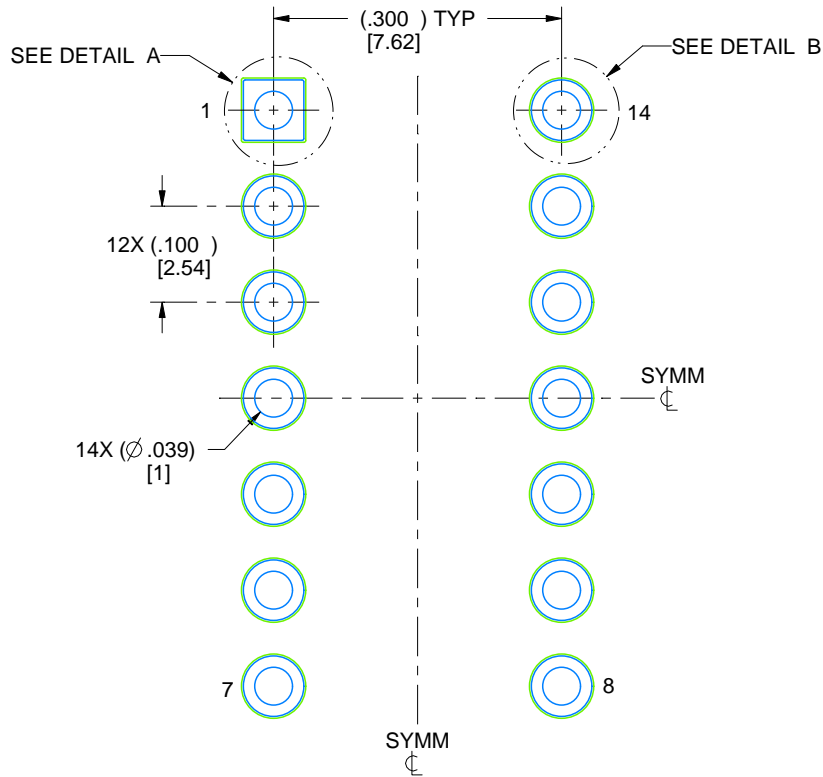
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

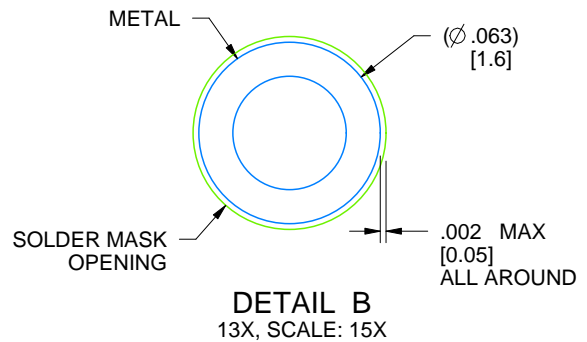
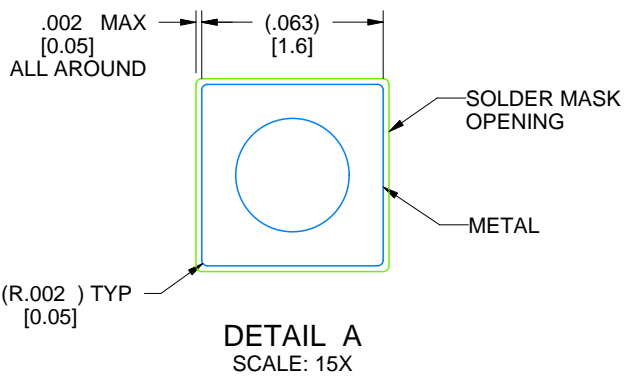
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CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



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