

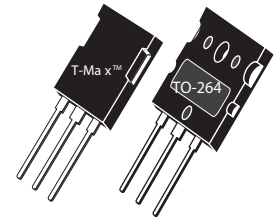


**THE DATASHEET OF
APT66F60B2**



N-Channel FREDFET

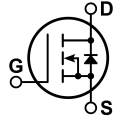
Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. A proprietary planar stripe design yields excellent reliability and manufacturability. Low switching loss is achieved with low input capacitance and ultra low C_{rss} "Miller" capacitance. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control slew rates during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency. Reliability in flyback, boost, forward, and other circuits is enhanced by the high avalanche energy capability.




APT66F60B2

APT66F60L

Single die FREDFET



FEATURES

- Fast switching with low EMI
- Low t_{rr} for high reliability
- Ultra low C_{rss} for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant 

TYPICAL APPLICATIONS

- ZVS phase shifted and other full bridge
- Half bridge
- PFC and other boost converter
- Buck converter
- Single and two switch forward
- Flyback

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	70	A
	Continuous Drain Current @ $T_C = 100^\circ\text{C}$	44	
I_{DM}	Pulsed Drain Current ^①	245	
V_{GS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy ^②	1845	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	33	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$			1135	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.11	°C/W
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.11		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	°C
T_L	Soldering Temperature for 10 Seconds (1.6mm from case)			300	
W_T	Package Weight		0.22		oz
			6.2		g
Torque	Mounting Torque (TO-264 Package), 4-40 or M3 screw			10	in·lbf
				1.1	N·m

Static Characteristics
T_J = 25°C unless otherwise specified
APT66F60B2_L

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{BR(DSS)}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	600			V
ΔV _{BR(DSS)} /ΔT _J	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D = 250μA		0.57		V/°C
R _{DS(on)}	Drain-Source On Resistance ^③	V _{GS} = 10V, I _D = 33A		0.075	0.09	Ω
V _{GS(th)}	Gate-Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 2.5mA	2.5	4	5	V
ΔV _{GS(th)} /ΔT _J	Threshold Voltage Temperature Coefficient			-10		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600V V _{GS} = 0V			250 1000	μA
I _{GSS}	Gate-Source Leakage Current	V _{GS} = ±30V			±100	nA

Dynamic Characteristics
T_J = 25°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g _{fs}	Forward Transconductance	V _{DS} = 50V, I _D = 33A		65		S
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 25V f = 1MHz		13190		pF
C _{rss}	Reverse Transfer Capacitance			135		
C _{oss}	Output Capacitance			1210		
C _{o(cr)} ^④	Effective Output Capacitance, Charge Related	V _{GS} = 0V, V _{DS} = 0V to 400V		645		pF
C _{o(er)} ^⑤	Effective Output Capacitance, Energy Related			335		
Q _g	Total Gate Charge	V _{GS} = 0 to 10V, I _D = 33A, V _{DS} = 300V		330		nC
Q _{gs}	Gate-Source Charge			70		
Q _{gd}	Gate-Drain Charge			140		
t _{d(on)}	Turn-On Delay Time	Resistive Switching V _{DD} = 400V, I _D = 33A R _G = 2.2Ω ^⑥ , V _{GG} = 15V		75		ns
t _r	Current Rise Time			85		
t _{d(off)}	Turn-Off Delay Time			225		
t _f	Current Fall Time			70		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			70	A
I _{SM}	Pulsed Source Current (Body Diode) ^①		246			
V _{SD}	Diode Forward Voltage	I _{SD} = 33A, T _J = 25°C, V _{GS} = 0V			1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} = 33A ^③ V _{DD} = 100V di _{SD} /dt = 100A/μs	T _J = 25°C	268	310	ns
			T _J = 125°C	474	570	
Q _{rr}	Reverse Recovery Charge		T _J = 25°C	1.6		μC
			T _J = 125°C	4.2		
I _{rrm}	Reverse Recovery Current		T _J = 25°C	11.4		A
		T _J = 125°C	16.9			
dv/dt	Peak Recovery dv/dt	I _{SD} ≤ 33A, di/dt ≤ 1000A/μs, V _{DD} = 400V, T _J = 125°C			20	V/ns

1 Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

2 Starting at T_J = 25°C, L = 3.39mH, R_G = 25Ω, I_{AS} = 33A.

3 Pulse test: Pulse Width < 380μs, duty cycle < 2%.

4 C_{o(cr)} is defined as a fixed capacitance with the same stored charge as C_{OSS} with V_{DS} = 67% of V_{(BR)DSS}.

5 C_{o(er)} is defined as a fixed capacitance with the same stored energy as C_{OSS} with V_{DS} = 67% of V_{(BR)DSS}. To calculate C_{o(er)} for any value of V_{DS} less than V_{(BR)DSS}, use this equation: C_{o(er)} = -1.28E-7/V_{DS}² + 5.36E-8/V_{DS} + 2.00E-10.

6 R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

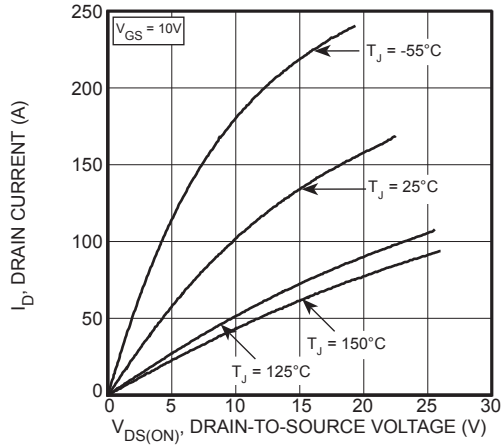


Figure 1, Output Characteristics

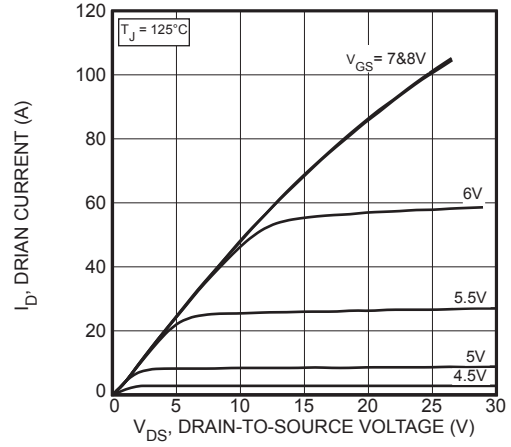


Figure 2, Output Characteristics

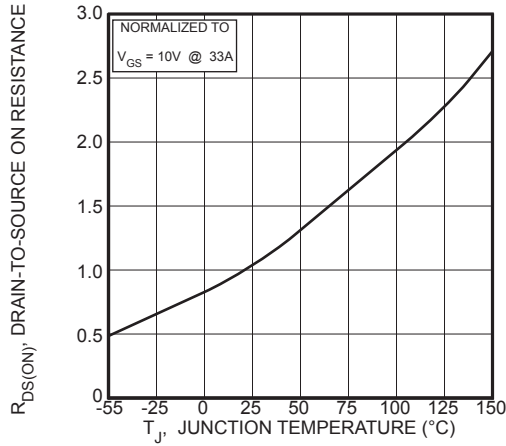


Figure 3, $R_{DS(ON)}$ vs Junction Temperature

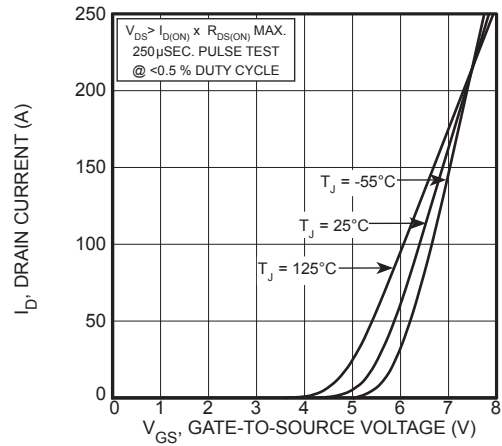


Figure 4, Transfer Characteristics

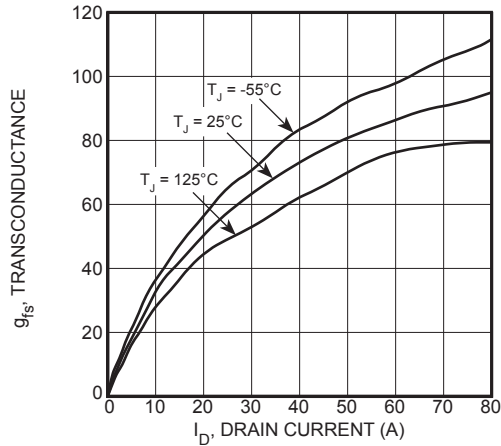


Figure 5, Gain vs Drain Current

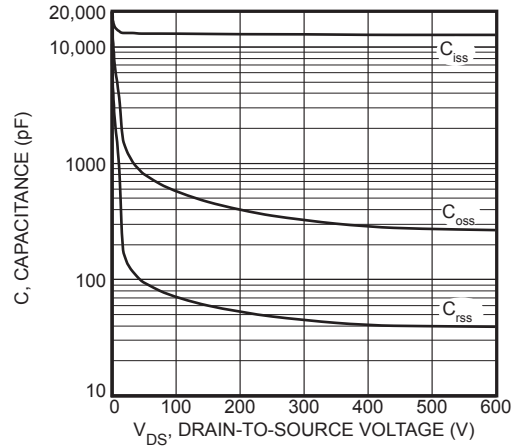


Figure 6, Capacitance vs Drain-to-Source Voltage

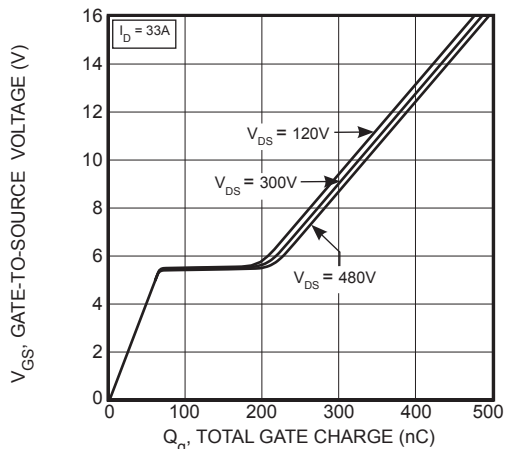


Figure 7, Gate Charge vs Gate-to-Source Voltage

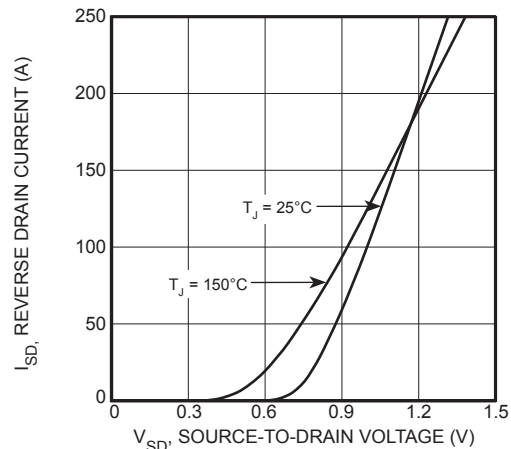
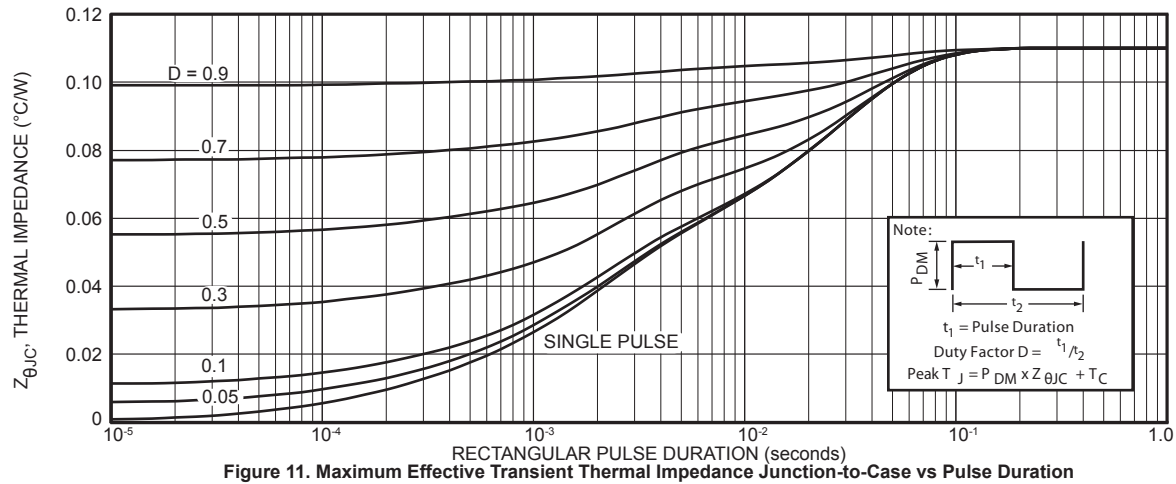
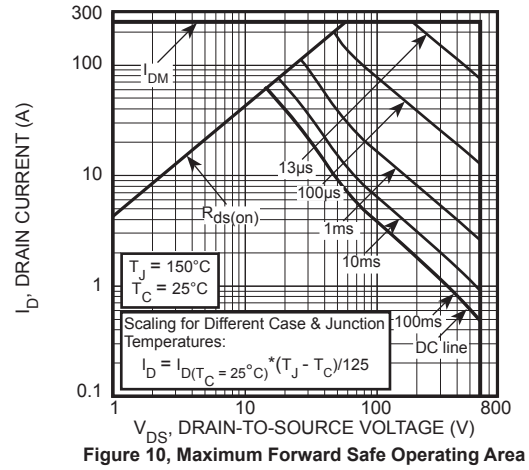
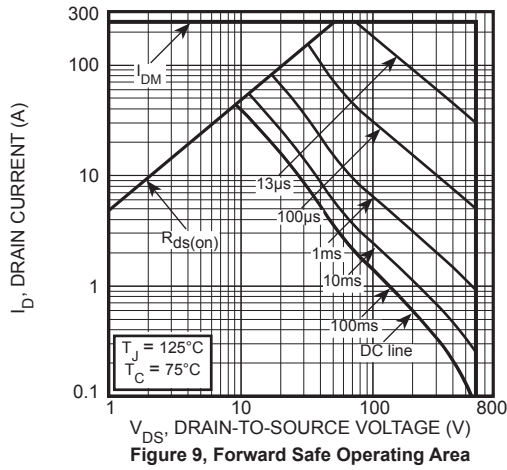


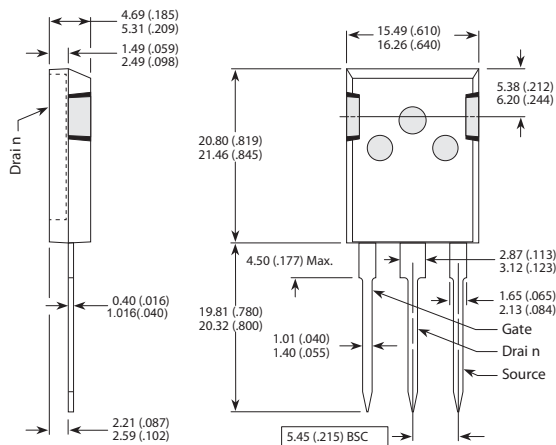
Figure 8, Reverse Drain Current vs Source-to-Drain Voltage



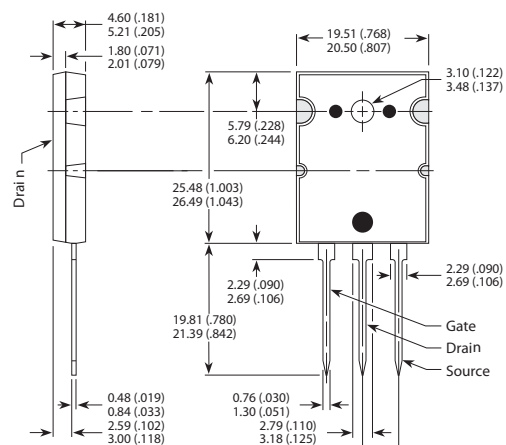
T-MAX® (B2) Package Outline

TO-264 (L) Package Outline

e3 100% Sn Plated



These dimensions are equal to the TO-247 without the mounting hole.
Dimensions in Millimeters and (Inches)



Dimensions in Millimeters and (Inches)

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