



**THE DATASHEET OF
SN74LVCH16244ADLR**



SN74LVCH16244A 16-Bit Buffer/Driver With 3-State Outputs

1 Features

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.1 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input or Output Voltage With 3.3-V V_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup or Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wireless and Telecom Infrastructures
- TV Set-top Boxes
- Electronic Points of Sale

3 Description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

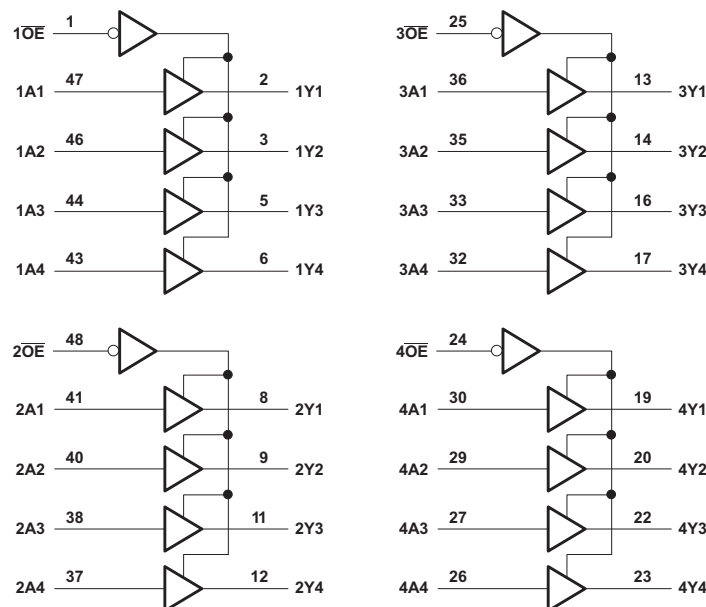
The SN74LVCH16244A device is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|----------------|------------|--------------------|
| SN74LVCH16244A | TSSOP (48) | 12.50 mm × 6.10 mm |
| | TVSOP (48) | 9.70 mm × 4.40 mm |
| | SSOP (48) | 15.88 mm × 7.49 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



Pin numbers shown are for the DGG, DGV, and DL packages.



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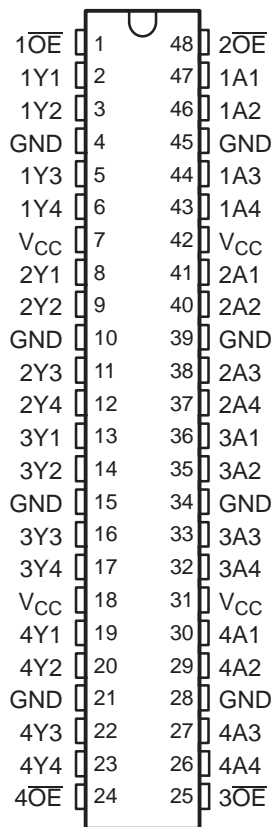
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (November 2005) to Revision B | Page |
|---|------|
| • Updated document to new TI data sheet format. | 1 |
| • Removed Ordering Information table. | 1 |
| • Updated I_{off} Feature bullet. | 1 |
| • Added Applications. | 1 |
| • Added Device Information table. | 1 |
| • Added Handling Ratings table. | 6 |
| • Changed MAX ambient temperature to 125°C. | 7 |
| • Added Thermal Information table. | 7 |
| • Updated $t_{sk(o)}$ values in Switching Characteristics table. | 8 |
| • Added Typical Characteristics. | 9 |

6 Pin Configuration and Functions

**DGG, DGV, OR DL PACKAGE
(TOP VIEW)**



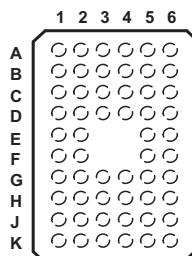
Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-------------------|-----|-----------------|
| NO. | NAME | | |
| 1 | 1 \overline{OE} | I | Output enable 1 |
| 2 | 1Y1 | O | 1Y1 Output |
| 3 | 1Y2 | O | 1Y2 Output |
| 4 | GND | — | Ground pin |
| 5 | 1Y3 | O | 1Y3 Output |
| 6 | 1Y4 | O | 1Y4 Output |
| 7 | V _{CC} | — | Power pin |
| 8 | 2Y1 | O | 2Y1 Output |
| 9 | 2Y2 | O | 2Y2 Output |
| 10 | GND | — | Ground pin |
| 11 | 2Y3 | O | 2Y3 Output |
| 12 | 2Y4 | O | 2Y4 Output |
| 13 | 3Y1 | O | 3Y1 Output |
| 14 | 3Y2 | O | 3Y2 Output |
| 15 | GND | — | Ground pin |
| 16 | 3Y3 | O | 3Y3 Output |
| 17 | 3Y4 | O | 3Y4 Output |
| 18 | V _{CC} | — | Power pin |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|-----|-------------------|-----|-----------------|
| NO. | NAME | | |
| 19 | 4Y1 | O | 4Y1 Output |
| 20 | 4Y2 | O | 4Y2 Output |
| 21 | GND | — | Ground pin |
| 22 | 4Y3 | O | 4Y3 Output |
| 23 | 4Y4 | O | 4Y4 Output |
| 24 | 4 \overline{OE} | I | Output enable 4 |
| 25 | 3 \overline{OE} | I | Output enable 3 |
| 26 | 4A4 | I | 4A4 Input |
| 27 | 4A3 | I | 4A3 Input |
| 28 | GND | — | Ground pin |
| 29 | 4A2 | I | 4A2 Input |
| 30 | 4A1 | I | 4A1 Input |
| 31 | VCC | — | Power pin |
| 32 | 3A4 | I | 3A4 Input |
| 33 | 3A3 | I | 3A3 Input |
| 34 | GND | — | Ground pin |
| 35 | 3A2 | I | 3A2 Input |
| 36 | 3A1 | I | 3A1 Input |
| 37 | 2A4 | I | 2A4 Input |
| 38 | 2A3 | I | 2A3 Input |
| 39 | GND | — | Ground pin |
| 40 | 2A2 | I | 2A2 Input |
| 41 | 2A1 | I | 2A1 Input |
| 42 | VCC | — | Power pin |
| 43 | 1A4 | I | 1A4 Input |
| 44 | 1A3 | I | 1A3 Input |
| 45 | GND | — | Ground pin |
| 46 | 1A2 | I | 1A2 Input |
| 47 | 1A1 | I | 1A1 Input |
| 48 | 2 \overline{OE} | I | Output enable 2 |

**QGL OR ZQL PACKAGE
(TOP VIEW)**

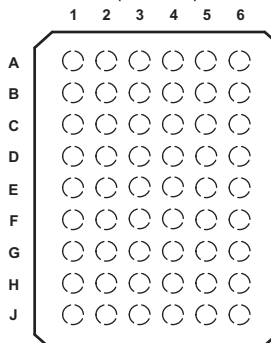


**Pin Assignments⁽¹⁾
(56-Ball QGL or ZQL Package)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|------------------|-----|-----------------|-----------------|-----|------------------|
| A | $\overline{1OE}$ | NC | NC | NC | NC | $\overline{2OE}$ |
| B | 1Y2 | 1Y1 | GND | GND | 1A1 | 1A2 |
| C | 1Y4 | 1Y3 | V _{CC} | V _{CC} | 1A3 | 1A4 |
| D | 2Y2 | 2Y1 | GND | GND | 2A1 | 2A2 |
| E | 2Y4 | 2Y3 | | | 2A3 | 2A4 |
| F | 3Y1 | 3Y2 | | | 3A2 | 3A1 |
| G | 3Y3 | 3Y4 | GND | GND | 3A4 | 3A3 |
| H | 4Y1 | 4Y2 | V _{CC} | V _{CC} | 4A2 | 4A1 |
| J | 4Y3 | 4Y4 | GND | GND | 4A4 | 4A3 |
| K | $\overline{4OE}$ | NC | NC | NC | NC | $\overline{3OE}$ |

(1) NC – No internal connection

**GRD OR ZRD PACKAGE
(TOP VIEW)**



**Pin Assignments⁽¹⁾
(54-Ball GRD or ZRD Package)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|------------------|------------------|-----|-----|
| A | 1Y1 | NC | $\overline{1OE}$ | $\overline{2OE}$ | NC | 1A1 |
| B | 1Y3 | 1Y2 | NC | NC | 1A2 | 1A3 |
| C | 2Y1 | 1Y4 | V _{CC} | V _{CC} | 1A4 | 2A1 |
| D | 2Y3 | 2Y2 | GND | GND | 2A2 | 2A3 |
| E | 3Y1 | 2Y4 | GND | GND | 2A4 | 3A1 |
| F | 3Y3 | 3Y2 | GND | GND | 3A2 | 3A3 |
| G | 4Y1 | 3Y4 | V _{CC} | V _{CC} | 3A4 | 4A1 |
| H | 4Y3 | 4Y2 | NC | NC | 4A2 | 4A3 |
| J | 4Y4 | NC | $\overline{4OE}$ | $\overline{3OE}$ | NC | 4A4 |

(1) NC – No internal connection

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------------|---|--------------------|-----------------------|------|
| V _{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | -50 | mA |
| I _O | Continuous output current | | ±50 | mA |
| | Continuous current through each V _{CC} or GND | | ±100 | mA |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 Handling Ratings

| | | MIN | MAX | UNIT | |
|--------------------|---------------------------|--|-----|------|---|
| T _{stg} | Storage temperature range | -65 | 150 | °C | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|------------------------------------|------------------------|------------------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | |
| | | V _{CC} = 2.7 V to 3.6 V | | 0.8 | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | High or low state | 0 | V _{CC} | V |
| | | 3-state | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | −4 | mA |
| | | V _{CC} = 2.3 V | | −8 | |
| | | V _{CC} = 2.7 V | | −12 | |
| | | V _{CC} = 3 V | | −24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 2.7 V | | 12 | |
| | | V _{CC} = 3 V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | | 10 | ns/V |
| T _A | Operating free-air temperature | −40 | 125 | | °C |

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DGG | DGV | DL | UNIT |
|-------------------------------|--|---------|---------|---------|------|
| | | 48 PINS | 48 PINS | 48 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 64.3 | 78.4 | 68.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 17.6 | 30.7 | 34.7 | |
| R _{θJB} | Junction-to-board thermal resistance | 31.5 | 41.8 | 41.0 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 1.1 | 3.8 | 12.3 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 31.2 | 41.3 | 40.4 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------------|--|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 3.6 V | V _{CC} - 0.2 | | | V |
| | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -8 mA | 2.3 V | 1.7 | | | |
| | I _{OH} = -12 mA | 2.7 V | 2.2 | | | |
| | | 3 V | 2.4 | | | |
| I _{OH} = -24 mA | 3 V | 2.2 | | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | | | 0.2 | V |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | I _{OL} = 8 mA | 2.3 V | | | 0.7 | |
| | I _{OL} = 12 mA | 2.7 V | | | 0.4 | |
| | I _{OL} = 24 mA | 3 V | | | 0.55 | |
| I _I | V _I = 0 to 5.5 V | 3.6 V | | | ±5 | μA |
| I _{I(hold)} | V _I = 0.58 V | 1.65 V | 15 | | | μA |
| | V _I = 1.07 V | | -15 | | | |
| | V _I = 0.7 V | 2.3 V | 45 | | | |
| | V _I = 1.7 V | | -45 | | | |
| | V _I = 0.8 V | 3 V | 75 | | | |
| | V _I = 2 V | | -75 | | | |
| | V _I = 0 to 3.6 V ⁽²⁾ | 3.6 V | | | ±500 | |
| I _{off} | V _I or V _O = 5.5 V | 0 | | | ±10 | μA |
| I _{OZ} | V _O = 0 to 5.5 V | 3.6 V | | | ±10 | μA |
| I _{CC} | V _I = V _{CC} or GND | 3.6 V | I _O = 0 | | 20 | μA |
| | 3.6 V ≤ V _I ≤ 5.5 V ⁽³⁾ | | | | 20 | |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | | | 500 | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | | 5.5 | | pF |
| C _o | V _O = V _{CC} or GND | 3.3 V | | 6 | | pF |

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current required to switch the input from one state to another.

(3) This applies in the disabled state only.

7.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

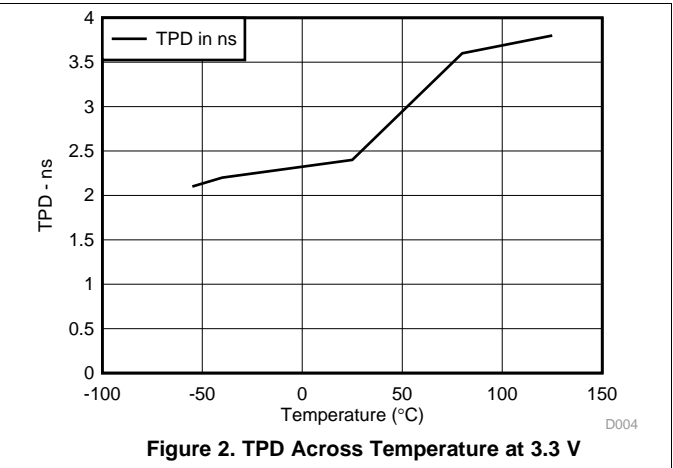
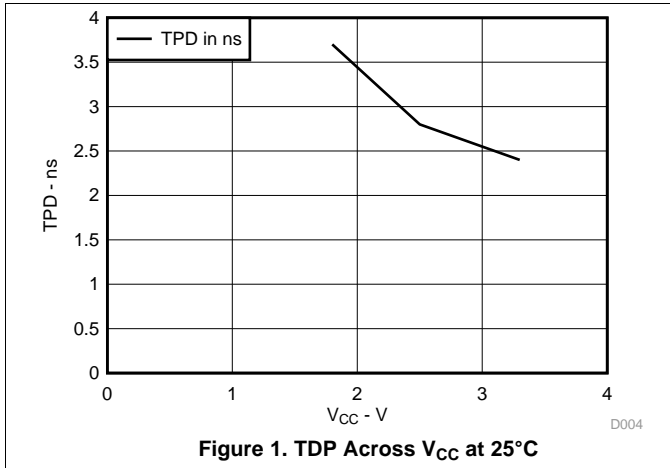
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|--------------------|------------------------|-------------|----------------------------------|------|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 1.5 | 6.6 | 1 | 3.9 | 1 | 4.7 | 1.1 | 4.1 | ns |
| t _{en} | $\overline{\text{OE}}$ | Y | 1.5 | 7.5 | 1 | 4.7 | 1 | 5.8 | 1 | 4.6 | ns |
| t _{dis} | $\overline{\text{OE}}$ | Y | 1.5 | 10.3 | 1 | 5.3 | 1 | 6.2 | 1.8 | 5.8 | ns |
| t _{sk(o)} | | | | 1 | | 1 | | 1 | | 1 | ns |

7.7 Operating Characteristics

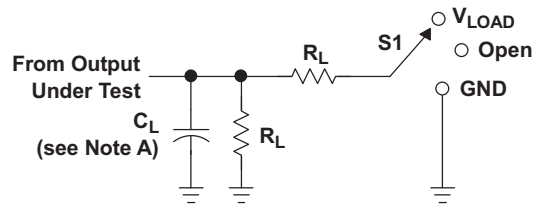
 T_A = 25°C

| PARAMETER | | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT | |
|-----------------|---|------------------|-------------------------|-------------------------|-------------------------|------|----|
| | | | TYP | TYP | TYP | | |
| C _{pd} | Power dissipation capacitance per buffer/driver | Outputs enabled | f = 10 MHz | 33 | 32 | 35 | pF |
| | | Outputs disabled | | 2 | 2 | 3 | |

7.8 Typical Characteristics

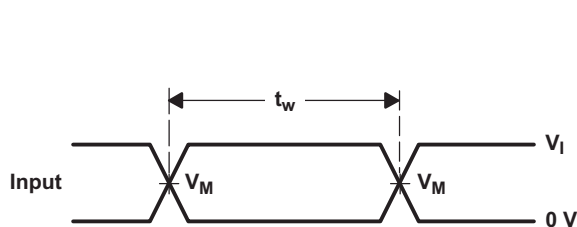
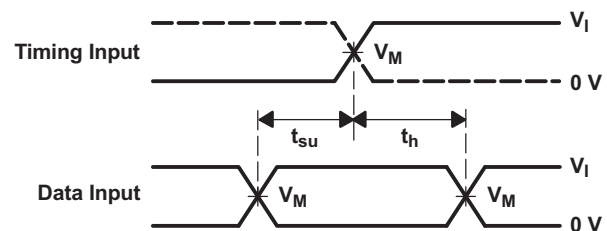
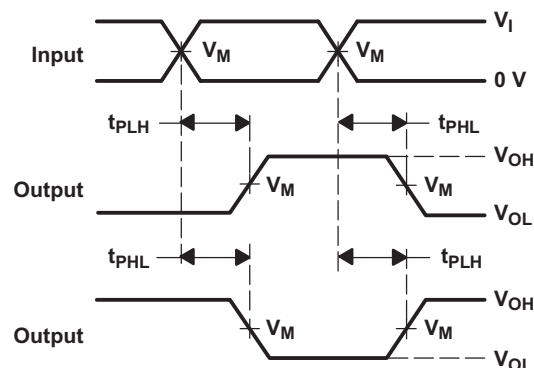
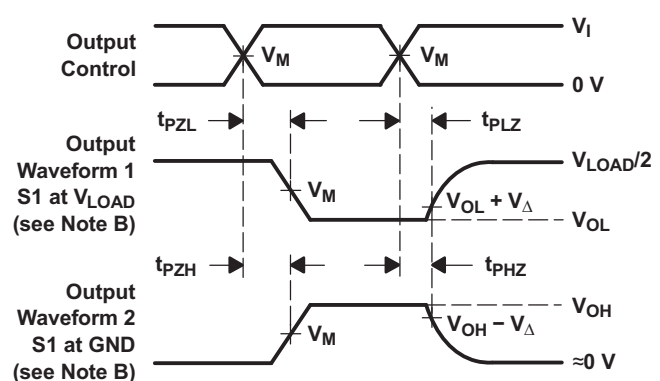


8 Parameter Measurement Information


LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |


**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74LVCH16244A device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

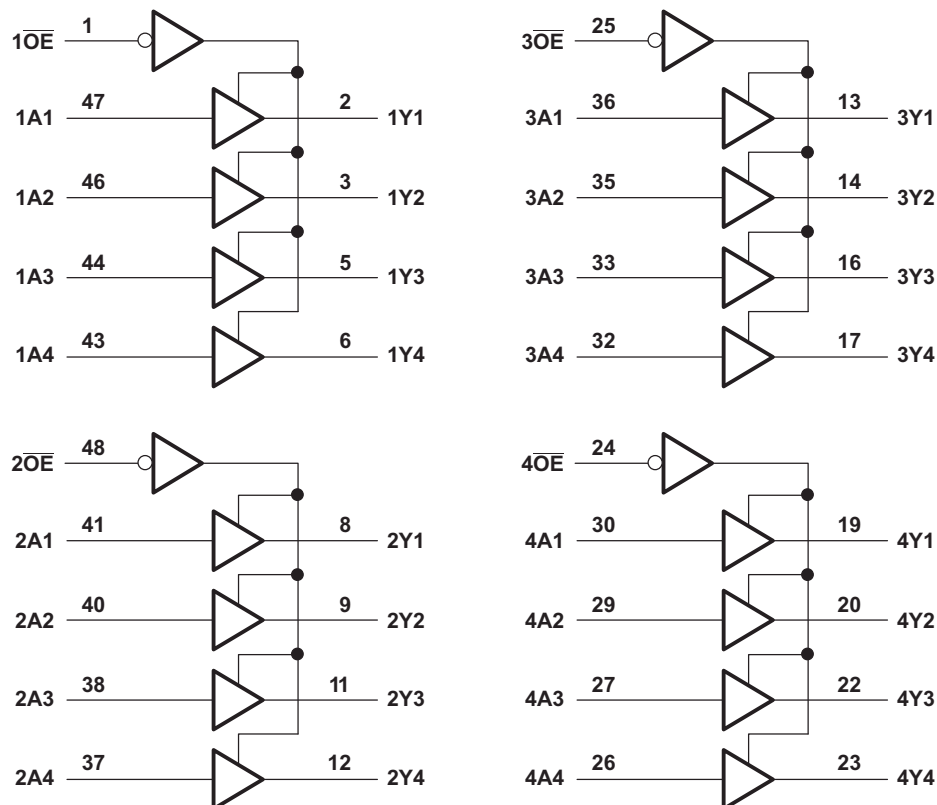
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

The SN74LVCH16244A device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

9.2 Functional Block Diagram



Pin numbers shown are for the DGG, DGV, and DL packages.

9.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

**Table 1. Function Table
(Each 4-bit Buffer)**

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

10 Application and Implementation

10.1 Application Information

The SN74LVCH16244A device is a 16-bit buffer driver. This device can be used as four 4-bit, two 8-bit, or one 16-bit buffer. It allows data transmission from the A bus to the Y bus with 4 separate enable pins that control 4 bits each. The output-enable (\overline{OE}) input can be used to disable sections of the device so that the buses are effectively isolated. The device has 5.5 V tolerant inputs at any valid V_{CC} . This allows the device to be used in multi-power systems, and it can be used for down translation. Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

10.2 Typical Application

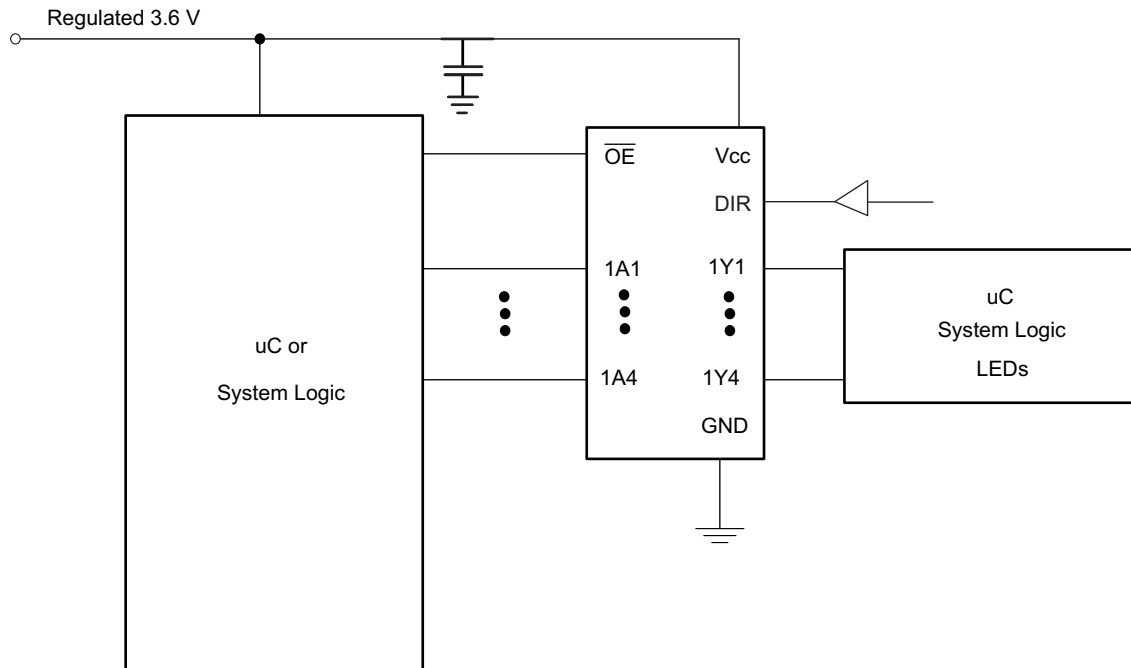


Figure 4. Typical Application Diagram

10.2.1 Design Requirements

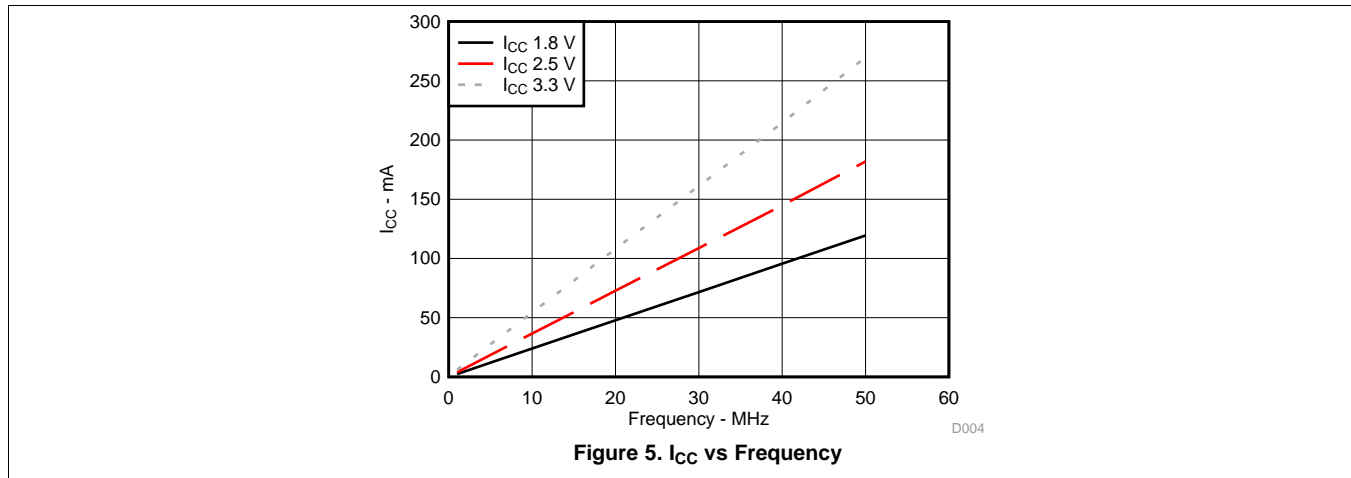
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels: See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple V_{CC} pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 6](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

12.2 Layout Example

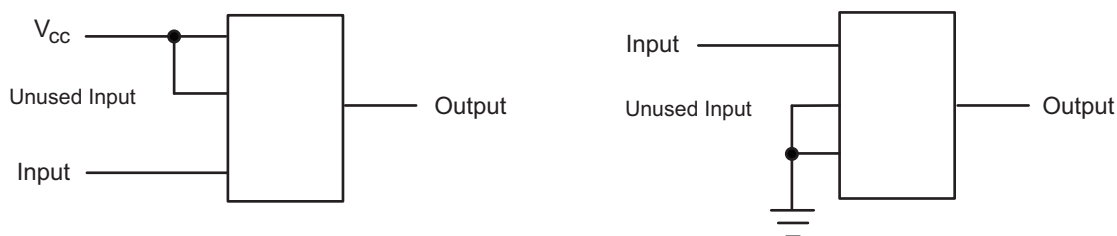


Figure 6. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

Widebus is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVCH16244ADGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVCH16244A | Samples |
| SN74LVCH16244ADGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LDH244A | Samples |
| SN74LVCH16244ADL | ACTIVE | SSOP | DL | 48 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVCH16244A | Samples |
| SN74LVCH16244ADLG4 | ACTIVE | SSOP | DL | 48 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVCH16244A | Samples |
| SN74LVCH16244ADLR | ACTIVE | SSOP | DL | 48 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVCH16244A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

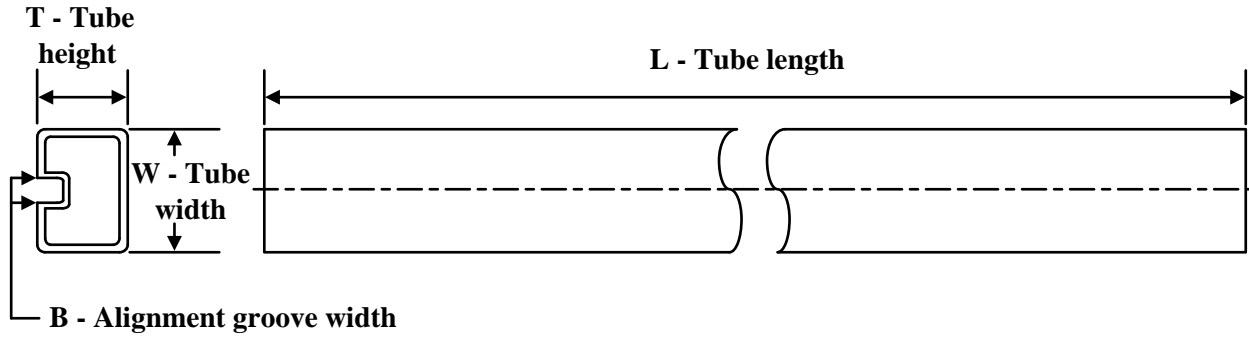

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVCH16244ADGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74LVCH16244ADGVR | TVSOP | DGV | 48 | 2000 | 330.0 | 16.4 | 7.1 | 10.2 | 1.6 | 12.0 | 16.0 | Q1 |
| SN74LVCH16244ADLR | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVCH16244ADGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVCH16244ADGVR | TVSOP | DGV | 48 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVCH16244ADLR | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |

TUBE


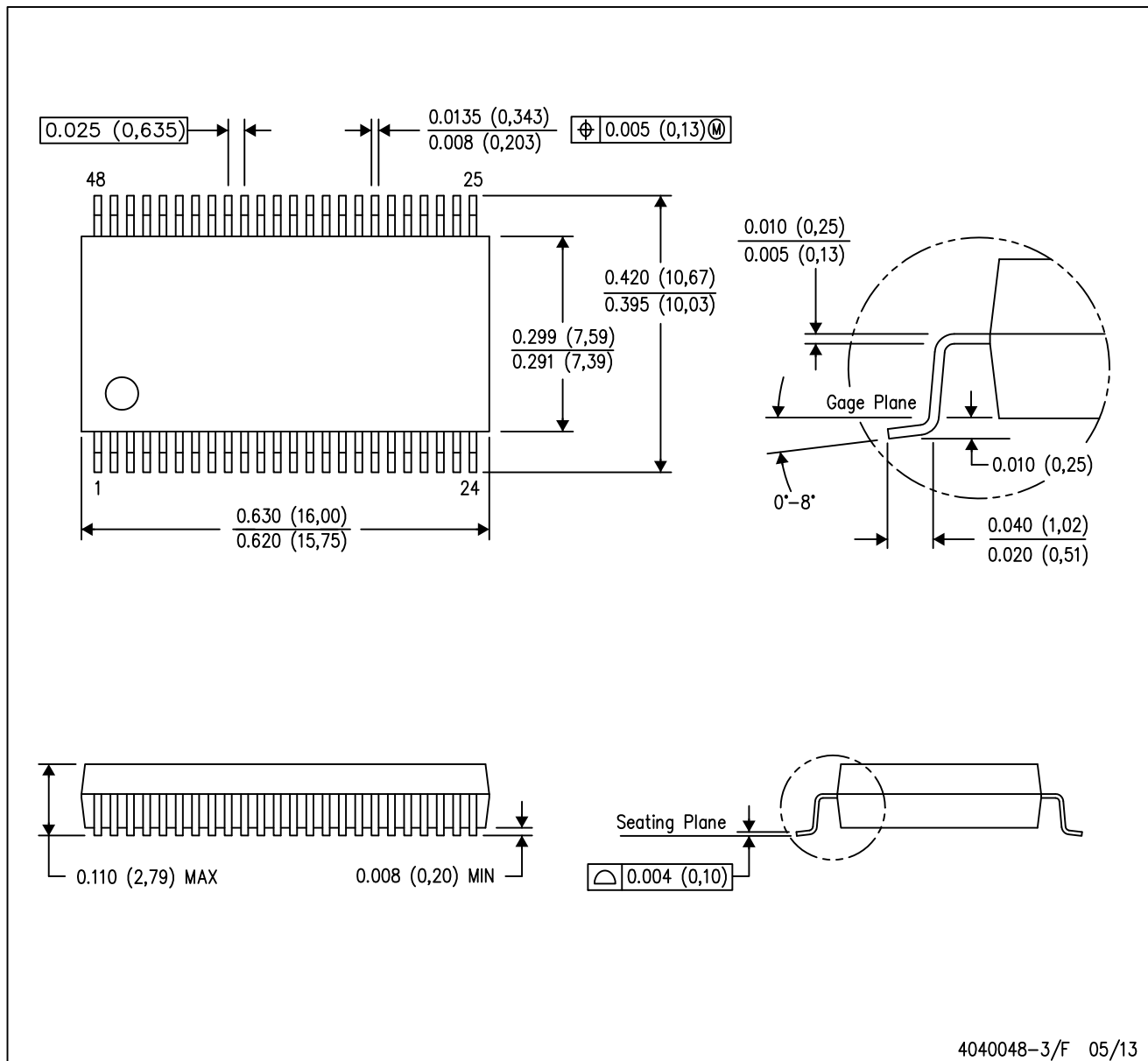
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVCH16244ADL | DL | SSOP | 48 | 25 | 473.7 | 14.24 | 5110 | 7.87 |
| SN74LVCH16244ADLG4 | DL | SSOP | 48 | 25 | 473.7 | 14.24 | 5110 | 7.87 |

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

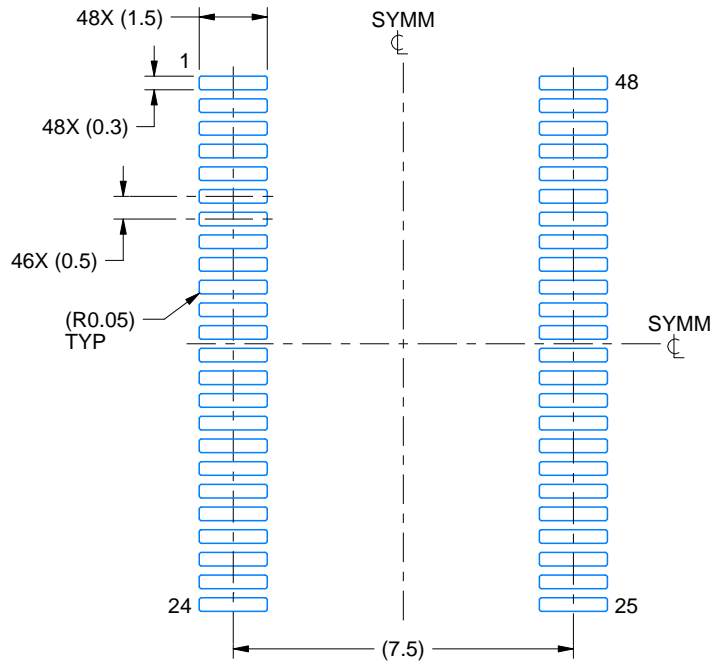
PowerPAD is a trademark of Texas Instruments.

EXAMPLE BOARD LAYOUT

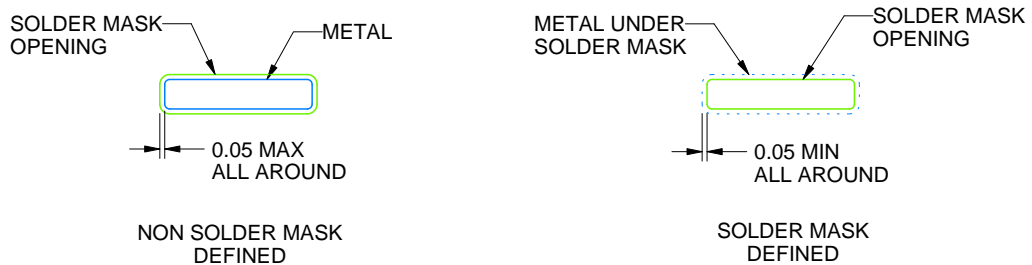
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

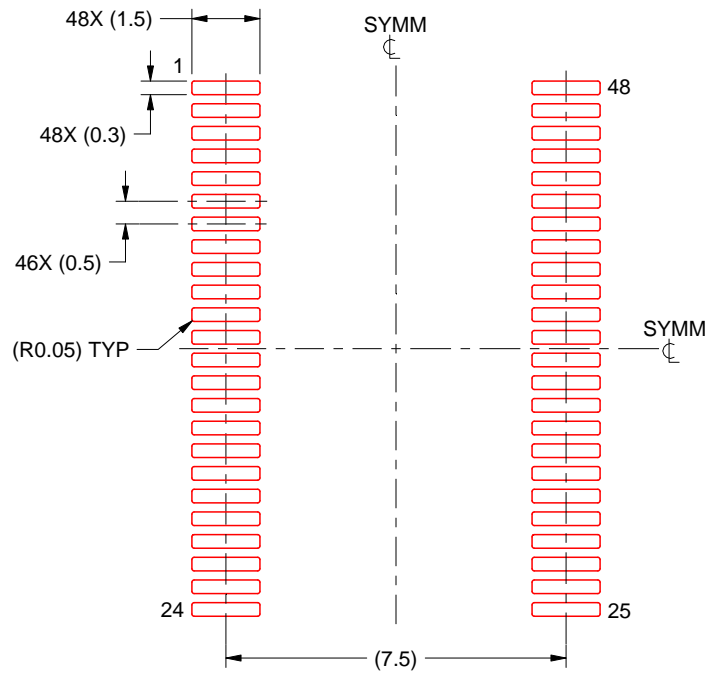
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

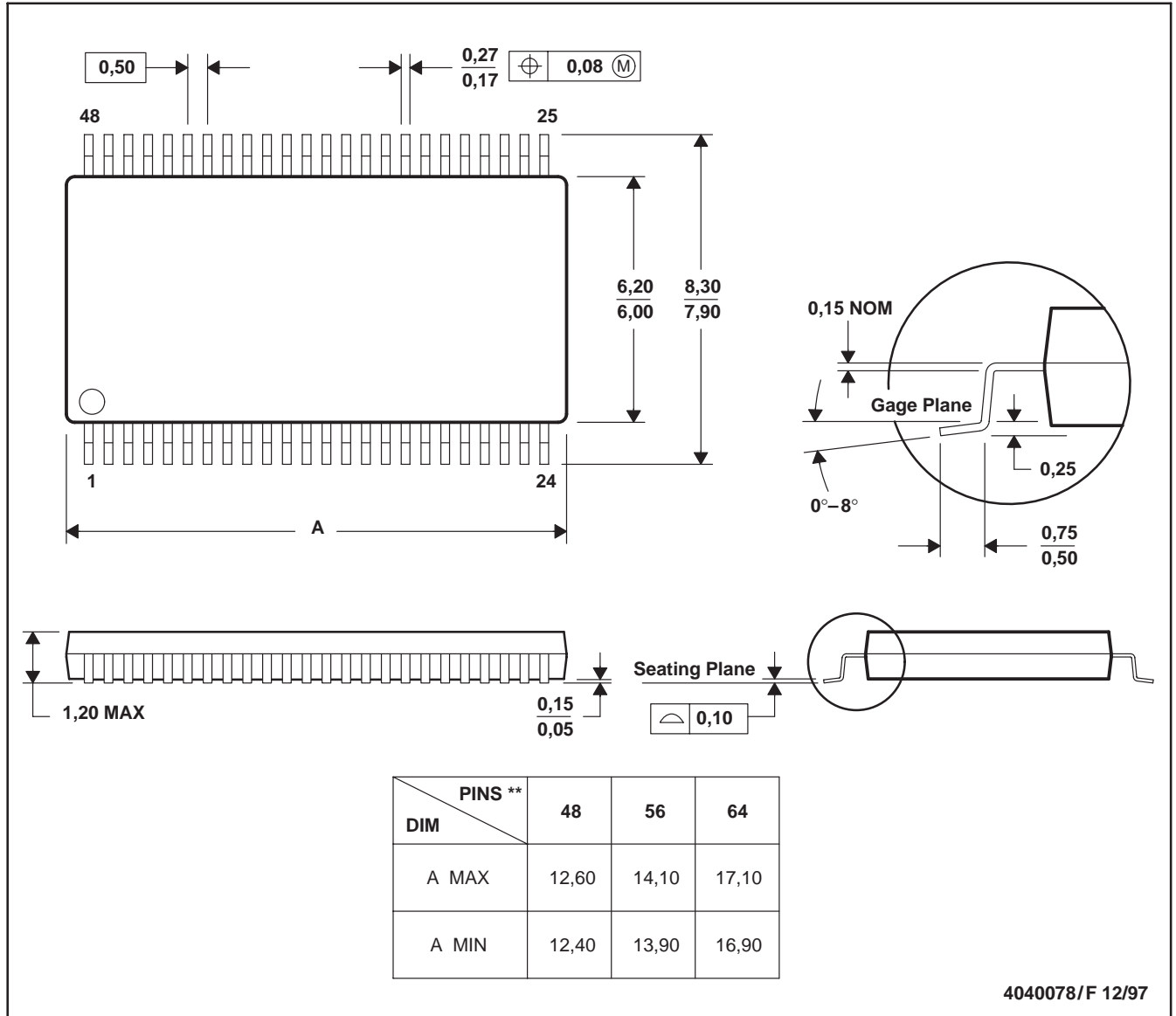
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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