THE DATASHEET OF

AP2151SG-13

Description

The AP2141 and AP2151 are integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. This family of devices complies with USB 2.0 and is available with both polarities of Enable input. They offer current and thermal limiting and short circuit protection as well as controlled rise time and undervoltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and does not require any external components.

All devices are available in SO-8, MSOP-8EP, SOT25 and U-DFN2018-6 packages.

Features

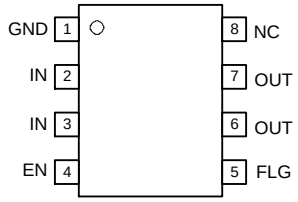
- Single USB Port Power Switches
- Over-Current and Thermal Protection
- 0.8A Accurate Current Limiting
- Reverse Current Blocking
- 95mΩ On-Resistance
- Input Voltage Range: 2.7V to 5.5V
- 0.6ms Typical Rise Time
- Very Low Shutdown Current: 1µA (Max)
- Fault Report (FLG) with Blanking Time (7ms Typ)
- ESD Protection: 4kV HBM, 400V MM
- Active High (AP2151) or Active Low (AP2141) Enable
- Ambient Temperature Range -40°C to +85°C
- SOT25, SO-8, MSOP-8EP (Exposed Pad), and U-DFN2018-6: Available in “Green” Molding Compound (No Br, Sb)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- 15kV ESD Protection per IEC 61000-4-2 (With External Capacitance)
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified

Applications

- Consumer Electronics – LCD TV & Monitor, Game Machines
- Communications – Set-Top Box, GPS, Smartphone
- Computing – Laptop, Desktop, Servers, Printers, Docking Station, HUB

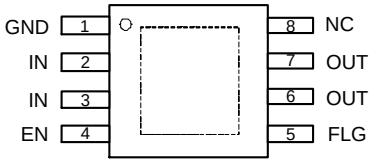
Pin Assignments

(Top View)



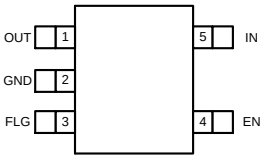
SO-8

(Top View)



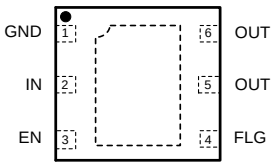
MSOP-8EP

(Top View)



SOT25

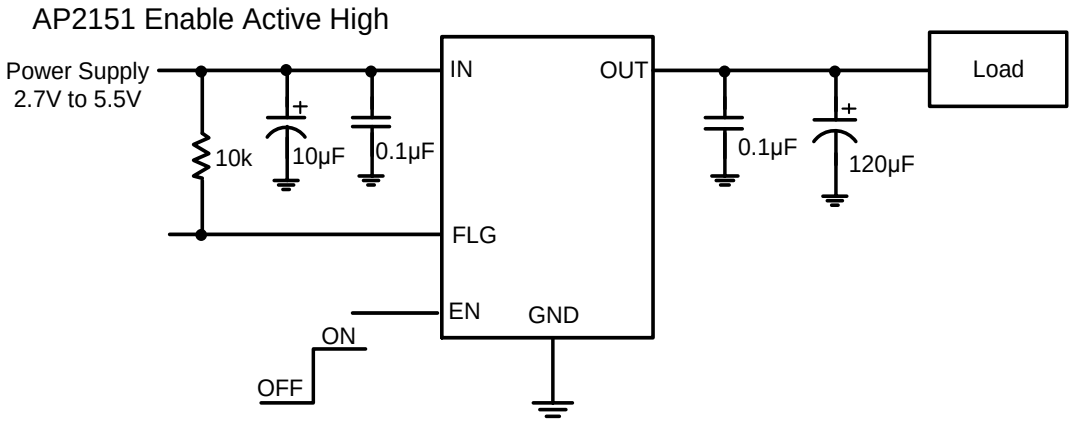
(Top View)



U-DFN2018-6

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



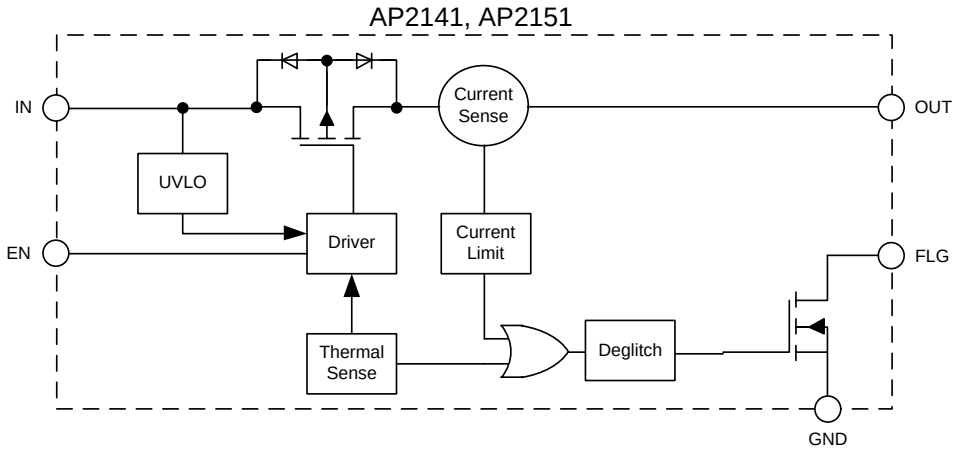
Available Options

Part Number	Channel	Enable Pin (EN)	Current Limit (Typical)	Recommended Maximum Continuous Load Current
AP2141	1	Active Low	0.8A	0.5A
AP2151	1	Active High	0.8A	0.5A

Pin Descriptions

Pin Name	Pin Number				Function
	SO-8	MSOP-8EP	SOT25	U-DFN2018-6	
GND	1	1	2	1	Ground
IN	2, 3	2, 3	5	2	Voltage Input Pin (all IN pins must be tied together externally)
EN	4	4	4	3	Enable Input Active Low (AP2141) or Active High (AP2151)
FLG	5	5	3	4	Over-Current and Over-Temperature Fault Report Open-Drain flag is active low when triggered
OUT	6, 7	6, 7	1	5, 6	Voltage Output Pin (all OUT pins must be tied together externally)
NC	8	8	—	—	No internal connection; recommend tie to OUT pins
Exposed Pad	—	Exposed Pad	—	Exposed Pad	Exposed Pad It should be externally connected to GND plane and thermal mass for enhanced thermal impedance. It should not be used as electrical ground conduction path.

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter			Ratings	Units
ESD	HBM	Human Body Model ESD Protection		4	kV
	MM	Machine Model ESD Protection for SO-8, MSOP-8EP, SOT25 Packages		400	V
	MM	Machine Model ESD Protection for U-DFN2018-6, SO-8 Packages		300	V
	IEC System Level	Surges per EN61000-4-2. 1999 applied to output terminals of EVM (Note 5)	Air	15	kV
		Surges per EN61000-4-2. 1999 applied to output terminals of EVM (Note 5)	Contact	8	kV
V_{IN}	Input Voltage			6.5	V
V_{OUT}	Output Voltage			V_{IN} +0.3	V
V_{EN} , V_{FLG}	Enable Voltage			6.5	V
I_{LOAD}	Maximum Continuous Load Current			Internal Limited	A
$T_{J(MAX)}$	Maximum Junction Temperature			+150	°C
T_{ST}	Storage Temperature Range (Note 4)			-65 to +150	°C

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Notes: 4. UL Recognized Rating from -30°C to +70°C (Diodes qualified T_{ST} from -65°C to +150°C).
5. External capacitors need to be connected to the output, EVM board tested with capacitor 2.2µF 50V 0805. This level is a pass test only and not a limit.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
V_{IN}	Input Voltage	2.7	5.5	V
I_{OUT}	Output Current	0	500	mA
T_A	Operating Ambient Temperature	-40	+85	°C
V_{IL}	EN Input Logic Low Voltage	0	0.8	V
V_{IH}	EN Input Logic High Voltage	2	V_{IN}	V

Electrical Characteristics (@T_A = +25°C, V_{IN} = 5.0V, unless otherwise specified.)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{UVLO}	Input UVLO	R_{LOAD} = 1kΩ			1.6	1.9	2.5	V
I_{SHDN}	Input Shutdown Current	Disabled, I_{OUT} = 0			—	0.5	1	μA
I_Q	Input Quiescent Current	Enabled, I_{OUT} = 0			—	45	70	μA
I_{LEAK}	Input Leakage Current	Disabled, OUT Grounded			—	—	1	μA
I_{REV}	Reverse Leakage Current	Disabled, V_{IN} = 0V, V_{OUT} = 5V, I_{REV} at V_{IN}			—	1	—	μA
$R_{DS(ON)}$	Switch On-Resistance	V_{IN} = 5V, I_{OUT} = 0.5A	T_A = +25°C	SOT25, SO-8, MSOP-8EP	—	95	115	mΩ
				U-DFN2018-6	—	90	110	
			-40°C ≤ T_A ≤ +85°C		—	—	140	
		V_{IN} = 3.3V, I_{OUT} = 0.5A	T_A = +25°C		—	120	140	
			-40°C ≤ T_A ≤ +85°C		—	—	170	
I_{SHORT}	Short-Circuit Current Limit	Enabled into Short Circuit, C_L = 22μF			—	0.6	—	A
I_{LIMIT}	Over-Load Current Limit	V_{IN} = 5V, V_{OUT} = 4.8V, C_L = 22μF, -40°C ≤ T_A ≤ +85°C			0.6	0.8	1.0	A
I_{TRIG}	Current Limiting Trigger Threshold	Output Current Slew Rate (<100A/s), C_L = 22μF			—	1.0	—	A
I_{SINK}	EN Input Leakage	V_{EN} = 5V			—	—	1	μA
$t_{D(ON)}$	Output Turn-On Delay Time	C_L = 1μF, R_{LOAD} = 10Ω			—	0.05	—	ms
t_R	Output Turn-On Rise Time	C_L = 1μF, R_{LOAD} = 10Ω			—	0.6	1.5	ms
$t_{D(OFF)}$	Output Turn-Off Delay Time	C_L = 1μF, R_{LOAD} = 10Ω			—	0.01	—	ms
t_F	Output Turn-Off Fall Time	C_L = 1μF, R_{LOAD} = 10Ω			—	0.05	0.1	ms
R_{FLG}	FLG Output FET On-Resistance	I_{FLG} =10mA			—	20	40	Ω
t_{BLANK}	FLG Blanking Time	C_{IN} = 10μF, C_L = 22μF			4	7	15	ms
T_{SHDN}	Thermal Shutdown Threshold	Enabled, R_{LOAD} = 1kΩ			—	+140	—	°C
T_{HYS}	Thermal Shutdown Hysteresis	—			—	+25	—	°C
θ_{JA}	Thermal Resistance Junction-to-Ambient	SO-8 (Note 6)			—	110	—	°C/W
		MSOP-8EP (Note 7)			—	60	—	°C/W
		SOT25 (Note 8)			—	157	—	°C/W
		U-DFN2018-6 (Note 9)			—	70	—	°C/W

Notes:
6. Test condition for SO-8: Device mounted on FR-4, 2oz copper, with minimum recommended pad layout.
7. Test condition for MSOP-8EP: Device mounted on 2" x 2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
8. Test condition for SOT25: Device mounted on FR-4, 2oz copper, with minimum recommended pad layout.
9. Test condition for U-DFN2018-6: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad on top layer and 3 vias to bottom layer 1.0"x1.4" ground plane.

Typical Performance Characteristics

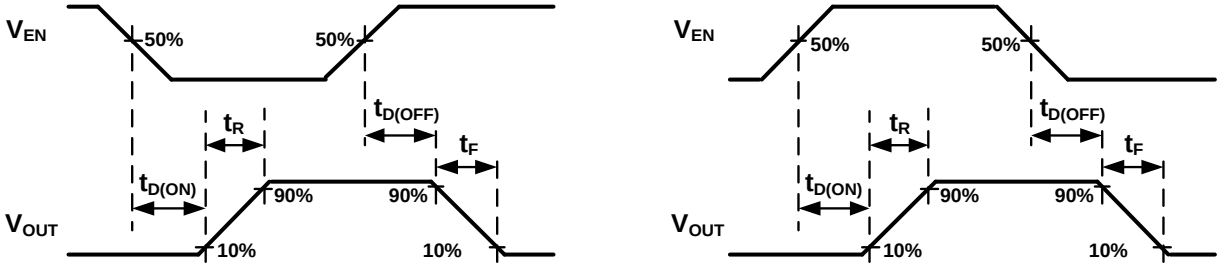
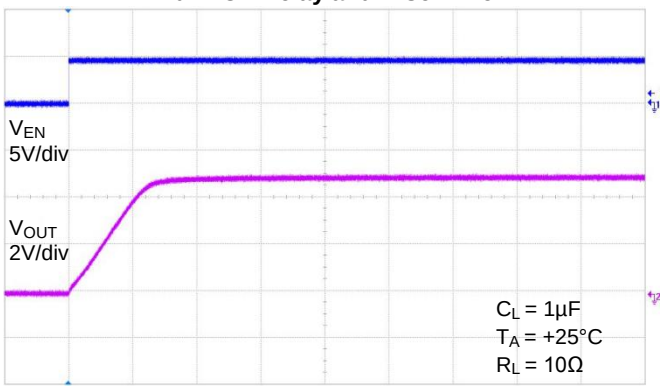


Figure 1. Voltage Waveforms: AP2141 (Left), AP2151 (Right)

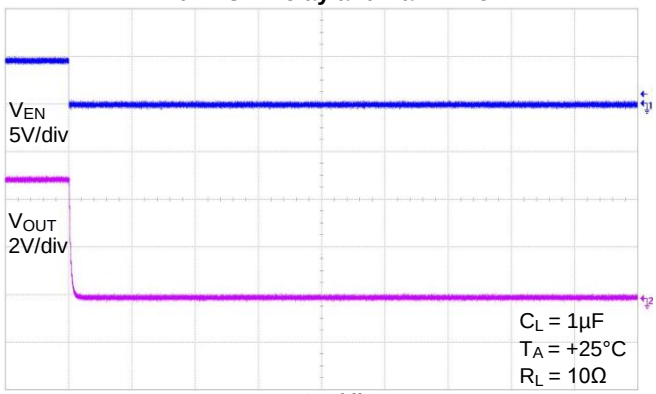
All Enable Plots are for AP2151 Active High

Turn-On Delay and Rise Time



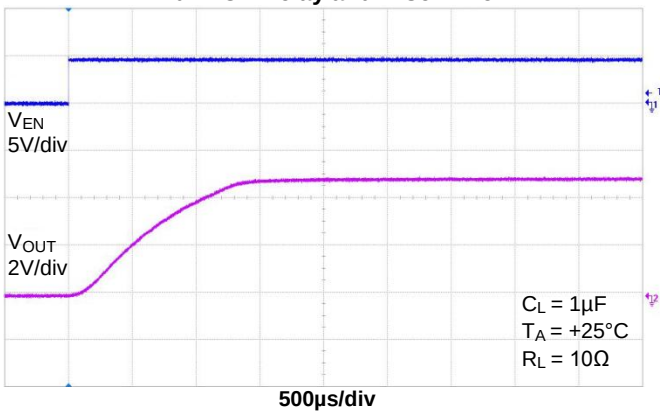
500µs/div

Turn-Off Delay and Fall Time



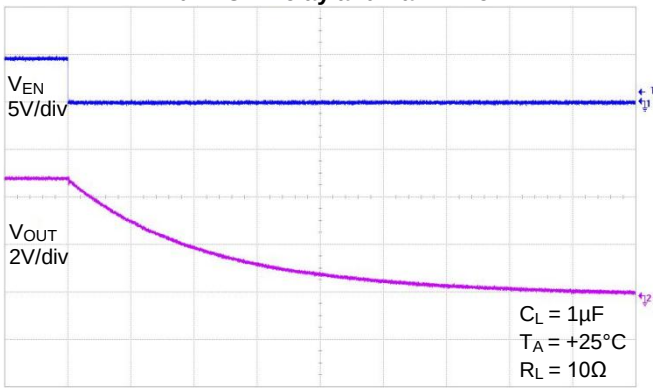
500µs/div

Turn-On Delay and Rise Time



500µs/div

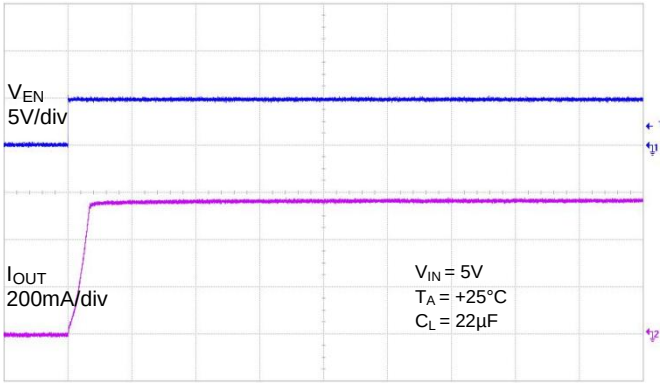
Turn-Off Delay and Fall Time



500µs/div

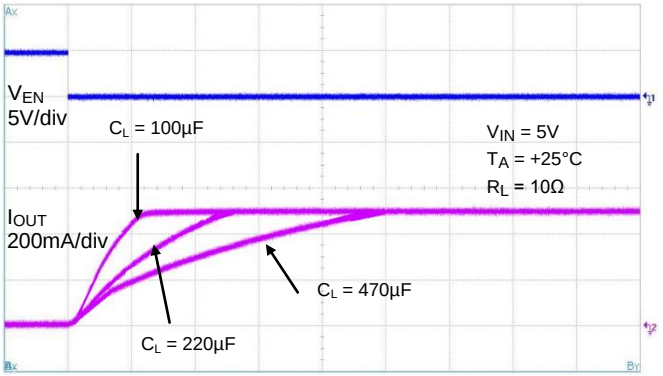
Typical Performance Characteristics (Cont.)

Short Circuit Current, Device Enabled Into Short



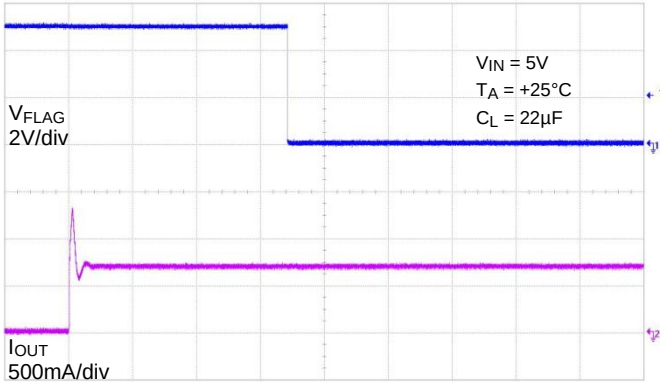
500µs/div

Inrush Current



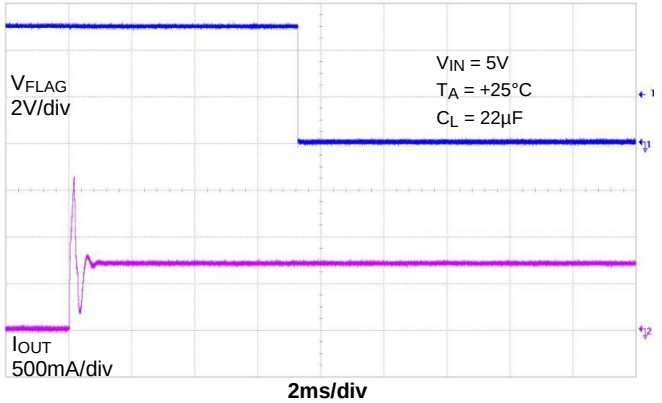
1ms/div

3Ω Load Connected to Enabled Device



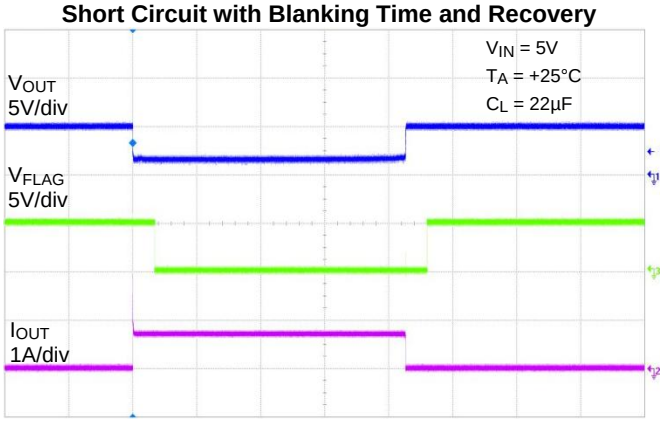
2ms/div

2Ω Load Connected to Enabled Device



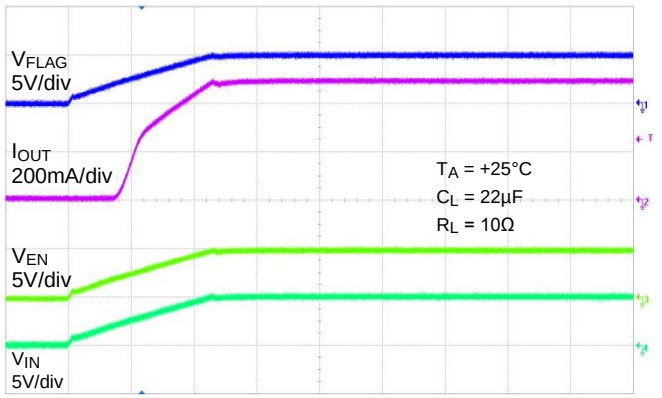
2ms/div

Short Circuit with Blanking Time and Recovery



20ms/div

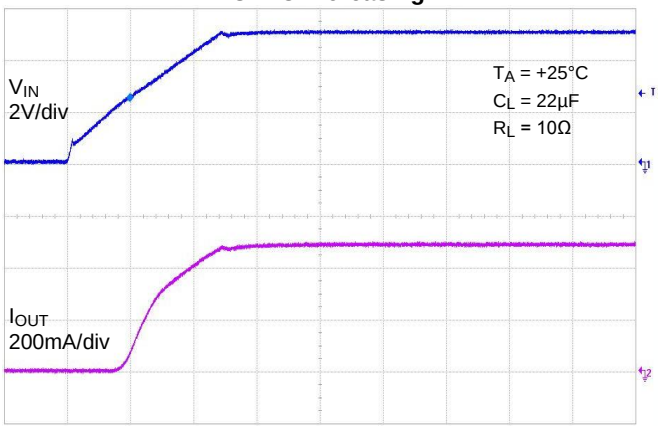
Power On



1ms/div

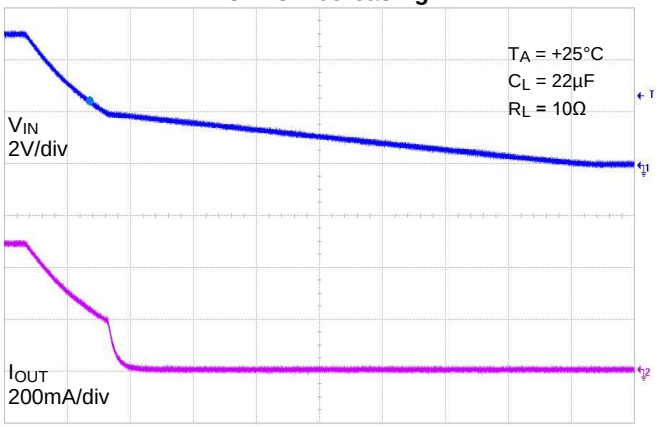
Typical Performance Characteristics (Cont.)

UVLO Increasing

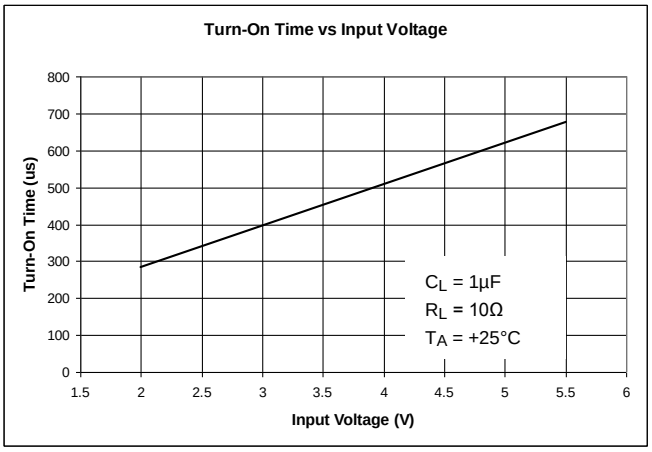


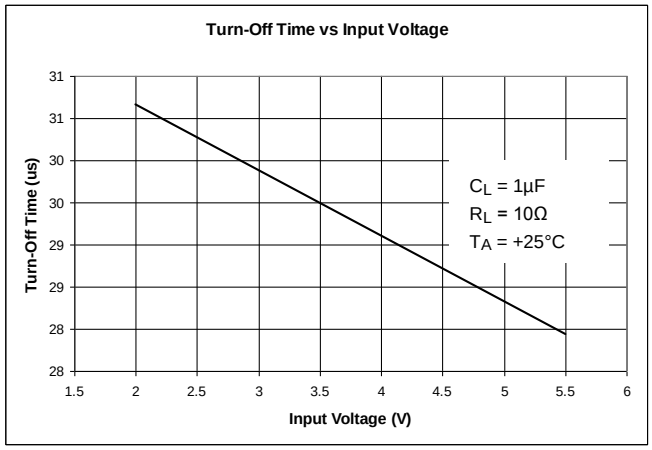
1ms/div

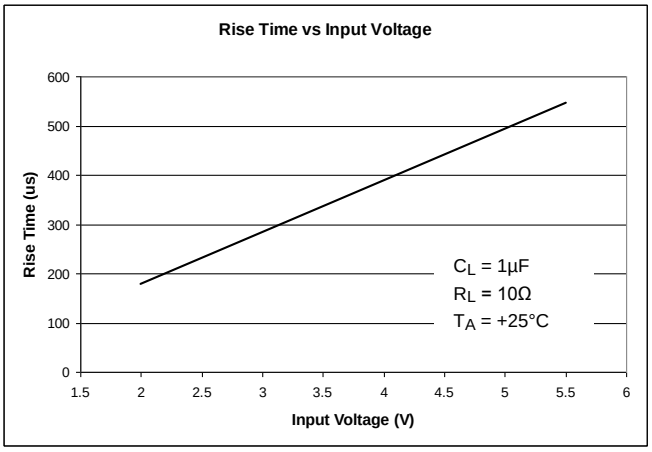
UVLO Decreasing

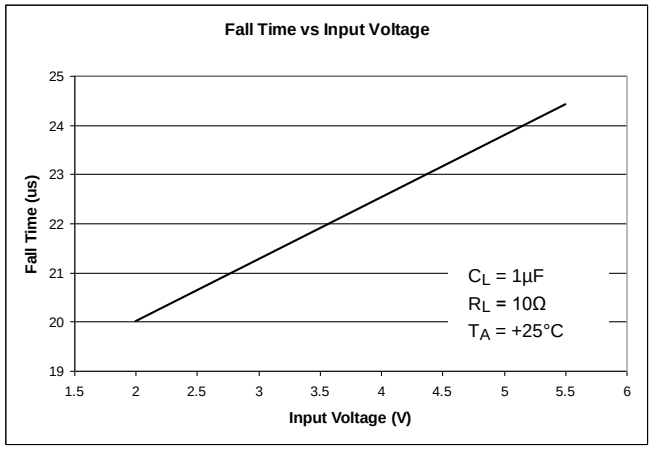


10ms/div

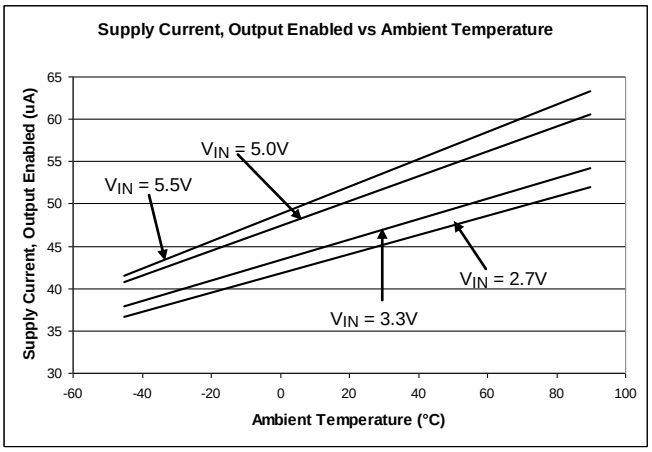


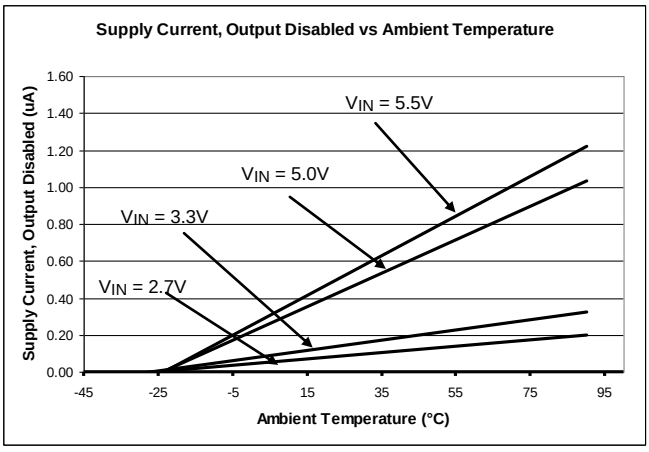


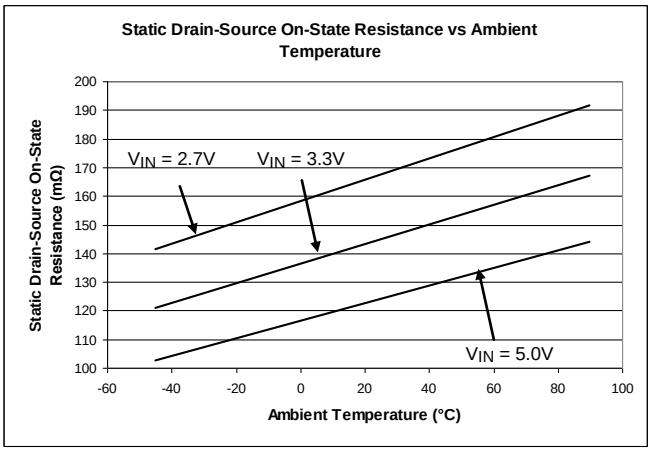


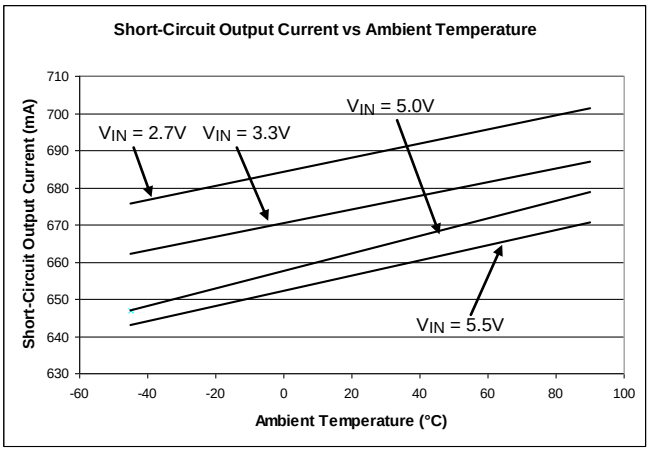


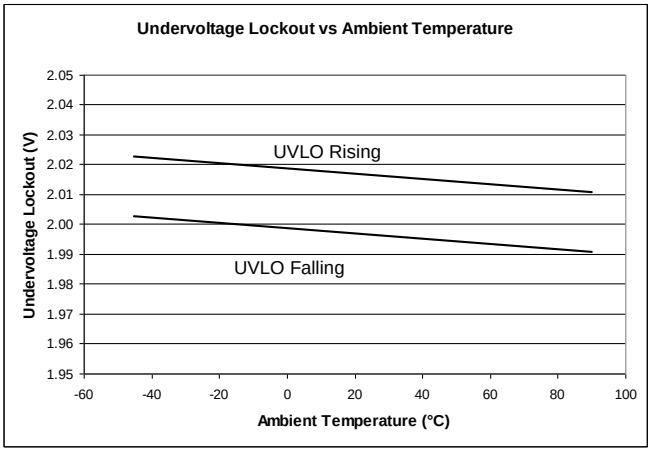
Typical Performance Characteristics (Cont.)

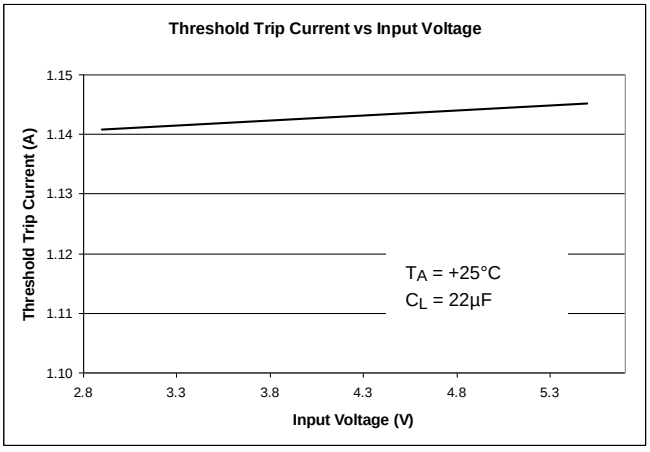




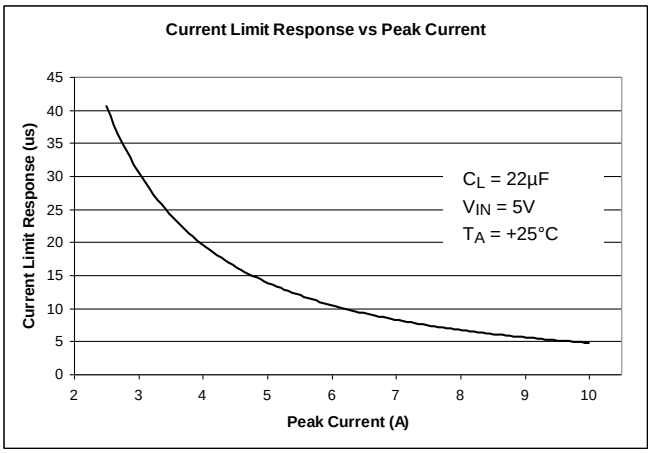








Typical Performance Characteristics (Cont.)



Application Information

Power Supply Considerations

A 0.01µF to 0.1µF X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the input (10µF minimum) and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01µF to 0.1µF ceramic capacitor improves the immunity of the device to short-circuit transients.

Over-current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before V_{IN} has been applied. The AP2141/AP2151 senses the short circuit and immediately clamps output current to a certain safe level namely I_{SHORT}.

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at I_{LIMIT}.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold (I_{TRIG}) is reached or until the thermal limit of the device is exceeded. The AP2141/AP2151 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at I_{LIMIT}.

Note that when the output has been shorted to GND at extremely low temperature (< -30°C), a minimum 120µF electrolytic capacitor on the output pin is recommended. A correct capacitor type with capacitor voltage rating and temperature characteristics must be properly chosen so that capacitance value does not drop too low at the extremely low temperature operation. A recommended capacitor should have temperature characteristics of less than 10% variation of capacitance change when operated at extremely low temp. Our recommended aluminum electrolytic capacitor type is Panasonic FC series.

FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7ms deglitch timeout. The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 7ms deglitch timeout. The FLG will be triggered at above 500mA to indicate possible Over-Current condition. The AP2141/AP2151 is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.

Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature (T_A) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:
T_A = Ambient temperature °C
$R_{\theta JA}$ = Thermal resistance
P_D = Total power dissipation

Application Information (Cont.)

Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2141/AP2151 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately +140°C due to excessive power dissipation in an over-current or short-circuit condition, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately +25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown or over-current occurs with 7ms deglitch.

Under-Voltage Lockout (UVLO)

Undervoltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 1.9V, even if the switch is enabled. Whenever the input voltage falls below approximately 1.9V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

Host/Self-Powered HUBs

Hosts and self-powered hubs (SPH) have a local power supply that powers the embedded functions and the downstream ports (see Figure 2). This power supply must provide from 5.25V to 4.75V to the board side of the downstream connection under both full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

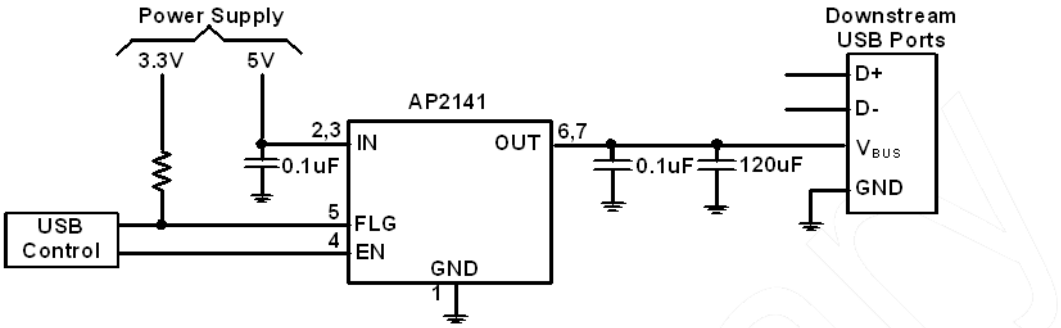


Figure 2. Typical One-Port USB Host / Self-Powered Hub

Generic Hot-Plug Applications

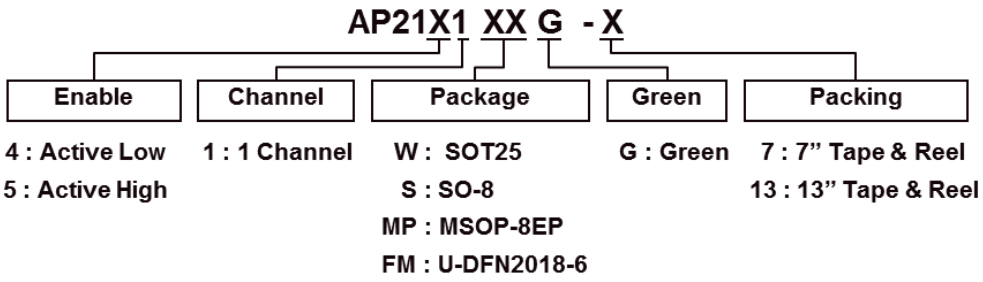
In many applications it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise and fall times of the AP2141/AP2151, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2141/AP2151 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

By placing the AP2141/AP2151 between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.

Dual-Purpose Port Applications

AP2141/AP2151 is not recommended for use in dual-purpose port applications in which a single port is used for data communication between the host and peripheral devices while simultaneously maintaining a charge to the battery of the peripheral device. An example of such a non-recommended application is a shared HDMI/MHL (Mobile High-definition Link) port that allows streaming video between an HDTV or set-top box and a smartphone or tablet while maintaining a charge to the smartphone or tablet battery. If a voltage is maintained across the output of the AP2141/AP2151 when the output is disabled and the V_{IN} of the device is subsequently ramped up, an overstress condition to the AP2141/AP2151 may result.

Ordering Information

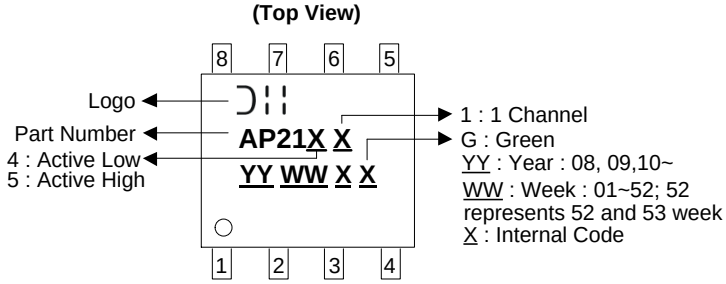


Part Number	Package Code	Packaging (Note 10)	7" / 13" Tape and Reel	
			Quantity	Part Number Suffix
AP21X1WG-7	W	SOT25	3,000/Tape & Reel	-7
AP21X1SG-13	S	SO-8	2,500/Tape & Reel	-13
AP21X1MPG-13	MP	MSOP-8EP	2,500/Tape & Reel	-13
AP21X1FMG-7	FM	U-DFN2018-6	3,000/Tape & Reel	-7

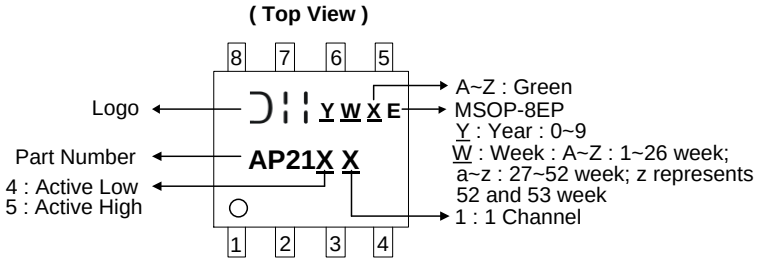
Note: 10. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

(1) SO-8



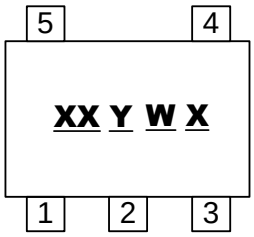
(2) MSOP-8EP



Marking Information (Cont.)

(3) SOT25

(Top View)

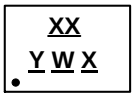


XX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Green

Device	Package Type	Identification Code
AP2141W	SOT25	HR
AP2151W	SOT25	HS

(4) U-DFN2018-6

(Top View)



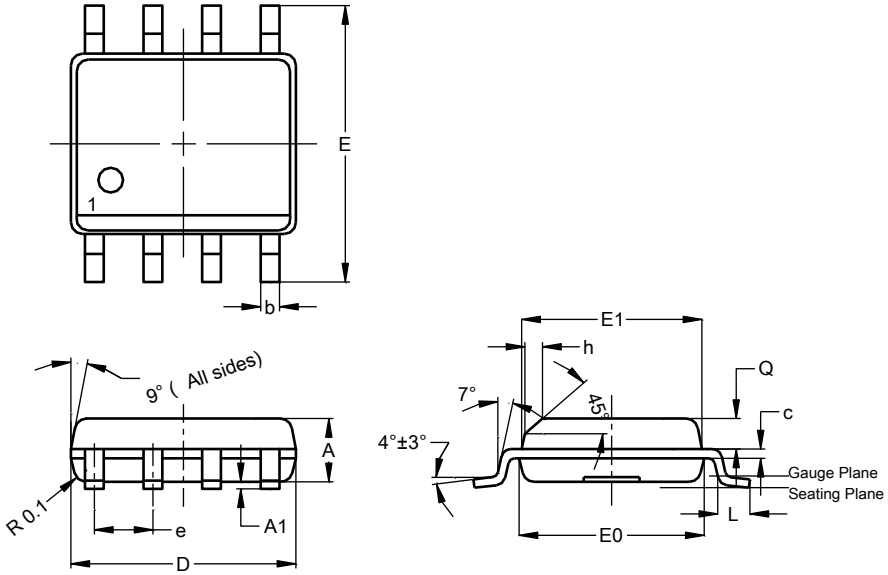
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Green

Device	Package Type	Identification Code
AP2141FM	U-DFN2018-6	HR
AP2151FM	U-DFN2018-6	HS

Package Outline Dimensions

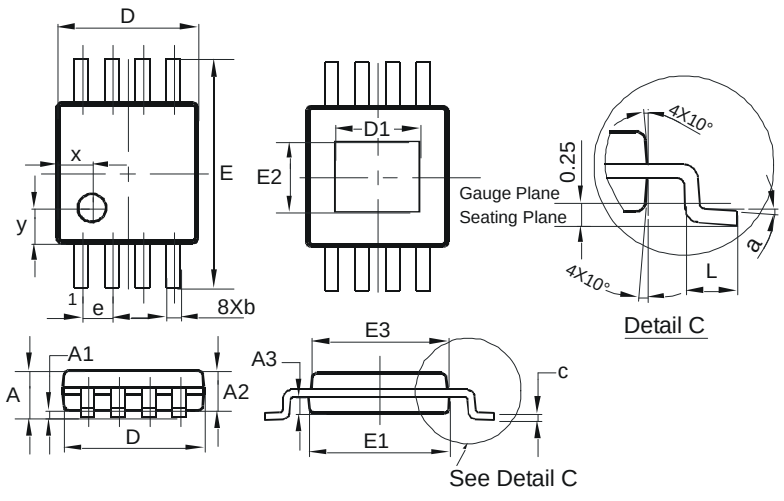
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) SO-8



SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

(2) MSOP-8EP

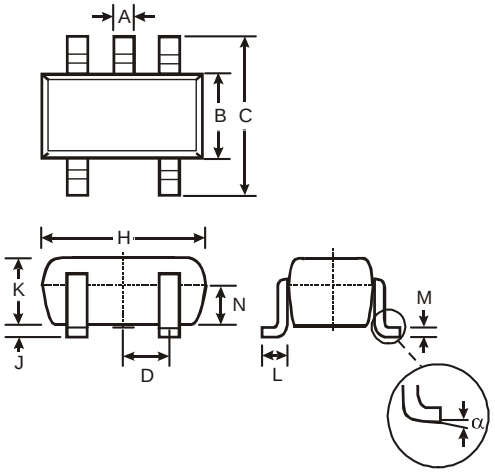


MSOP-8EP			
Dim	**Min**	**Max**	**Typ**
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

Package Outline Dimensions (Cont.)

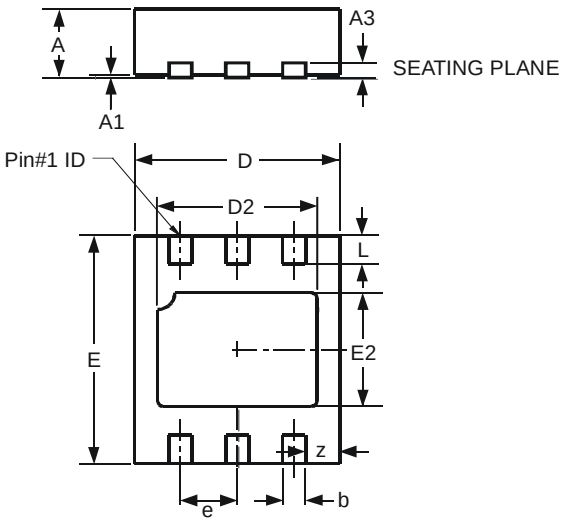
Please see http://www.diodes.com/package-outlines.html for the latest version.

(3) SOT25



SOT25			
Dim	**Min**	**Max**	**Typ**
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	—	—	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	—
All Dimensions in mm			

(4) U-DFN2018-6

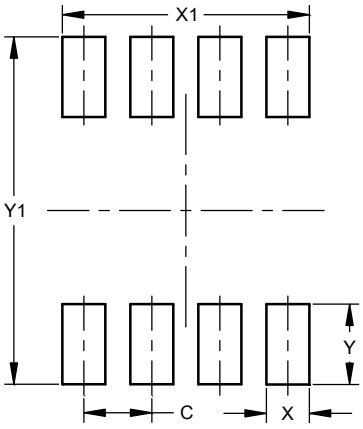


U-DFN2018-6			
Dim	**Min**	**Max**	**Typ**
A	0.545	0.605	0.575
A1	0	0.05	0.02
A3	—	—	0.13
b	0.15	0.25	0.20
D	1.750	1.875	1.80
D2	1.30	1.50	1.40
e	—	—	0.50
E	1.95	2.075	2.00
E2	0.90	1.10	1.00
L	0.20	0.30	0.25
z	—	—	0.30
All Dimensions in mm			

Suggested Pad Layout

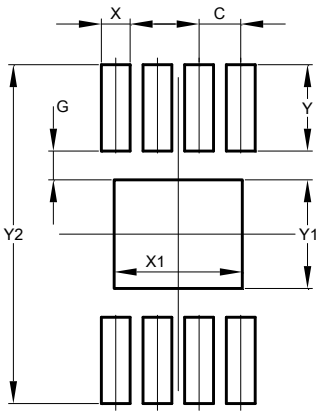
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) SO-8



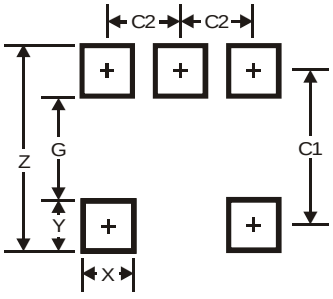
Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

(2) MSOP-8EP



Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

(3) SOT25

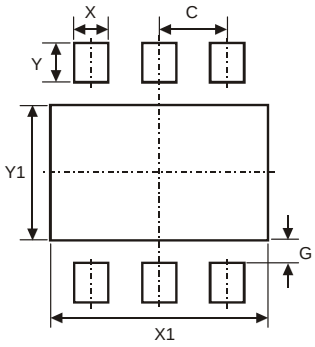


Dimensions	Value
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

Suggested Pad Layout (Cont.)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(4) U-DFN2018-6



Dimensions	Value (in mm)
C	0.50
G	0.20
X	0.25
X1	1.60
Y	0.35
Y1	1.20

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