THE DATASHEET OF

MRFE6S9125NR1

Freescale Semiconductor
Technical Data

Document Number: MRFE6S9125N
Rev. 0, 10/2007

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRFE6S9125NR1
MRFE6S9125NBR1

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

880 MHz, 27 W AVG., 28 V
SINGLE N-CDMA, GSM EDGE
LATERAL N-CHANNEL
RF POWER MOSFETs

N-CDMA Application

- Typical Single-Carrier N-CDMA Performance @ 880 MHz, V_{DD} = 28 Volts, I_{DQ} = 950 mA, P_{out} = 27 Watts Avg., IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13) Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
  Power Gain — 20.2 dB
  Drain Efficiency — 31%
  ACPR @ 750 kHz Offset = -45.7 dBc in 30 kHz Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 880 MHz, 3 dB Overdrive, Designed for Enhanced Ruggedness

GSM EDGE Application

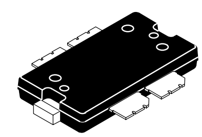
- Typical GSM EDGE Performance: V_{DD} = 28 Volts, I_{DQ} = 700 mA, P_{out} = 60 Watts Avg., Full Frequency Band (865-960 MHz or 920-960 MHz)
  Power Gain — 20 dB
  Drain Efficiency — 40%
  Spectral Regrowth @ 400 kHz Offset = -63 dBc
  Spectral Regrowth @ 600 kHz Offset = -78 dBc
  EVM — 1.8% rms

GSM Application

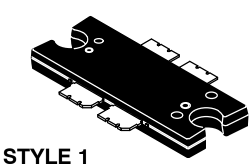
- Typical GSM Performance: V_{DD} = 28 Volts, I_{DQ} = 700 mA, P_{out} = 125 Watts, Full Frequency Band (920-960 MHz)
  Power Gain — 19 dB
  Drain Efficiency — 62%

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRF6S9125NR1



CASE 1484-04, STYLE 1
TO-272 WB-4
PLASTIC
MRF6S9125NBR1

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +66	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +12	Vdc
Maximum Operation Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 125 W CW Case Temperature 76°C, 27 W CW	$R_{\theta JC}$	 0.44 0.45	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Tools (Software & Tools)/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

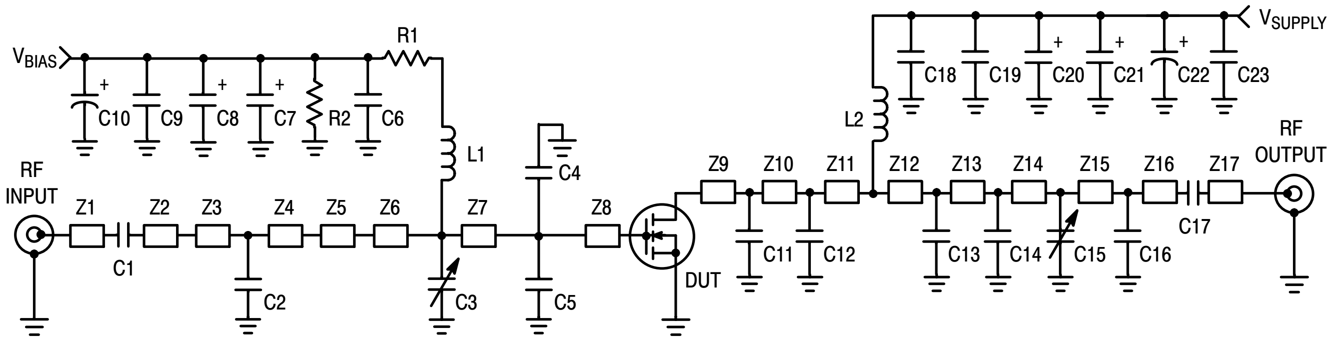
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 66 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	10	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 400 μAdc)	$V_{GS(th)}$	1	2.1	3	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 950 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2	2.86	4	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.74 Adc)	$V_{DS(on)}$	0.05	0.24	0.3	Vdc
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.9	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	64	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	350	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 950 mA, P_{out} = 27 W Avg. N-CDMA, f = 880 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Channel Bandwidth @ ±750 kHz Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF.					
Power Gain	G_{ps}	19	20.2	24	dB
Drain Efficiency	η_D	29	31	—	%
Adjacent Channel Power Ratio	ACPR	—	-45.7	-44	dBc
Input Return Loss	IRL	—	-18	-9	dB

1. Part is internally input matched.

(continued)

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 700 mA, P_{out} = 60 W Avg., 920-960 MHz, EDGE Modulation					
Power Gain	G_{ps}	—	20	—	dB
Drain Efficiency	η_D	—	40	—	%
Error Vector Magnitude	EVM	—	1.8	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-63	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-78	—	dBc
Typical CW Performances (In Freescale GSM Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 700 mA, P_{out} = 125 W, 920-960 MHz					
Power Gain	G_{ps}	—	19	—	dB
Drain Efficiency	η_D	—	62	—	%
Input Return Loss	IRL	—	-12	—	dB
P_{out} @ 1 dB Compression Point, CW (f = 880 MHz)	P1dB	—	125	—	W
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 950 mA, 865-900 MHz Bandwidth					
Video Bandwidth @ 125 W PEP P_{out} where IM3 = -30 dBc (Tone Spacing from 100 kHz to VBW) ΔIMD3 = IMD3 @ VBW frequency - IMD3 @ 100 kHz <1 dBc (both sidebands)	VBW	—	10	—	MHz
Gain Flatness in 35 MHz Bandwidth @ P_{out} = 27 W Avg.	G_F	—	0.93	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.011	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.205	—	dBm/°C



Z1, Z17	0.200″ x 0.080″ Microstrip	Z10	0.057″ x 0.620″ Microstrip
Z2	1.060″ x 0.080″ Microstrip	Z11	0.119″ x 0.620″ Microstrip
Z3	0.382″ x 0.220″ Microstrip	Z12	0.450″ x 0.220″ Microstrip
Z4	0.108″ x 0.220″ Microstrip	Z13	0.061″ x 0.220″ Microstrip
Z5	0.200″ x 0.420″ x 0.620″ Taper	Z14	0.078″ x 0.220″ Microstrip
Z6	0.028″ x 0.620″ Microstrip	Z15	0.692″ x 0.080″ Microstrip
Z7	0.236″ x 0.620″ Microstrip	Z16	0.368″ x 0.080″ Microstrip
Z8	0.050″ x 0.620″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030″, ε_r = 2.55
Z9	0.238″ x 0.620″ Microstrip		

Figure 1. MRFE6S9125NR1(NBR1) Test Circuit Schematic

Table 6. MRFE6S9125NR1(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	20 pF Chip Capacitor	ATC100B200FT500XT	ATC
C2	6.2 pF Chip Capacitor	ATC100B6R2BT500XT	ATC
C3, C15	0.8-8.0 pF Variable Capacitors, Gigatrim	27291SL	Johanson
C4, C5	11 pF Chip Capacitors	ATC100B110FT500XT	ATC
C6, C18, C19	0.56 μF, 50 V Chip Capacitors	C1825C564J5RAC	Kemet
C7, C8	47 μF, 16 V Tantalum Capacitors	T491B476K016AT	Kemet
C9, C23	47 pF Chip Capacitors	ATC700B470FT500XT	ATC
C10	100 μF, 50 V Electrolytic Capacitor	MCHT101M1HB-1017-RH	Multicomp
C11, C12	12 pF Chip Capacitors	ATC100B120FT250XT	ATC
C13, C14	5.1 pF Chip Capacitors	ATC100B5R1BT250XT	ATC
C16	0.3 pF Chip Capacitor	ATC700B0R3BT500XT	ATC
C17	39 pF Chip Capacitor	ATC700B390FT500XT	ATC
C20, C21	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C22	470 μF, 63 V Electrolytic Capacitor	EKME630ELL471MK25S	Multicomp
L1	7.15 nH Inductor	1606-7J	CoilCraft
L2	8.0 nH Inductor	A03T	CoilCraft
R1	15 Ω, 1/3 W Chip Resistor	CRCW121015R0FKEA	Vishay
R2	560 kΩ, 1/4 W Resistor	CRCW12065600FKEA	Vishay

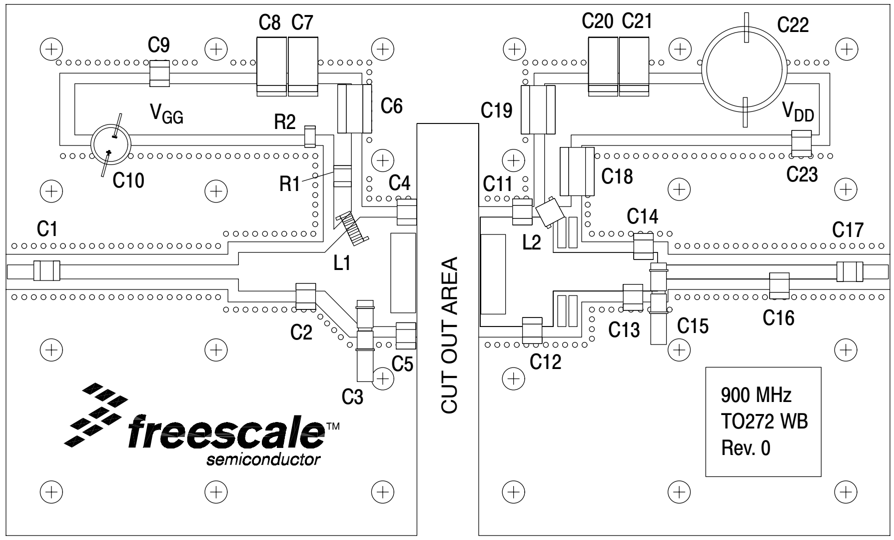


Figure 2. MRFE6S9125NR1(NBR1) Test Circuit Component Layout

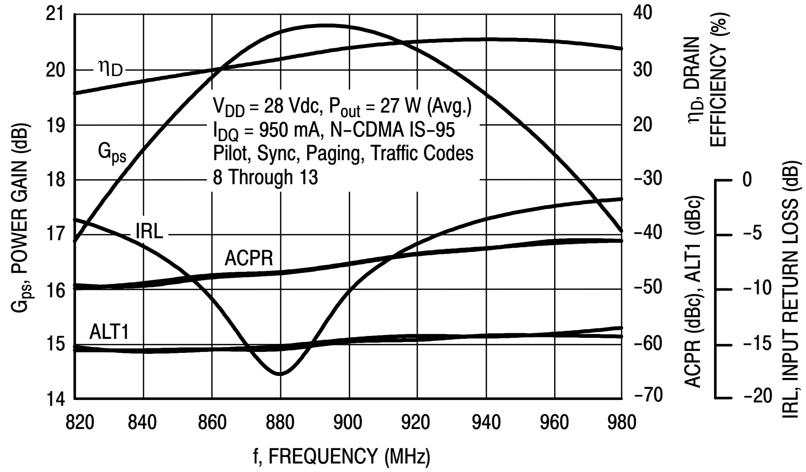


Figure 3. Single-Carrier N-CDMA Broadband Performance @ P_{out} = 27 Watts Avg.

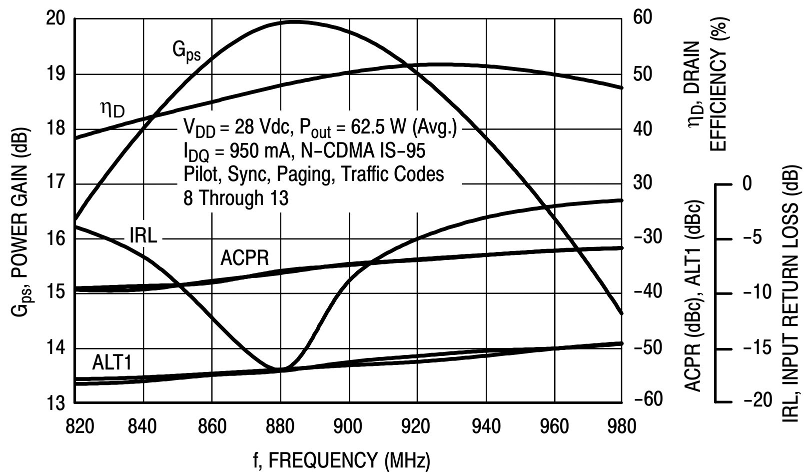


Figure 4. Single-Carrier N-CDMA Broadband Performance @ P_{out} = 62.5 Watts Avg.

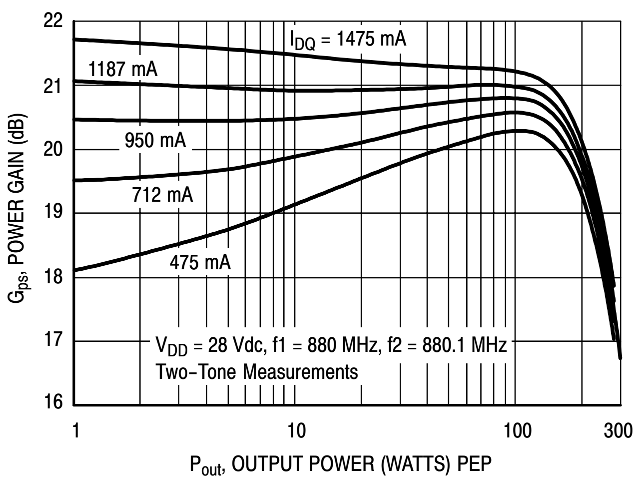


Figure 5. Two-Tone Power Gain versus Output Power

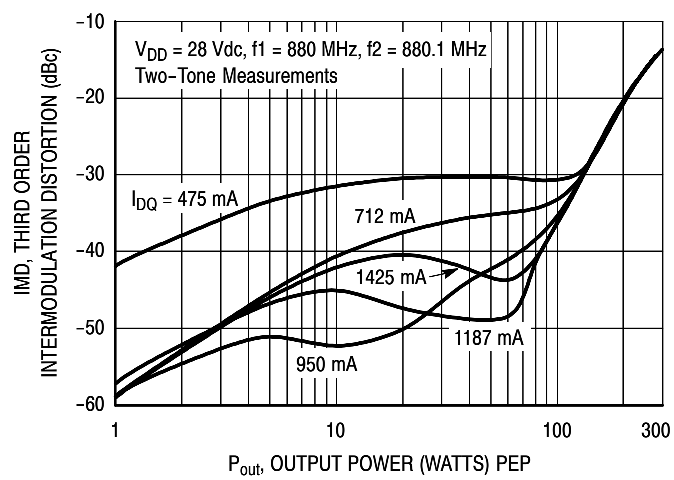


Figure 6. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

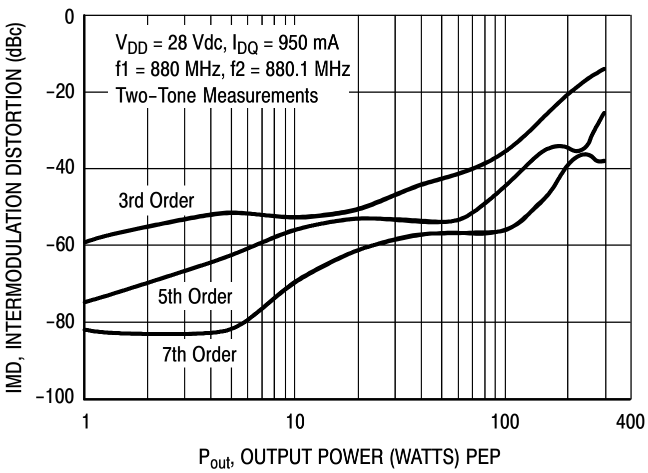


Figure 7. Intermodulation Distortion Products versus Output Power

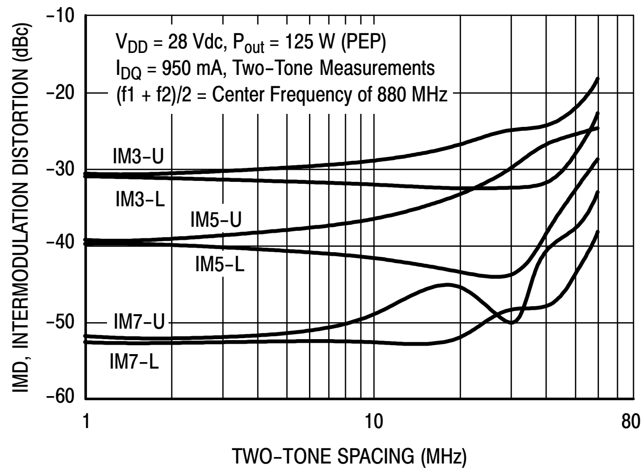


Figure 8. Intermodulation Distortion Products versus Tone Spacing

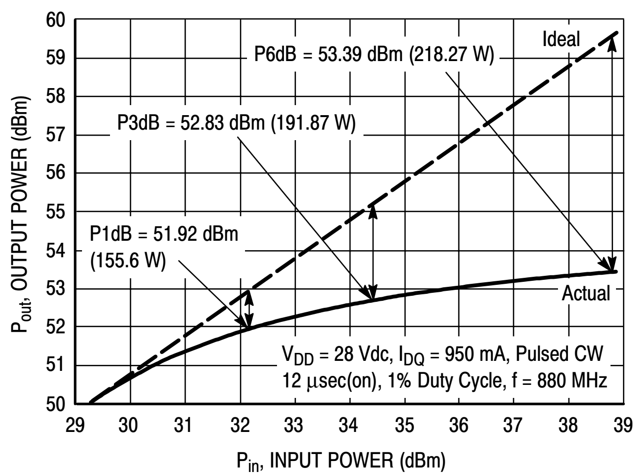


Figure 9. Pulsed CW Output Power versus Input Power

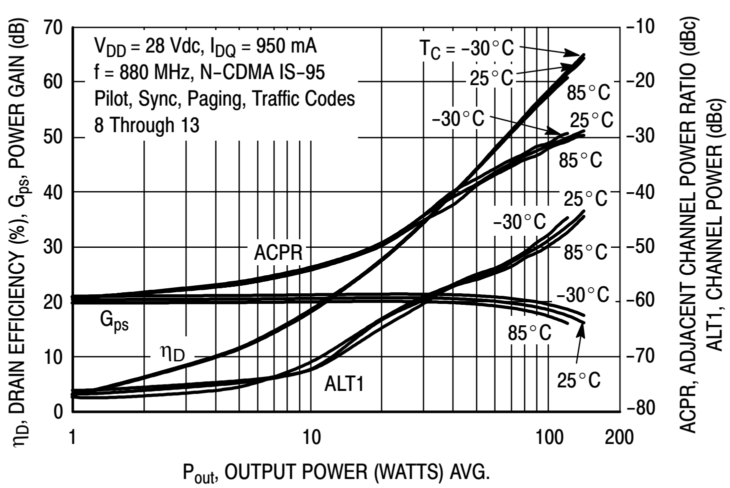


Figure 10. Single-Carrier N-CDMA ACPR, ALT1, Power Gain and Drain Efficiency versus Output Power

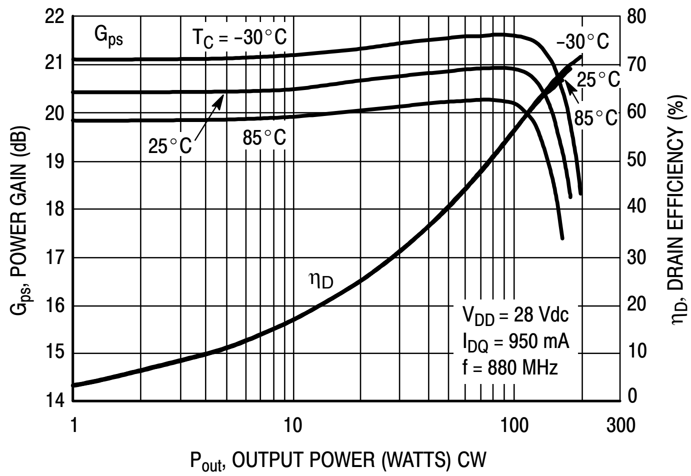


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

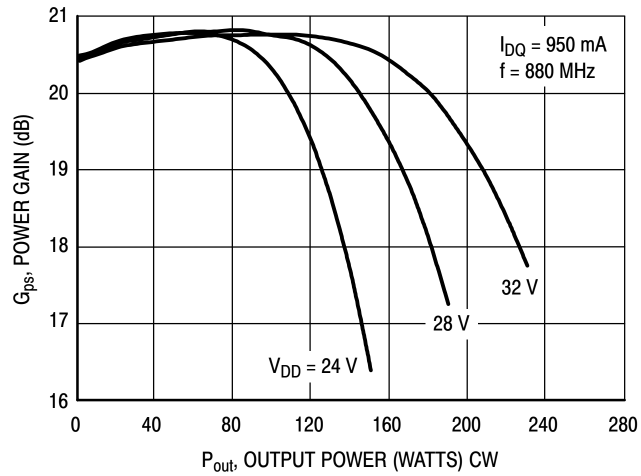
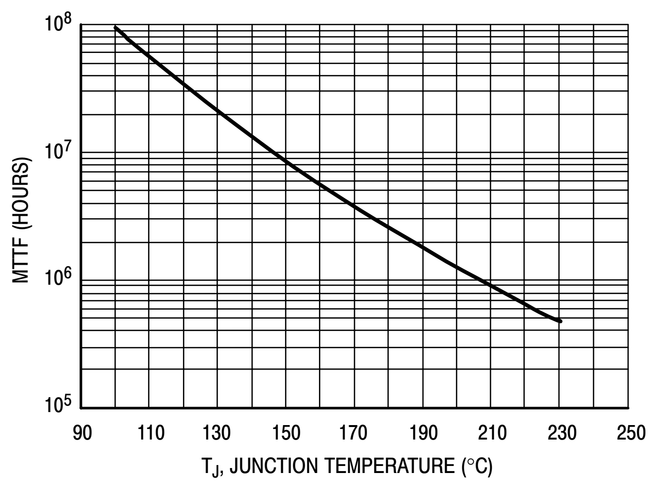


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 27 W Avg., and η_D = 31%.

MTTF calculator available at http://www.freescale.com/rf. Select Tools (Software & Tools)/Calculators to access MTTF calculators by product.

Figure 13. MTTF versus Junction Temperature

N-CDMA TEST SIGNAL

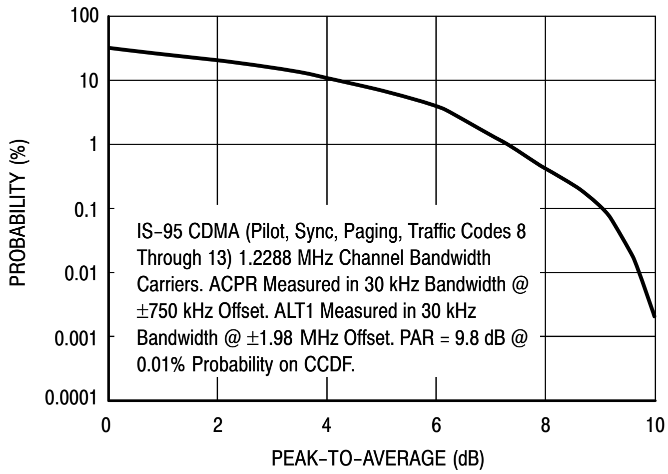


Figure 14. Single-Carrier CCDF N-CDMA

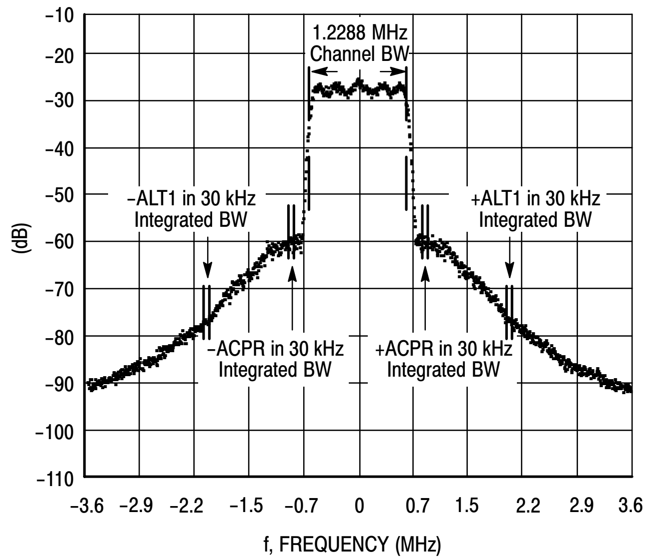
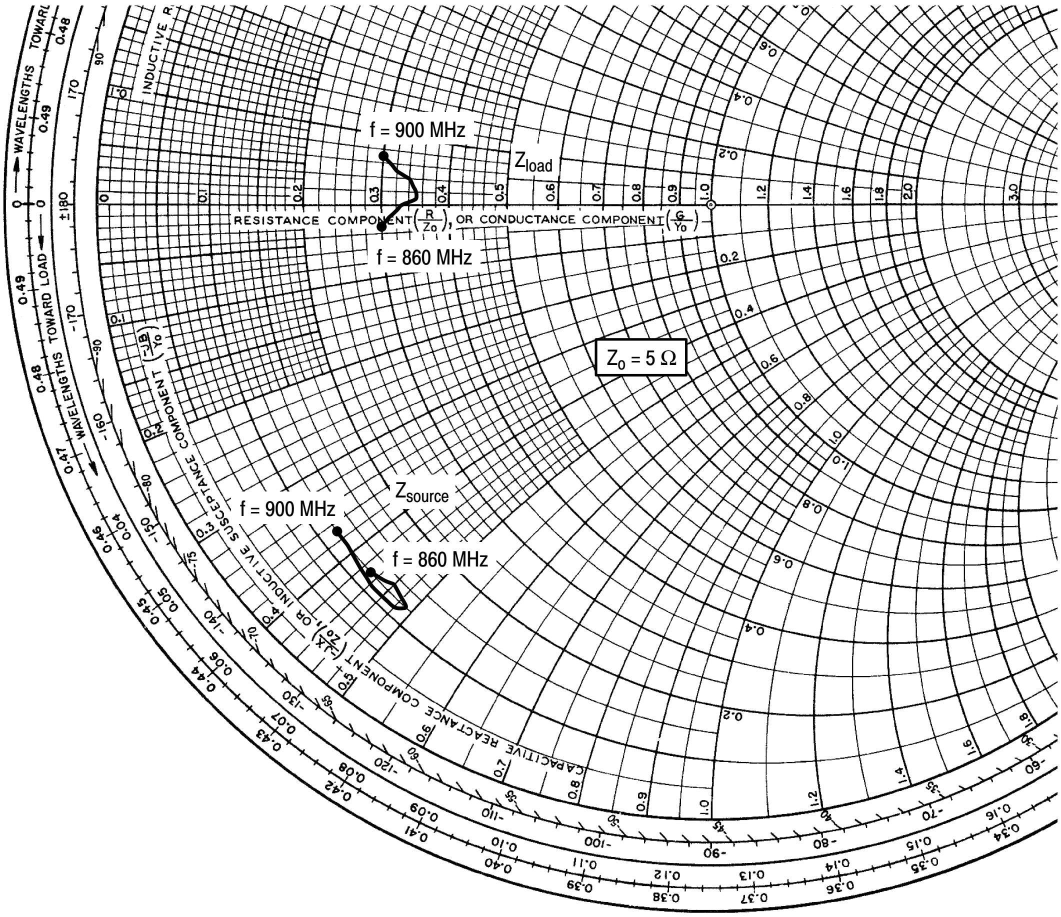


Figure 15. Single-Carrier N-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 950 mA, P_{out} = 27 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
860	0.62 - j2.13	1.48 - j0.14
865	0.64 - j2.31	1.56 - j0.09
870	0.62 - j2.45	1.66 - j0.02
875	0.59 - j2.43	1.73 + j0.04
880	0.57 - j2.42	1.74 + j0.11
885	0.54 - j2.36	1.68 + j0.19
890	0.57 - j2.18	1.61 + j0.25
895	0.58 - j1.94	1.52 + j0.33
900	0.59 - j1.86	1.48 + j0.37

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

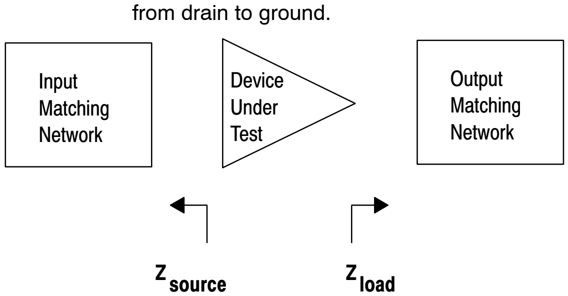
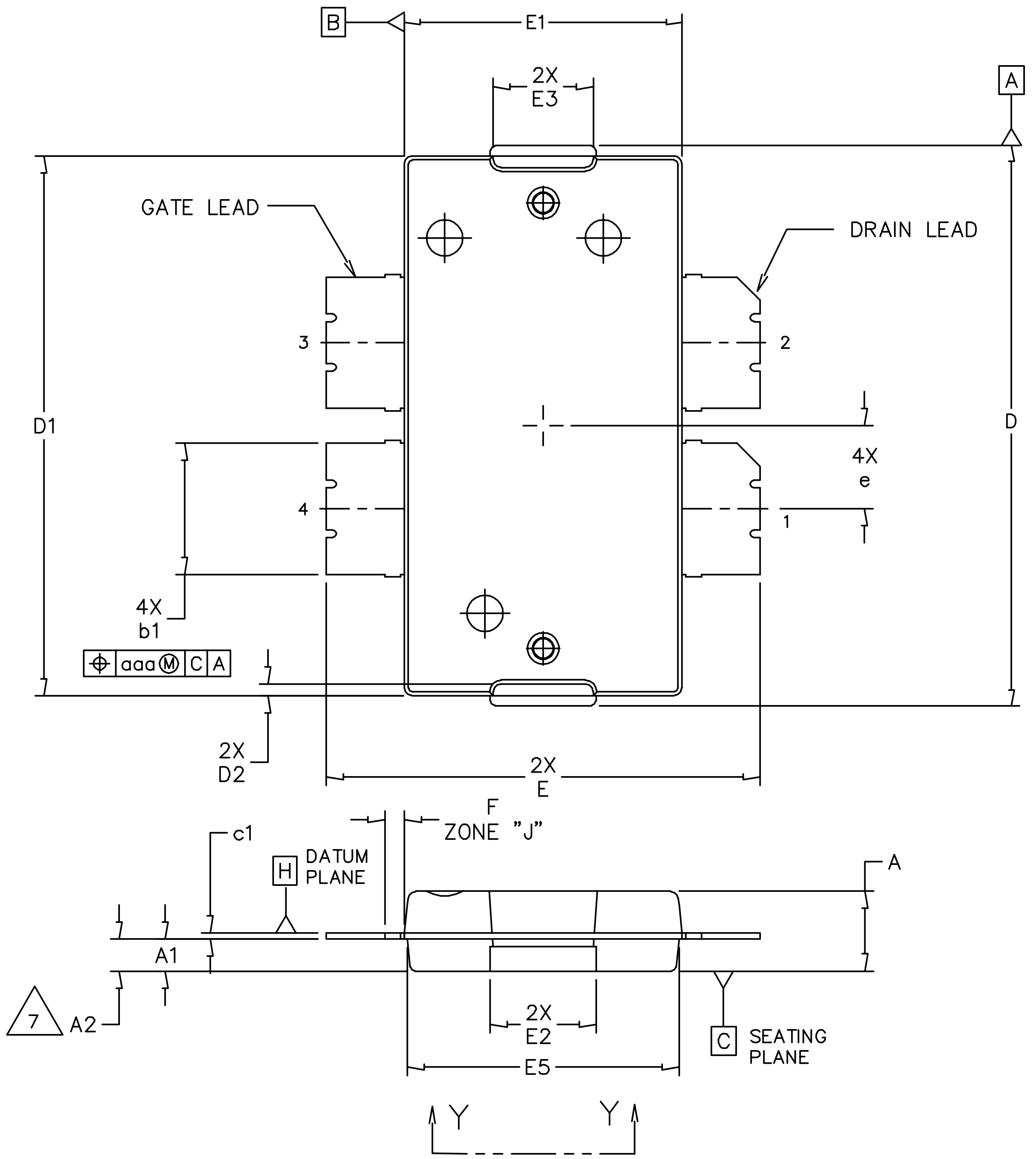


Figure 16. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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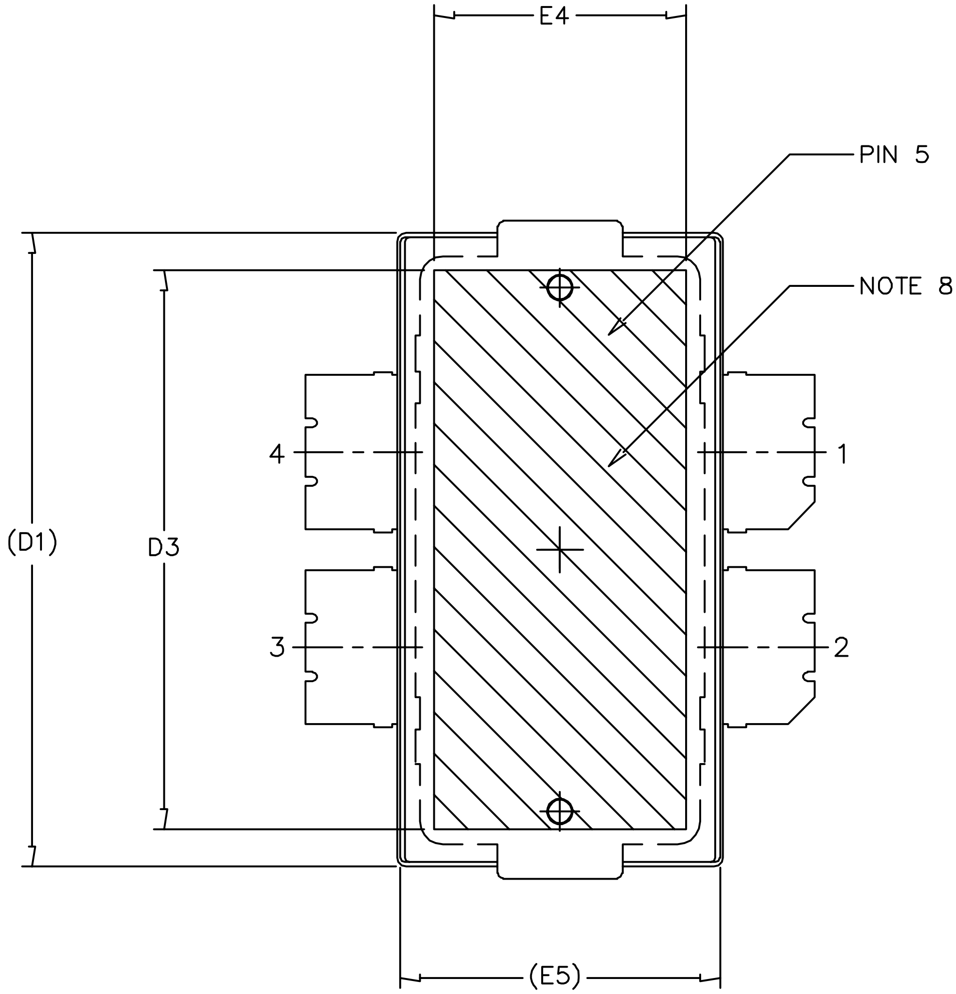
		CASE NUMBER: 1486−03	13 AUG 2007
		STANDARD: NON−JEDEC	



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TITLE: TO–270 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10577D	REV: D
	CASE NUMBER: 1486–03	13 AUG 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – DRAIN
PIN 3 – GATE
PIN 4 – GATE
PIN 5 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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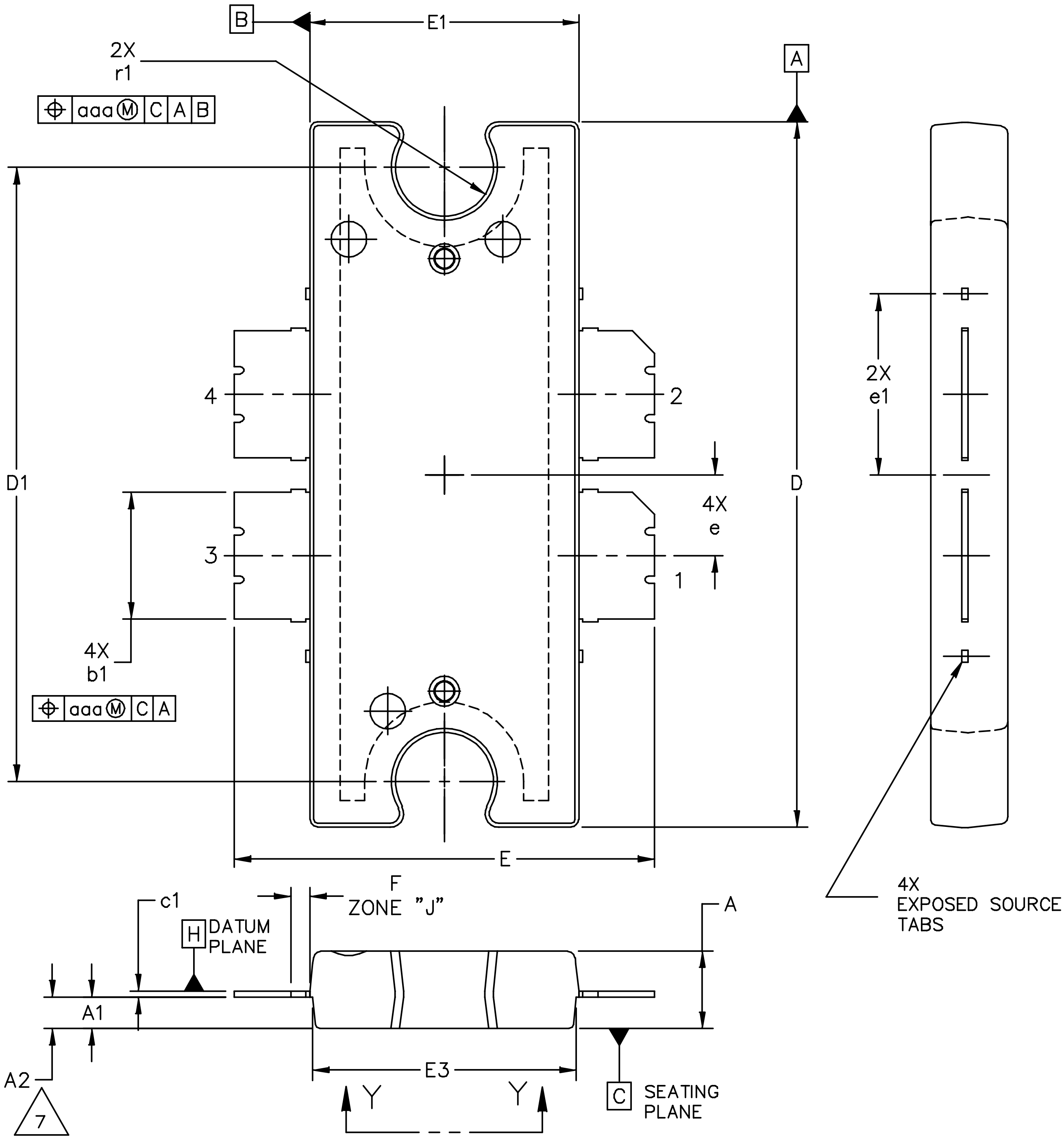

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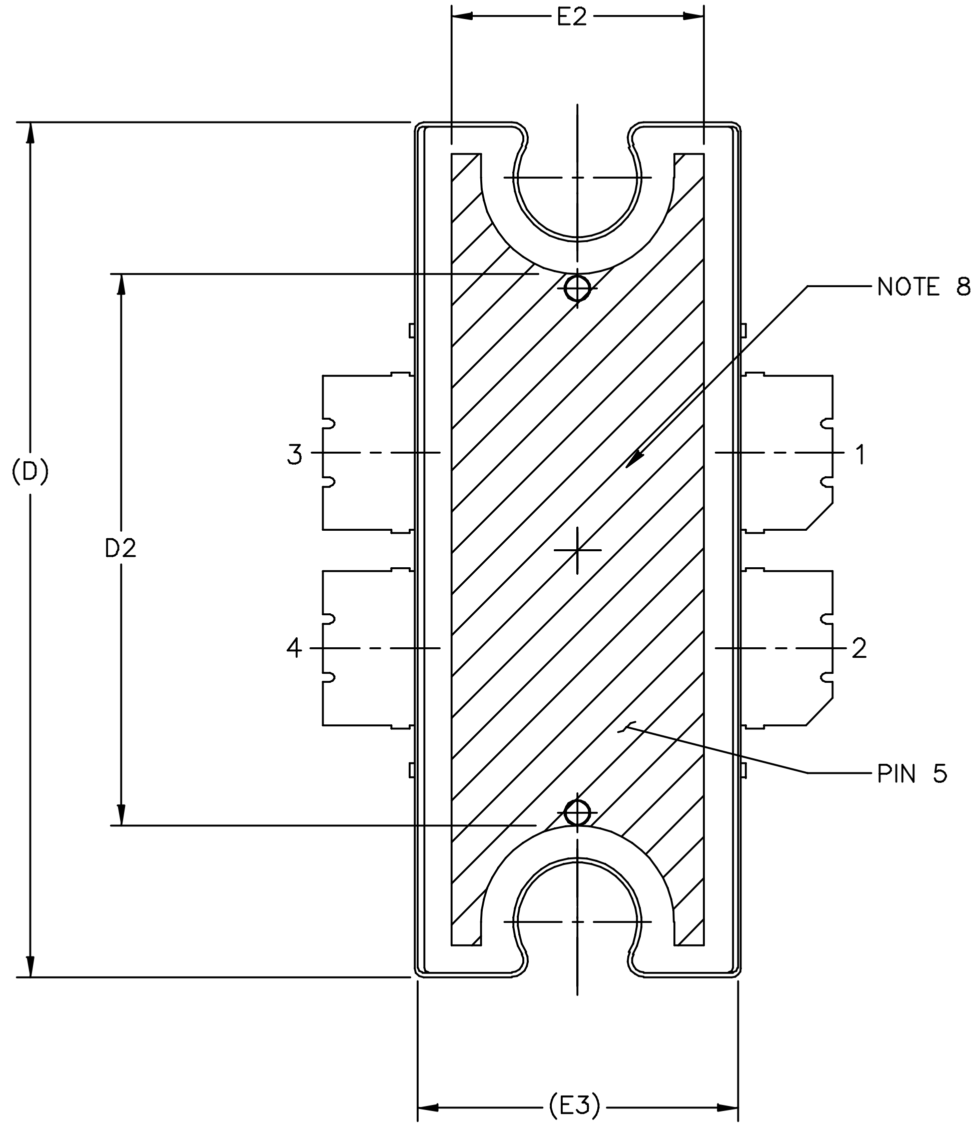

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	CASE NUMBER: 1484−04	31 AUG 2007
	STANDARD: NON−JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
PIN 1 – DRAIN PIN 2 – DRAIN
PIN 3 – GATE PIN 4 – GATE
PIN 5 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO–272 4 LEAD WIDE BODY	DOCUMENT NO: 98ASA10575D	REV: E
	CASE NUMBER: 1484–04	31 AUG 2007
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2007	• Initial Release of Data Sheet

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