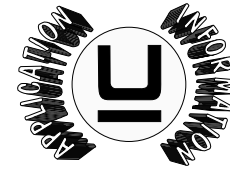




**THE DATASHEET OF  
PIC16LV54A-02/SO**





# Programmable, Off-Line, PWM Controller

## FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current Off Line Start Circuit
- Voltage Feed Forward or Current Mode Control
- High Current Totem Pole Output
- 50% Absolute Max Duty Cycle
- PWM Latch for Single Pulse Per Period
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On Both Initially and After Fault Shutdown
- Shutdown Upon Over or Under Voltage Sensing
- Latch Off or Continuous Retry After Fault
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL or 20 Pin PLCC Package

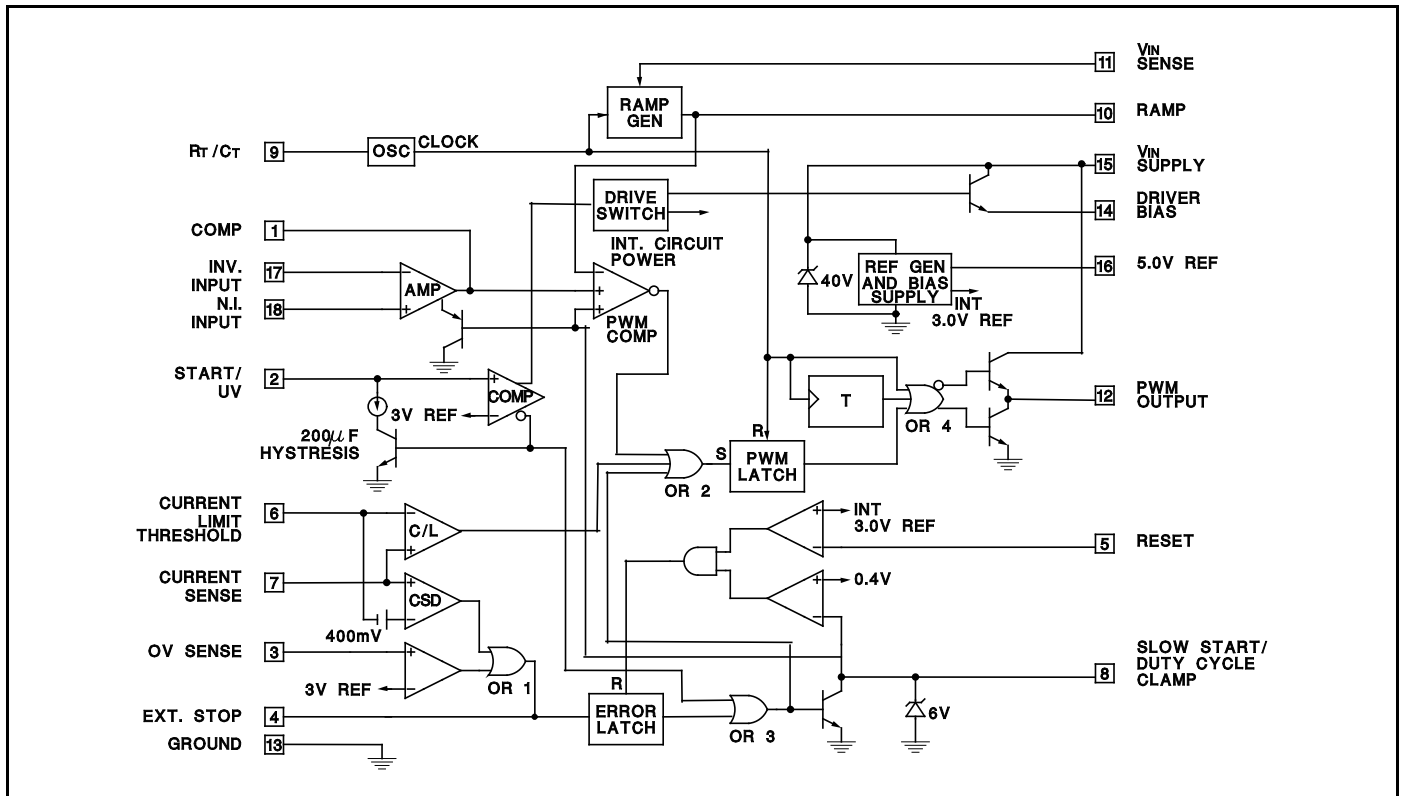
## DESCRIPTION

The UC1851 family of PWM controllers are optimized for off-line primary side control. These devices include a high current totem pole output stage and a toggle flip-flop for absolute 50% duty cycle limiting. In all other respects this line of controllers is pin for pin compatible with the UC1841 series. Inclusion of all major housekeeping functions in these high performance controllers makes them ideal for use in cost sensitive applications.

Important features of these controllers include low current start-up, linear feed-forward for constant volt-second operation, and compatibility with both voltage or current mode control. In addition, these devices include a programmable start threshold, as well as programmable over-voltage, under-voltage, and over current fault thresholds. The fault latch on these devices can be configured for automatic restart, or latched off response to a fault.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages, or for surface mount applications, a 20 Pin PLCC. The UC1851 is characterized for -55°C to +125°C operation while the UC2851 and UC3851 are designed for -40°C to +85°C and 0°C to +70°C, respectively.

## BLOCK DIAGRAM

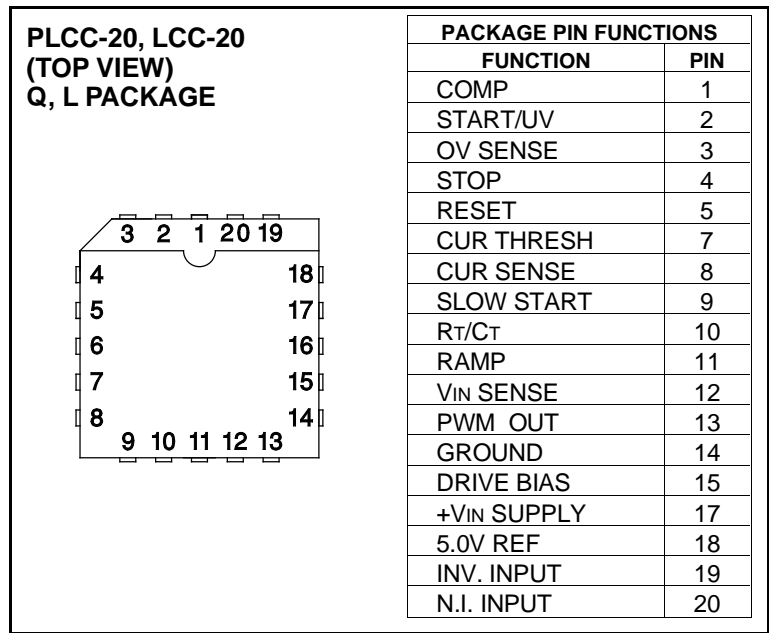
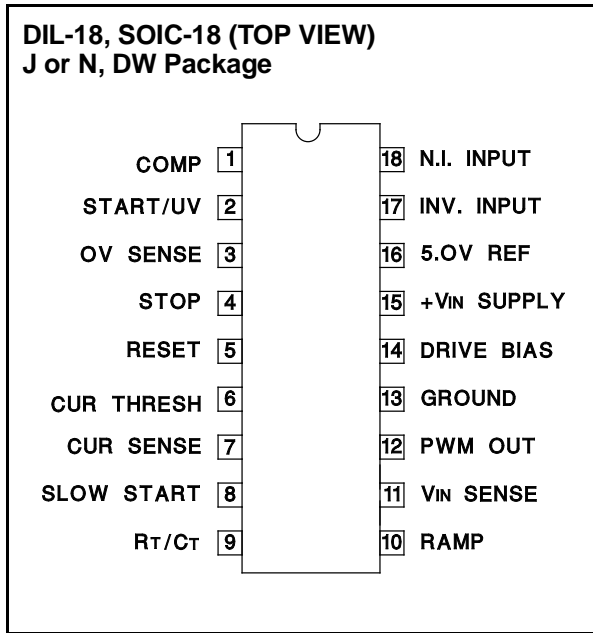


**ABSOLUTE MAXIMUM RATINGS (Note 1)**

Supply Voltage, +VIN (Pin 15)	
Voltage Driven	+32V
Current Driven, 100mA maximum	Self-limiting
PWM Output Voltage (Pin 12)	40V
PWM Output Current, Steady-State (Pin 12)	400mA
PWM Output Peak Energy Discharge	20μJoules
Driver Bias Current (Pin 14)	-200mA
Reference Output Current (Pin 16)	-50mA
Slow-Start Sink Current (Pin 8)	20mA
VIN Sense Current (Pin 11)	10mA
Current Limit Inputs (Pins 6 & 7)	-0.5 to +5.5V
Stop Input (Pin 4)	-0.3 to +5.5V

Comparator Inputs  
(Pins 1–7, 9–11, 16). Internally clamped at 12V  
Power Dissipation at TA = 25°C (Note 3). 1000mW  
Power Dissipation at TC = 25°C (Note 3). 2000mW  
Operating Junction Temperature. -55°C to +150°C  
Storage Temperature Range. -65°C to +150°C  
Lead Temperature (Soldering, 10 sec) +300°C  
*Note 1: All voltages are with respect to ground, Pin 13.*  
*Currents are positive-into, negative-out of the specified terminal*  
*Note 2: All pin numbers are referenced to DIL-18 package.*  
*Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.*

**CONNECTION DIAGRAMS**



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; VIN = 20V, RT = 20kΩ, CT = .001 mfd, RR = 10kΩ, CR = .001mfd. Current Limit Threshold = 200mV, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Power Inputs</b>								
Start-Up Current	VIN = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	VIN = 30V, Pin 2 = 3.5V		15	21		15	21	mA
Supply OV Clamp	VIN = 20mA	33	39	45	33	39	45	V
<b>Reference Section</b>								
Reference Voltage	TJ = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	VIN = 8 to 30V		10	15		10	20	mV
Load Regulation	IL = 0 to 10mA		10	20		10	30	mV
Total Ref Variation	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	VREF = 0, TJ = 25°C		-80	-100		-80	-100	mA
<b>Oscillator</b>								
Nominal Frequency	TJ = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	VIN = 8 to 30V		0.5	1		0.5	1	%
Total Ref Variation	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	RT = 2kΩ, CT = 330pF	500			500			kHz

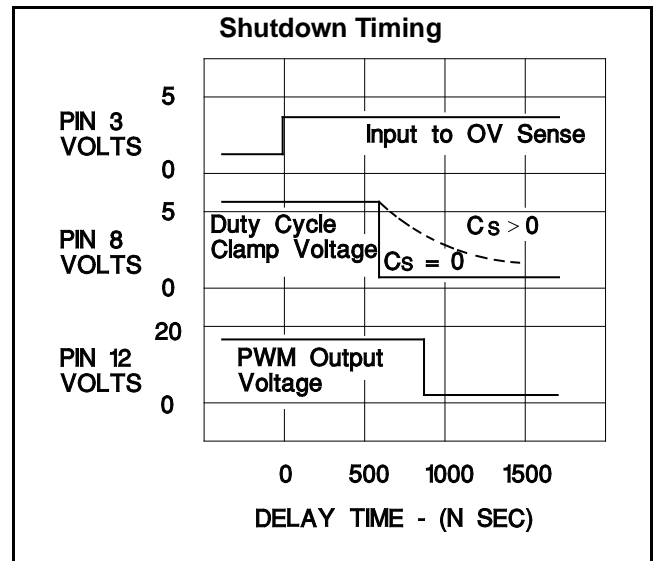
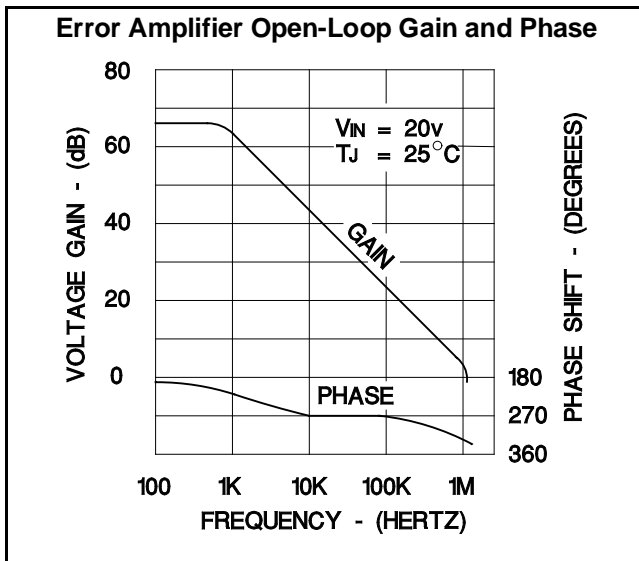
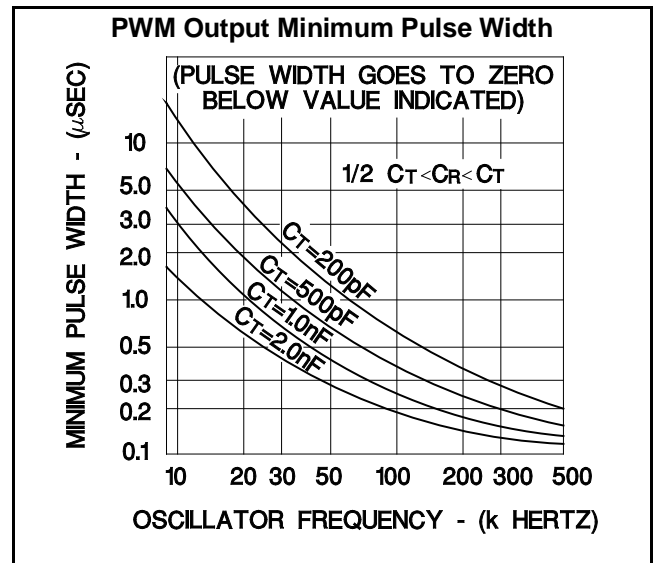
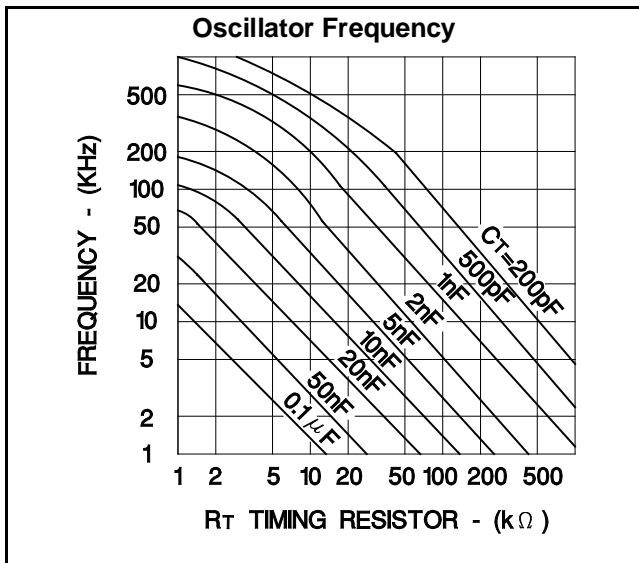
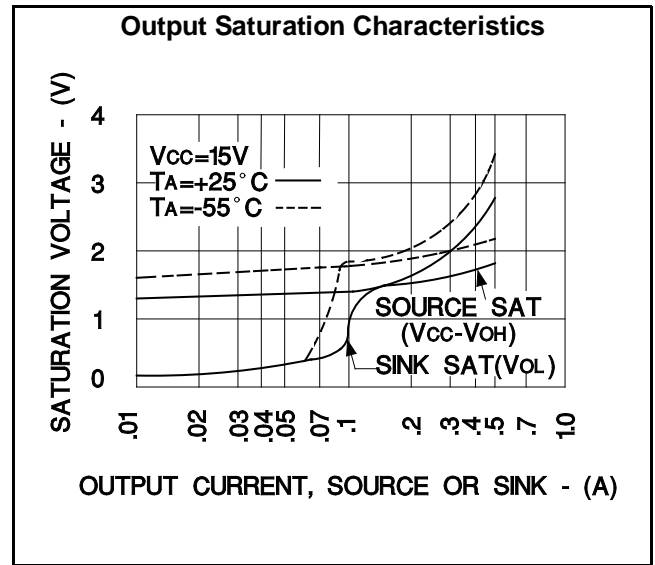
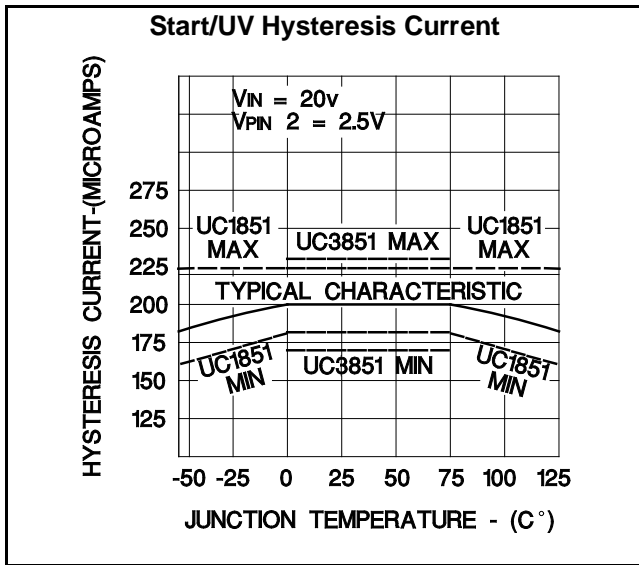
**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for the UC1851,  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  for the UC2851, and  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  for the UC3851;  $V_{IN} = 20\text{V}$ ,  $R_T = 20\text{k}\Omega$ ,  $C_T = .001\text{ mfd}$ ,  $R_R = 10\text{k}\Omega$ ,  $C_R = .001\text{ mfd}$ . Current Limit Threshold =  $200\text{mV}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Ramp Generator</b>								
Ramp Current, Minimum	$I_{SENSE} = -10\mu\text{A}$		-11	-14		-11	-14	$\mu\text{A}$
Ramp Current, Maximum	$I_{SENSE} = 1.0\text{mA}$	-0.9	-95		-0.9	-95		$\text{mA}$
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	$\text{V}$
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	$\text{V}$
<b>Error Amplifier</b>								
Input Offset Voltage	$V_{CM} = 5.0\text{V}$		0.5	5		2	10	$\text{mV}$
Input Bias Current			0.5	2		1	5	$\mu\text{A}$
Input Offset Current				0.5			0.5	$\mu\text{A}$
Open Loop Gain	$\Delta V_O = 1\text{ to }3\text{V}$	60	66		60	66		$\text{dB}$
Output Swing (Max Output $\leq$ Ramp Peak - $100\text{mV}$ )	Minimum Total Range	0.3		3.5	0.3		3.5	$\text{V}$
CMRR	$V_{CM} = 1.5\text{ to }5.5\text{V}$	70	80		70	80		$\text{dB}$
PSRR	$V_{IN} = 8\text{ to }30\text{V}$	70	80		70	80		$\text{dB}$
Short Circuit Current	$V_{COMP} = 0\text{V}$		-4	-10		-4	-10	$\text{mA}$
Gain Bandwidth (Note 1)	$T_J = 25^{\circ}\text{C}$ , $A_{VOL} = 0\text{dB}$	1	2		1	2		$\text{MHz}$
Slew Rate (Note 1)	$T_J = 25^{\circ}\text{C}$ , $A_{VCL} = 0\text{dB}$		0.8			0.8		$\text{V}/\mu\text{s}$
<b>PWM Section</b>								
Continuous Duty Cycle Range (other than zero) (Note 1)	Minimum Total Continuous Range Ramp Peak $< 4.2\text{V}$	2		46	2		46	$\%$
Output High Level	$I_{SOURCE} = 20\text{mA}$	18	18.5		18	18.5		$\text{V}$
	$I_{SOURCE} = 200\text{mA}$	17	18.5		17	18.5		$\text{V}$
Rise Time (Note 1)	$T_J = 25^{\circ}\text{C}$ , $C_L = 1\text{nF}$		50	150		50	150	$\text{ns}$
Fall Time (Note 1)	$T_J = 25^{\circ}\text{C}$ , $C_L = 1\text{nF}$		50	150		50	150	$\text{ns}$
Output Saturation	$I_{OUT} = 20\text{mA}$		0.2	0.4		0.2	0.4	$\text{V}$
	$I_{OUT} = 200\text{mA}$		1.7	2.2		1.7	2.2	$\text{V}$
Comparator Delay (Note 1)	Pin 8 to Pin 12, $T_J = 25^{\circ}\text{C}$ , $R_L = 1\text{k}\Omega$		300	500		300	500	$\text{ns}$
<b>Sequencing Functions</b>								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	$\text{V}$
Input Bias Current	Pins 3, 5 = $0\text{V}$		-1.0	-4.0		-1.0	-4.0	$\mu\text{A}$
Input Leakage	Pins 3, 5 = $10\text{V}$		0.1	2.0		0.1	2.0	$\mu\text{A}$
Start/UV Hysteresis Current	Pin 2 = $2.5\text{V}$	170	200	220	170	200	230	$\mu\text{A}$
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	$\text{V}$
Error Latch Activate Current	Pin 4 = $0\text{V}$ , Pin 3 $> 3\text{V}$		-120	-200		-120	-200	$\mu\text{A}$
Driver Bias Saturation Voltage, $V_{IN-V_{OH}}$	$I_B = -50\text{mA}$		2	3		2	3	$\text{V}$
Driver Bias Leakage	$V_B = 0\text{V}$		-0.1	-10		-0.1	-10	$\mu\text{A}$
Slow-Start Saturation	$I_S = 10\text{mA}$		0.2	0.5		0.2	0.5	$\text{V}$
Slow-Start Leakage	$V_S = 4.5\text{V}$		0.1	2.0		0.1	2.0	$\mu\text{A}$
<b>Current Control</b>								
Current Limit Offset			0	5		0	10	$\text{mV}$
Current Shutdown Offset		370	400	430	360	400	440	$\text{mV}$
Input Bias Current	Pin 7 = $0\text{V}$		-2	-5		-2	-5	$\mu\text{A}$
Common Mode Range (Note 1)		-0.4		3.0	-0.4		3.0	$\text{V}$
Current Limit Delay (Note 1)	$T_J = 25^{\circ}\text{C}$ , Pin 7 to 12, $R_L = 1\text{k}$		200	400		200	400	$\text{ns}$

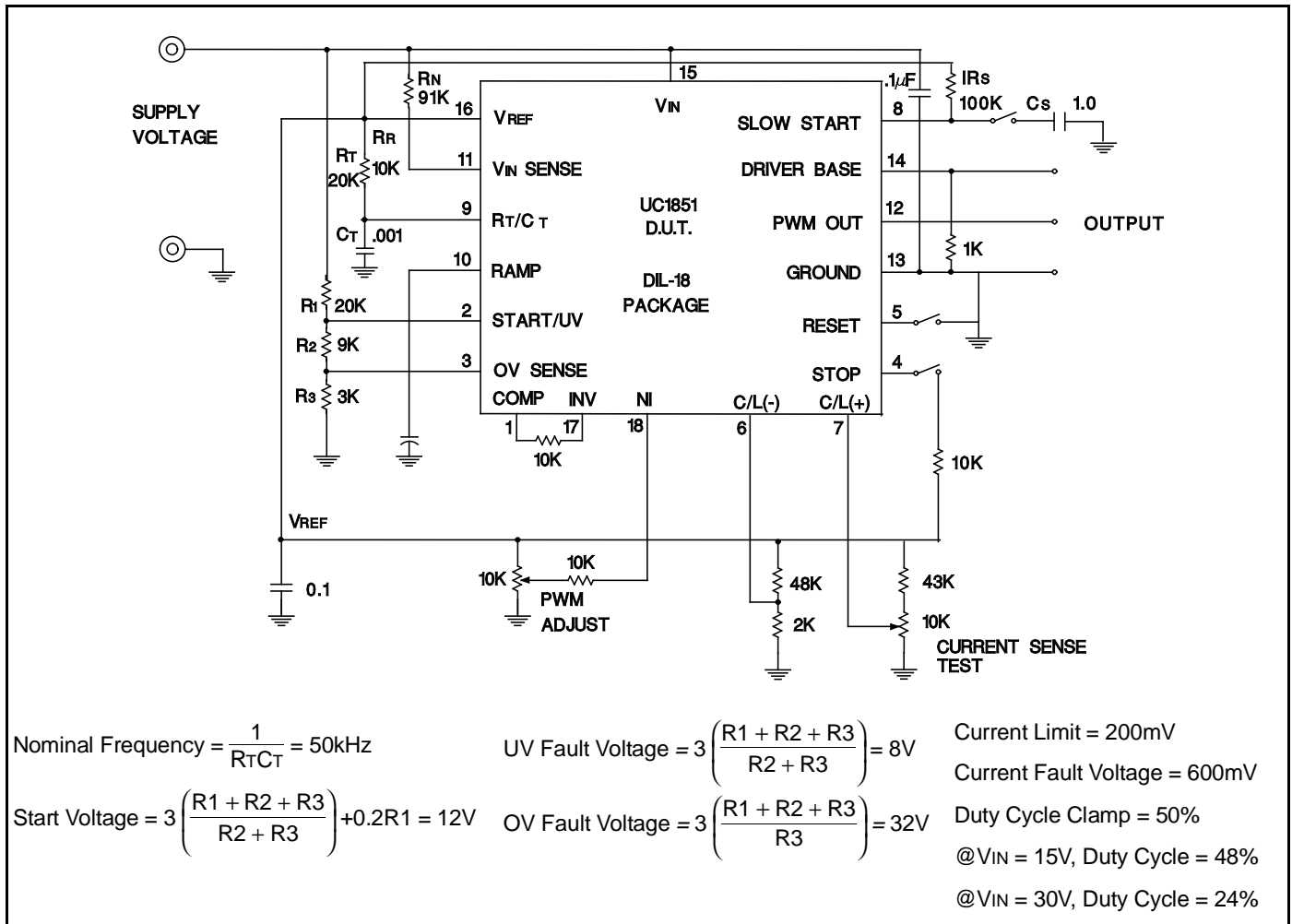
Note 1: Guaranteed by design. Not 100% tested in production.

## FUNCTIONAL DESCRIPTION

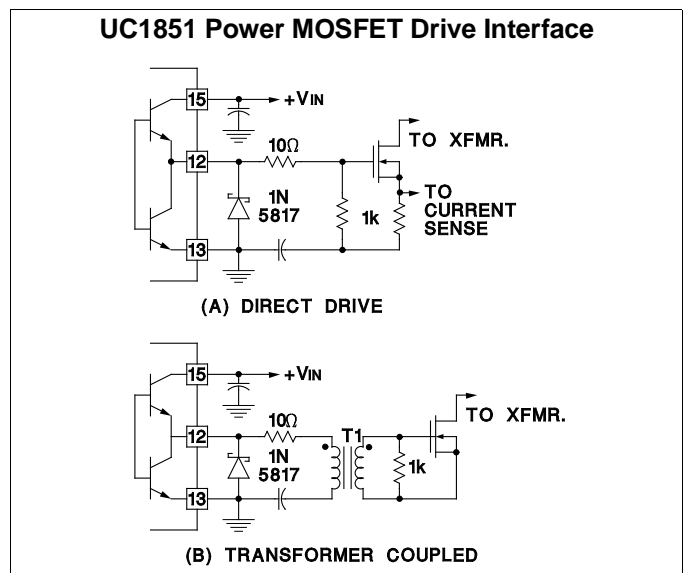
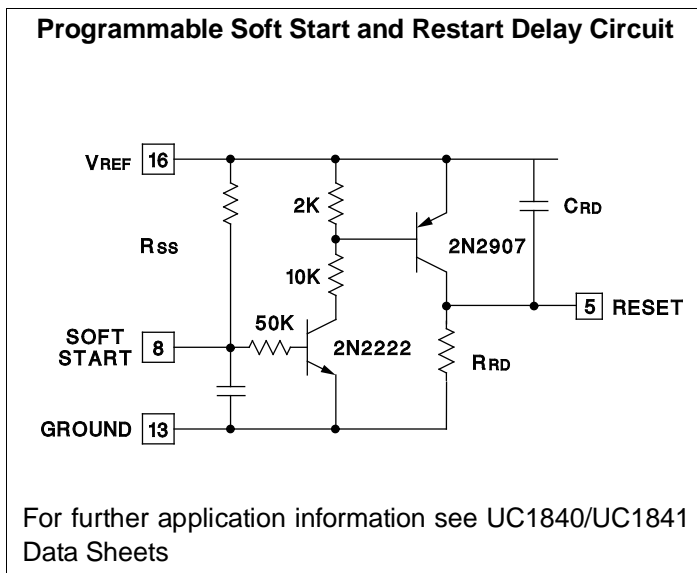
<b>PWM CONTROL</b>	
1. Oscillator	Generates a fixed-frequency internal clock from an external $R_T$ and $C_T$ . Frequency = $\frac{K_C}{R_T C_T}$ where $K_C$ is a first-order correction factor $\approx 0.3 \log (C_T \times 10^{12})$ .
2. Ramp Generator:	Develops linear ramp with slope defined externally by $\frac{dV}{dT} = \frac{\text{sense voltage}}{R R C_R}$ . $C_R$ is normally selected $\leq C_T$ and its value will have some effect upon valley duty cycle. Limiting the minimum value for $I_{SENSE}$ into pin 11 will establish a maximum duty cycle clamp. $C_R$ terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of $\pm 2\%$ . 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Totem pole output stage capable of sourcing and sinking 1 amp peak current. The active "on" state is high.
<b>SEQUENCING FUNCTIONS</b>	
1. Start/UV Sense:	With an increasing voltage, this comparator generates a turn-on signal and releases the slow start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200 $\mu$ A hysteresis current.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive to external circuitry upon start-up.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
<b>PROTECTION FUNCTIONS</b>	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (Typically 3V) b. Stop > 2.4V (Typically 1.6V) c. Current Sense 400mV over threshold. (Typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop:	A voltage over 2.4 will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a Typical Delay of 13ms/ $\mu$ F.



OPEN-LOOP CIRCUIT



High Peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 13 in a single ground point.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2851DW	ACTIVE	SOIC	DW	18	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2851DW	<a href="#">Samples</a>
UC2851N	ACTIVE	PDIP	N	18	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UC2851N	<a href="#">Samples</a>
UC3851DW	LIFEBUY	SOIC	DW	18	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3851DW	
UC3851DWTR	ACTIVE	SOIC	DW	18	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3851DW	<a href="#">Samples</a>
UC3851N	ACTIVE	PDIP	N	18	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3851N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UC2851DW	DW	SOIC	18	40	507	12.83	5080	6.6
UC2851N	N	PDIP	18	20	506	13.97	11230	4.32
UC3851DW	DW	SOIC	18	40	507	12.83	5080	6.6
UC3851N	N	PDIP	18	20	506	13.97	11230	4.32

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