THE DATASHEET OF

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PSoC® 5: CY8C53 Family Datasheet

Programmable System-on-Chip (PSoC®)

General Description

With its unique array of configurable blocks, PSoC® 5 is a true system level solution providing microcontroller unit (MCU), memory, analog, and digital peripheral functions in a single chip. The CY8C53 family offers a modern method of signal acquisition, signal processing, and control with high accuracy, high bandwidth, and high flexibility. Analog capability spans the range from thermocouples (near DC voltages) to ultrasonic signals. The CY8C53 family can handle dozens of data acquisition channels and analog inputs on every GPIO pin. The CY8C53 family is also a high-performance configurable digital system with some part numbers including interfaces such as USB and multi-master I^2C. In addition to communication interfaces, the CY8C53 family has an easy to configure logic array, flexible routing to all I/O pins, and a high-performance 32-bit ARM® Cortex™-M3 microprocessor core. Designers can easily create system-level designs using a rich library of prebuilt components and boolean primitives using PSoC® Creator™, a hierarchical schematic design entry tool. The CY8C53 family provides unparalleled opportunities for analog and digital bill of materials integration while easily accommodating last minute design changes through simple firmware updates.

Features

- 32-bit ARM Cortex-M3 CPU core
  - DC to 67 MHz operation
  - Flash program memory, up to 256 KB, 100,000 write cycles, 20-year retention, multiple security features
  - Up to 64 KB SRAM memory
  - 128 bytes of cache memory
  - 2-KB electrically erasable programmable read-only memory (EEPROM) memory, 1 million cycles, and 20 years retention
  - 24-channel direct memory access (DMA) with multilayer AMBA high-performance bus (AHB) bus access
    - Programmable chained descriptors and priorities
    - High bandwidth 32-bit transfer support
- Low voltage, ultra low power
  - Operating voltage range: 2.7 V to 5.5 V
  - 6 mA at 6 MHz
  - Low power modes including:
    - 2-µA sleep mode
    - 300-nA hibernate mode with RAM retention
- Versatile I/O system
  - 46 to 70 I/Os (60 GPIOs, 8 SIOs, 2 USBIOs))
  - Any GPIO to any digital or analog peripheral routability
  - LCD direct drive from any GPIO, up to 46x16 segments
  - CapSense® support from any GPIO[1]
  - 1.2 V to 5.5 V I/O interface voltages, up to 4 domains
  - Maskable, independent IRQ on any pin or port
  - Schmitt-trigger transistor-transistor logic (TTL) inputs
  - All GPIOs configurable as open drain high/low, pull-up/pull-down, High-Z, or strong output
  - 25 mA sink on SIO
- Digital peripherals
  - 20 to 24 programmable logic device (PLD) based universal digital blocks (UDBs)
  - Full-Speed (FS) USB 2.0 12 Mbps using a 24 MHz external oscillator
  - Up to four 16-bit configurable timer, counter, and PWM blocks
  - Library of standard peripherals
    - 8-, 16-, 24-, and 32-bit timers, counters, and PWMs
    - SPI, UART, and I^2C
    - Many others available in catalog
  - Library of advanced peripherals
    - Cyclic redundancy check (CRC)
    - Pseudo random sequence (PRS) generator
    - Local interconnect network (LIN) bus 2.0
    - Quadrature decoder
- Analog peripherals ($2.7\ V \le V_{DDA} \le 5.5\ V$)
  - 1.024 V ±1% internal voltage reference
  - Successive approximation register (SAR) analog-to-digital converter (ADC), 12-bit at 700 ksps
  - Two 8-bit 5.5 Msps current digital-to-analog converters (DAC) (IDACs) or 1 Msps voltage DACs (VDACs)
  - Four comparators with 95-ns response time
  - Two uncommitted opamps with 10-mA drive capability
  - Two configurable multifunction analog blocks. Example configurations are programmable gain amplifier (PGA), transimpedance amplifier (TIA), mixer, and sample and hold
  - CapSense support
- Programming, debug, and trace
  - Serial wire debug (SWD) and single-wire viewer (SWV) interfaces
  - Cortex-M3 flash patch and breakpoint (FPB) block
  - Cortex-M3 data watchpoint and trace (DWT) generates data trace information
  - Cortex-M3 instrumentation trace macrocell (ITM) can be used for printf-style debugging
  - DWT and ITM blocks communicate with off-chip debug and trace systems via the SWV interface
  - Bootloader programming supportable through I^2C, SPI, UART, USB, and other interfaces
- Precision, programmable clocking
  - 3 to 48 MHz internal oscillator over full temperature and voltage range
  - 4 to 25 MHz crystal oscillator for crystal PPM accuracy
  - Internal PLL clock generation up to 67 MHz
  - 32.768 kHz watch crystal oscillator
  - Low power internal oscillator at 1, 33, and 100 kHz
- Temperature and packaging
  - -40°C to +85°C degrees industrial temperature
  - 68-pin QFN and 100-pin TQFP package options

Note
1. GPIOs with opamp outputs are not recommended for use with CapSense.

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1. Architectural Overview

Introducing the CY8C53 family of ultra low-power, flash Programmable System-on-Chip (PSoC®) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C53 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

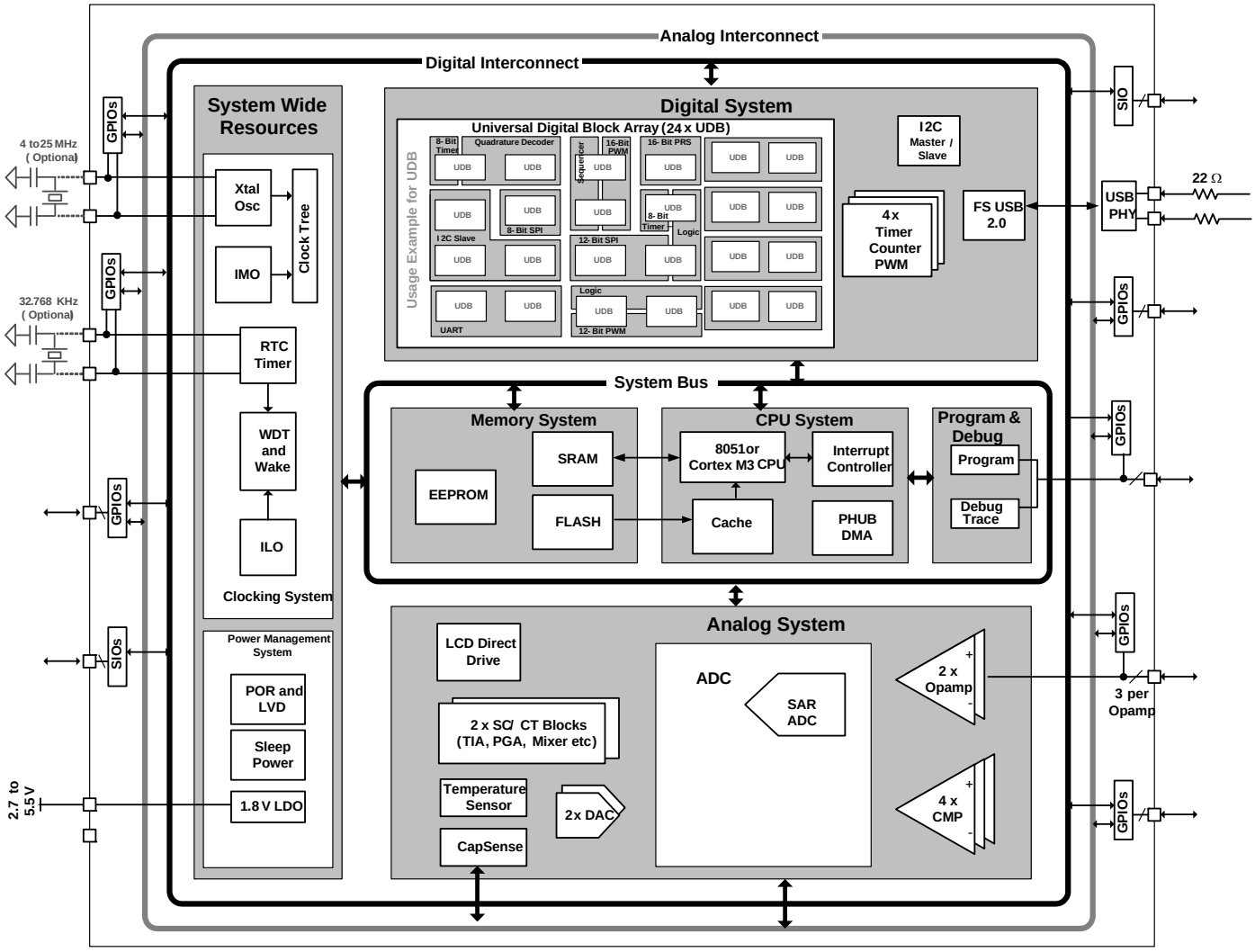


Figure 1-1 illustrates the major components of the CY8C53 family. They are:

- ARM Cortex-M3 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the digital system interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. The designer can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C53 family these blocks can include four 16-bit timer, counter, and PWM blocks; I^2C slave, master, and multimaster and Full-Speed USB.

For more details on the peripherals see the "Example Peripherals" section on page 32 of this data sheet. For information on UDBs, DSI, and other digital blocks, see the "Digital Subsystem" section on page 32 of this data sheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 1% error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Analog mixers
- Voltage references
- Analog-to-Digital Converters (ADC)
- Digital-to-Analog Converters (DACs)

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals.

The CY8C53 family also offers a SAR ADC. Featuring 12-bit conversions at up to 700 k samples per second, it also offers low nonlinearity and offset errors. It is well suited for a variety of higher speed analog applications.

Two high speed voltage or current DACs support 8-bit output signals at an update rate of up to 5.5 Msps. They can be routed out of any GPIO pin. You can create higher resolution voltage DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADC and DACs, the analog subsystem provides multiple:

- Comparators
- Uncommitted opamps
- Configurable switched capacitor/continuous time (SC/CT) blocks. These support:
  - Transimpedance amplifiers
  - Programmable gain amplifiers
  - Mixers
  - Other similar analog components

See the "Analog Subsystem" section on page 44 of this data sheet for more details.

PSoC's CPU subsystem is built around a 32-bit three-stage pipelined ARM Cortex-M3 processor running at up to 67 MHz. The Cortex-M3 includes a tightly integrated nested vectored interrupt controller (NVIC) and various debug and trace modules. The overall CPU subsystem includes a DMA controller, cache, and interrupt controller. The NVIC provides low latency, nested interrupts, and tail-chaining of interrupts and other features to increase the efficiency of interrupt handling. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The presence of cache improves the access speed of instructions by the CPU.

PSoC's nonvolatile subsystem consists of flash and byte-writeable EEPROM. It provides up to 256 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling boot loaders. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Two KB of byte-writable EEPROM is available on-chip to store application data.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the V_{DDIO} pins. Every GPIO has analog I/O, LCD drive, flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow V_{OH} to be set independently of V_{DDIO} when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with Full-Speed USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 25 of this data sheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The internal main oscillator (IMO) is the master clock base for the system, and has 5% accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 48 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate system clock frequencies up to 67 MHz from the IMO, external crystal, or external reference clock. It also contains a separate, very low-power internal low speed oscillator (ILO) for the sleep and watchdog timers. A 32.768 kHz external watch crystal is also supported for use in real time clock (RTC) applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C53 family supports a wide supply operating range from 2.7 to 5.5 V. This allows operation from regulated supplies such as 3.3 V ± 10% or 5.0 V ± 10%, or directly from a wide range of battery types.

PSoC supports a wide range of low power modes. These include a 300-nA hibernate mode with RAM retention and a 2-µA sleep mode.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 6 mA when the CPU is running at 6 MHz.

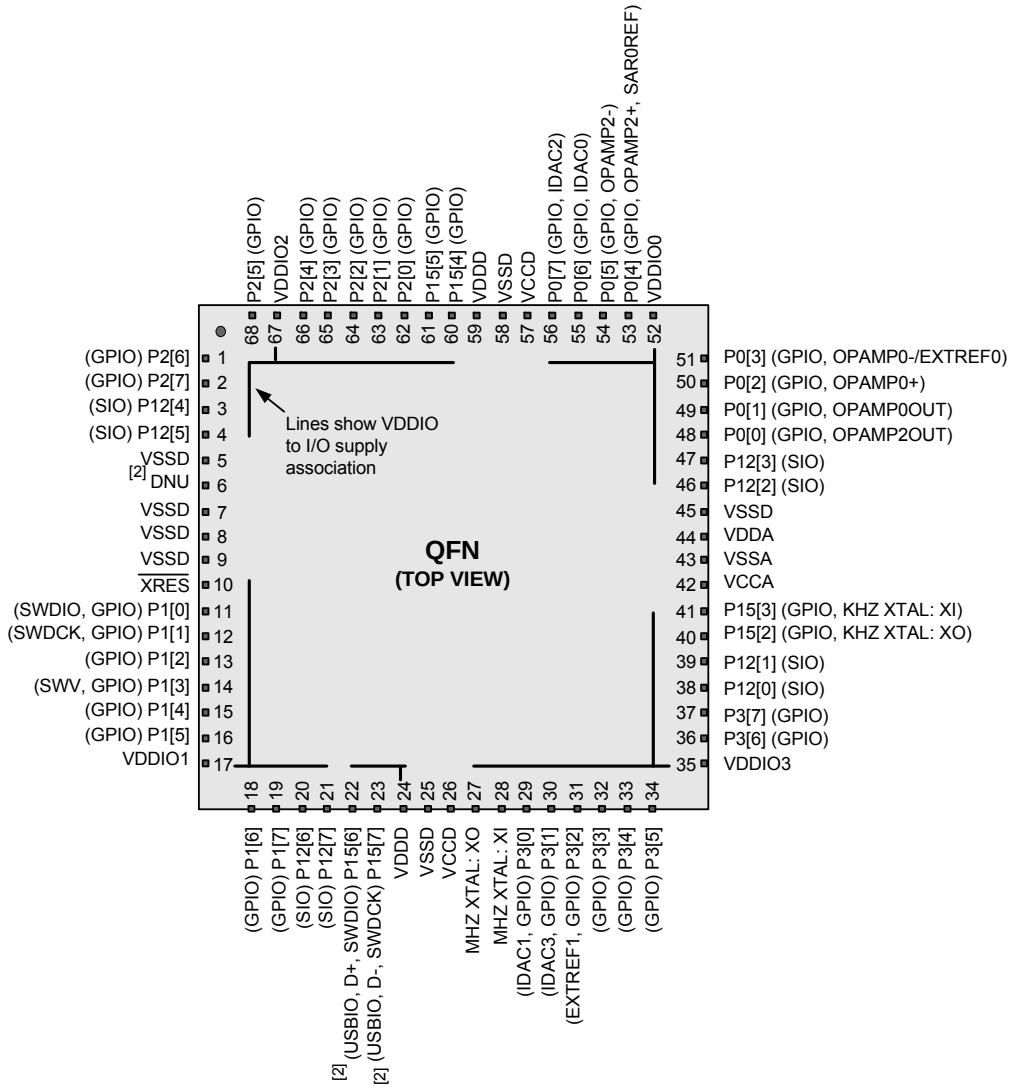
The details of the PSoC power modes are covered in the "Power System" section on page 22 of this data sheet.

PSoC uses a SWD interface for programming, debug, and test. Using this standard interface enables the designer to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. The Cortex-M3 debug and trace modules include FPB, DWT, and ITM. These modules have many features to help solve difficult debug and trace problems. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 53 of this data sheet.

2. Pinouts

The VDDIO pin that supplies a particular set of pins is indicated by the black lines drawn on the pinout diagrams in Figure 2-1 and Figure 2-2. Using the VDDIO pins, a single PSoC can support multiple interface voltage levels, eliminating the need for off-chip level shifters. Each VDDIO may sink up to 20 mA total to its associated I/O pins and opamps, and each set of VDDIO associated pins may sink up to 100 mA.

Figure 2-1. 68-Pin QFN Part Pinout[3]



Notes
2. Pins labeled Do Not Use (DNU) must be left floating. USB pins on devices without USB are DNU.
3. The center pad on the QFN package should be connected to digital ground (V_{SSD}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Figure 2-2. 100-Pin TQFP Part Pinout

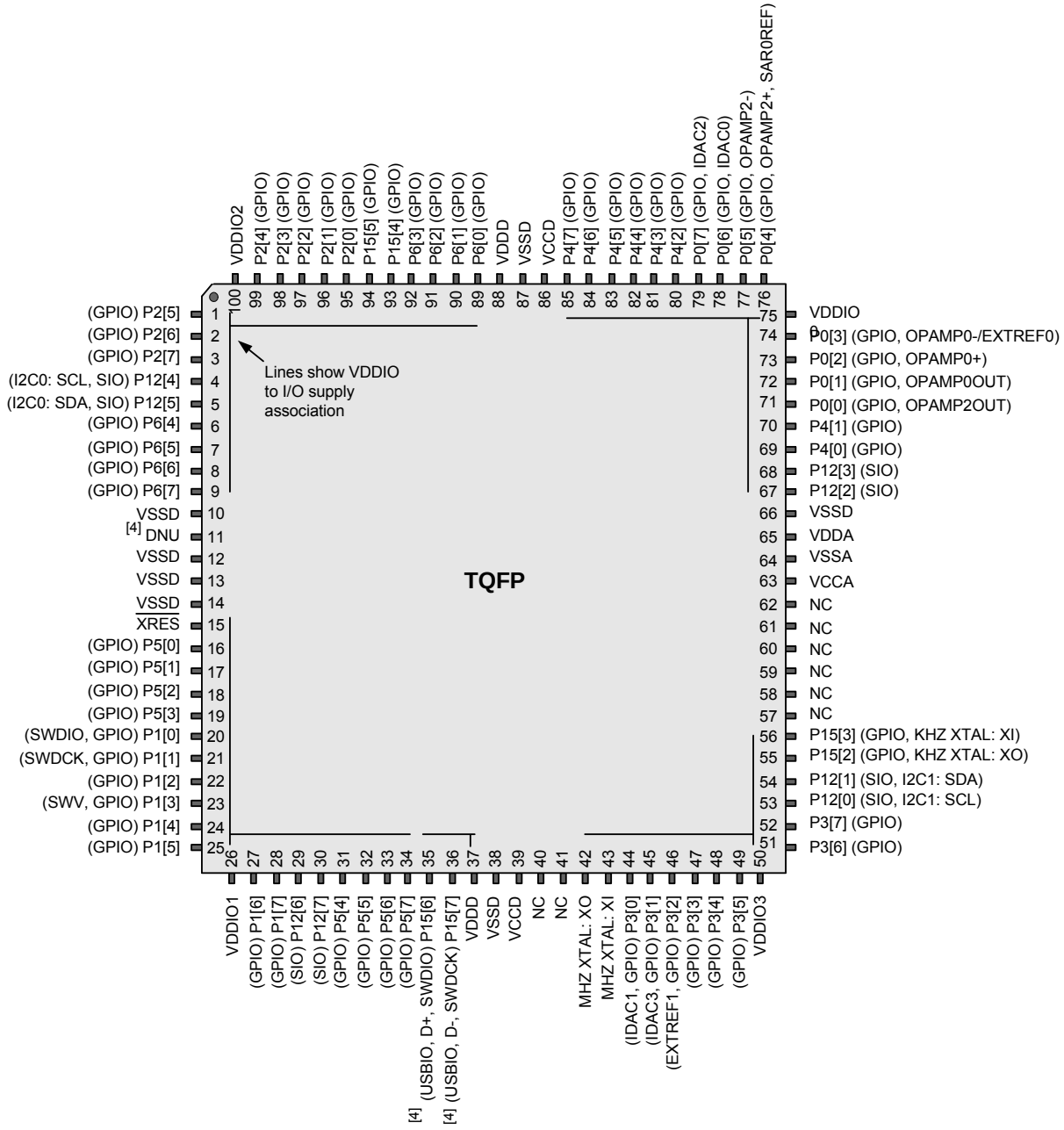


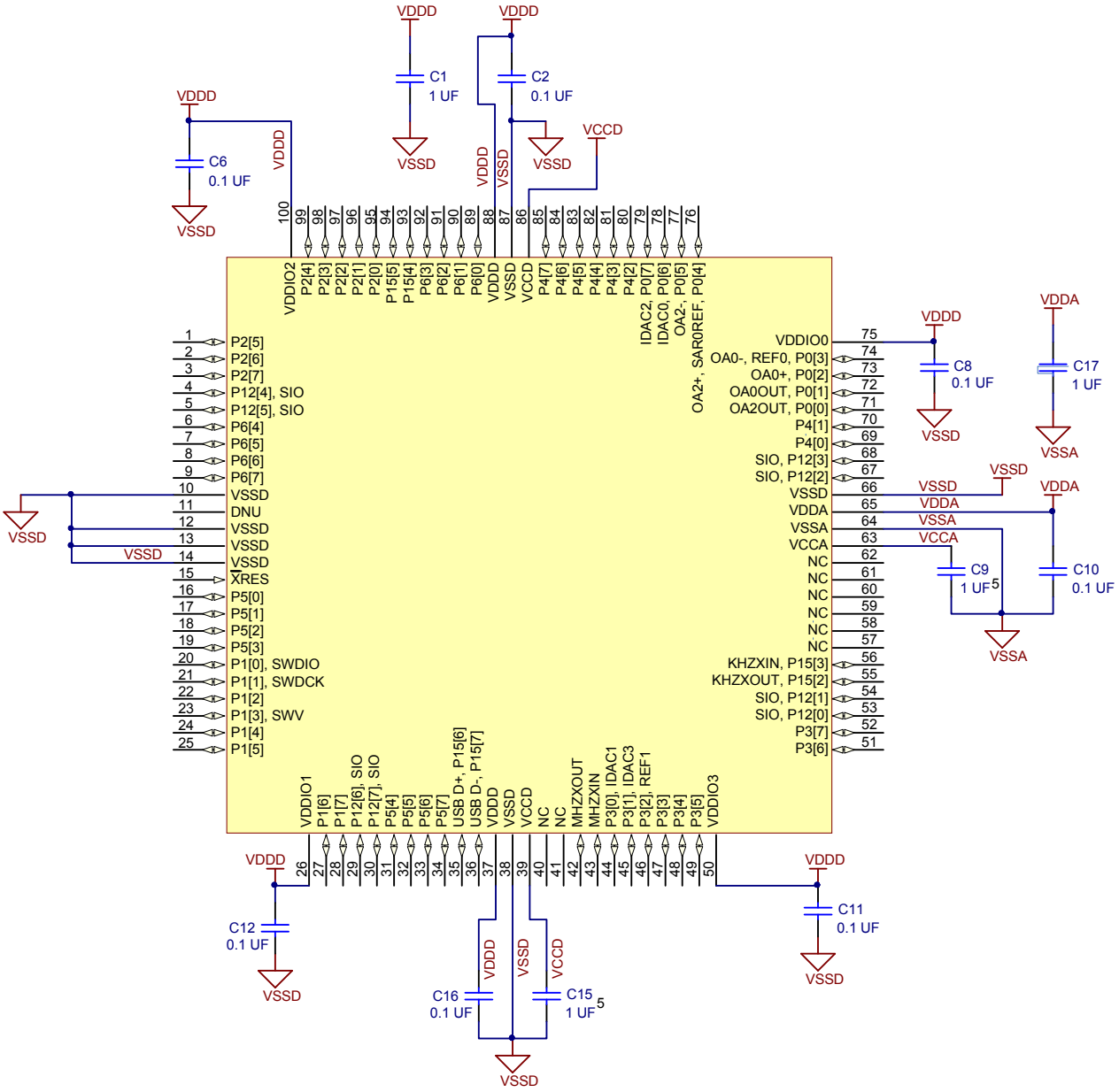
Figure 2-3 and Figure 2-4 on page 9 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a 2-layer board.

- The two pins labeled V_{DDD} must be connected together.
- The two pins labeled V_{CCD} must be connected together, with capacitance added, as shown in Figure 2-3 and Power System on page 22. The trace between the two V_{CCD} pins should be as short as possible.
- The two pins labeled V_{SSD} must be connected together.

Note
4. Pins labeled Do Not Use (DNU) must be left floating. USB pins on devices without USB are DNU.

For information on circuit board layout issues for mixed signals, refer to the application note AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5.

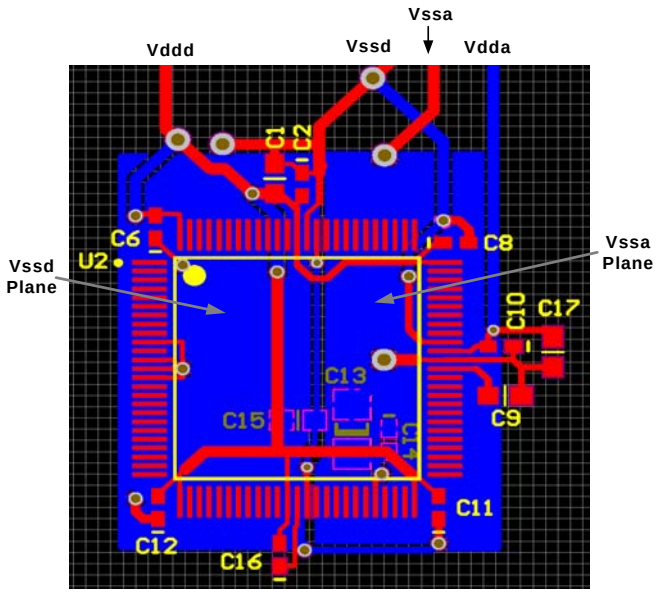
Figure 2-3. Example Schematic for 100-Pin TQFP Part with Power Connections



Note The two V_{CCD} pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-4.

Note
5. 10 µF is required for sleep mode. See Table 11-3.

Figure 2-4. Example PCB Layout for 100-Pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC2. Low resistance output pin for high current DACs (IDAC).

OpAmp0out, OpAmp2out. High current output of uncommitted opamp[6].

Extref0, Extref1. External reference input to the analog system.

OpAmp0-, OpAmp2-. Inverting input to uncommitted opamp.

OpAmp0+, OpAmp2+. Noninverting input to uncommitted opamp.

SAR0ref. External reference for SAR ADC.

GPIO. General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[6].

kHz XTAL: Xo, kHz XTAL: Xi. 32.768 kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi. 4 to 25 MHz crystal oscillator pin. If a crystal is not used then Xi must be shorted to ground and Xo must be left floating.

SIO. Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK. Serial Wire Debug Clock programming and debug port connection. When programming and debugging using SWD is done over USBIOs, the SWDCK pin of port P1[1] is not available for use as a general purpose I/O and should be externally pulled down using a resistor of less than 100 KΩ.

SWDIO. Serial Wire Debug Input and Output programming and debug port connection.

SWV. Single Wire Viewer output.

USBIO, D+. Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from V_{DDD} instead of from a V_{DDIO}. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D-. Provides D- connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from V_{DDD} instead of from a V_{DDIO}. Pins are DNU on devices without USB.

V_{CCA}. Output of analog core regulator and input to analog core. Requires a 1 µF capacitor to V_{SSA} (10 µF is required for sleep mode. See Table 11-3). Regulator output not for external use.

V_{CCD}. Output of digital core regulator and input to digital core. The two V_{CCD} pins must be shorted together, with the trace between them as short as possible, and a 1 µF capacitor to V_{SSD} (10 µF is required for sleep mode. See Table 11-3); see Power System on page 22. Regulator output not for external use.

V_{DDA}. Supply for all analog peripherals and analog core regulator. **V_{DDA} must be the highest voltage present on the device. All other supply pins must be less than or equal to V_{DDA}.**[7]

V_{DDD}. Supply for all digital peripherals and digital core regulator. V_{DDD} must be less than or equal to V_{DDA}.[7]

V_{SSA}. Ground for all analog peripherals.

V_{SSD}. Ground for all digital logic and I/O pins.

V_{DDIO0}, V_{DDIO1}, V_{DDIO2}, V_{DDIO3}. Supply for I/O pins. Each V_{DDIO} must be tied to a valid operating voltage (2.7 V to 5.5 V), and must be less than or equal to V_{DDA}.

$\overline{XRES}$. External reset pin. Active low with internal pull-up.

RSVD. Reserved pins.

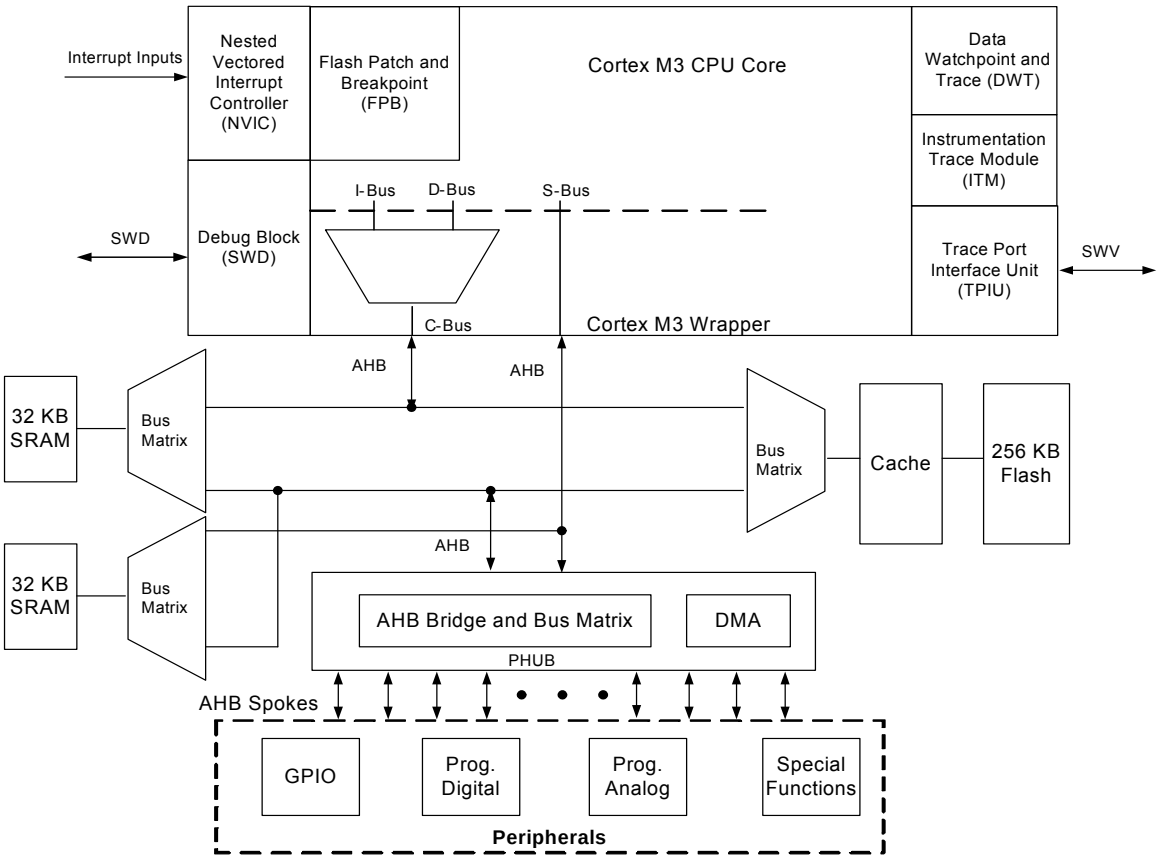
Notes
6. GPIOs with opamp outputs are not recommended for use with CapSense.
7. V_{DDD} and V_{DDA} must be brought up in synchronization with each other, that is, at the same rates and levels. V_{DDA} must be greater than or equal to all other supplies.

4. CPU

4.1 ARM Cortex-M3 CPU

The CY8C53 family of devices has an ARM Cortex-M3 CPU core. The Cortex-M3 is a low power 32-bit three-stage pipelined Harvard architecture CPU that delivers 1.25 DMIPS/MHz. It is intended for deeply embedded applications that require fast interrupt handling features.

Figure 4-1. ARM Cortex-M3 Block Diagram



The Cortex-M3 CPU subsystem includes these features:

- ARM Cortex-M3 CPU
- Programmable NVIC, tightly integrated with the CPU core
- Full-featured debug and trace module, tightly integrated with the CPU core
- Up to 128 KB of flash memory, 2 KB of EEPROM, and 32 KB of SRAM
- Cache controller with 128 bytes of memory
- Peripheral HUB (PHUB)
- DMA controller

4.1.1 Cortex-M3 Features

The Cortex-M3 CPU features include:

- 4-GB address space. Predefined address regions for code, data, and peripherals. Multiple buses for efficient and simultaneous accesses of instructions, data, and peripherals.
- The Thumb®-2 instruction set, which offers ARM-level performance at Thumb-level code density. This includes 16-bit and 32-bit instructions. Advanced instructions include:
  - Bit-field control
  - Hardware multiply and divide
  - Saturation
  - If-Then
  - Wait for events and interrupts
  - Exclusive access and barrier
  - Special register access

  The Cortex-M3 does not support ARM instructions.

- Bit-band support for the SRAM region. Atomic bit-level write and read operations for SRAM addresses.
- Unaligned data storage and access. Contiguous storage of data of different byte lengths.
- Operation at two privilege levels (privileged and user) and in two modes (thread and handler). Some instructions can only be executed at the privileged level. There are also two stack pointers: Main (MSP) and Process (PSP). These features support a multitasking operating system running one or more user-level processes.
- Extensive interrupt and system exception support.

4.1.2 Cortex-M3 Operating Modes

The Cortex-M3 operates at either the privileged level or the user level, and in either the thread mode or the handler mode. Because the handler mode is only enabled at the privileged level, there are actually only three states, as shown in Table 4-1.

Table 4-1. Operational Level

Condition	Privileged	User
Running an exception	Handler mode	Not used
Running main program	Thread mode	Thread mode

At the user level, access to certain instructions, special registers, configuration registers, and debugging components is blocked. Attempts to access them cause a fault exception. At the privileged level, access to all instructions and registers is allowed.

The processor runs in the handler mode (always at the privileged level) when handling an exception, and in the thread mode when not.

4.1.3 CPU Registers

The Cortex-M3 CPU registers are listed in Table 4-2. Registers R0-R15 are all 32 bits wide.

Table 4-2. Cortex M3 CPU Registers

Register	Description
R0-R12	General purpose registers R0-R12 have no special architecturally defined uses. Most instructions that specify a general purpose register specify R0-R12. ■ Low Registers: Registers R0-R7 are accessible by all instructions that specify a general purpose register. ■ High Registers: Registers R8-R12 are accessible by all 32-bit instructions that specify a general purpose register; they are not accessible by all 16-bit instructions.

Table 4-2. Cortex M3 CPU Registers (continued)

Register	Description
R13	R13 is the stack pointer register. It is a banked register that switches between two 32-bit stack pointers: the Main Stack Pointer (MSP) and the Process Stack Pointer (PSP). The PSP is used only when the CPU operates at the user level in thread mode. The MSP is used in all other privilege levels and modes. Bits[0:1] of the SP are ignored and considered to be 0, so the SP is always aligned to a word (4 byte) boundary.
R14	R14 is the Link Register (LR). The LR stores the return address when a subroutine is called.
R15	R15 is the Program Counter (PC). Bit 0 of the PC is ignored and considered to be 0, so instructions are always aligned to a half word (2 byte) boundary.
xPSR	The Program status registers are divided into three status registers, which are accessed either together or separately: ■ Application Program Status Register (APSR) holds program execution status bits such as zero, carry, negative, in bits[27:31]. ■ Interrupt Program Status Register (IPSR) holds the current exception number in bits[0:8]. ■ Execution Program Status Register (EPSR) holds control bits for interrupt continuable and IF-THEN instructions in bits[10:15] and [25:26]. Bit 24 is always set to 1 to indicate Thumb mode. Trying to clear it causes a fault exception.
PRIMASK	A 1-bit interrupt mask register. When set, it allows only the nonmaskable interrupt (NMI) and hard fault exception. All other exceptions and interrupts are masked.
FAULTMASK	A 1-bit interrupt mask register. When set, it allows only the NMI. All other exceptions and interrupts are masked.
BASEPRI	A register of up to nine bits that define the masking priority level. When set, it disables all interrupts of the same or higher priority value. If set to 0 then the masking function is disabled.
CONTROL	A 2-bit register for controlling the operating mode. Bit 0: 0 = privileged level in thread mode, 1 = user level in thread mode. Bit 1: 0 = default stack (MSP) is used, 1 = alternate stack is used. If in thread mode or user level then the alternate stack is the PSP. There is no alternate stack for handler mode; the bit must be 0 while in handler mode.

4.2 Cache Controller

The CY8C53 family has 128 bytes of direct mapped instruction cache between the CPU and the flash memory. This allows the CPU to access instructions much faster. The cache is enabled by default but user have the option to disable it.

4.3 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.3.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8-, 16-, 24-, and 32-bit addressing and data

Table 4-3. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU
2	PHUB local configuration, Power manager, Clocks, IC, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, I2C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

4.3.2 DMA Features

- 24 DMA channels
- Each channel has one or more transaction descriptors (TDs) to configure channel behavior. Up to 127 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64k bytes
- Large transactions may be broken into smaller bursts of 1 to 127 bytes
- TDs may be nested and/or chained for complex transactions

4.3.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100% of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-4 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

Table 4-4. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

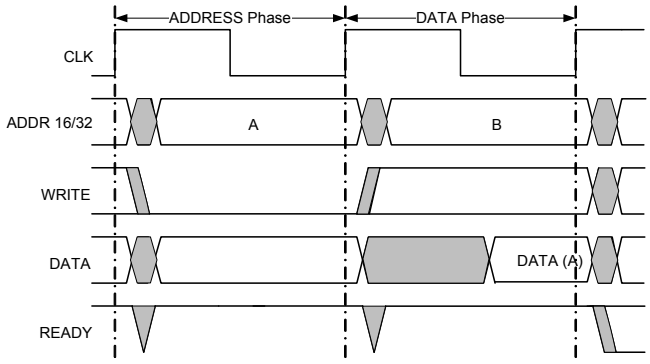
4.3.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

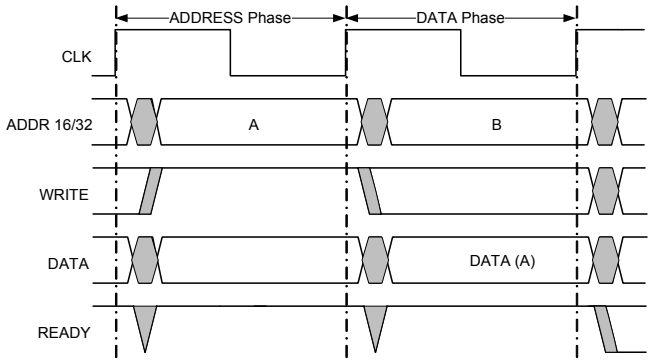
4.3.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in Figure 4-2. For more description on other transfer modes, refer to the Technical Reference Manual.

Figure 4-2. DMA Timing Diagram



Basic DMA Read Transfer without wait states



Basic DMA Write Transfer without wait states

4.3.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.3.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.3.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.3.4.5 Indexed DMA

In an indexed DMA case, an external master requires access to locations on the system bus as if those locations were shared memory. As an example, a peripheral may be configured as an SPI or I^2C slave where an address is received by the external master. That address becomes an index or offset into the internal system bus memory space. This is accomplished with an initial “address fetch” TD that reads the target address location from the peripheral and writes that value into a subsequent TD in the chain. This modifies the TD chain on the fly. When the “address fetch” TD completes it moves on to the next TD, which has the new address information embedded in it. This TD then carries out the data transfer with the address location required by the external master.

4.3.4.6 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.3.4.7 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.3.4.8 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

4.4 Interrupt Controller

The Cortex-M3 NVIC supports 16 system exceptions and 32 interrupts from peripherals, as shown in Table 4-5.

Table 4-5. Cortex-M3 Exceptions and Interrupts

Exception Number	Exception Type	Priority	Exception Table Address Offset	Function
			0x00	Starting value of R13 / MSP
1	Reset	–3 (highest)	0x04	Reset
2	NMI	–2	0x08	Non maskable interrupt
3	Hard fault	–1	0x0C	All classes of fault, when the corresponding fault handler cannot be activated because it is currently disabled or masked
4	MemManage	Programmable	0x10	Memory management fault, for example, instruction fetch from a nonexecutable region
5	Bus fault	Programmable	0x14	Error response received from the bus system; caused by an instruction prefetch abort or data access error
6	Usage fault	Programmable	0x18	Typically caused by invalid instructions or trying to switch to ARM mode
7 – 10	–	–	0x1C – 0x28	Reserved
11	SVC	Programmable	0x2C	System service call via SVC instruction
12	Debug monitor	Programmable	0x30	Debug monitor
13	–	–	0x34	Reserved
14	PendSV	Programmable	0x38	Deferred request for system service
15	SYSTICK	Programmable	0x3C	System tick timer
16 – 47	IRQ	Programmable	0x40 – 0x3FC	Peripheral interrupt request #0 - #31

Bit 0 of each exception vector indicates whether the exception is executed using ARM or Thumb instructions. Because the Cortex-M3 only supports Thumb instructions, this bit must always be 1. The Cortex-M3 non maskable interrupt (NMI) input can be routed to any pin, via the DSI, or disconnected from all pins. See "DSI Routing Interface Description" section on page 39.

The NVIC handles interrupts from the peripherals, and passes the interrupt vectors to the CPU. It is closely integrated with the CPU for low latency interrupt handling. Features include:

- 32 interrupts. Multiple sources for each interrupt.
- Configurable number of priority levels: from 3 to 8.
- Dynamic reprioritization of interrupts.
- Priority grouping. This allows selection of preempting and non preempting interrupt levels.
- Support for tail-chaining, and late arrival, of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. All interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Table 4-6. Interrupt Vector Table

Interrupt #	Cortex-M3 Exception #	Fixed Function	DMA	UDB
0	16	Low voltage detect (LVD)	phub_termout0[0]	udb_intr[0]
1	17	Cache	phub_termout0[1]	udb_intr[1]
2	18	Reserved	phub_termout0[2]	udb_intr[2]
3	19	Pwr Mgr	phub_termout0[3]	udb_intr[3]
4	20	PICU[0]	phub_termout0[4]	udb_intr[4]
5	21	PICU[1]	phub_termout0[5]	udb_intr[5]
6	22	PICU[2]	phub_termout0[6]	udb_intr[6]
7	23	PICU[3]	phub_termout0[7]	udb_intr[7]
8	24	PICU[4]	phub_termout0[8]	udb_intr[8]
9	25	PICU[5]	phub_termout0[9]	udb_intr[9]
10	26	PICU[6]	phub_termout0[10]	udb_intr[10]
11	27	PICU[12]	phub_termout0[11]	udb_intr[11]
12	28	PICU[15]	phub_termout0[12]	udb_intr[12]
13	29	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	30	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	31	I^2C	phub_termout0[15]	udb_intr[15]
16	32	Reserved	phub_termout1[0]	udb_intr[16]
17	33	Reserved	phub_termout1[1]	udb_intr[17]
18	34	Reserved	phub_termout1[2]	udb_intr[18]
19	35	Reserved	phub_termout1[3]	udb_intr[19]
20	36	Reserved	phub_termout1[4]	udb_intr[20]
21	37	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	38	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	39	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	40	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	41	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	42	Reserved	phub_termout1[10]	udb_intr[26]
27	43	Reserved	phub_termout1[11]	udb_intr[27]
28	44	Reserved	phub_termout1[12]	udb_intr[28]
29	45	Decimator Int	phub_termout1[13]	udb_intr[29]
30	46	phub_err_int	phub_termout1[14]	udb_intr[30]
31	47	eeprom_fault_int	phub_termout1[15]	udb_intr[31]

5. Memory

5.1 Static RAM

CY8C53 static RAM (SRAM) is used for temporary data storage. Code can be executed at full speed from the portion of SRAM that is located in the code space. This process is slower from SRAM above 0x20000000. The device provides up to 64 KB of SRAM. The CPU or the DMA controller can access all of SRAM. The SRAM can be accessed simultaneously by the Cortex-M3 CPU and the DMA controller if accessing different 32-KB blocks.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data and bulk data storage. The main flash memory area contains up to 256 KB of user program space.

Up to an additional 32 KB of flash space is available for storing device configuration data and bulk user data. User code may not be run out of this flash memory section. The flash output is 9 bytes wide with 8 bytes of data and 1 additional byte.

The flash programming interface performs flash erasing, programming and setting code protection levels. Flash In System Serial Programming (ISSP), typically used for production programming, is possible through the SWD interface. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I^2C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of configuration or general-purpose data.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the "Device Security" section on page 55). For more information on how to take full advantage of the security features in PSoC, see the PSoC 5 TRM.

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	–
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte addressable nonvolatile memory. The CY8C53 has 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into two sections, each containing 64 rows of 16 bytes each.

The CPU cannot execute out of EEPROM.

5.5 Memory Map

The Cortex-M3 has a fixed address map, which allows peripherals to be accessed by simple memory access instructions.

5.5.1 Address Map

The 4-GB address space is divided into the ranges shown in Table 5-2:

Table 5-2. Address Map

Address Range	Size	Use
0x00000000 – 0x1FFFFFFF	0.5 GB	Program code. This includes the exception vector table at power up, which starts at address 0.
0x20000000 – 0x3FFFFFFF	0.5 GB	Static RAM. This includes a 1 MByte bit-band region starting at 0x20000000 and a 32 Mbyte bit-band alias region starting at 0x22000000.
0x40000000 – 0x5FFFFFFF	0.5 GB	Peripherals.
0x60000000 – 0x9FFFFFFF	1 GB	External RAM.
0xA0000000 – 0xDFFFFFFF	1 GB	External peripherals.
0xE0000000 – 0xFFFFFFFF	0.5 GB	Internal peripherals, including the NVIC and debug and trace modules.

Table 5-3. Peripheral Data Address Map

Address Range	Purpose
0x00000000 – 0x0003FFFF	256K Flash
0x1FFF8000 – 0x1FFFFFFF	32K SRAM in Code region
0x20000000 – 0x20007FFF	32K SRAM in SRAM region
0x40004000 – 0x400042FF	Clocking, PLLs, and oscillators
0x40004300 – 0x400043FF	Power management
0x40004500 – 0x400045FF	Ports interrupt control
0x40004700 – 0x400047FF	Flash programming interface

Table 5-3. Peripheral Data Address Map (continued)

Address Range	Purpose
0x40004800 – 0x400048FF	Cache controller
0x40004900 – 0x400049FF	I^2C controller
0x40004E00 – 0x40004EFF	Decimator
0x40004F00 – 0x40004FFF	Fixed timer/counter/PWMs
0x40005000 – 0x400051FF	I/O ports control
0x40005800 – 0x40005FFF	Analog Subsystem Interface
0x40006000 – 0x400060FF	USB Controller
0x40006400 – 0x40006FFF	UDB Configuration
0x40007000 – 0x40007FFF	PHUB Configuration
0x40008000 – 0x400087FF	EEPROM
0x40010000 – 0x4001FFFF	Digital Interconnect Configuration
0xE0000000 – 0xE00FFFFF	Cortex-M3 PPB Registers, including NVIC, debug, and trace

The bit-band feature allows individual bits in SRAM to be read or written as atomic operations. This is done by reading or writing bit 0 of corresponding words in the bit-band alias region. For example, to set bit 3 in the word at address 0x20000000, write a 1 to address 0x2200000C. To test the value of that bit, read address 0x2200000C and the result is either 0 or 1 depending on the value of the bit.

Most memory accesses done by the Cortex-M3 are aligned, that is, done on word (4-byte) boundary addresses. Unaligned accesses of words and 16-bit half-words on nonword boundary addresses can also be done, although they are less efficient.

5.5.2 Address Map and Cortex-M3 Buses

The ICode and DCode buses are used only for accesses within the Code address range, 0 - 0x1FFFFFFF.

The system bus is used for data accesses and debug accesses within the ranges 0x20000000 – 0xDFFFFFFF and 0xE0100000 – 0xFFFFFFFF. Instruction fetches can also be done within the range 0x20000000 – 0x3FFFFFFF, although these can be slower than instruction fetches via the ICode bus.

The private peripheral bus (PPB) is used within the Cortex-M3 to access system control registers and debug and trace module registers.

6. System Integration

6.1 Clocking System

The clocking system generates, divides, and distributes clocks throughout the PSoC system. The IMO and PLL together can generate up to a 67 MHz clock, accurate to ±5% over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. All of the system clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows designers to build clocking systems with minimal input. The designer can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent PSoC.

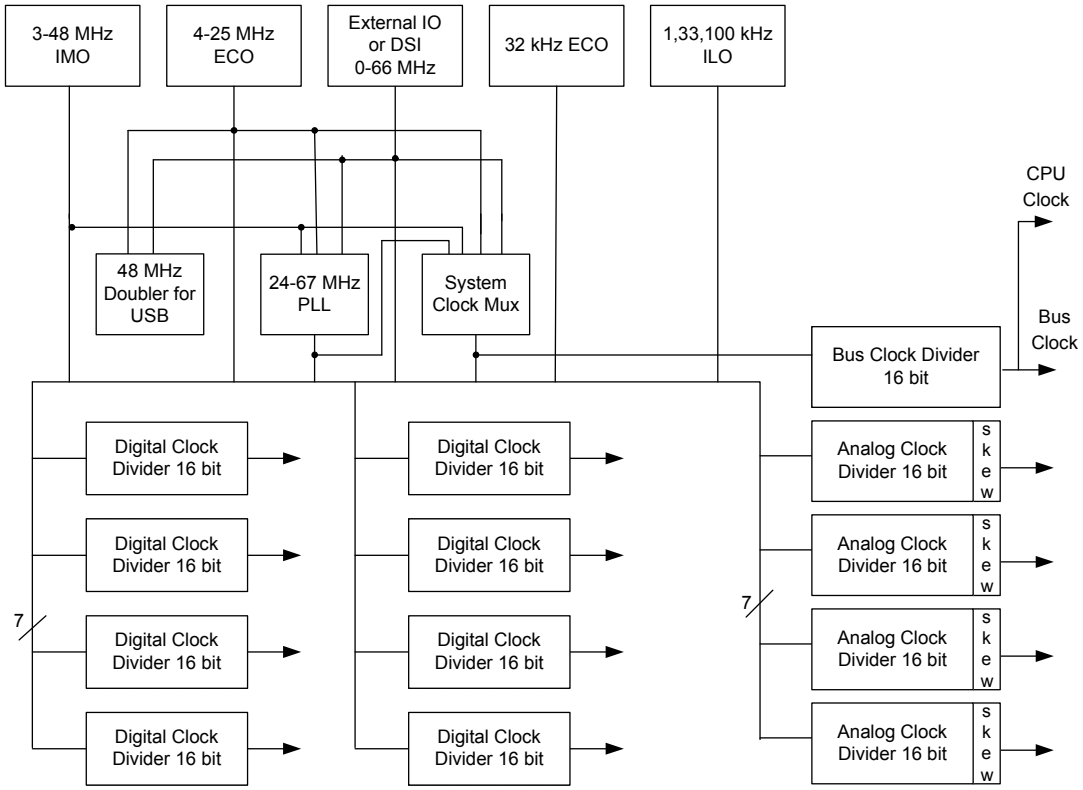
Key features of the clocking system include:

- Seven general purpose clock sources
  - 3 to 48 MHz IMO, ±5% at 3 MHz
  - 4 to 25 MHz external crystal oscillator (MHzECO)
  - Clock doubler provides a doubled clock frequency output for the USB block, see USB Clock Domain on page 21
  - DSI signal from an external I/O pin or other logic
  - 24 to 67 MHz fractional PLL sourced from IMO, MHzECO, or DSI
  - 1 kHz, 33 kHz, 100 kHz ILO for watchdog timer (WDT) and sleep timer
  - 32.768 kHz external crystal oscillator (kHzECO) for RTC
- Independently sourced clock dividers in all clocks
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the CPU bus and CPU clock
- Automatic clock configuration in PSoC Creator

Table 6-1. Oscillator Summary

Source	Fmin	Tolerance at Fmin	Fmax	Tolerance at Fmax	Startup Time
IMO	3 MHz	±5% over voltage and temperature	48 MHz	±10%	12 µs max
MHzECO	4 MHz	Crystal dependent	25 MHz	Crystal dependent	5 ms typ, max is crystal dependent
DSI	0 MHz	Input dependent	66 MHz	Input dependent	Input dependent
PLL	24 MHz	Input dependent	67 MHz	Input dependent	250 µs max
Doubler	48 MHz	Input dependent	48 MHz	Input dependent	1 µs max
ILO	1 kHz	–50%, +100%	100 kHz	-55%, +100%	15 ms max in lowest power mode
kHzECO	32 kHz	Crystal dependent	32 kHz	Crystal dependent	500 ms typ, max is crystal dependent

Figure 6-1. Clocking Subsystem



6.1.1 Internal Oscillators

6.1.1.1 Internal Main Oscillator

The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from ±5% at 3 MHz, up to ±10% at 48 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency. The IMO provides clock outputs at 3, 6, 12, 24, and 48 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works at input frequency of 24 MHz, providing 48 MHz for the USB. It can be configured to use a clock from the MHzECO or the DSI (external pin). The doubler is typically used to clock the USB.

6.1.1.3 Phase-Locked Loop

The PLL allows low frequency, high accuracy clocks to be multiplied to higher frequencies. This is a tradeoff between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 67 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 µs (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO, or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low power modes.

6.1.1.4 Internal Low Speed Oscillator

The ILO provides clock frequencies for low power consumption, including the sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz.

The 1 kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to long sleep intervals using the central timewheel (CTW). The central timewheel is a free running counter clocked by the ILO 1 kHz output. The central timewheel is always enabled except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low power mode. Firmware can reset the central timewheel.

The central timewheel can be programmed to wake the system periodically and optionally issue an interrupt. This enables flexible, periodic wakeups from low power modes or coarse timing applications. Systems that require accurate timing should use the RTC capability instead of the central timewheel. The 100 kHz clock (CLK100K) works as a low-power system clock to

run the CPU. It can also generate fast time intervals using the fast timewheel.

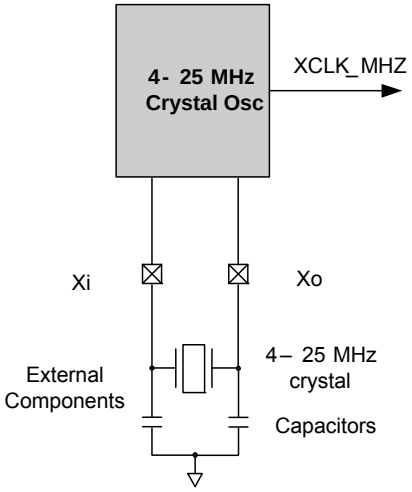
The fast timewheel is a 100 kHz, 5-bit counter clocked by the ILO that can also be used to generate periodic interrupts. The fast timewheel settings are programmable, and the counter automatically resets when the terminal count is reached. This enables flexible, periodic interrupts to the CPU at a higher rate than is allowed using the central timewheel. The fast timewheel can generate an optional interrupt each time the terminal count is reached. The 33 kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768 kHz ECO clock with no need for a crystal. The fast timewheel cannot be used as a wakeup source and must be turned off before entering sleep or hibernate mode.

6.1.2 External Oscillators

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports crystals in the range of 4 to 25 MHz. When used in conjunction with the PLL, it can generate CPU and system clocks up to the device's maximum frequency (see Phase-Locked Loop on page 19). The MHzECO with a 24 MHz crystal can be used with the clock doubler to generate a 48 MHz clock for the USB. If a crystal is not used then Xi must be shorted to ground and Xo must be left floating. MHzECO accuracy depends on the crystal chosen.

Figure 6-2. MHzECO Block Diagram

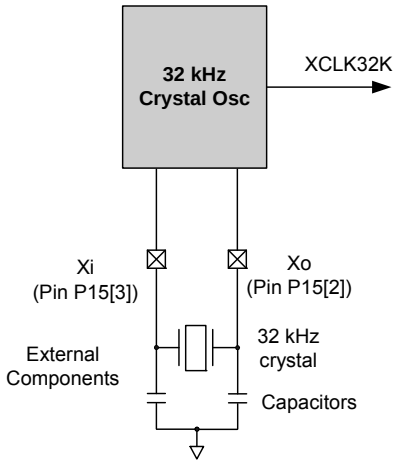


6.1.2.2 32.768 kHz ECO

The 32.768 kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768 kHz watch crystal (see Figure 6-3). The RTC uses a 1-second interrupt to implement the RTC functionality in firmware.

The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the "GPIO" section on page 61.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and Universal Digital Blocks.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers and the CPU. The CPU clock is directly derived from the bus clock.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as the ADC. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50% duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

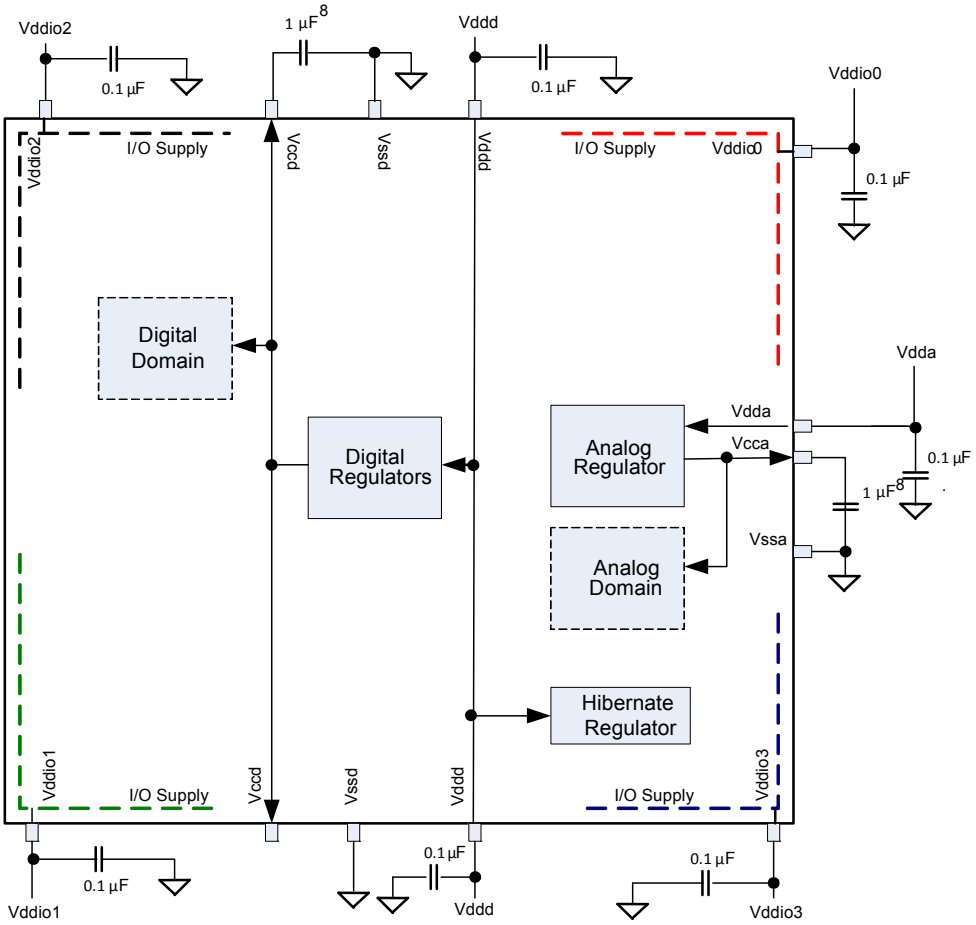
6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from the MHzECO or DSI signal.

6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled V_{DDA}, V_{DDD}, and Vddiox, respectively. It also includes two internal 1.8 V regulators that provide the digital (V_{CCD}) and analog (V_{CCA}) supplies for the internal core logic. The output pins of the regulators (V_{CCD} and V_{CCA}) and the V_{DDIO} pins must have capacitors connected as shown in Figure 6-4 (10 µF is required for sleep mode. See Table 11-3). The two V_{CCD} pins must be shorted together, with as short a trace as possible. The power system also contains a hibernate regulator.

Figure 6-4. PSoC Power System



Note The two V_{CCD} pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-4.

Note
8. 10 µF is required for sleep mode. See Table 11-3.

6.2.1 Power Modes

PSoC 5 devices have four different power modes, as shown in Table 6-2 and Table 6-3. The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low power and portable devices.

PSoC 5 power modes, in order of decreasing power consumption are:

- Active
- Alternate Active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from reset Figure 6-5 illustrates the allowable transitions between power modes. Sleep and hibernate modes should not be entered until all V_{DDIO} supplies are at valid voltage levels and interrupts are enabled.

Table 6-2. Power Modes

Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (programmable)	Wakeup, reset, manual register entry	Any interrupt	Any (programmable)	All regulators available.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off	Manual register entry	Any interrupt	Any (programmable)	All regulators available.
Sleep	All subsystems automatically disabled	Manual register entry	CTW[10]	ILO	All regulators available.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry			Only hibernate regulator active.

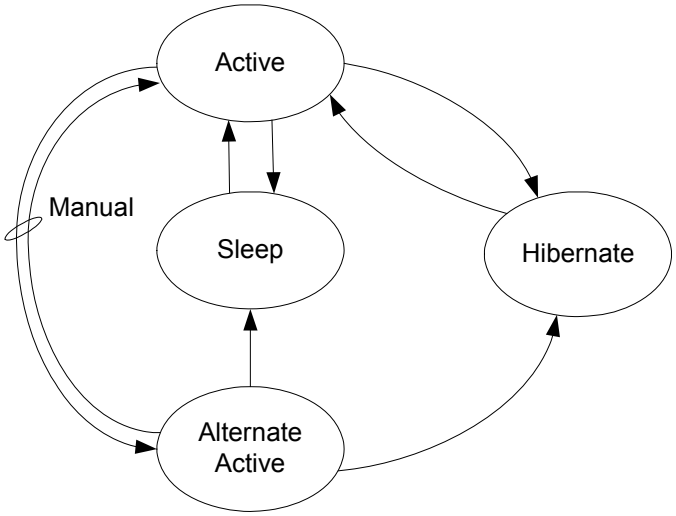
Table 6-3. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (Typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	–	6 mA[9]	Yes	All	All	All	–	All
Alternate Active	–	–	User defined	All	All	All	–	All
Sleep	125 µs typ	2 µA[10]	No	None	None	ILO	CTW	XRES
Hibernate	–	300 nA	No	None	None	None	–	XRES

Notes

9. Bus clock off. Execute from CPU instruction buffer at 6 MHz. See Table 11-2 on page 58.
10. During sleep mode, the CTW generates periodic interrupts to wake up the device. This affects the average current, which is a composite of the sleep mode current and active mode current, and the time spent in each mode. With the maximum wakeup interval of 128 ms, and at wakeup the CPU executes only the standard PSoC Creator sleep API (for a duty cycle of 0.2%), the average current draw is typically 35 µA.

Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode powers down the CPU and other internal circuitry to reduce power consumption. However, supervisory services such as the central timewheel (CTW) remain available in this mode. The device can wake up using CTW or system reset. The wake up time from sleep mode is 125 µs (typical).

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external reset (XRES).

6.2.1.5 Wakeup Events

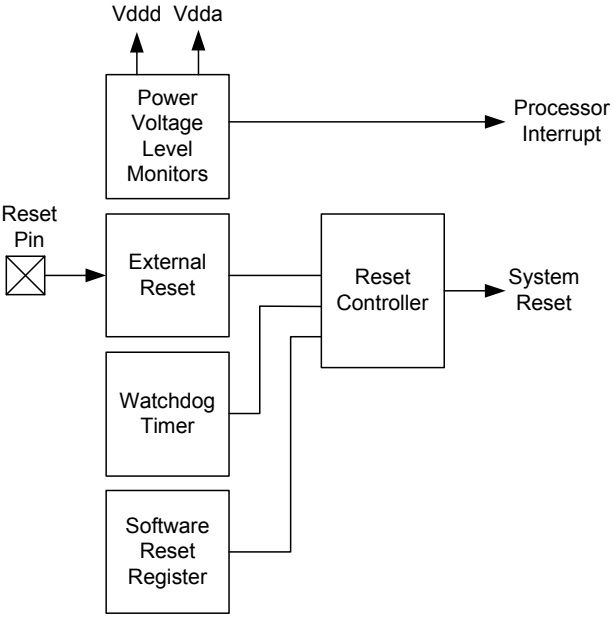
Wakeup events can come from the central timewheel or device reset. A wakeup event restores the system to active mode. The central timewheel allows the system to periodically wake up, poll peripherals, do voltage monitoring, or perform real-time functions. Reset event sources include the external reset pin (XRES).

6.3 Reset

CY8C53 has multiple internal and external reset sources available. The reset sources are:

- Power source monitoring - The analog and digital power voltages, V_{DDA}, V_{DDD}, V_{CCA}, and V_{CCD} are monitored in several different modes during power up and active mode. The monitors are programmable to generate an interrupt to the processor under certain conditions.
- External - The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to Vddio1. V_{DDD}, V_{DDA}, and Vddio1 must all have voltage applied before the part comes out of reset.
- Watchdog timer - A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset. The watchdog timer can be used only when the part remains in active mode.
- Software - The device can be reset under program control.

Figure 6-6. Resets



The term **system reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Power Voltage Level Monitors

- IPOR - Initial Power on Reset

  At initial power on, IPOR monitors the power voltages V_{DDD} and V_{DDA}, both directly at the pins and at the outputs of the corresponding internal regulators. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 100 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

  To save power the IPOR circuit is disabled when the internal digital supply is stable. When the voltage is high enough, the IMO starts.

- ALVI, DLVI, AHVI - Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

  Interrupt circuits are available to detect when V_{DDA} and V_{DDD} go outside a voltage range. For AHVI, V_{DDA} is compared to a fixed trip level. For ALVI and DLVI, V_{DDA} and V_{DDD} are compared to trip levels that are programmable, as listed in Table 6-4.

Table 6-4. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	V_{DDD}	2.7 V-5.5 V	2.45 V-5.45 V in 250 mV increments. The 2.45 V setting is used for LVD.
ALVI	V_{DDA}	2.7 V-5.5 V	2.45 V-5.45 V in 250 mV increments. The 2.45 V setting is used for LVD
AHVI	V_{DDA}	2.7 V-5.5 V	5.75 V

The monitors are disabled until after IPOR. The monitors are not available in low-power modes. To monitor voltages in sleep mode, wake up periodically using the CTW. After wakeup, the 2.45 V LVI interrupt may trigger. Voltage monitoring is not available in hibernate mode.

6.3.2 Other Reset Sources

- XRES - External Reset

  CY8C53 has a dedicated XRES pin which, holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

  The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

- SRES - Software Reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- WRES - Watchdog Timer Reset

  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event. The watchdog timer can be used only when the part remains in active mode.

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the V_{DDIO} pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both General Purpose I/O (GPIO) and Special I/O (SIO) provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense[6], and LCD segment drive, while SIO pins are used for voltages in excess of V_{DDA} and for programmable output voltages.

- Features supported by both GPIO and SIO:
  - Separate I/O supplies and voltages for up to four groups of I/O
  - Digital peripherals use DSI to connect the pins
  - Input or output or both for CPU and DMA
  - Eight drive modes
  - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
  - Dedicated port interrupt vector for each port
  - Slew rate controlled digital output drive mode
  - Access port control and configuration registers on either port basis or pin basis
  - Separate port read (PS) and write (DR) data registers to avoid

- Additional features only provided on the GPIO pins:
  - LCD segment drive on LCD equipped devices
  - CapSense on CapSense equipped devices[6]
  - Analog input and output capability
  - Continuous 100 µA clamp current capability
  - Standard drive strength down to 2.7 V
- Additional features only provided on SIO pins:
  - Higher drive strength than GPIO
  - Hot swap capability (5 V tolerance at any operating V_{DD})
  - Programmable and regulated high input and output drive levels down to 1.2 V
  - No analog input or LCD capability
  - Over voltage tolerance up to 5.5 V
  - SIO can act as a general purpose analog comparator
- USBIO features:
  - Full speed USB 2.0 I/O
  - Highest drive strength for general purpose use
  - Input, output, or both for CPU and DMA
  - Input, output, or both for digital peripherals
  - Digital output (CMOS) drive mode
  - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

Figure 6-7. GPIO Block Diagram

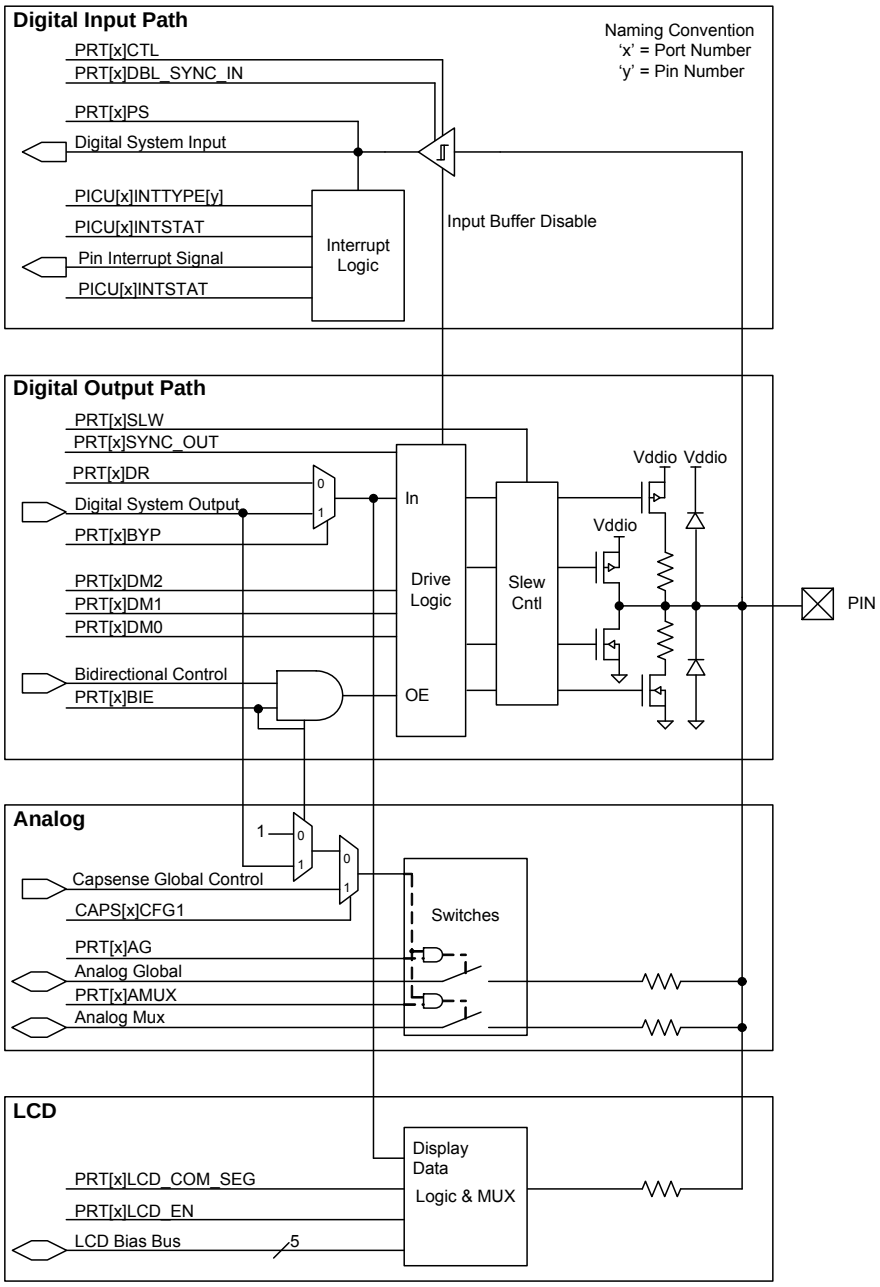


Figure 6-8. SIO Input/Output Block Diagram

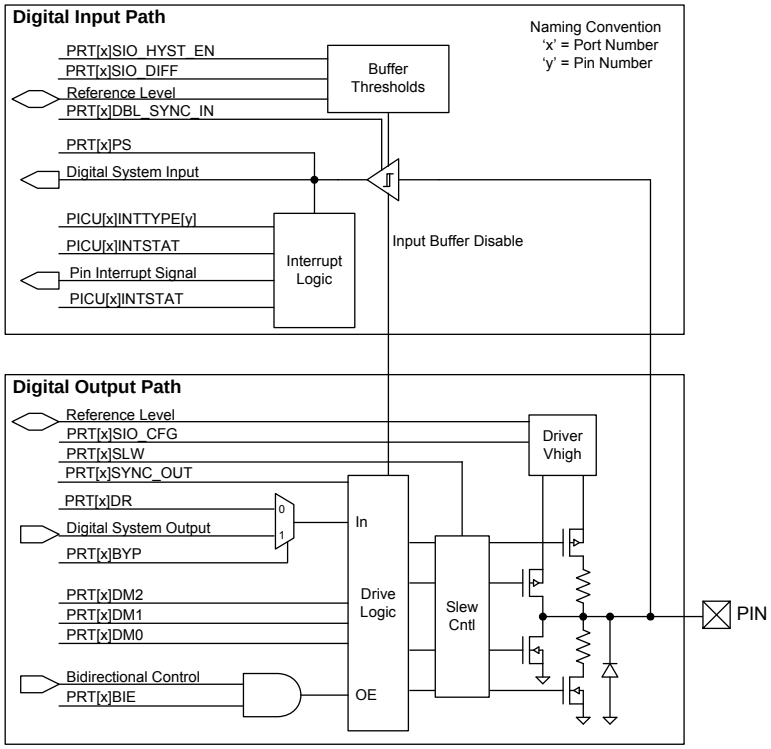
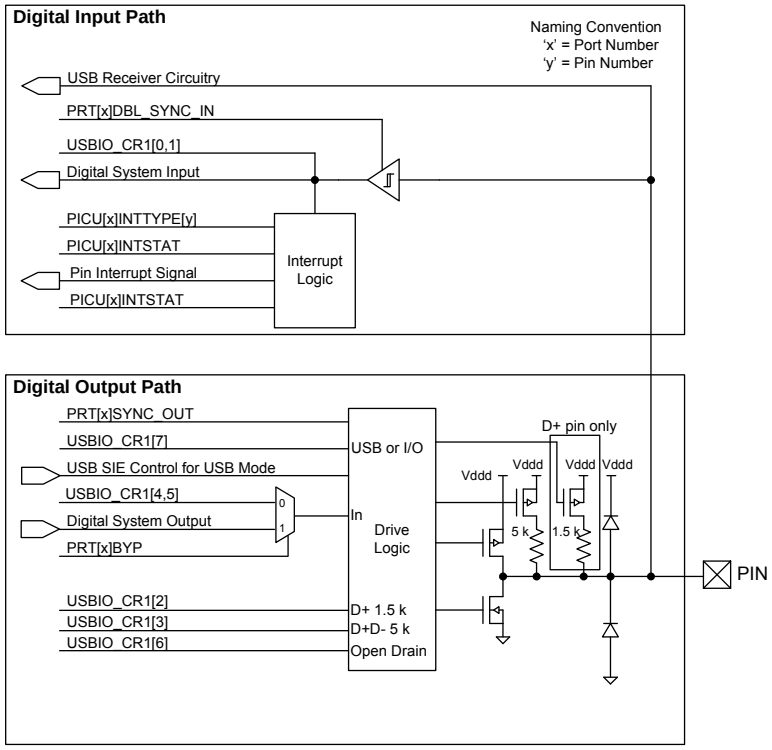


Figure 6-9. USBIO Block Diagram



6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-5. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-10 depicts a simplified pin view based on each of the eight drive modes. Table 6-5 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-10. Drive Mode

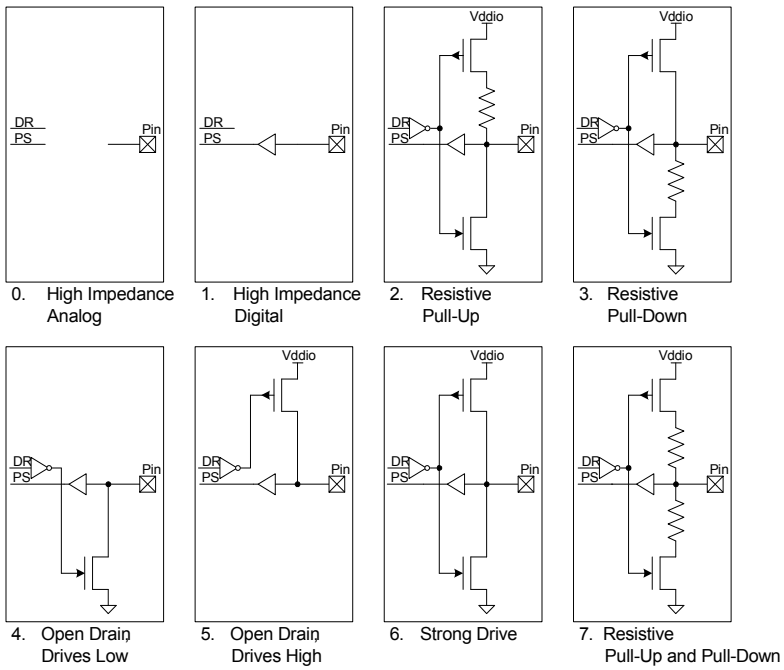


Table 6-5. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedence analog	0	0	0	High-Z	High-Z
1	High Impedance digital	0	0	1	High-Z	High-Z
2	Resistive pull-up[11]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down[11]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High-Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High-Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down[11]	1	1	1	Res High (5K)	Res Low (5K)

- High Impedance Analog

  The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

  To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

- High Impedance Digital

  The input buffer is enabled for digital signal input. This is the standard high impedance (HiZ) state recommended for digital inputs.

Note
11. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

- Resistive pull-up or resistive pull-down

  Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

- Open drain, drives high and open drain, drives low

  Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I^2C bus signal lines.

- Strong drive

  Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

- Resistive pull-up and pull-down

  Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

High speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRTxDM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRTxSLW registers.

6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to “1” and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

While level sensitive interrupts are not directly supported; Universal Digital Blocks (UDB) provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip’s analog (V_{DDA}) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine V_{DDIO} capability for a given port and pin.

The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the V_{DDIO} supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[6]. See the “CapSense” section on page 51 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the “LCD Direct Drive” section on page 50 for details.

6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO's respective V_{DDIO}. SIO pins are individually configurable to output either the standard V_{DDIO} level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see Figure 6-11). The "DAC" section on page 51 has more details on VDAC use and reference routing to the SIO pins. Resistive pull-up and pull-down drive modes are not available with SIO in regulated output mode.

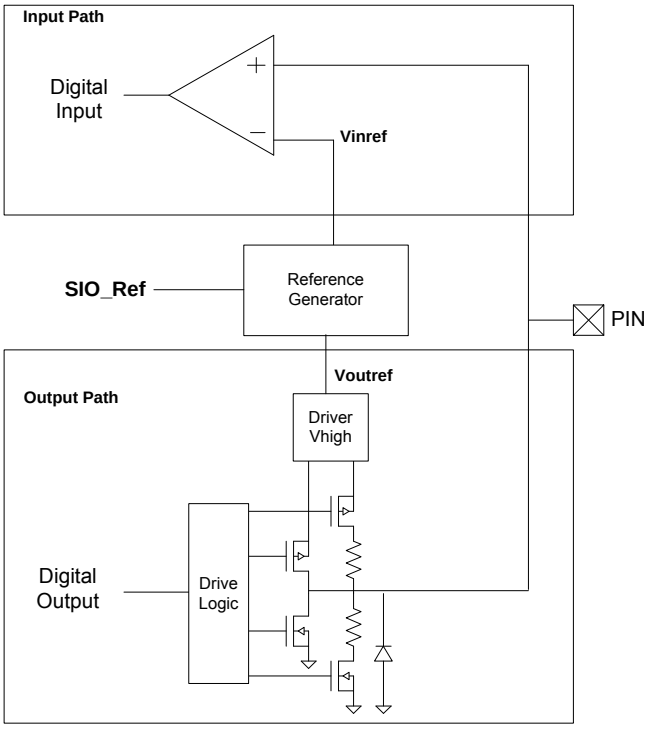
6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which, is used to set the digital input buffer reference level for interface to external signals that differ in voltage from V_{DDIO}. The reference sets the pins voltage threshold for a high logic level (see Figure 6-11). Available input thresholds are:

- 0.5 × V_{DDIO}
- 0.4 × V_{DDIO}
- 0.5 × V_{REF}
- V_{REF}

Typically a voltage DAC (VDAC) generates the V_{REF} reference. "DAC" section on page 51 has more details on VDAC use and reference routing to the SIO pins.

Figure 6-11. SIO Reference for Input and Output



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the Adjustable Input Level section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold.

The digital input path in Figure 6-8 on page 28 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a GPIO pin's protection diode.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage ($V_{DDIO} < V_{IN} < V_{DDA}$) tolerance feature at any operating V_{DD}.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit.
- The GPIO pins must be limited to 100 µA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the V_{DDIO} supply.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the V_{DDIO} supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I^2C where different devices are running from different supply voltages. In the I^2C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I^2C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 2.7 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated V_{DDIO} supply pin.

The I/O pin must be configured into a high impedance drive mode, open drain low drive mode, or pull-down drive mode, for over voltage tolerance to work properly. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

At reset, all I/Os are reset to the High Impedance Analog state.

6.4.17 Low Power Functionality

In all low power modes the I/O pins retain their state until the part is awakened and changed or reset.

6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in "Pinouts" on page 5. The special features are:

- Digital
  - 32.768 kHz crystal oscillator
  - SWD and SWV interface pins
  - External reset
- Analog
  - Opamp inputs and outputs
  - High current IDAC outputs
  - External reference inputs

7. Digital Subsystem

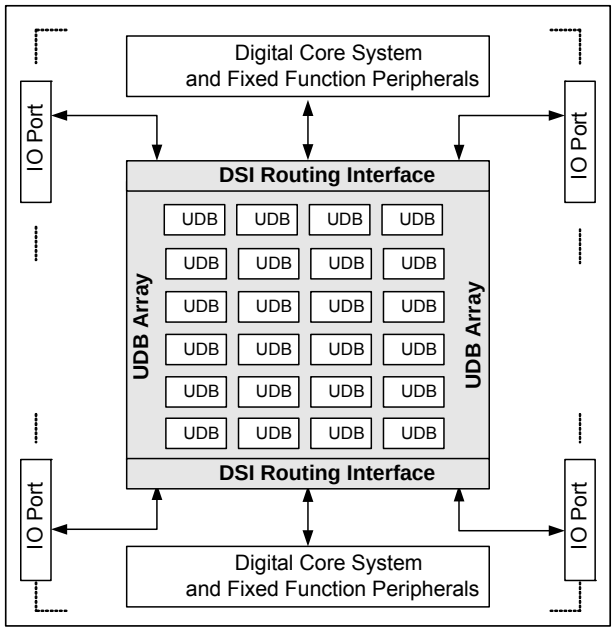
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. Designers do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- Universal Digital Blocks (UDB) - These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal Digital Block Array - UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- Digital System Interconnect (DSI) - Digital signals from UDBs, fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the Digital System Interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the Universal Digital Block Array.

Figure 7-1. CY8C53 Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C53 family's UDBs and analog blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the data sheet, and the list is always growing. An example of a component available for use in CY8C53 family, but, not explicitly called out in this data sheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C53 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Communications
  - I^2C (1 to 3 UDBs)
  - UART (1 to 3 UDBs)
- Functions
  - PWM (1 to 2 UDBs)
- Logic (x CPLD product terms per logic function)
  - NOT
  - OR
  - XOR
  - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C53 family. The exact amount of hardware resources (SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Amplifiers
  - TIA
  - PGA
  - opamp
- ADC
  - Successive Approximation (SAR)
- DACs
  - Current
  - Voltage
  - PWM
- Comparators
- Mixers

7.1.3 Example System Function Components

The following is a sample of the system function components available in PSoC Creator for the CY8C53 family. The exact amount of hardware resources (UDBs, SC/CT blocks, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- CapSense
- LCD Drive
- LCD Control
- Filters

7.1.4 Designing with PSoC Creator

7.1.4.1 More Than a Typical IDE

A successful design tool allows for the rapid development and deployment of both simple and complex designs. It reduces or eliminates any learning curve. It makes the integration of a new design into the production stream straightforward.

PSoC Creator is that design tool.

PSoC Creator is a full featured Integrated Development Environment (IDE) for hardware and software design. It is optimized specifically for PSoC devices and combines a modern, powerful software development platform with a sophisticated graphical design tool. This unique combination of tools makes PSoC Creator the most flexible embedded design platform available.

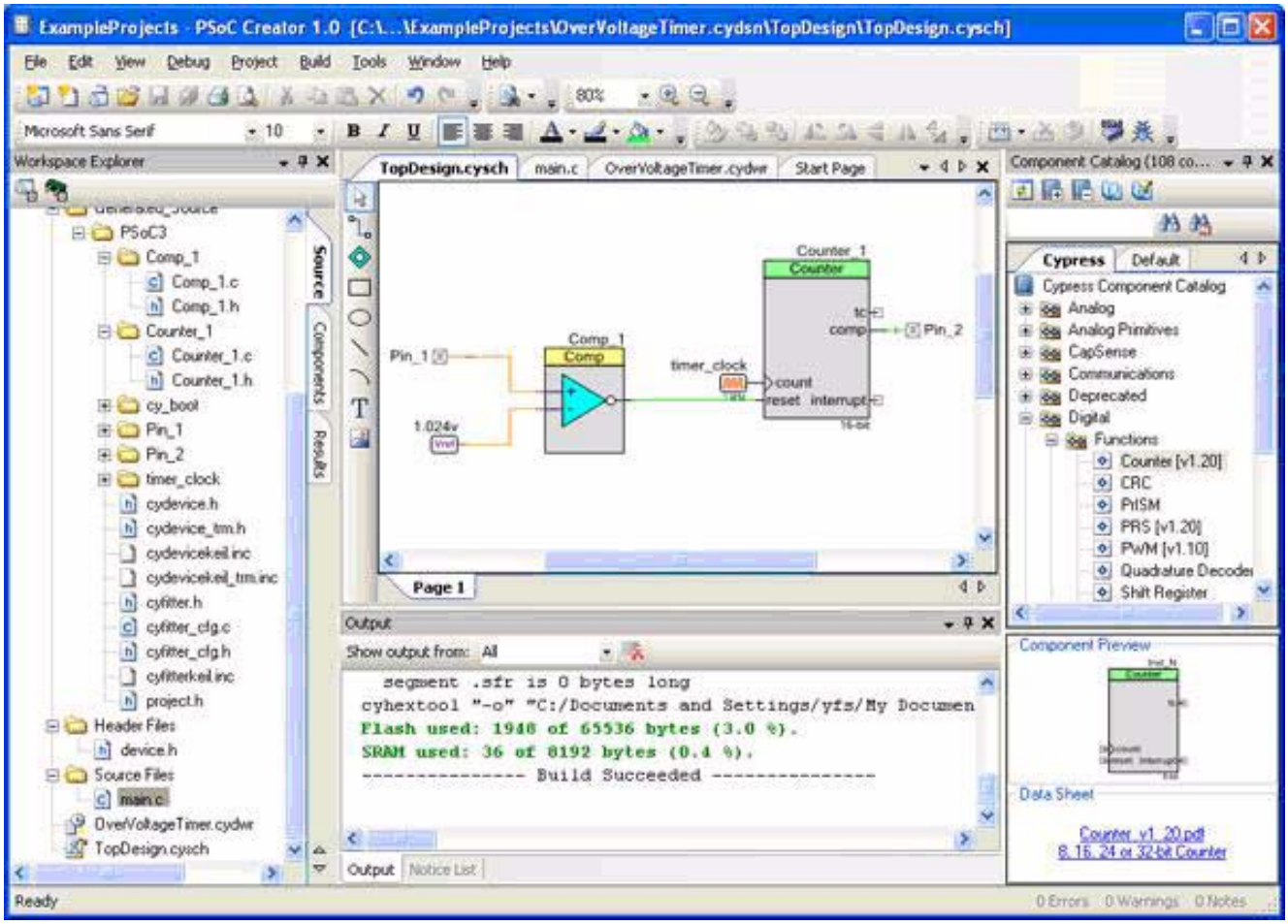
Graphical design entry simplifies the task of configuring a particular part. You can select the required functionality from an extensive catalog of components and place it in your design. All components are parameterized and have an editor dialog that allows you to tailor functionality to your needs.

PSoC Creator automatically configures clocks and routes the I/O to the selected pins and then generates APIs to give the application complete control over the hardware. Changing the PSoC device configuration is as simple as adding a new component, setting its parameters, and rebuilding the project.

At any stage of development you are free to change the hardware configuration and even the target processor. To retarget your application (hardware and software) to new devices, even from 8- to 32-bit families, just select the new device and rebuild.

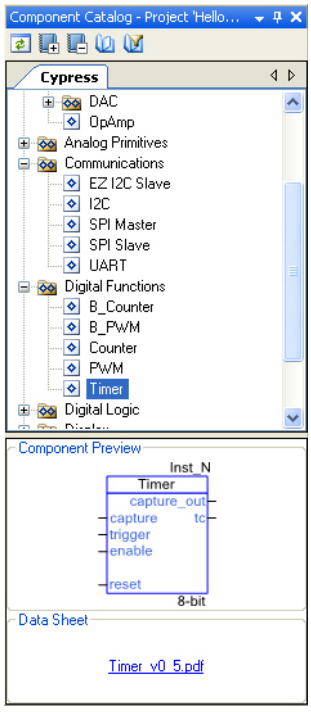
You also have the ability to change the C compiler and evaluate an alternative. Components are designed for portability and are validated against all devices, from all families, and against all supported tool chains. Switching compilers is as easy as editing from the project options and rebuilding the application with no errors from the generated APIs or boot code.

Figure 7-2. PSoC Creator Framework



7.1.4.2 Component Catalog

Figure 7-3. Component Catalog



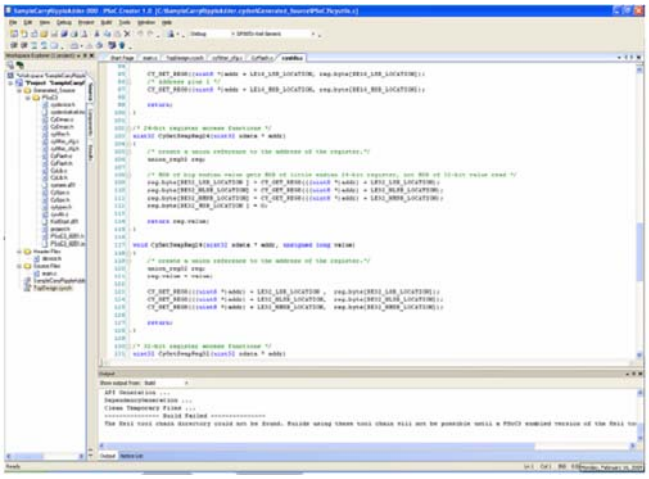
The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC, DACs, and filters, and communication protocols, such as I^2C and USB. See "Example Peripherals" section on page 32 for more details about available peripherals. All content is fully characterized and carefully documented in data sheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

7.1.4.4 Software Development

Figure 7-4. Code Editor

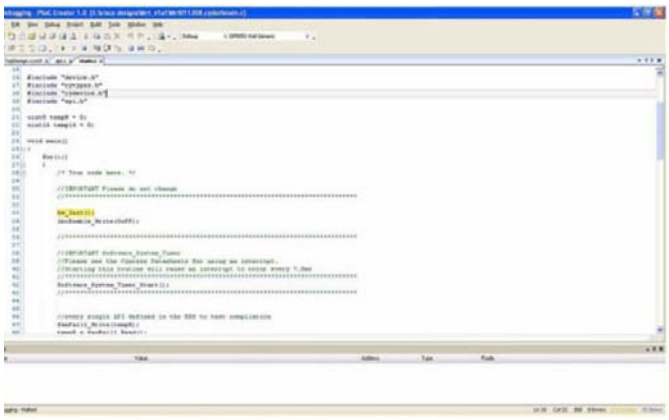


Anchoring the tool is a modern, highly customizable user interface. It includes project management and integrated editors for C and assembler source code, as well the design entry tools.

Project build control leverages compiler technology from top commercial vendors such as ARM® Limited, Keil™, and CodeSourcery (GNU). Free versions of Keil C51 and GNU C Compiler (GCC) for ARM, with no restrictions on code size or end product distribution, are included with the tool distribution. Upgrading to more optimizing compilers is a snap with support for the professional Keil C51 product and ARM RealView™ compiler.

7.1.4.5 Nonintrusive Debugging

Figure 7-5. PSoC Creator Debugger



With SWD debug connectivity available on all devices, the PSoC Creator debugger offers full control over the target device with minimum intrusion. Breakpoints and code execution commands are all readily available from toolbar buttons and an impressive lineup of windows—register, locals, watch, call stack, memory and peripherals—make for an unparalleled level of visibility into the system.

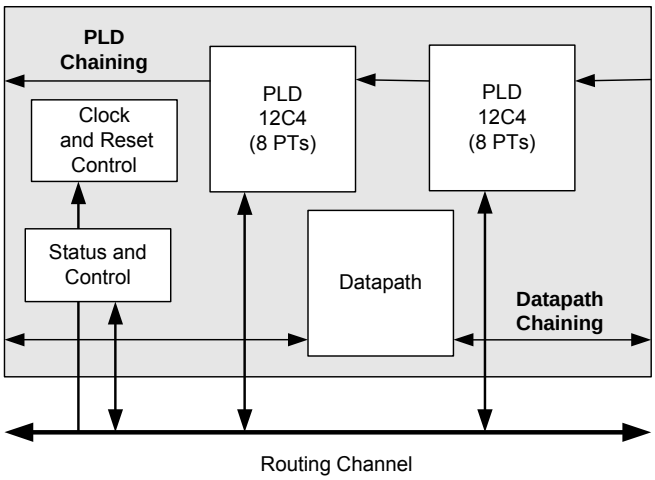
PSoC Creator contains all the tools necessary to complete a design, and then to maintain and extend that design for years to come. All steps of the design flow are carefully integrated and optimized for ease-of-use and to maximize productivity.

7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^2C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-6. UDB Block Diagram



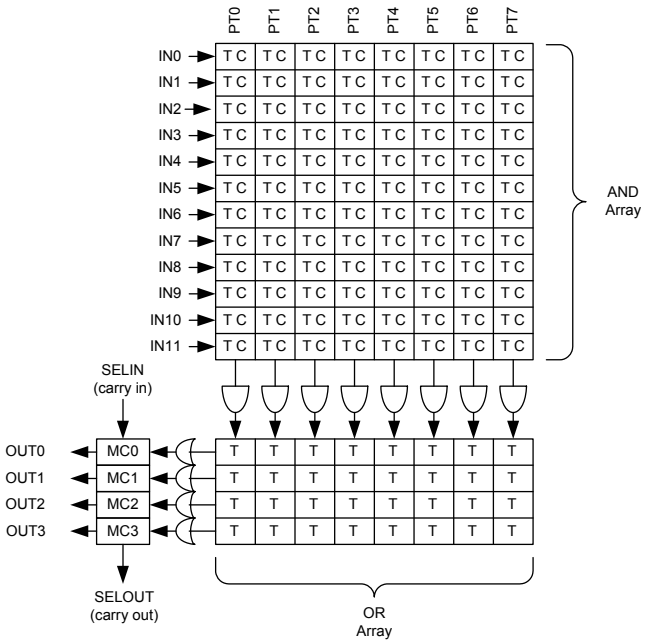
The main component blocks of the UDB are:

- PLD blocks - There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module - This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and Control Module - The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module - This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, look up tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-7. PLD 12C4 Structure

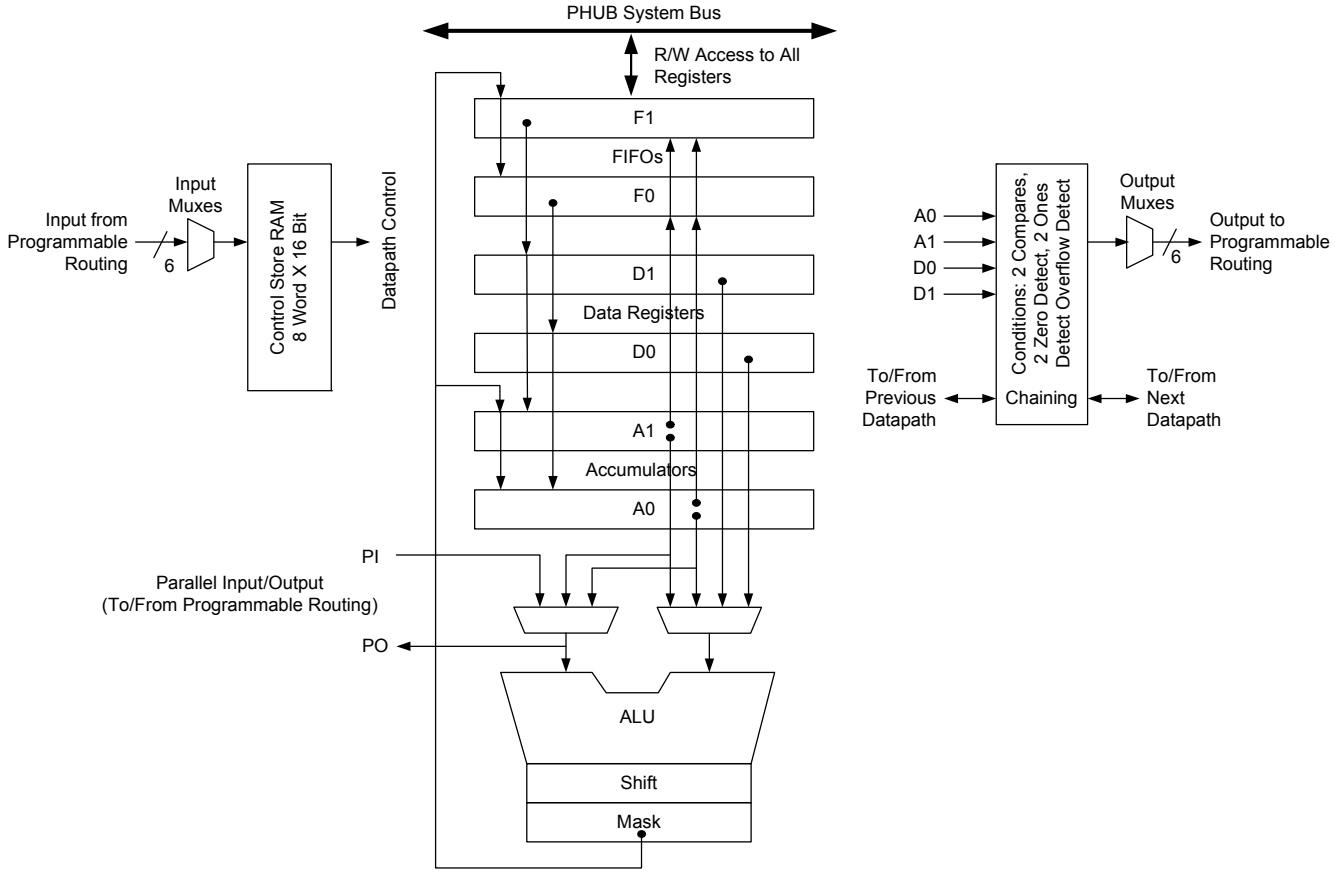


One 12C4 PLD block is shown in Figure 7-7. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V 10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

7.2.2 Datapath Module

The datapath contains an 8-bit single cycle ALU, with associated compare and condition generation logic. This datapath block is optimized to implement embedded functions, such as timers, counters, integrators, PWMs, PRS, CRC, shifters and dead band generators and many others.

Figure 7-8. Datapath Top Level



7.2.2.6 Working Registers

The datapath contains six primary working registers, which are accessed by CPU firmware or DMA during normal operation.

Table 7-1. Working Datapath Registers

Name	Function	Description
A0 and A1	Accumulators	These are sources and sinks for the ALU and also sources for the compares.
D0 and D1	Data Registers	These are sources for the ALU and sources for the compares.
F0 and F1	FIFOs	These are the primary interface to the system bus. They can be a data source for the data registers and accumulators or they can capture data from the accumulators or ALU. Each FIFO is four bytes deep.

7.2.2.7 Dynamic Datapath Configuration RAM

Dynamic configuration is the ability to change the datapath function and internal configuration on a cycle-by-cycle basis, under sequencer control. This is implemented using the 8-word x 16-bit configuration RAM, which stores eight unique 16-bit wide configurations. The address input to this RAM controls the sequence, and can be routed from any block connected to the UDB routing matrix, most typically PLD logic, I/O pins, or from the outputs of this or other datapath blocks.

ALU

The ALU performs eight general purpose functions. They are:

- Increment
- Decrement
- Add
- Subtract
- Logical AND
- Logical OR
- Logical XOR
- Pass, used to pass a value through the ALU to the shift register, mask, or another UDB register

Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

7.2.2.8 Conditionals

Each datapath has two compares, with bit masking options. Compare operands include the two accumulators and the two data registers in a variety of configurations. Other conditions include zero detect, all ones detect, and overflow. These conditions are the primary datapath outputs, a selection of which can be driven out to the UDB routing matrix. Conditional computation can use the built in chaining to neighboring UDBs to operate on wider data widths without the need to use routing resources.

7.2.2.9 Variable MSB

The most significant bit of an arithmetic and shift function can be programmatically specified. This supports variable width CRC and PRS functions, and in conjunction with ALU output masking, can implement arbitrary width timers, counters and shift blocks.

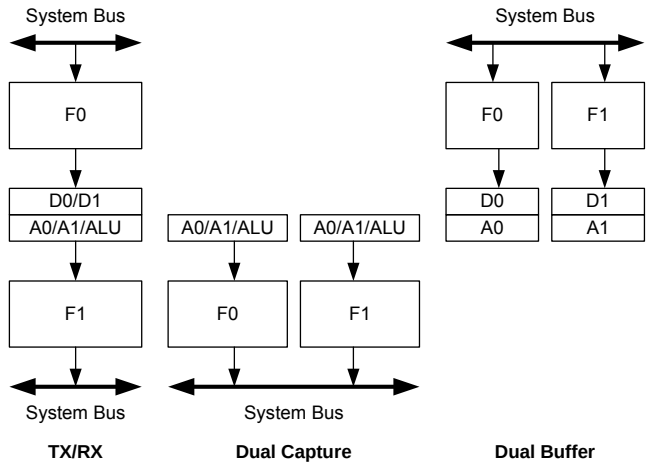
7.2.2.10 Built in CRC/PRS

The datapath has built in support for single cycle Cyclic Redundancy Check (CRC) computation and Pseudo Random Sequence (PRS) generation of arbitrary width and arbitrary polynomial. CRC/PRS functions longer than 8 bits may be implemented in conjunction with PLD logic, or built in chaining may be use to extend the function into neighboring UDBs.

7.2.2.11 Input/Output FIFOs

Each datapath contains two four-byte deep FIFOs, which can be independently configured as an input buffer (system bus writes to the FIFO, datapath internal reads the FIFO), or an output buffer (datapath internal writes to the FIFO, the system bus reads from the FIFO). The FIFOs generate status that are selectable as datapath outputs and can therefore be driven to the routing, to interact with sequencers, interrupts, or DMA.

Figure 7-9. Example FIFO Configurations



7.2.2.12 Chaining

The datapath can be configured to chain conditions and signals such as carries and shift data with neighboring datapaths to create higher precision arithmetic, shift, CRC/PRS functions.

7.2.2.13 Time Multiplexing

In applications that are over sampled, or do not need high clock rates, the single ALU block in the datapath can be efficiently shared with two sets of registers and condition generators. Carry and shift out data from the ALU are registered and can be selected as inputs in subsequent cycles. This provides support for 16-bit functions in one (8-bit) datapath.

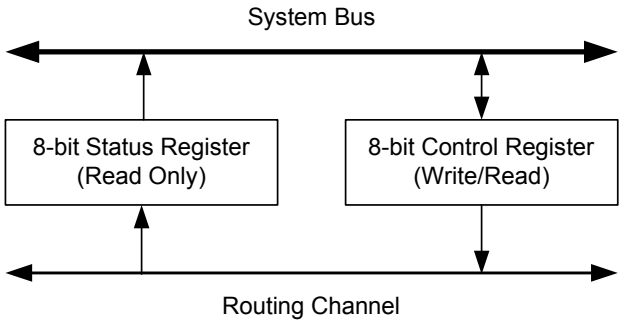
7.2.2.14 Datapath I/O

There are six inputs and six outputs that connect the datapath to the routing matrix. Inputs from the routing provide the configuration for the datapath operation to perform in each cycle, and the serial data inputs. Inputs can be routed from other UDB blocks, other device peripherals, device I/O pins, and so on. The outputs to the routing can be selected from the generated conditions, and the serial data outputs. Outputs can be routed to other UDB blocks, device peripherals, interrupt and DMA controller, I/O pins, and so on.

7.2.3 Status and Control Module

The primary purpose of this circuitry is to coordinate CPU firmware interaction with internal UDB operation.

Figure 7-10. Status and Control Registers



The bits of the control register, which may be written to by the system bus, are used to drive into the routing matrix, and thus provide firmware with the opportunity to control the state of UDB processing. The status register is read-only and it allows internal UDB state to be read out onto the system bus directly from internal routing. This allows firmware to monitor the state of UDB processing. Each bit of these registers has programmable connections to the routing matrix and routing connections are made depending on the requirements of the application.

7.2.3.15 Usage Examples

As an example of control input, a bit in the control register can be allocated as a function enable bit. There are multiple ways to enable a function. In one method the control bit output would be routed to the clock control block in one or more UDBs and serve as a clock enable for the selected UDB blocks. A status example is a case where a PLD or datapath block generated a condition, such as a “compare true” condition that is captured and latched by the status register and then read (and cleared) by CPU firmware.

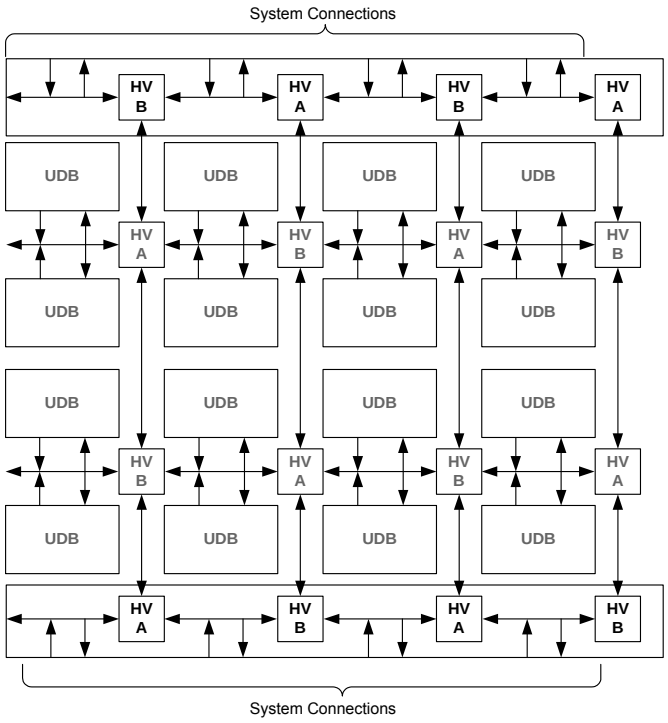
7.2.3.16 Clock Generation

Each subcomponent block of a UDB including the two PLDs, the datapath, and Status and Control, has a clock selection and control block. This promotes a fine granularity with respect to allocating clocking resources to UDB component blocks and allows unused UDB resources to be used by other functions for maximum system efficiency.

7.3 UDB Array Description

Figure 7-11 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-11. Digital System Interface Structure

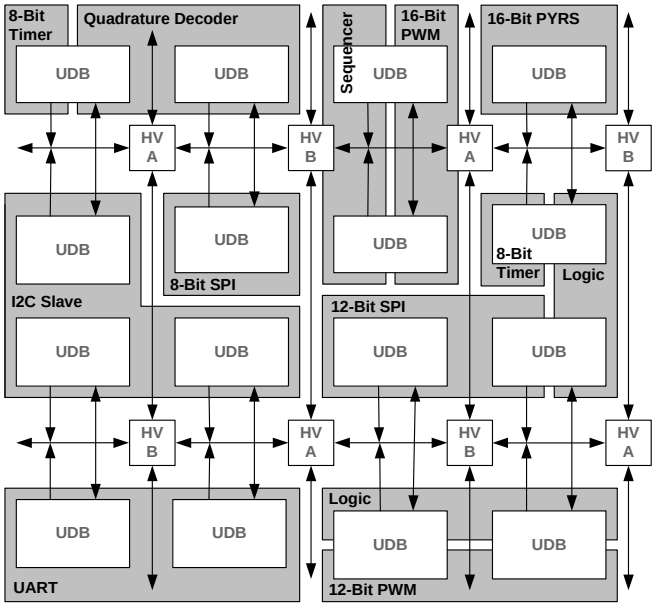


7.3.1 UDB Array Programmable Resources

Figure 7-12 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit Timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-12. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

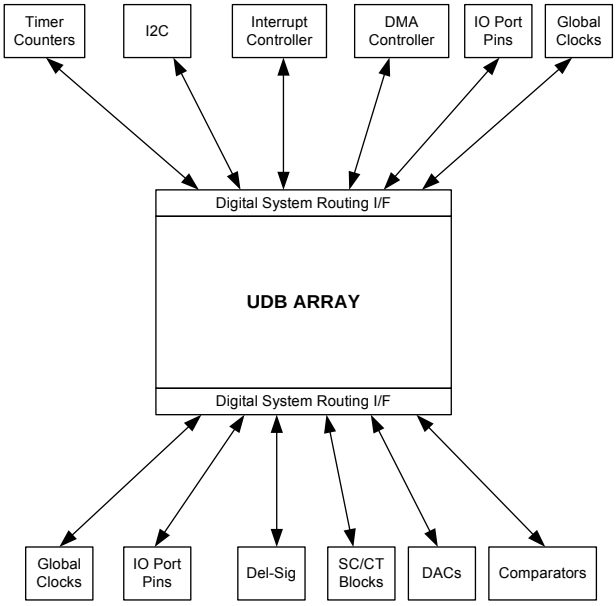
The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-13 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

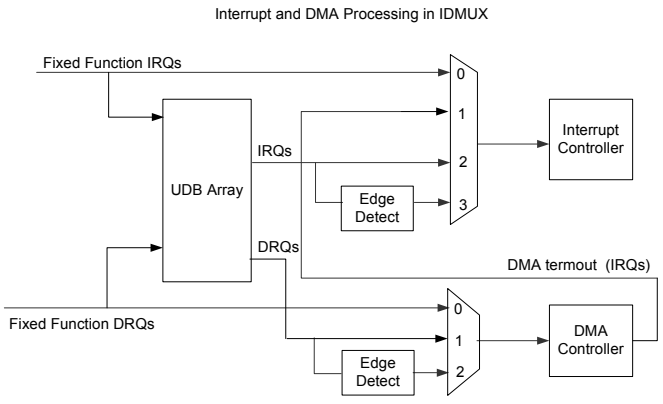
- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

Figure 7-13. Digital System Interconnect



Interrupt and DMA routing is very flexible in the CY8C53 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-14 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-14. Interrupt and DMA Processing in the IDMUX



7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the system clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-15. I/O Pin Synchronization Routing

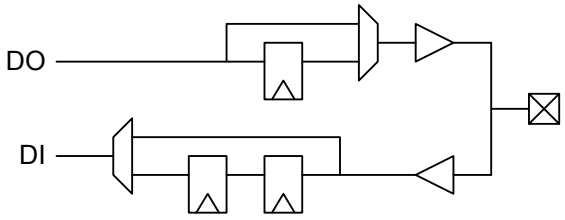
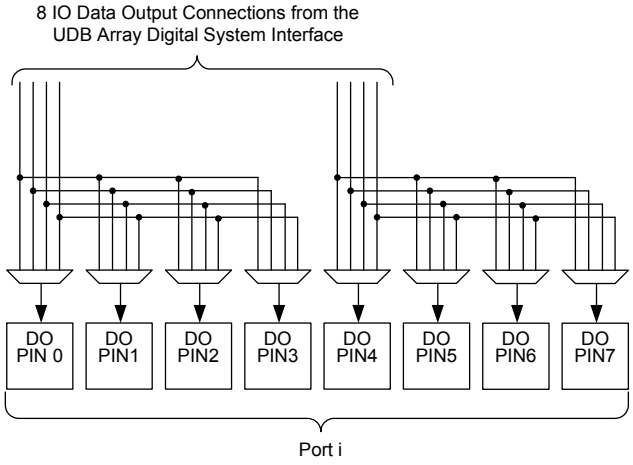
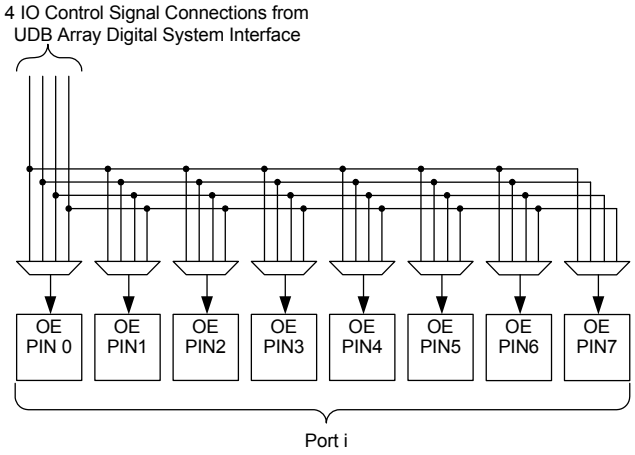


Figure 7-16. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Figure 7-17. I/O Pin Output Enable Connectivity



7.5 USB

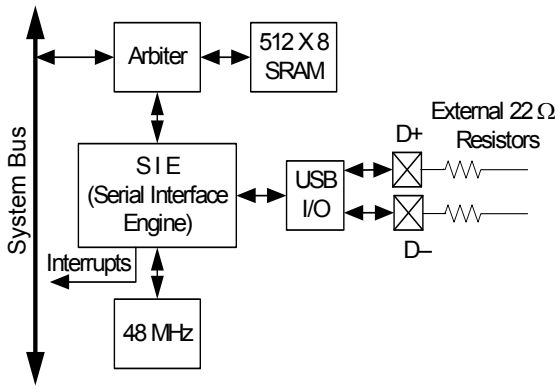
PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 25.

When using USB, either a crystal must be used (24 MHz with MHzECO) or a similar high-accuracy clock source must be provided externally through a pin and the DSI. Also, bus clock must be equal to 33 MHz. See *Section 6.1* on page 18 for details.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Two memory modes
  - Manual Memory Management with No DMA Access
  - Manual Memory Management with Manual DMA Access
- Internal 3.3 V regulator for transceiver
- Interrupts on bus and each endpoint event
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

Figure 7-18. USB



7.6 Timers, Counters, and PWMs

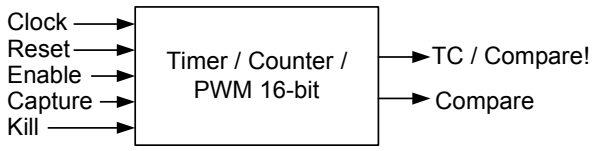
The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows designers to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output and terminal count output (optional complementary compare output). The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-19. Timer/Counter/PWM



7.7 I²C

The I²C peripheral provides a synchronous two wire interface designed to interface the PSoC device with a two wire I²C serial communication bus. The bus is compliant with Philips 'The I²C Specification' version 2.1. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

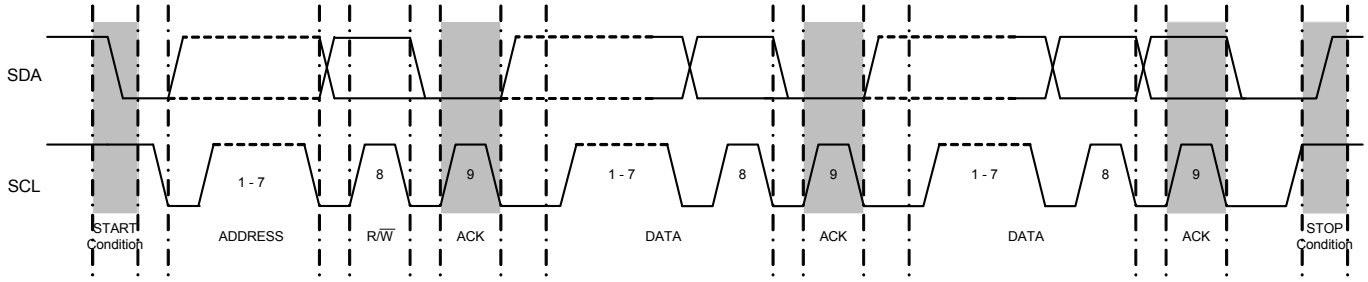
To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master)[12]. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through the DSI routing and allows direct connections to any GPIO or SIO pins.

I²C features include:

- Slave and Master, Transmitter, and Receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 400 Kbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)

Data transfers follow the format shown in Figure 7-20. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Figure 7-20. I²C Complete Transfer Timing



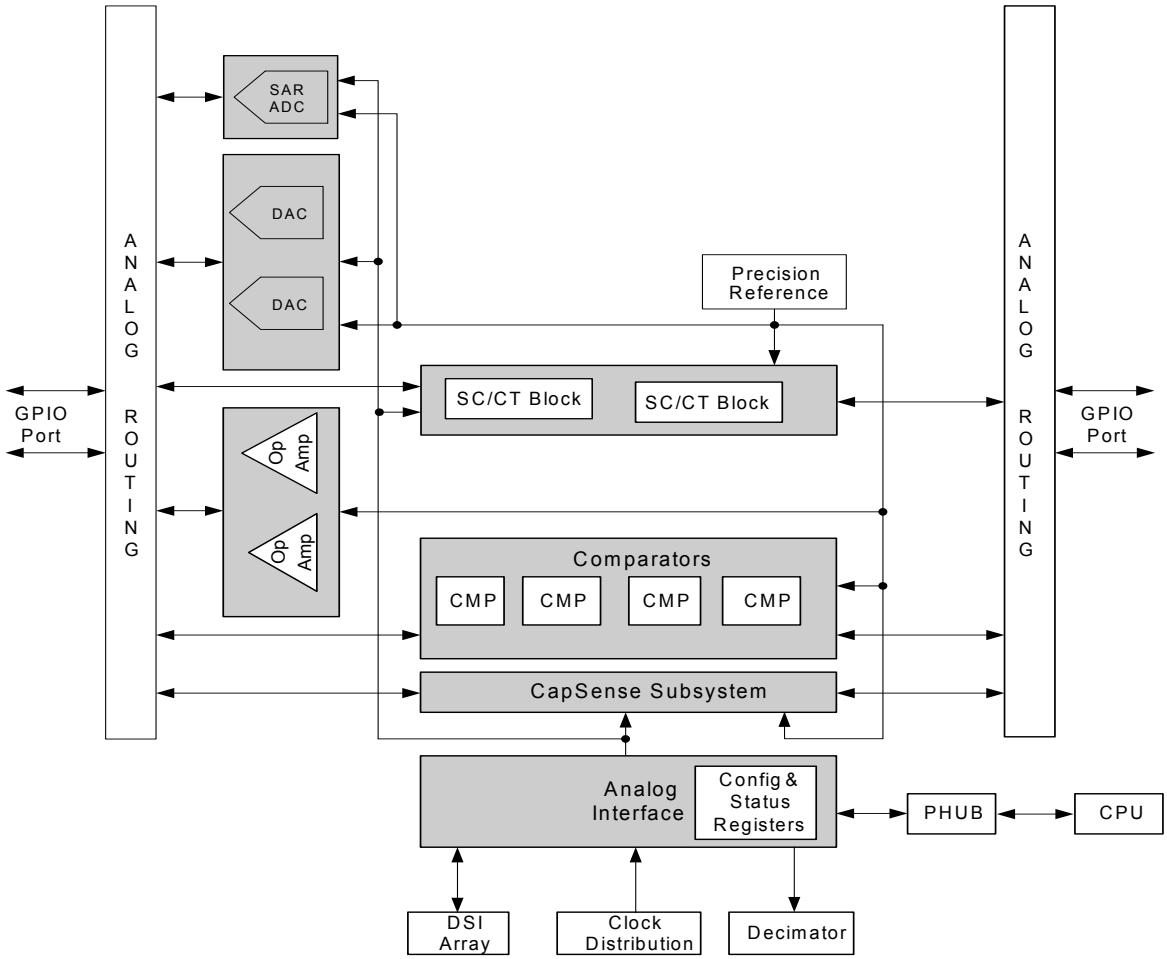
Note
12. Fixed-block I2C does not support undefined bus conditions. These conditions should be avoided, or the UDB-based I2C component should be used instead.

8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses
- Successive approximation (SAR) ADC
- Two 8-bit DACs that provide either voltage or current output
- Four comparators with optional connection to configurable LUT outputs
- Two configurable switched capacitor/continuos time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer
- Two opamps for internal use and connection to GPIO that can be used as high current output buffers
- CapSense subsystem to enable capacitive touch sensing
- Precision reference for generating an accurate analog voltage for internal analog blocks

Figure 8-1. Analog Subsystem Block Diagram



The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and also connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

8.1 Analog Routing

The PSoC 5 family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks. All analog routing switches are open when the device is in sleep or hibernate mode.

For information on how to make pin selections for optimal analog routing, refer to the application note, AN58304 - PSoC® 3 and PSoC® 5 - Pin Selection for Analog Designs.

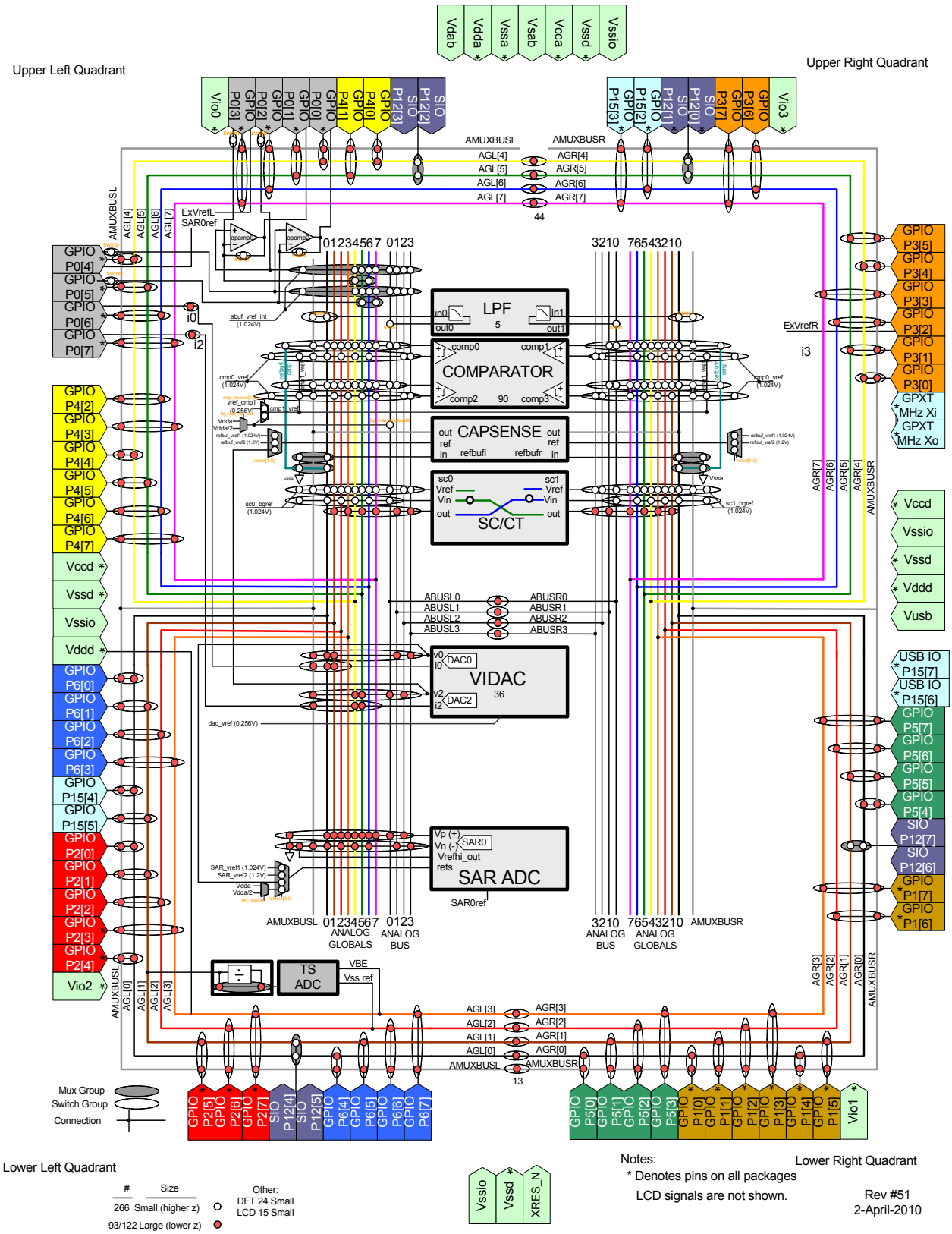
8.1.1 Features

- Flexible, configurable analog routing architecture
- 16 Analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus
- 8 Analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the PSoC 5 family. The analog routing architecture is divided into four quadrants as shown in Figure 8-2. Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in PSoC 5, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in Figure 8-2.

Figure 8-2. CY8C53 Analog Interconnect



Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in PSoC 5, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

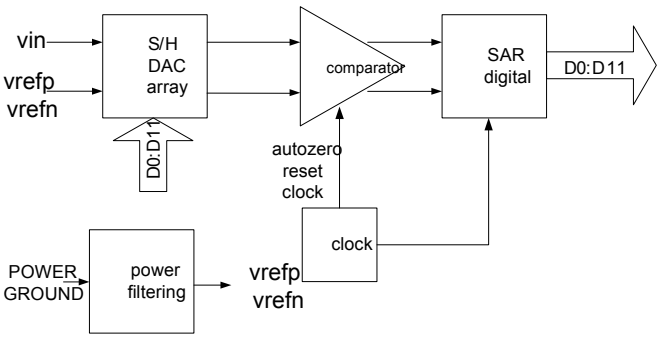
8.2 Successive Approximation ADC

The CY8C53 family of devices has a Successive Approximation (SAR) ADC. This ADC is 12-bit at up to 700 ksps, with single-ended or differential inputs, making it useful for a wide variety of sampling and control applications.

8.2.1 Functional Description

In a SAR ADC an analog input signal is sampled and compared with the output of a DAC. A binary search algorithm is applied to the DAC and used to determine the output bits in succession from MSB to LSB. A block diagram of one SAR ADC is shown in Figure 8-3.

Figure 8-3. SAR ADC Block Diagram



The input is connected to the analog globals and muxes. The maximum clock rate is 14 MHz.

8.2.2 Conversion Signals

Writing a start bit or assertion of a Start of Frame (SOF) signal is used to start a conversion. SOF can be used in applications where the sampling period is longer than the conversion time, or when the ADC needs to be synchronized to other hardware. This signal is optional and does not need to be connected if the SAR ADC is running in a continuous mode. A digital clock or UDB output can be used to drive this input. When the SAR is first powered up or awakened from any of the sleeping modes, there is a power up wait time of 10 µs before it is ready to start the first conversion.

When the conversion is complete, a status bit is set and the output signal End of Frame (EOF) asserts and remains asserted until the value is read by either the DMA controller or the CPU. The EOF signal may be used to trigger an interrupt or a DMA request.

8.2.3 Operational Modes

A ONE_SHOT control bit is used to set the SAR ADC conversion mode to either continuous or one conversion per SOF signal. DMA transfer of continuous samples, without CPU intervention, is supported.

8.3 Comparators

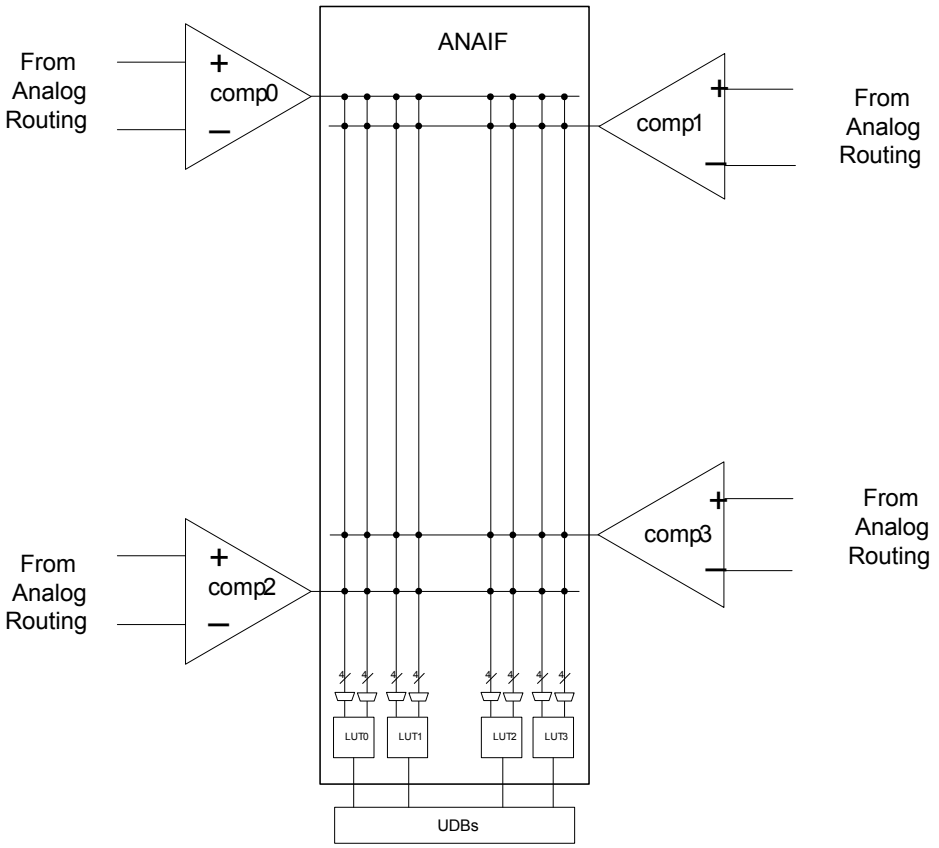
The CY8C53 family of devices contains four comparators. Comparators have these features:

- Input offset factory trimmed to less than 15 mV
- Rail-to-rail common mode input range (V_{SSA} to V_{CCA})
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low power
- Comparator outputs can be routed to look up tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB Digital System Interface.

Figure 8-4. Analog Comparator



8.3.2 LUT

The CY8C53 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-1.

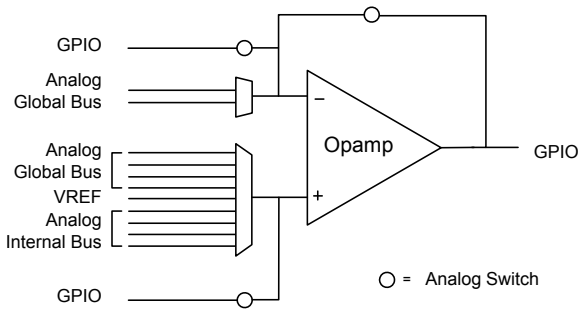
Table 8-1. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	**FALSE** (‘0’)
0001b	**A** AND **B**
0010b	**A** AND (NOT **B**)
0011b	A
0100b	(NOT **A**) AND **B**
0101b	B
0110b	**A** XOR **B**
0111b	**A** OR **B**
1000b	**A** NOR **B**
1001b	**A** XNOR **B**
1010b	NOT **B**
1011b	**A** OR (NOT **B**)
1100b	NOT **A**
1101b	(NOT **A**) OR **B**
1110b	**A** NAND **B**
1111b	**TRUE** (‘1’)

8.4 Opamps

The CY8C53 family of devices contain two general purpose opamps.

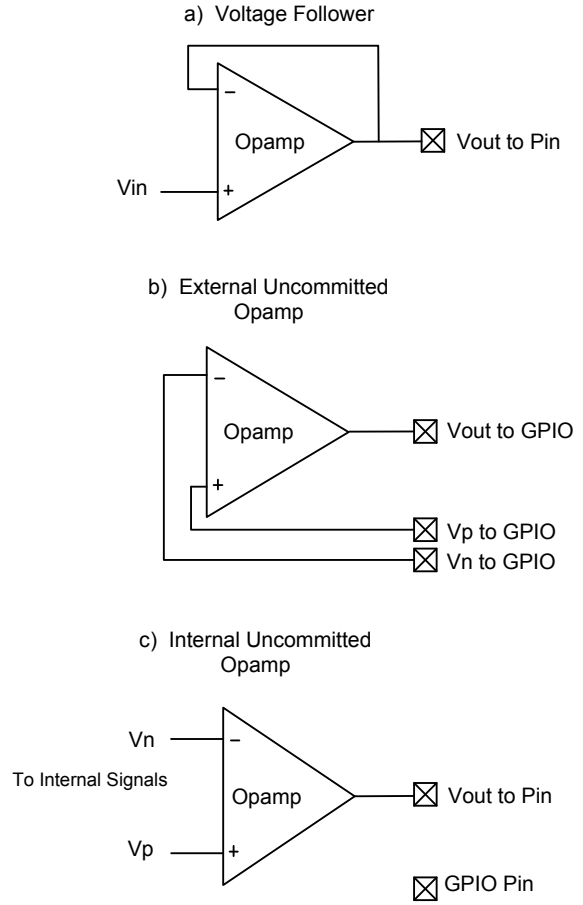
Figure 8-5. Opamp



The opamp is uncommitted and can be configured as a gain stage or voltage follower on external or internal signals.

See Figure 8-6. In any configuration, the input and output signals can all be connected to the internal global signals and monitored with an ADC, or comparator. The configurations are implemented with switches between the signals and GPIO pins.

Figure 8-6. Opamp Configurations



The opamp inputs are able to swing rail-to-rail. The output swing is capable of rail-to-rail operation at low current output, within 50 mV of the rails. When driving high current loads (about 10 mA) the output voltage may only get within 500 mV of the rails.

8.5 Programmable SC/CT Blocks

The CY8C53 family of devices contains two switched capacitor/continuous time (SC/CT) blocks in a device. Each switched capacitor/continuous time block is built around a single rail-to-rail high bandwidth opamp.

Switched capacitor is a circuit design technique that uses capacitors plus switches instead of resistors to create analog functions. These circuits work by moving charge between capacitors by opening and closing different switches. Nonoverlapping in phase clock signals control the switches, so that not all switches are ON simultaneously.

The PSoC Creator tool offers a user friendly interface, which allows you to easily program the SC/CT blocks. Switch control and clock phase control configuration is done by PSoC Creator so users only need to determine the application use parameters such as gain, amplifier polarity, V_{REF} connection, and so on.

The same opamps and block interfaces are also connectable to an array of resistors which allows the construction of a variety of continuous time functions.

The opamp and resistor array is programmable to perform various analog functions including

- Naked Operational Amplifier - Continuous Mode
- Unity-Gain Buffer - Continuous Mode
- Programmable Gain Amplifier (PGA) - Continuous Mode
- Transimpedance Amplifier (TIA) - Continuous Mode
- Up/Down Mixer - Continuous Mode
- Sample and Hold Mixer (NRZ S/H) - Switched Cap Mode
- First Order Analog to Digital Modulator - Switched Cap Mode

8.5.1 Naked Opamp

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

8.5.2 Unity Gain

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a -3 dB bandwidth greater than 6.0 MHz.

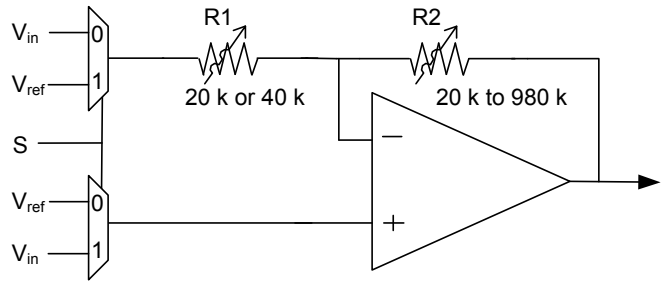
8.5.3 PGA

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-7. The schematic in Figure 8-7 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-2.

Table 8-2. Bandwidth

Gain	Bandwidth
1	6.0 MHz
24	340 kHz
48	220 kHz
50	215 kHz

Figure 8-7. PGA Resistor Settings



The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

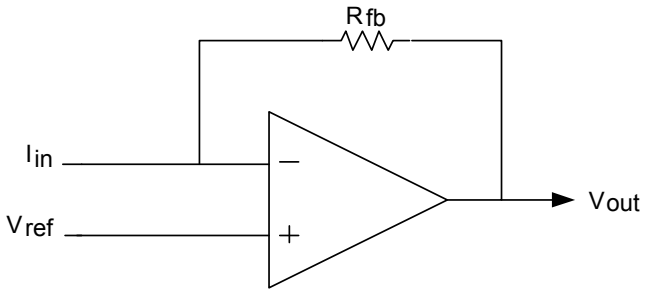
8.5.4 TIA

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current I_{in}, the output voltage is V_{REF} - I_{in} x R_{fb}, where V_{REF} is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-3 shows the possible values of Rfb and associated configuration settings.

Table 8-3. Feedback Resistor Settings

Configuration Word	Nominal R_{fb} (KΩ)
000b	20
001b	30
010b	40
011b	60
100b	120
101b	250
110b	500
111b	1000

Figure 8-8. Continuous Time TIA Schematic



The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the V_{REF} TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

8.6 LCD Direct Drive

The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C53 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

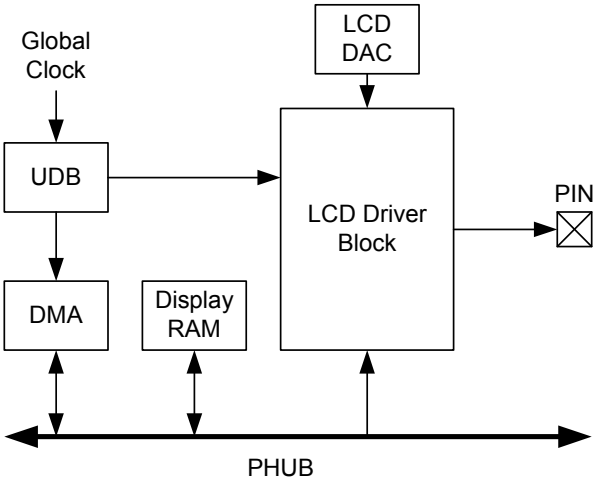
PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels

- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane x 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization
- LCD driver configurable to be active when PSoC is in limited active mode

Figure 8-9. LCD System



8.6.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.6.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

8.6.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

8.6.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-Sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.8 Temp Sensor

Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

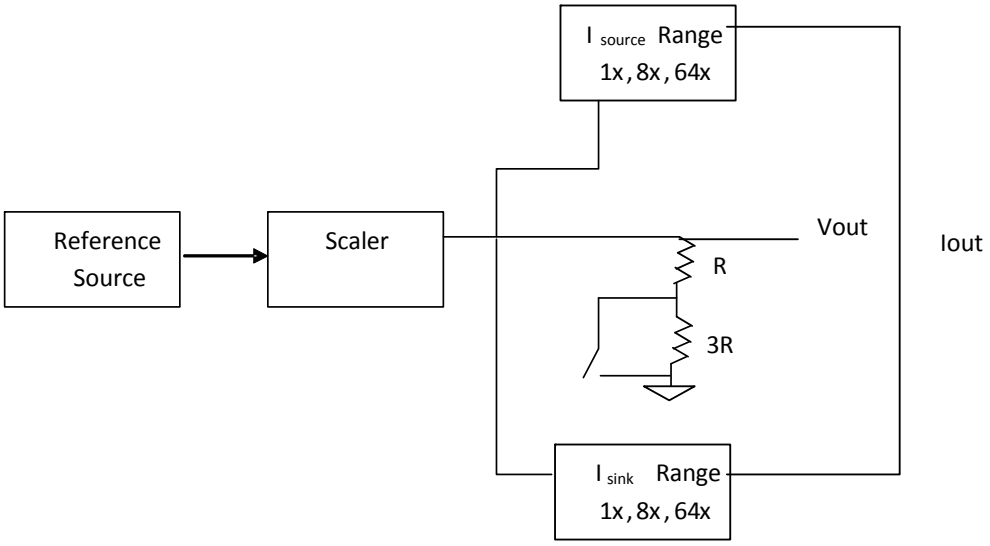
8.9 DAC

The CY8C53 parts contain two Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features.

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25% of gain error
- Source and sink option for current output
- 5.5 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Note that a write of a new value to the DAC may result in an indeterminate value on the DAC output. To output the desired value, write or strobe the DAC twice with the same value. Since the first write may result in an indeterminate output, the time between the two writes should be minimized. This applies to writes by CPU, DMA, and strobe.

Figure 8-10. DAC Block Diagram



8.9.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.9.2 Voltage DAC

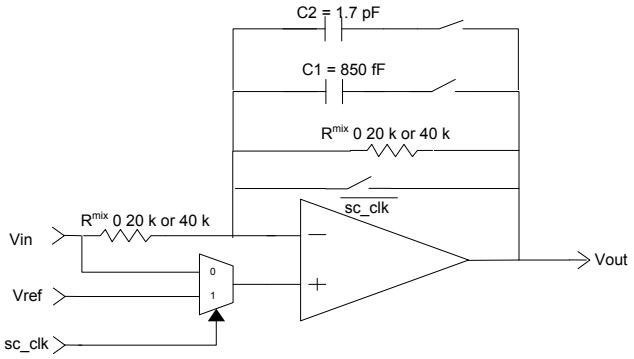
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk - Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

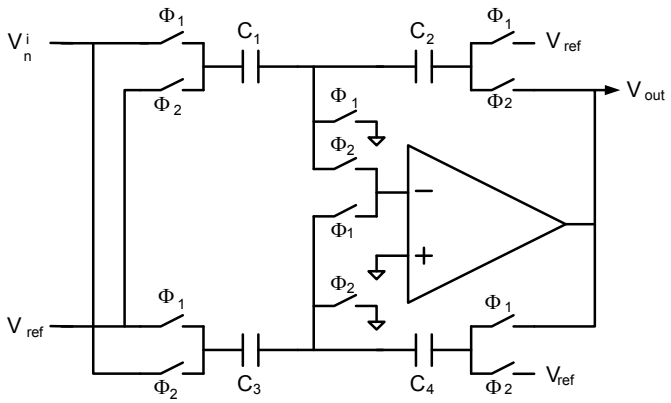
Figure 8-11. Mixer Configuration



8.11 Sample and Hold

The main application for a sample and hold, is to hold a value stable while an ADC is performing a conversion. Some applications require multiple signals to be sampled simultaneously, such as for power calculations (V and I).

Figure 8-12. Sample and Hold Topology (Φ1 and Φ2 are opposite phases of a clock)



8.11.1 Down Mixer

The S+H can be used as a mixer to down convert an input signal. This circuit is a high bandwidth passive sample network that can sample input signals up to 14 MHz. This sampled value is then held using the opamp with a maximum clock rate of 4 MHz. The output frequency is at the difference between the input frequency and the highest integer multiple of the Local Oscillator that is less than the input.

8.11.2 First Order Modulator - SC Mode

A first order modulator is constructed by placing the switched capacitor block in an integrator mode and using a comparator to provide a 1-bit feedback to the input. Depending on this bit, a reference voltage is either subtracted or added to the input signal. The block output is the output of the comparator and not the integrator in the modulator case. The signal is downshifted and buffered and then processed by a decimator to make a delta-sigma converter or a counter to make an incremental converter. The accuracy of the sampled data from the first-order modulator is determined from several factors.

The main application for this modulator is for a low frequency ADC with high accuracy. Applications include strain gauges, thermocouples, precision voltage, and current measurement

9. Programming, Debug Interfaces, Resources

The Cortex-M3 has internal debugging components, tightly integrated with the CPU, providing the following features:

- SWD access
- Flash Patch and Breakpoint (FPB) block for implementing breakpoints and code patches
- Data Watchpoint and Trigger (DWT) block for implementing watchpoints, trigger resources, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf-style debugging

PSoC devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. SWD supports all programming and debug features of the device. The SWV provides trace output from the DWT and ITM.

For more information on PSoC 5 programming, refer to the application note AN64359 - In-System Programming for PSoC® 5.

Cortex-M3 debug and trace functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE software provides fully integrated programming and debug support for PSoC devices. The low cost MiniProg3 programmer and debugger is designed to provide full programming and debug support of PSoC devices in conjunction with the PSoC Creator IDE. PSoC interfaces are fully compatible with industry standard third party tools.

All Cortex-M3 debug and trace modules are disabled by default and can only be enabled in firmware. If not enabled, the only way to reenable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables them. Disabling debug and trace features, robust flash protection, and hiding custom analog and digital functionality inside the PSoC device provide a level of security not possible with multichip application solutions. Additionally, all device interfaces can be permanently disabled (Device Security) for applications concerned about phishing attacks due to a maliciously reprogrammed device. Permanently disabling interfaces is not recommended in most applications because the designer then cannot access the device. Because all programming, debug, and test interfaces are disabled when Device Security is enabled, PSoCs with Device Security enabled may not be returned for failure analysis.

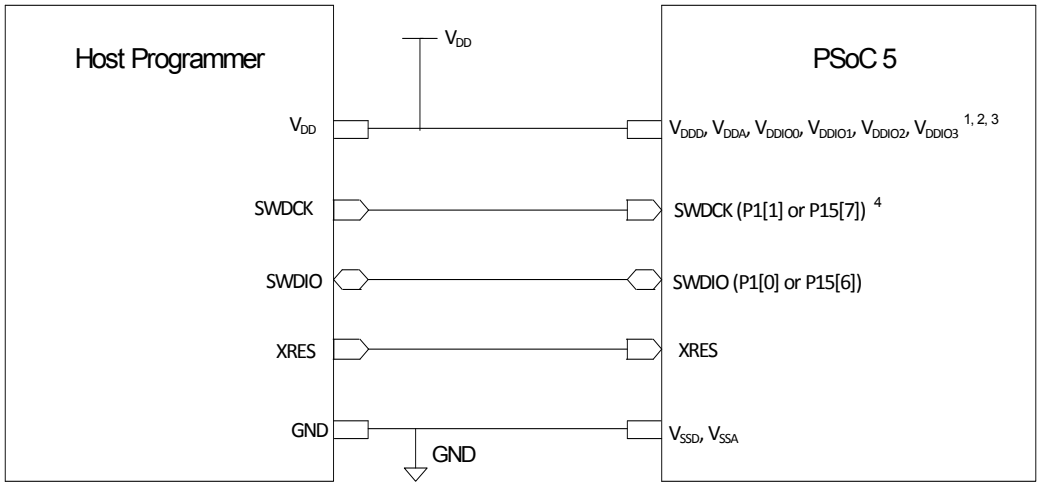
9.1 Debug Port Acquisition

Prior to programming or debugging, the debug port must be acquired. There is a time window after reset within which the Port Acquire must be completed. This window is initially 8 µs; if eight clocks are detected on the SWDCK line within the 8 µs period, the time window will then be extended to 400 µs to complete the port acquire operation. The port acquire key must be transmitted over one of the two SWD pin pairs; see SWD Interface. For a detailed description of the acquire key sequence, refer to the Technical Reference Manual

9.2 SWD Interface

SWD uses two pins, either two port 1 pins or the USBIO D+ and D- pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock (SWDCK) and the other is used for data input and output (SWDIO). SWD can be enabled on only one of the pin pairs at a time. When USB pins D+ and D- are used for SWD function, the SWDCK pin of port P1[1] is not available for use as a general purpose I/O and it should be externally pulled down using a resistor of less than 100 KΩ. SWD is used for debugging or for programming the flash memory. In addition, the SWD interface supports the SWV trace output. The SWD interface also includes the SWV interface, see SWV Interface on page 55. When using the SWD/SWV pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD/SWV use. The SWV trace output is automatically activated whenever the SWD is activated.

Figure 9-1. SWD Interface Connections between PSoC 5 and Programmer



[1] The voltage levels of the Host Programmer and the PSoC 5 voltage domains involved in programming should be the same. XRES pin is powered by V_{DDIO1}. The USB SWD pins are powered by V_{DDD}. So for programming using the USB SWD pins with XRES pin, the V_{DDD}, V_{DDIO1} of PSoC 5 should be at the same voltage level as Host V_{DD}. Rest of PSoC 5 voltage domains (V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by V_{DDIO1}. So V_{DDIO1} of PSoC 5 should be at same voltage level as host V_{DD} for Port 1 SWD programming. Rest of PSoC 5 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 5.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] When USB SWD pins are used for Programming, the P1[1] SWDCK pin must be externally connected to Ground using external pull-down resistor (around 100 K resistor). This is required for P15[7] SWDCK signal to be seen by PSoC 5's internal logic.

9.3 Debug Features

The CY8C53 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Six program address breakpoints and two literal access breakpoints
- Data watchpoint events to CPU
- Patch and remap instruction from flash to SRAM
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger

9.4 Trace Features

The following trace features are supported:

- Data watchpoint on access to data address, address range, or data value
- Software event monitoring, “printf-style” debugging

9.5 SWV Interface

The SWV interface provides trace data to a debug host via the Cypress MiniProg3 or an external trace port analyzer.

9.6 Programming Features

The SWD interface provides full programming support. The entire device can be erased, programmed, and verified. Designers can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 5 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0x50536F43) to a Write Once Latch (WOL). The WOL must be programmed at $V_{DDD} \leq 3.3$ V and $T_J = 25$ °C ±15 °C.

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a ‘1’ if a super-majority (28 of 32) of its bits match a pre-determined pattern (0x50536F43); it outputs a ‘0’ if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0x50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see “Flash Security” section on page 16). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out via Serial Wire Debug (SWD) port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 5 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

10. Development Support

The CY8C53 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit psoc.cypress.com/getting-started to find out more.

10.1 Documentation

A suite of documentation, to ensure that you can find answers to your questions quickly, supports the CY8C53 family. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component data sheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: PSoC Creator makes designing with PSoC as easy as dragging a peripheral onto a schematic, but, when low level details of the PSoC device are required, use the technical reference manual (TRM) as your guide.

Note Visit www.arm.com for detailed documentation about the Cortex-M3 CPU.

10.2 Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

10.3 Tools

With industry standard cores, programming, and debugging interfaces, the CY8C53 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

11. Electrical Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component data sheets for full AC/DC specifications of individual functions. See the "Example Peripherals" section on page 32 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_J	Operating die temperature		–55	–	110	°C
T_{STG}	Storage temperature	Recommended storage temperature is +25 °C ±25 °C. Extended duration storage temperatures above 85 °C degrade reliability.	–55	25	100	°C
V_{DDA}	Analog supply voltage relative to V_{SSA}		–0.5	–	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{CCA}	Direct analog core voltage input		–0.5	–	1.95	V
V_{CCD}	Direct digital core voltage input		–0.5	–	1.95	V
V_{SSA}	Analog ground voltage		V_{SSD} – 0.5	–	V_{SSD} + 0.5	V
V_{GPIO}[13]	DC input voltage on GPIO	Includes signals sourced by V_{DDA} and routed internal to the pin.	V_{SSD} – 0.5	–	V_{DDIO} + 0.5	V
V_{SIO}	DC input voltage on SIO	Output disabled	V_{SSD} – 0.5	–	7	V
		Output enabled	V_{SSD} – 0.5	–	6	V
I_{VDDIO}	Current per V_{DDIO} supply pin	Source	–	–	20	mA
		Sink	–	–	100	
LU	Latch up current[14]		–100	–	100	mA
ESD_{HBM}	Electrostatic discharge voltage	Human body model	500	–	–	V
ESD_{CDM}	ESD voltage	Charge device model	500	–	–	V

Note Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to maximum conditions for extended periods of time may affect device reliability. When used below maximum conditions but above normal operating conditions the device may not operate to specification.

Notes
13. The V_{DDIO} supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
14. Meets or exceeds JEDEC Spec EIA/JESD78 IC latch up test, at up to 85 °C.

11.2 Device Level Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions				Min	Typ	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled				2.7	–	5.5	V
V_{DDD}	Digital supply voltage relative to V_{SSD}	Digital core regulator enabled				2.7	–	V_{DDA}[15]	V
V_{DDIO}[16]	I/O supply voltage relative to V_{SSIO}					2.7	–	V_{DDA}[15]	V
		Device Configuration	**V_{DDX}**	**F_{CPU}**	**Temp**				
I_{DD}[17]	Active Mode	Only IMO and CPU clock enabled. CPU executing simple loop from cache	2.7 V to 5.5 V	6 MHz	–40 °C	–	2.2	3	mA
					25 °C	–	2.4	3.5	
					85 °C	–	2.8	3.5	
		IMO enabled, bus clock and CPU clock enabled. CPU executing complex program from flash	2.7 V to 5.5 V	3 MHz	–40 °C	–	3.4	4	
					25 °C	–	3.6	4.5	
					85 °C	–	4.2	5	
				6 MHz	–40 °C	–	5.6	6	
					25 °C	–	6	7	
					85 °C	–	6.6	7.5	
				12 MHz	–40 °C	–	10	11	
					25 °C	–	11	12	
					85 °C	–	12	13	
				24 MHz	–40 °C	–	17	19	
					25 °C	–	18	20	
					85 °C	–	20	22	
				48 MHz	–40 °C	–	31	34	
					25 °C	–	33	35	
					85 °C	–	36	39	
				63 MHz	–40 °C	–	36	39	
					25 °C	–	37	40	
					85 °C	–	40	44	

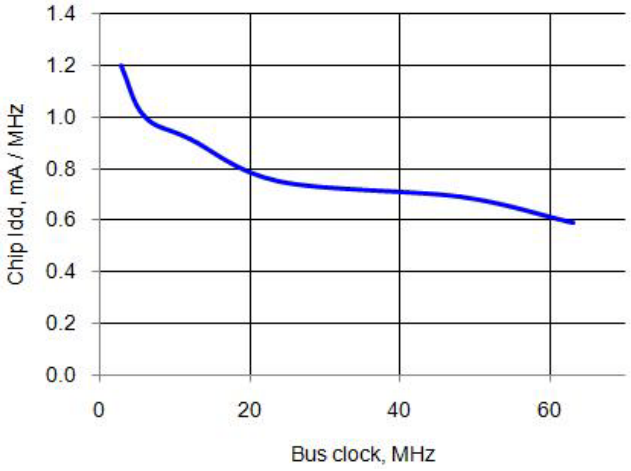
Notes

15. V_{DDD} and V_{DDA} must be brought up in synchronization with each other, that is, at the same rates and levels. V_{DDA} must be greater than or equal to all other supplies.
16. The V_{DDIO} supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
17. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective data sheets, available in PSoC Creator, the integrated design environment. To estimate total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device data sheet and component data sheets..

Table 11-2. DC Specifications (continued)

Parameter	Description	Conditions			Min	Typ	Max	Units
		Device Configuration	$V_{DD} = V_{DDIO}$	Temp				
	Sleep Mode[18]	CPU = OFF SleepTimer=ON POR = ON	4.5 V to 5.5 V	–40 °C	–	1.4	–	µA
				25 °C	–	1.2	–	
				85 °C	–	11	–	
			2.7 V to 3.6 V	–40 °C	–	1.2	–	
				25 °C	–	2	–	
				85 °C	–	10	–	
	Hibernate Mode	All oscillators and regulators off, except hibernate regulator. SRAM retention	4.5 V to 5.5 V	–40 °C	–	0.3	–	µA
				25 °C	–	0.6	–	
				85 °C	–	10	–	
			2.7 V to 3.6 V	–40 °C	–	0.2	–	
				25 °C	–	0.3	–	
				85 °C	–	8	–	
I_{DDAR}	Analog current consumption while device is reset[20]	$V_{DDA} \le 3.6$ V			–	0.3	–	mA
		$V_{DDA} > 3.6$ V			–	1.4	–	mA
I_{DDDR}	Digital current consumption while device is reset[20]	$V_{DDD} \le 3.6$ V			–	1.1	–	mA
		$V_{DDD} > 3.6$ V			–	0.7	–	mA

Figure 11-1. Active Mode Device I_{DD}, mA/MHz



Notes
18. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.
19. Based on device characterization (Not production tested).
20. Based on device characterization (not production tested). USBIO pins tied to ground (VSSD).

Table 11-3. AC Specifications[19]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU frequency		DC	–	67.01	MHz
F_{BUSCLK}	Bus frequency		DC	–	67.01	MHz
Svdd	V_{DD} ramp rate		–	–	0.066	V/µs
$T_{STARTUP}$	Time from $V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA}$ ≥ min operating voltage to CPU executing code at reset vector	No PLL used, IMO boot mode 12 MHz typ.	–	45	80	µs
T_{SLEEP}	Wakeup from sleep – CTW timeout to beginning of execution of next CPU instruction		–	125	–	µs
T_{SLEEP_INT}	Sleep timer periodic wakeup interval		–	–	128	ms

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		2.7	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor[21]	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 22	–	1	10	µF

Figure 11-2. Regulators V_{CC} vs V_{DD}

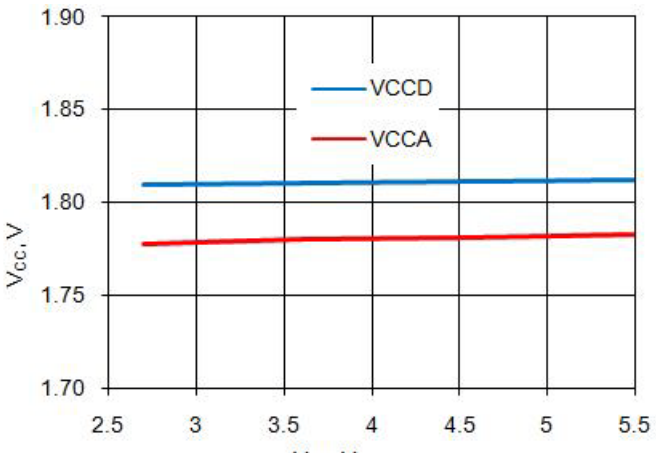
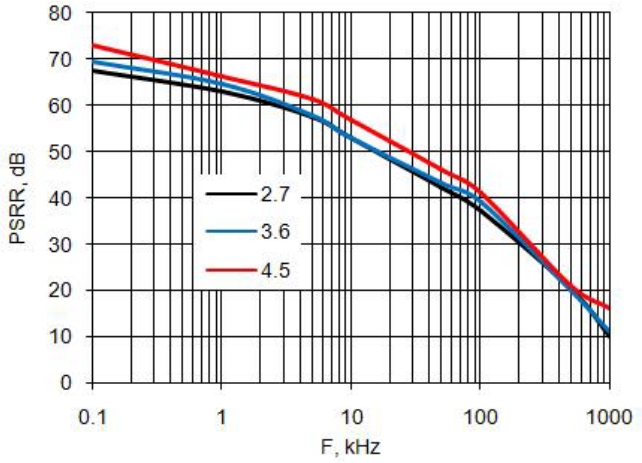


Figure 11-3. Digital Regulator PSRR vs Frequency and V_{DD}



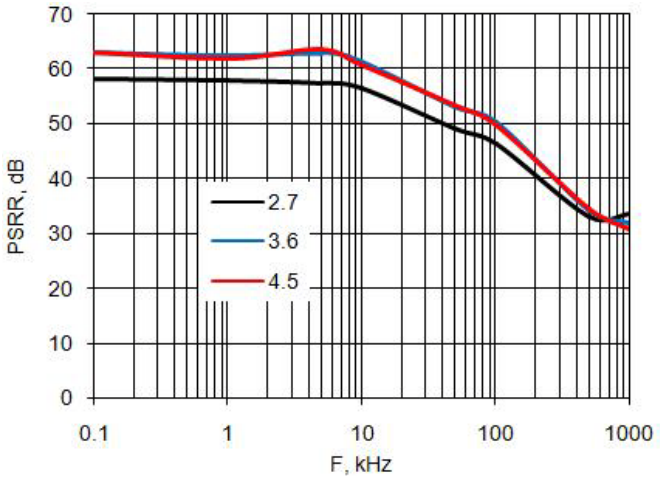
Note
21. 10 µF is required for sleep mode. See Table 11-3.

11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		2.7	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor[24]	±10%, X5R ceramic or better	–	1	10	µF

Figure 11-4. Analog Regulator PSRR vs Frequency and V_{DD}



11.4 Inputs and Outputs

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.4.1 GPIO

Table 11-6. GPIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold	CMOS Input, PRT[x]CTL = 0	0.7 × V_{DDIO}	–	–	V
V_{IL}	Input voltage low threshold	CMOS Input, PRT[x]CTL = 0	–	–	0.3 × V_{DDIO}	V
V_{IH}	Input voltage high threshold	LVTTL Input, PRT[x]CTL = 1	2.0	–	–	V
V_{IL}	Input voltage low threshold	LVTTL Input, PRT[x]CTL = 1	–	–	0.8	V
V_{OH}	Output voltage high	I_{OH} = 4 mA at 3.3 V_{DDIO}	V_{DDIO} – 0.6	–	–	V
V_{OL}	Output voltage low	I_{OL} = 8 mA at 3.3 V_{DDIO}	–	–	0.6	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I_{IL}	Input leakage current (absolute value)[22]	25 °C, V_{DDIO} = 3.0 V	–	–	2	nA

Notes
22. Based on device characterization (Not production tested).
23. For information on designing with PSoC 3 oscillators, refer to the application note, AN54439 - PSoC® 3 and PSoC 5 External Oscillator.
24. 10 µF is required for sleep mode. See Table 11-3.

Table 11-6. GPIO DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
C_{IN}	Input capacitance[22]	GPIOs not shared with opamp outputs or kHzECO or SAR ADC external reference input	–	4	7	pF
		GPIOs shared with kHzECO[23]	–	5	7	pF
		GPIOs shared with opamp outputs	–	–	18	pF
		GPIO shared with SAR ADC external reference input	–	–	30	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[22]		–	150	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA
Rglobal	Resistance pin to analog global bus	25 °C, V_{DDIO} = 3.0 V	–	320	–	Ω
Rmux	Resistance pin to analog mux bus	25 °C, V_{DDIO} = 3.0 V	–	220	–	Ω

Figure 11-5. GPIO Output High Voltage and Current

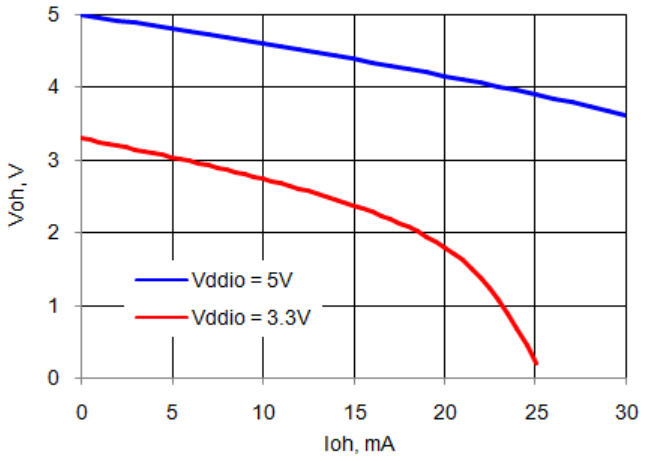


Figure 11-6. GPIO Output Low Voltage and Current

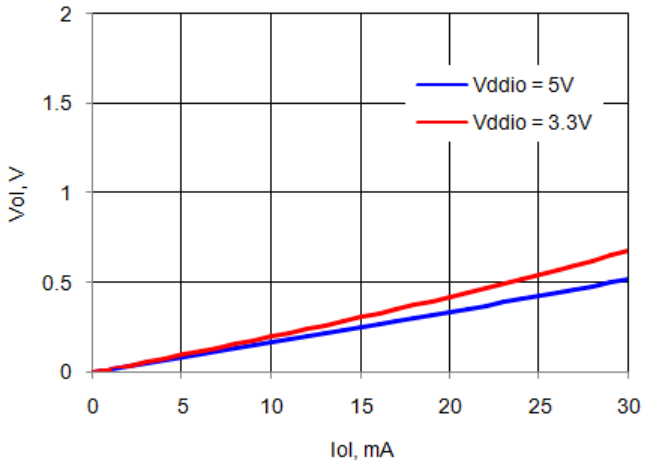


Table 11-7. GPIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode[25]	3.3 V V_{DDIO} Cload = 25 pF	–	–	12	ns
TfallF	Fall time in Fast Strong Mode[25]	3.3 V V_{DDIO} Cload = 25 pF	–	–	12	ns
TriseS	Rise time in Slow Strong Mode[25]	3.3 V V_{DDIO} Cload = 25 pF	–	–	60	ns
TfallS	Fall time in Slow Strong Mode[25]	3.3 V V_{DDIO} Cload = 25 pF	–	–	60	ns
Fgpioout	GPIO output operating frequency					
	Fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	3.3 V ≤ V_{DDIO} ≤ 5.5 V, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	7	MHz
	2.7 V ≤ V_{DDIO} < 3.3 V, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	3.5	MHz
Fgpioin	GPIO input operating frequency					
	2.7 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	66	MHz

Note
25. Based on device characterization (Not production tested).

Figure 11-7. GPIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

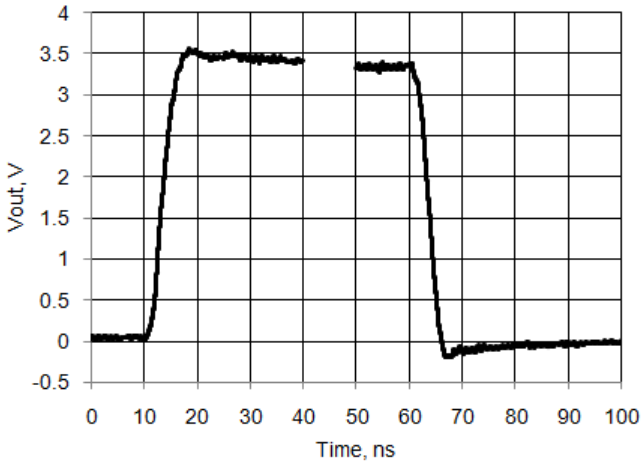
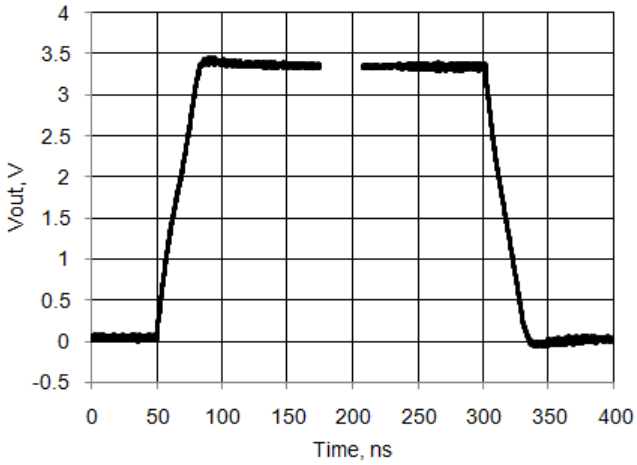


Figure 11-8. GPIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



11.4.2 SIO

Note that under certain conditions an SIO pin may cause up to 1 mA of additional current to be drawn from the related V_{DDIO} pin. If an SIO pin's voltage exceeds its V_{DDIO} supply by 0.5 V, the trigger condition is set. After the trigger condition is set, the SIO pin causes increased current when its voltage is between V_{SSD} + 0.5 V and V_{DDIO} – 0.5 V. The trigger condition is reset when the SIO pin is brought within the range of V_{SSD} to V_{SSD} + 0.5 V. The trigger condition may unknowningly be met during device powerup due to differences in supply ramps.

Table 11-8. SIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vinmax	Maximum input voltage	All allowed values of Vddio and Vddd, see *Section 11.2.1*	–	–	5.5	V
Vinref	Input voltage reference (Differential input mode)		0.5	–	0.52 × V_{DDIO}	V
Voutref	Output voltage reference (Regulated output mode)					
		V_{DDIO} > 3.7	1	–	V_{DDIO} – 1	V
		V_{DDIO} < 3.7	1	–	V_{DDIO} – 0.5	V
V_{IH}	Input voltage high threshold					
	GPIO mode	CMOS input	0.7 × V_{DDIO}	–	–	V
	Differential input mode[26]	Hysteresis disabled	SIO_ref + 0.2	–	–	V
V_{IL}	Input voltage low threshold					
	GPIO mode	CMOS input	–	–	0.3 × V_{DDIO}	V
	Differential input mode[26]	Hysteresis disabled	–	–	SIO_ref – 0.2	V
V_{OH}	Output voltage high					
	Unregulated mode	I_{OH} = 4 mA, V_{DDIO} = 3.3 V	V_{DDIO} – 0.4	–	–	V
	Regulated mode[26]	I_{OH} = 1 mA	SIO_ref – 0.65	–	Voutref + 0.2	V
	Regulated mode[26]	I_{OH} = 0.1 mA	SIO_ref – 0.3	–	SIO_ref + 0.2	V
V_{OL}	Output voltage low	V_{DDIO} = 3.30 V, I_{OL} = 25 mA	–	–	0.8	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I_{IL}	Input leakage current (absolute value)[27]					
	V_{IH} ≤ Vddsio	25 °C, Vddsio = 3.0 V, V_{IH} = 3.0 V	–	–	14	nA
	V_{IH} > Vddsio	25 °C, Vddsio = 0 V, V_{IH} = 3.0 V	–	–	10	µA

Notes
26. See Figure 6-8 on page 28 and Figure 6-11 on page 31 for more information on SIO reference.
27. Based on device characterization (Not production tested).

Table 11-8. SIO DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance[27]		–	–	7	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[27]	Single ended mode (GPIO mode)	–	150	–	mV
		Differential mode	–	35	–	mV
Idiode	Current through protection diode to V_{SSIO}		–	–	100	µA

Figure 11-9. SIO Output High Voltage and Current, Unregulated Mode

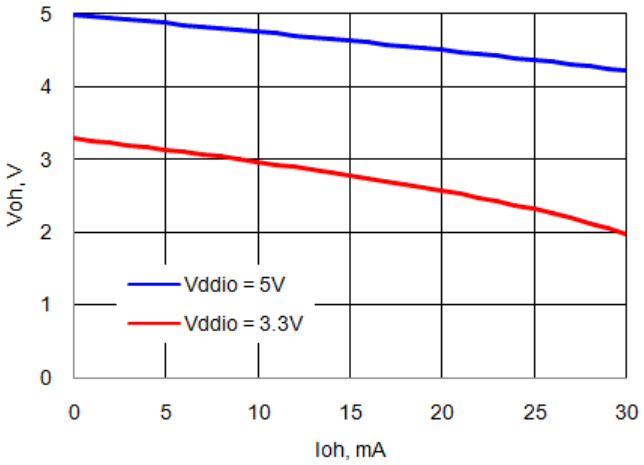


Figure 11-10. SIO Output High Voltage and Current, Regulated Mode

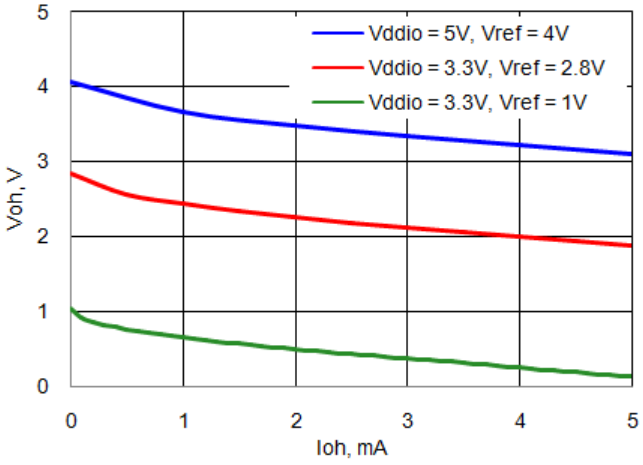
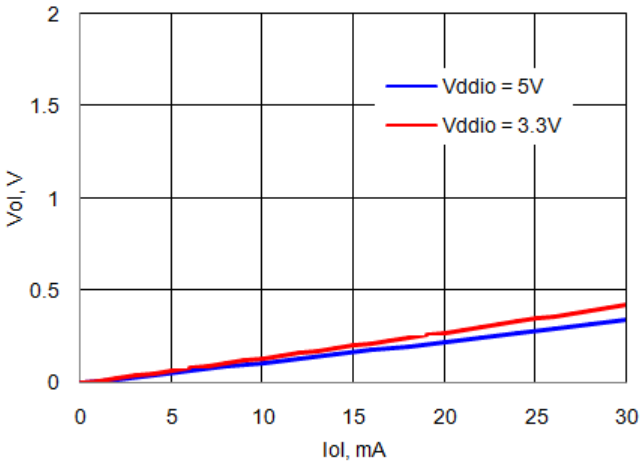


Figure 11-11. SIO Output Low Voltage and Current, Unregulated Mode



Note
28. Based on device characterization (Not production tested).

Table 11-9. SIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%)[28]	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%)[28]	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%)[28]	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	75	ns
TfallS	Fall time in Slow Strong Mode (90/10%)[28]	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	60	ns
Fsioout	SIO output operating frequency					
	Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	2.7 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency	90/10% V_{DDIO}	–	–	66	MHz

Figure 11-12. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

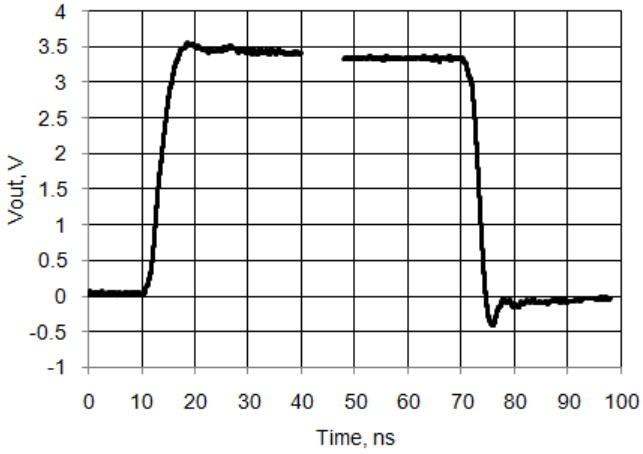
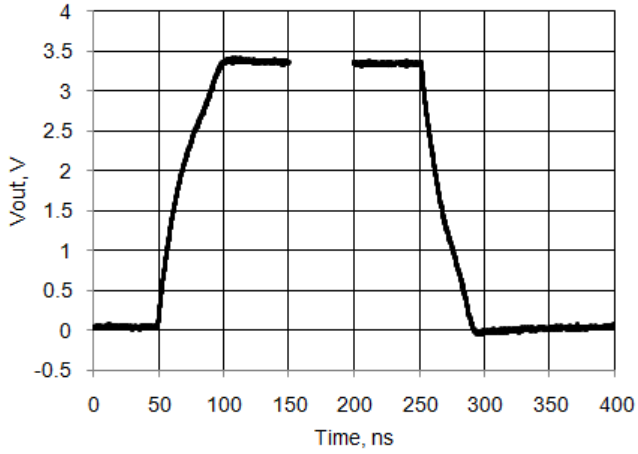


Figure 11-13. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



11.4.3 USBIO

For operation in GPIO mode, the standard range for V_{DDD} applies, see Device Level Specifications on page 58.

Table 11-10. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to Vss, internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low	15 kΩ ±5% to Vss, internal pull-up enabled	–	–	0.3	V
Vihgpio	Input voltage high, GPIO mode	$V_{DDD} \geq 3$ V	2	–	–	V
Vilgpio	Input voltage low, GPIO mode	$V_{DDD} \geq 3$ V	–	–	0.8	V
Vohgpio	Output voltage high, GPIO mode	I_{OH} = 4 mA, $V_{DDD} \geq 3$ V	2.4	–	–	V
Volgpio	Output voltage low, GPIO mode	I_{OL} = 4 mA, $V_{DDD} \geq 3$ V	–	–	0.3	V
Vdi	Differential input sensitivity	|(D+)–(D–)|	–	–	0.2	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single ended receiver threshold		0.8	–	2	V
Rps2	PS/2 pull-up resistance	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance[29]	Including Rext	28	–	44	Ω
C_{IN}	USB transceiver input capacitance		–	–	20	pF
I_{IL}[30]	Input leakage current (absolute value)	25 °C, V_{DDD} = 3.0 V	–	–	2	nA

Figure 11-14. USBIO Output High Voltage and Current, GPIO Mode

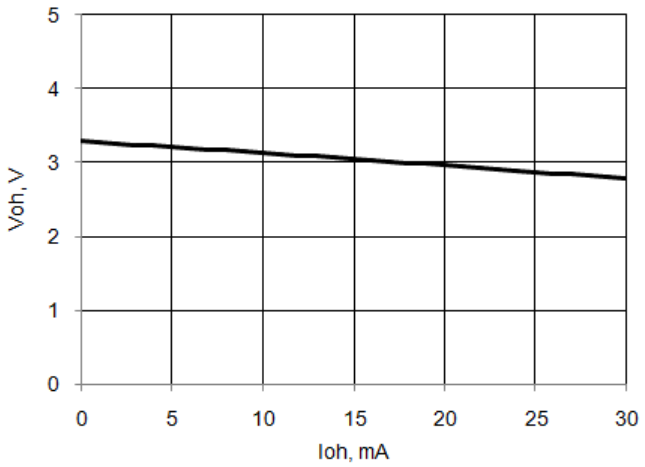
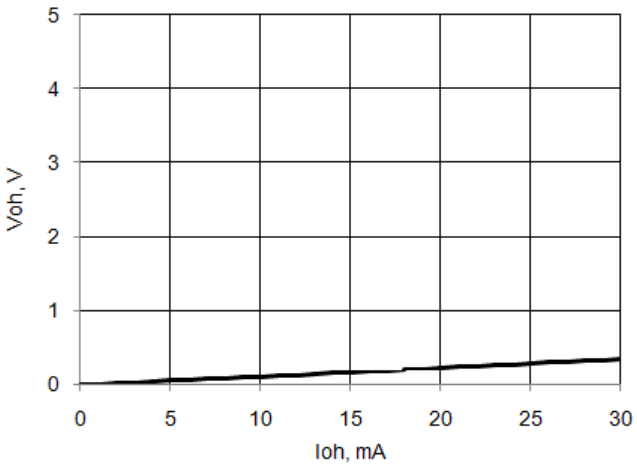


Figure 11-15. USBIO Output Low Voltage and Current, GPIO Mode



Note
29. This parameter is not production tested and cannot be guaranteed over all temperatures.
30. Based on device characterization (Not production tested).

Table 11-11. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate	Using external 24 MHz crystal	12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	3 V ≤ V_{DDD} ≤ 5.5 V	–	–	20	MHz
		V_{DDD} = 2.7 V	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 2.7 V, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 2.7 V, 25 pF load	–	–	40	ns

Figure 11-16. USBIO Output Rise and Fall Times, GPIO Mode, V_{DDD} = 3.3 V, 25 pF Load

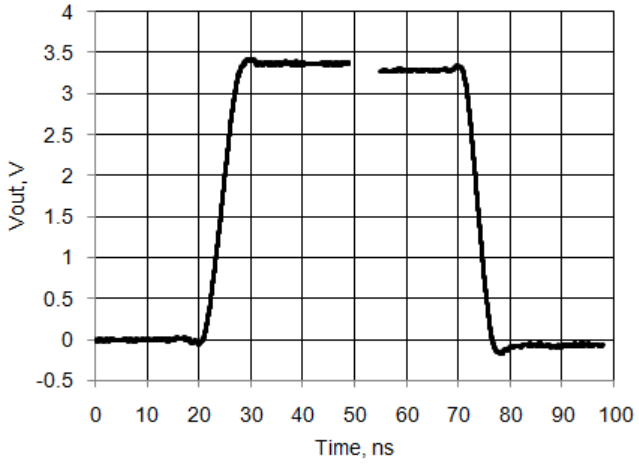


Table 11-12. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5}, $V_{USB_3.3}$, see USB DC Specifications on page 87	80%	–	135%	
Vcrs	Output signal crossover voltage		1.1	–	2.3	V

11.4.4 XRES

Table 11-13. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold		$0.7 \times V_{DDIO}$	–	–	V
V_{IL}	Input voltage low threshold		–	–	$0.3 \times V_{DDIO}$	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
C_{IN}	Input capacitance[31]		–	3	–	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[31]		–	100	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA

Table 11-14. XRES AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESET}	Reset pulse width		1	–	–	µs

11.5 Analog Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.5.1 Opamp

Table 11-15. Opamp DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_I	Input voltage range		V_{SSA}	–	V_{DDA}	V
V_{OS}	Input offset voltage	Operating temperature > 70 °C	–	–	3	mV
		Operating temperature –40 °C to 70 °C	–	–	2	mV
TCV_{OS}	Input offset voltage drift with temperature		–	–	±30	µV / °C
Ge1	Gain error, unity gain buffer mode	Rload = 1 kΩ	–	–	±0.1	%
C_{IN}	Input capacitance	Routing from pin	–	–	18	pF
Vo	Output voltage range	1 mA, source or sink	V_{SSA} + 0.05	–	V_{DDA} – 0.05	V
I_{OUT}	Output current, source or sink	V_{SSA} + 500 mV ≤ Vout ≤ V_{DDA} –500 mV	10	–	–	mA
I_{DD}	Quiescent current	Vssa + 50 mV < V_{IN} < V_{DDA}-50 mV	–	1	2.5	mA
CMRR	Common mode rejection ratio		80	–	–	dB
PSRR	Power supply rejection ratio		75	–	–	dB

Note
31. Based on device characterization (Not production tested).

Figure 11-17. Opamp Voffset vs Temperature, V_{DDA} = 5 V

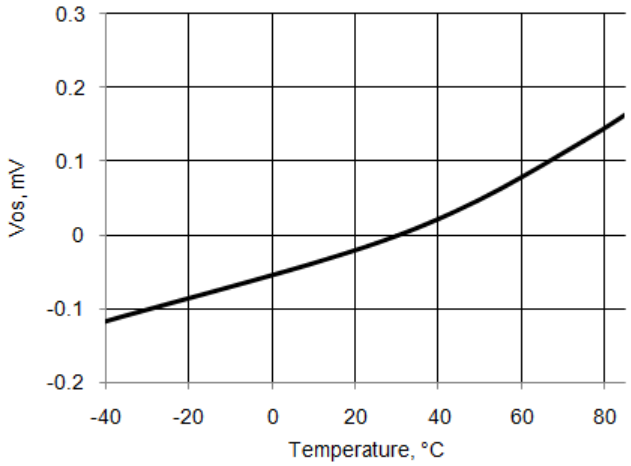


Figure 11-18. Opamp Output Voltage vs Load Current, 25 °C, V_{DDA} = 2.7 V

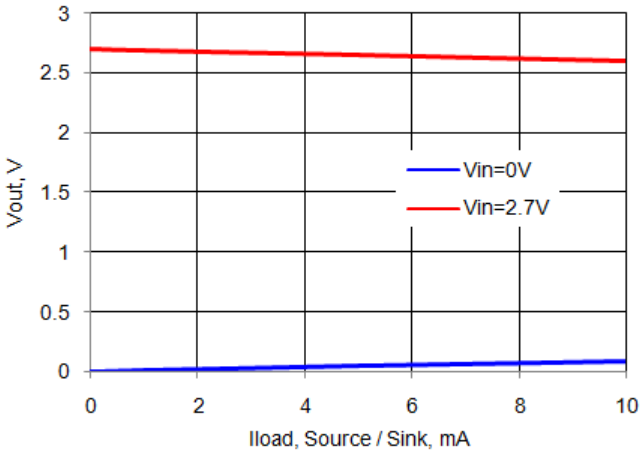


Figure 11-19. Opamp Voffset vs Vcommon and V_{DDA}, 25 °C

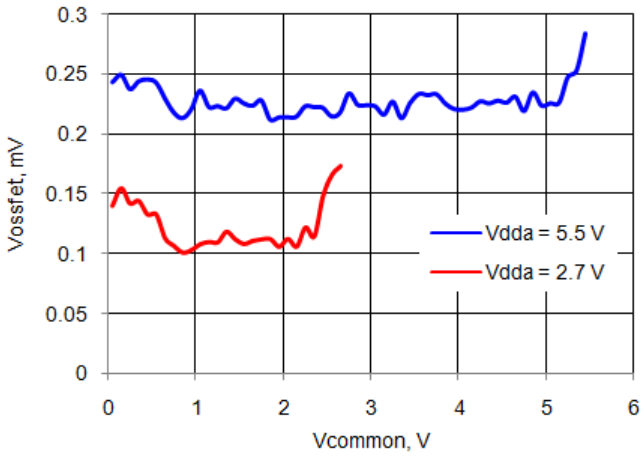


Figure 11-20. Opamp Operating Current vs V_{DDA}

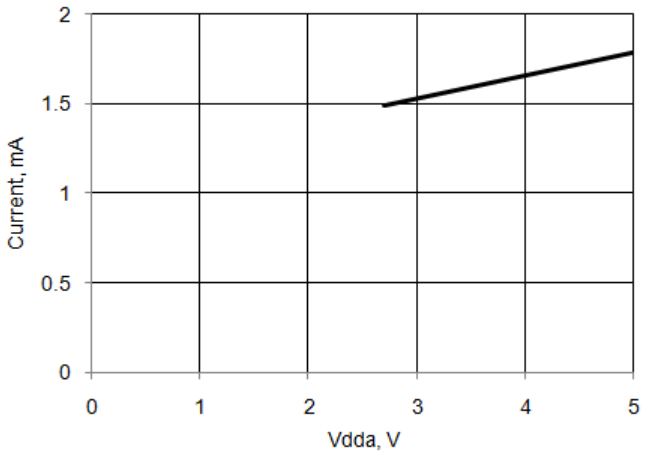


Table 11-16. Opamp AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
GBW	Gain-bandwidth product	200 pF load	3	–	–	MHz
SR	Slew rate, 20% - 80%	200 pF load	3	–	–	V/µs
e_n	Input noise density	Vdda = 5 V, at 100 kHz	–	45	–	nV/sqrtHz

Figure 11-21. Opamp Step Response, Rising

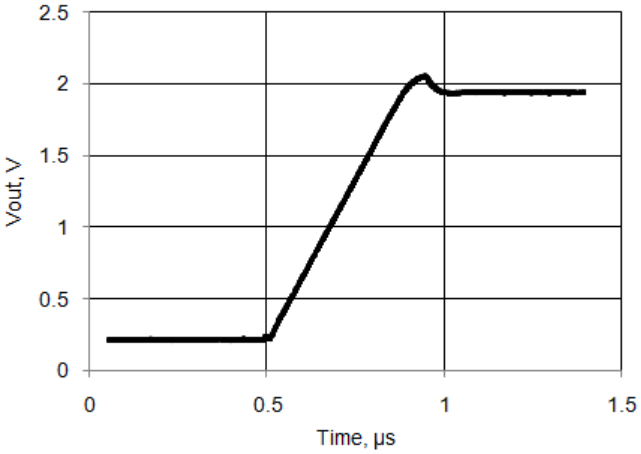


Figure 11-23. Opamp Step Response, Falling

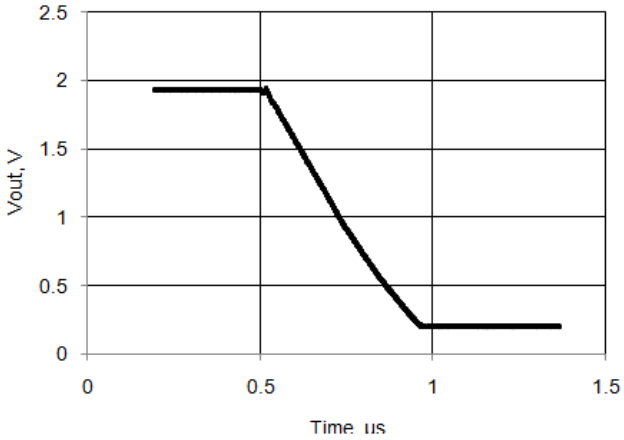
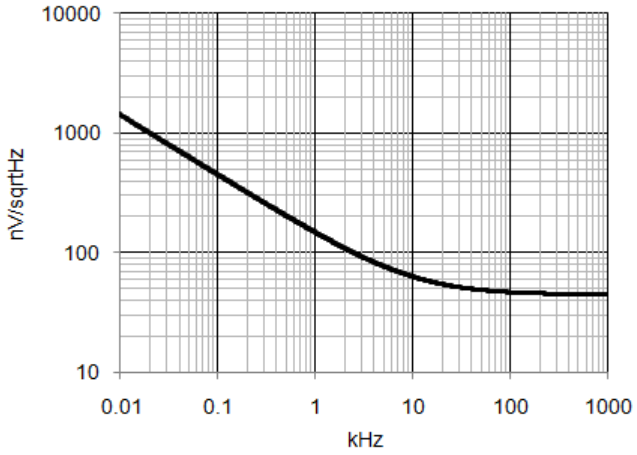


Figure 11-22. Opamp Noise vs Frequency, V_{DDA} = 5V



11.5.2 Voltage Reference

Table 11-17. Voltage Reference Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{REF}	Precision reference voltage	Initial trimming	1.017 (–0.7%)	1.024	1.033 (+0.9%)	V
	Temperature drift[32]		–	–	57	ppm/°C
	Long term drift		–	100	–	ppm/Khr
	Thermal cycling drift (stability)[32]		–	100	–	ppm

Note
32. Based on device characterization (Not production tested).

11.5.3 SAR ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- Fclk = 14 MHz
- Input range = ± V_{REF}
- Bypass capacitor of 10 µF

Table 11-18. SAR ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	12	bits
	Number of channels – single-ended		–	–	No of GPIO	
	Number of channels – differential	Differential pair is formed using a pair of neighboring GPIO.	–	–	No of GPIO/2	
	Monotonicity[33]		Yes	–	–	
Ge	Gain error	External reference	–	–	±0.2	%
V_{OS}	Input offset voltage	V_{CM} = 0 V	–	–	±2	mV
		V_{CM} = $V_{DD/2}$			±6	
I_{DD}	Current consumption		–	–	1	mA
	Input voltage range – single-ended[33]		V_{SSA}	–	V_{DDA}	V
	Input voltage range – differential[33]		V_{SSA}	–	V_{DDA}	V
PSRR	Power supply rejection ratio[33]		70	–	–	dB
CMRR	Common mode rejection ratio		35	–	–	dB
INL	Integral non linearity[33]	Internal reference from V_{BG}	–	–	±2	LSB
DNL	Differential non linearity[33]	Internal reference from V_{BG}	–	–	±2	LSB

Figure 11-24. SAR ADC DNL vs Output Code, Bypassed Internal Reference Mode

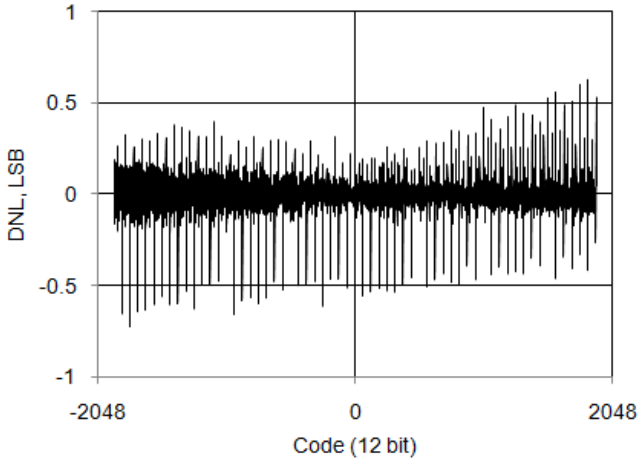


Figure 11-25. SAR ADC INL vs Output Code, Bypassed Internal Reference Mode

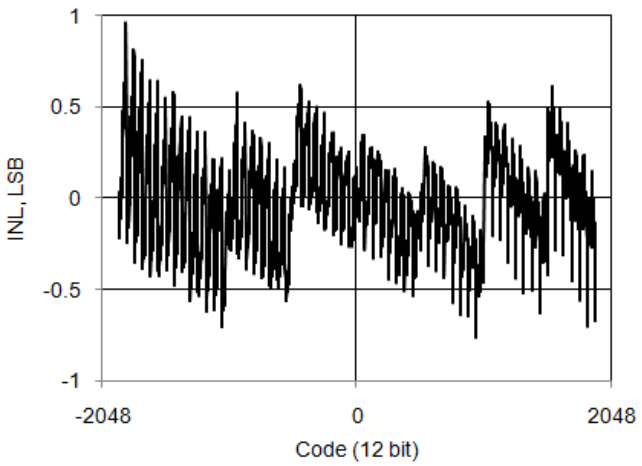


Figure 11-26. SAR ADC I_{DD} vs sps, V_{DDA} = 5 V, Continuous Sample Mode, External Reference Mode

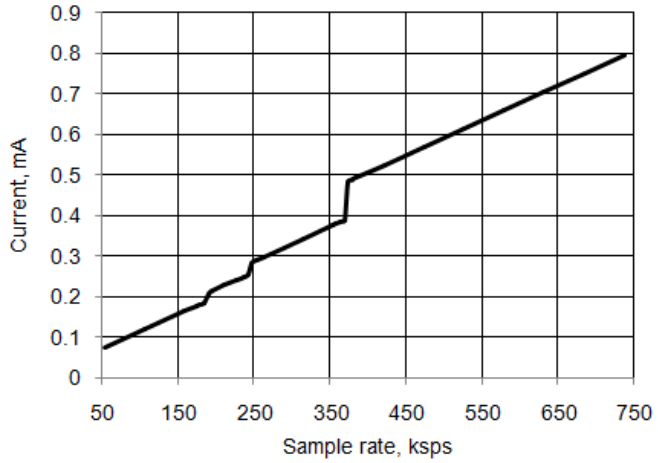


Table 11-19. SAR ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Sample rate[33]	With bypass capacitor	–	–	700	ksps
		Without bypass capacitor	–	–	100	
	Startup time[33]		–	–	10	µs
SINAD	Signal-to-noise ratio[33]	$V_{DDA} \le 3.6$ V, $V_{REF} \le 3.6$ V	57	–	–	dB
		3.6 V < $V_{DDA} \le 5.5$ V V_{REF} < 1.3 V or V_{REF} > 1.8 V	57	–	–	
THD	Total harmonic distortion[33]	$V_{DDA} \le 3.6$ V, $V_{REF} \le 3.6$ V	–	–	0.1	%
		3.6 V < $V_{DDA} \le 5.5$ V V_{REF} < 1.3 V or V_{REF} > 1.8 V	–	–	0.1	

Figure 11-27. SAR ADC Noise Histogram, 1000 samples, 700 ksps, Internal Reference No Bypass, V_{IN} = VREF/2

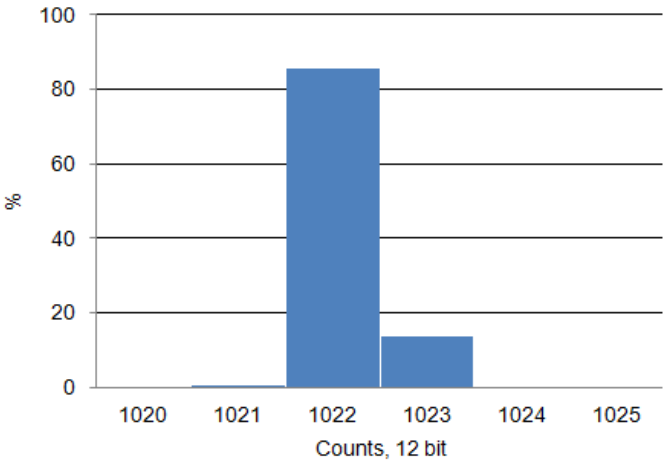
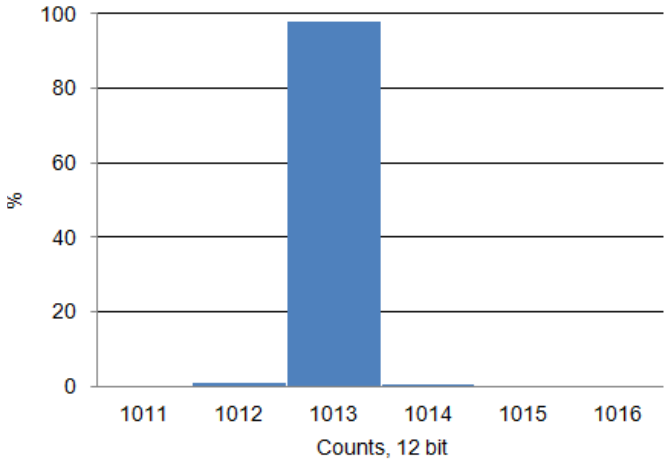
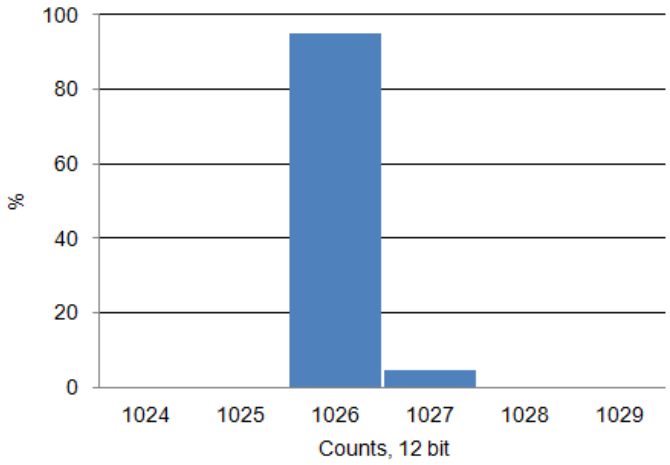


Figure 11-28. SAR ADC Noise Histogram, 1000 samples, 700 ksps, Internal Reference Bypassed, V_{IN} = VREF/2



Note
33. Based on device characterization (Not production tested).

Figure 11-29. SAR ADC Noise Histogram, 1000 samples, 700 ksps, External Reference, V_{IN} = VREF/2



11.5.4 Analog Globals

Table 11-20. Analog Globals DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through analog global	V_{DDA} = 3.0 V	–	1200	1500	Ω
Rppmuxbus	Resistance pin-to-pin through analog mux bus	V_{DDA} = 3.0 V	–	700	1000	Ω

11.5.5 Comparator

Table 11-21. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, Vin ≥ 0.5 V	–		15	mV
	Input offset voltage in slow mode	Factory trim, Vin ≥ 0.5 V	–		15	mV
V_{OS}	Input offset voltage in ultra low power mode		–	±12	–	mV
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA} – 0.1	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low power mode	V_{SSA}	–	V_{DDA} – 0.9	
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode[34]		–	–	400	µA
	Low current mode/slow mode[34]		–	–	100	µA
	Ultra low power mode[34]		–	6	–	µA

Table 11-22. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESP}	Response time, high current mode[34]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode[34]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low power mode[34]	50 mV overdrive, measured pin-to-pin	–	55	–	µs

11.5.6 Current Digital-to-analog Converter (IDAC)

All specifications are based on use of the low-resistance IDAC output pins (see Pin Descriptions on page 9 for details). See the IDAC component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-23. IDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	8	bits
I_{OUT}	Output current at code = 255	Range = 2.04 mA, code = 255, Rload = 600 Ω	–	2.04	–	mA
		Range = 255 µA, code = 255, Rload = 600 Ω	–	255	–	µA
		Range = 31.875 µA, code = 255, Rload = 600 Ω	–	31.875	–	µA
	Monotonicity		–	–	Yes	
Ezs	Zero scale error		–	0	±2.5	LSB
Eg	Gain error		–	–	±5	%
TC_Eg	Temperature coefficient of gain error	Range = 2.04 mA	–	–	0.04	% / °C
		Range = 255 µA	–	–	0.04	% / °C
		Range = 31.875 µA	–	–	0.05	% / °C
INL	Integral nonlinearity	Range = 255 µA, Codes 8 – 255, Rload = 600 Ω, Cload = 15 pF	–	–	±3	LSB
DNL	Differential nonlinearity, non-monotonic	Range = 255 µA, Rload = 600 Ω, Cload = 15 pF	–	–	±1.6	LSB
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to Vdda or Rload to Vssa, Vdiff from Vdda	1	–	–	V

Note
34. Based on device characterization (Not production tested).

Table 11-23. IDAC DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Slow mode, source mode, range = 31.875 µA	–	44	100	µA
		Slow mode, source mode, range = 255 µA,	–	33	100	µA
		Slow mode, source mode, range = 2.04 mA	–	33	100	µA
		Slow mode, sink mode, range = 31.875 µA	–	36	100	µA
		Slow mode, sink mode, range = 255 µA	–	33	100	µA
		Slow mode, sink mode, range = 2.04 mA	–	33	100	µA
		Fast mode, source mode, range = 31.875 µA	–	310	500	µA
		Fast mode, source mode, range = 255 µA	–	305	500	µA
		Fast mode, source mode, range = 2.04 mA	–	305	500	µA
		Fast mode, sink mode, range = 31.875 µA	–	310	500	µA
		Fast mode, sink mode, range = 255 µA	–	300	500	µA
		Fast mode, sink mode, range = 2.04 mA	–	300	500	µA

Figure 11-30. IDAC INL vs Input Code, Range = 255 µA, Source Mode

Figure 11-31. IDAC DNL vs Input Code, Range = 255 µA, Source Mode

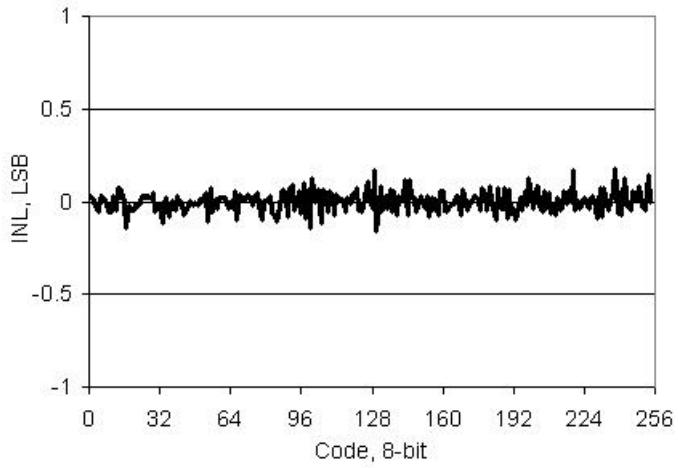


Figure 11-32. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

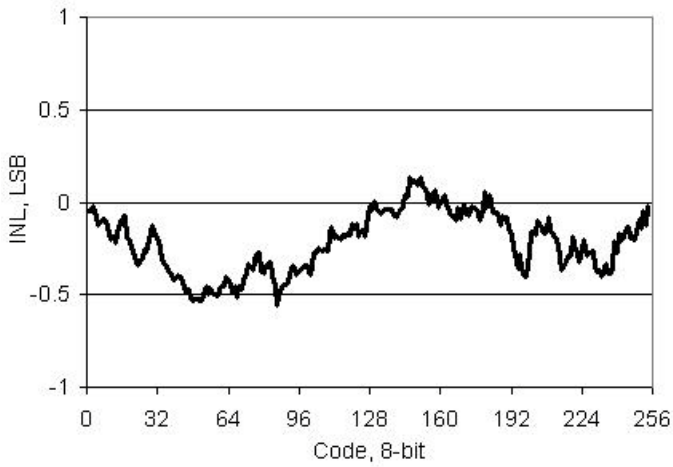


Figure 11-33. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode

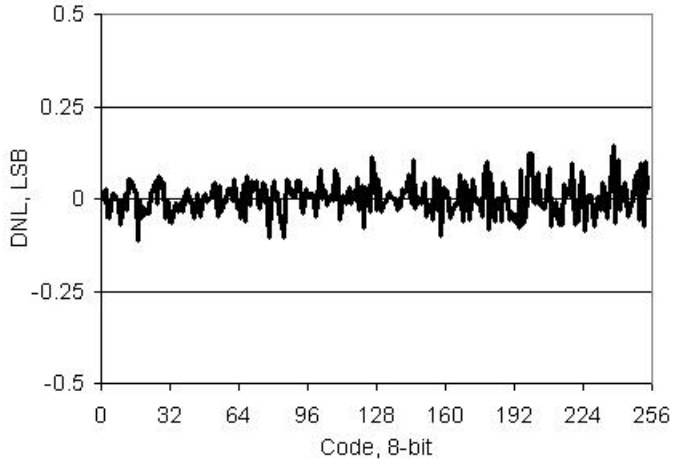


Figure 11-34. IDAC INL vs Temperature, Range = 255 µA, Fast Mode

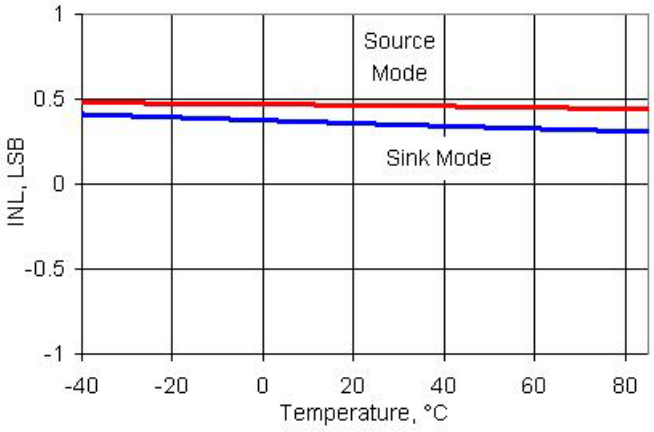


Figure 11-35. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

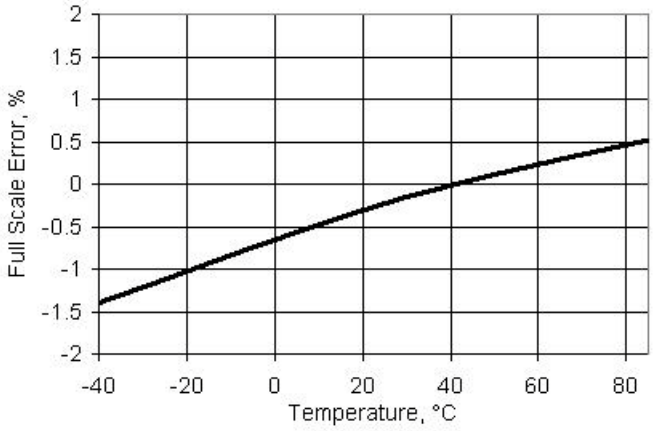


Figure 11-36. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

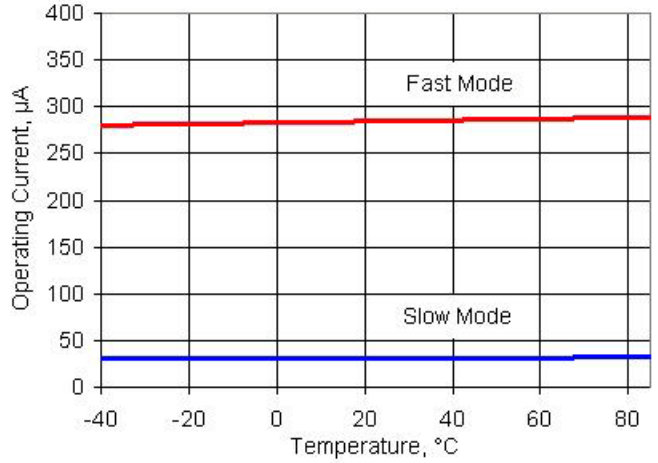


Figure 11-37. IDAC DNL vs Temperature, Range = 255 µA, Fast Mode

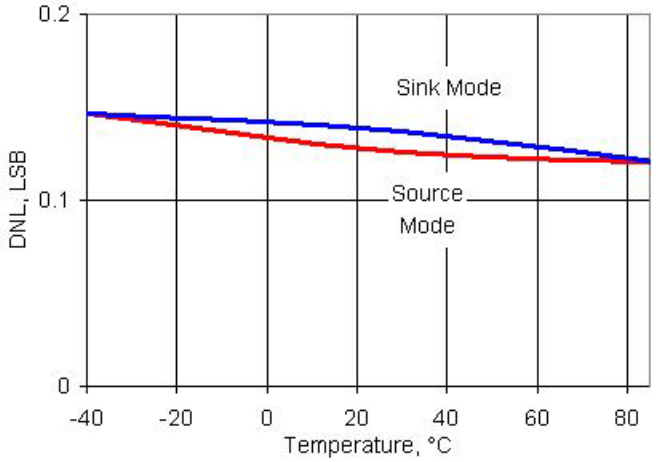


Figure 11-38. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

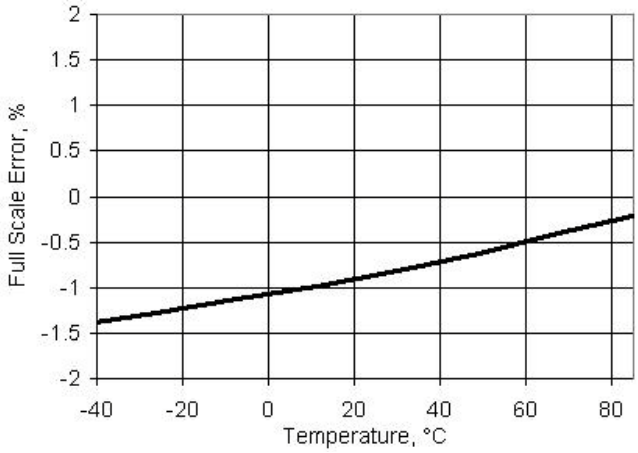


Figure 11-39. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

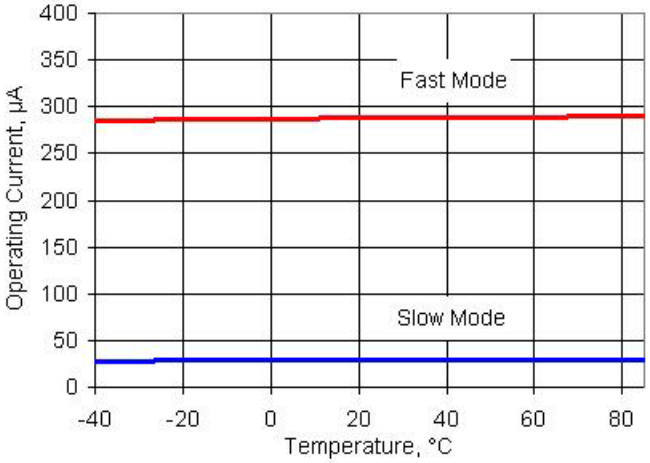


Table 11-24. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	5.5	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	180	ns
	Current noise	Range = 255 µA, source mode, fast mode, Vdda = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-40. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, Fast Mode, Vdda = 5 V

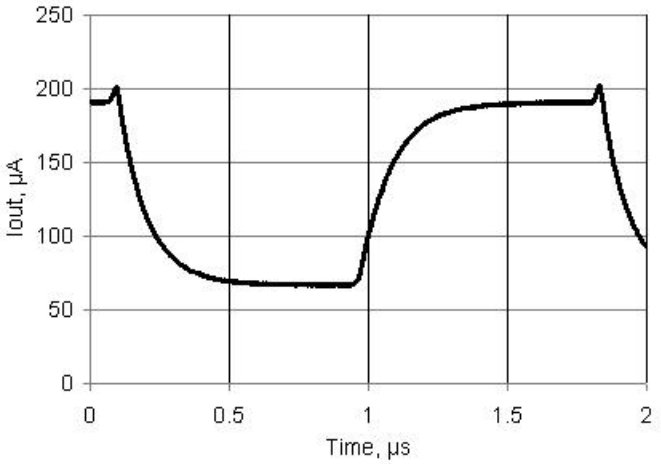


Figure 11-41. IDAC PSRR vs Frequency

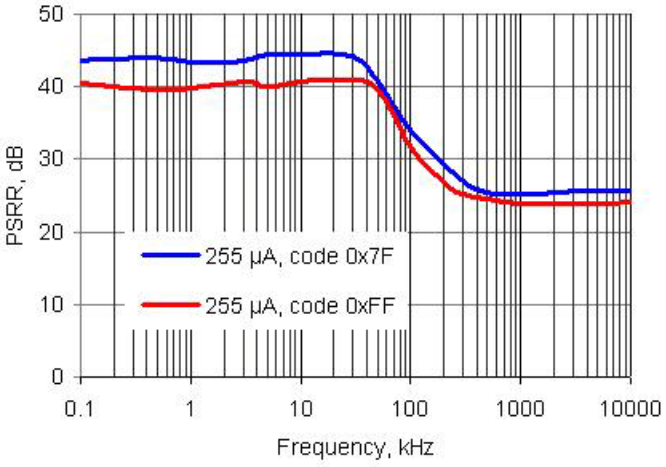


Figure 11-42. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, Fast Mode, Vdda = 5 V

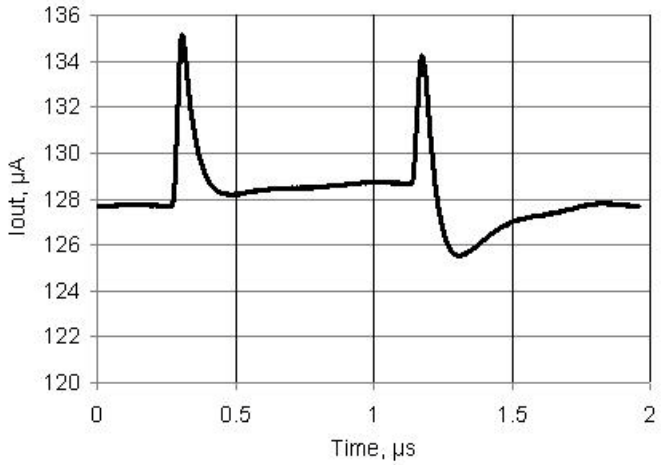
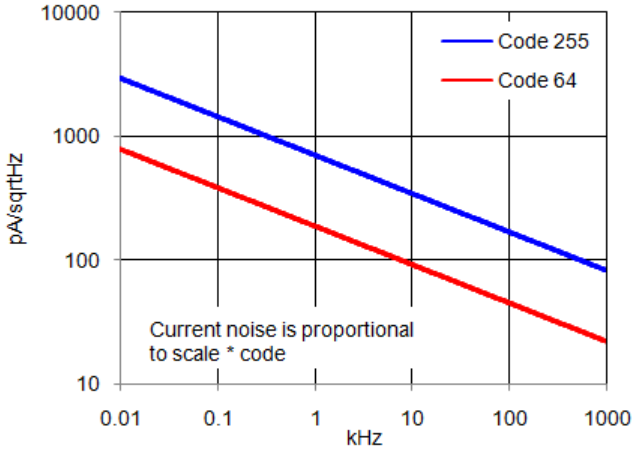


Figure 11-43. IDAC Current Noise, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V



11.5.7 Voltage Digital to Analog Converter (VDAC)

See the VDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-25. VDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	8	–	bits
INL1	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
DNL1	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
Rout	Output resistance	1 V scale	–	4	–	kΩ
		4 V scale	–	16	–	kΩ
V_{OUT}	Output voltage range, code = 255	1 V scale	–	1.02	–	V
		4 V scale, Vdda = 5 V	–	4.08	–	V
	Monotonicity		–	–	Yes	–
V_{OS}	Zero scale error		–	0	±0.9	LSB
Eg	Gain error	1 V scale	–	–	±5	%
		4 V scale	–	–	±5	%
TC_Eg	Temperature coefficient, gain error	1 V scale	–	–	0.03	%FSR / °C
		4 V scale	–	–	0.03	%FSR / °C
I_{DD}	Operating current	4 V slow mode	–	–	100	µA
		4 V fast mode	–	–	500	µA
		1 V slow mode	–	–	300	µA
		1 V fast mode	–	–	600	µA

Figure 11-44. VDAC INL vs Input Code, 1 V Mode

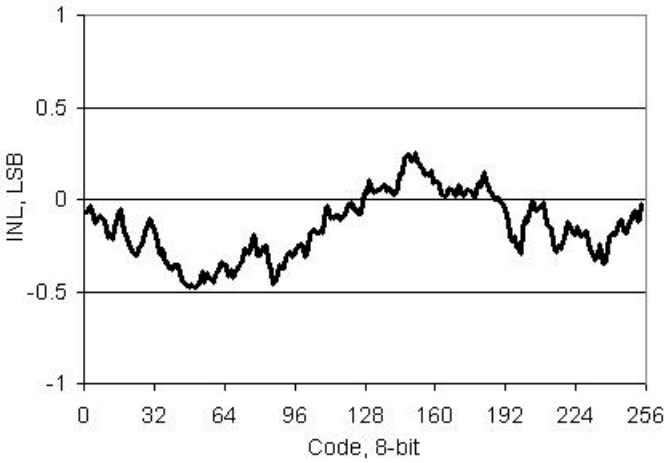


Figure 11-45. VDAC DNL vs Input Code, 1 V Mode

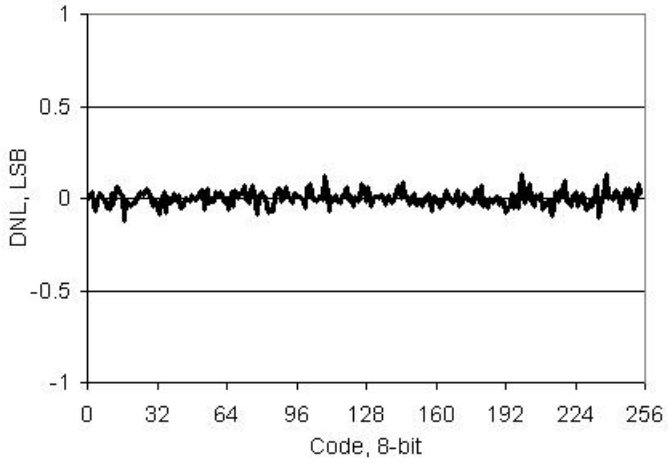


Figure 11-46. VDAC INL vs Temperature, 1 V Mode

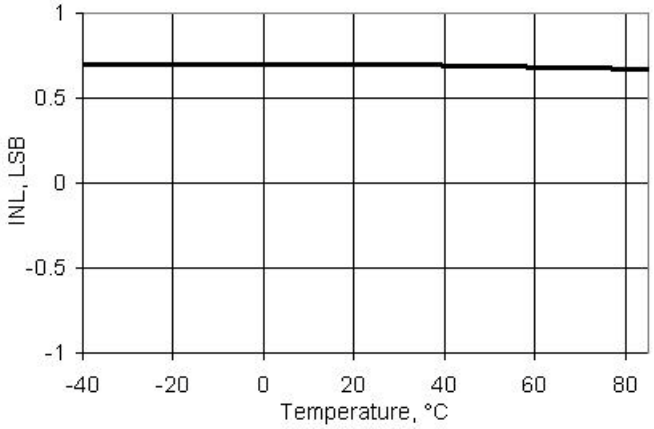


Figure 11-47. VDAC Full Scale Error vs Temperature, 1 V Mode

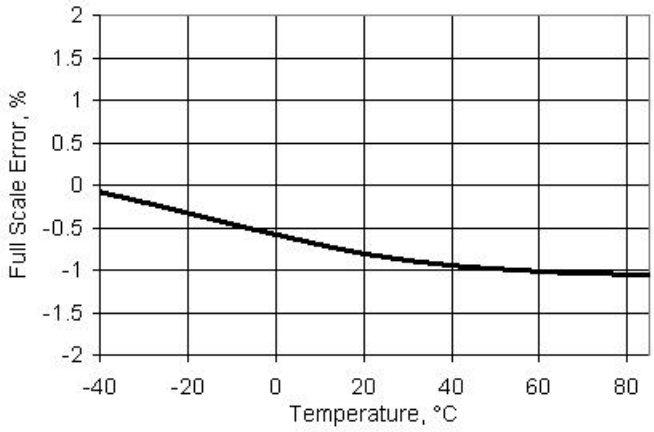


Figure 11-48. VDAC Operating Current vs Temperature, 1 V Mode, Slow Mode

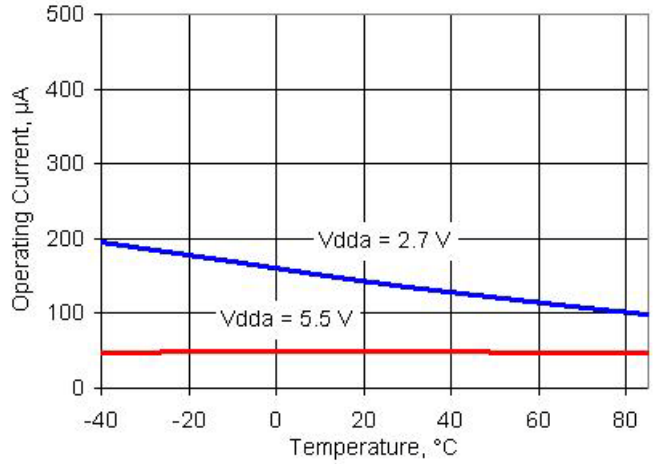


Figure 11-49. VDAC DNL vs Temperature, 1 V Mode

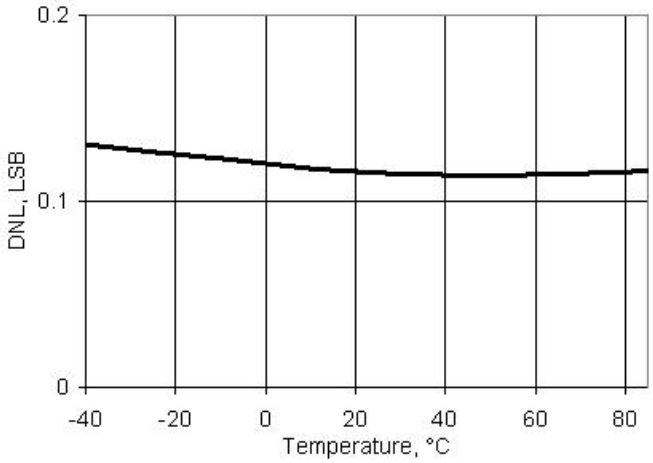


Figure 11-50. VDAC Full Scale Error vs Temperature, 4 V Mode

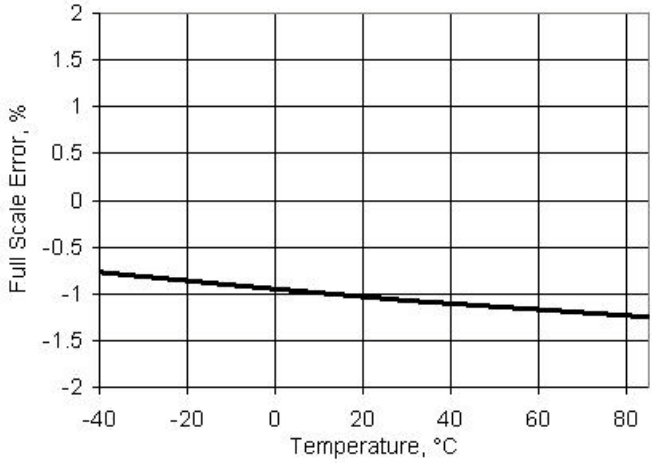


Figure 11-51. VDAC Operating Current vs Temperature, 1 V Mode, Fast Mode

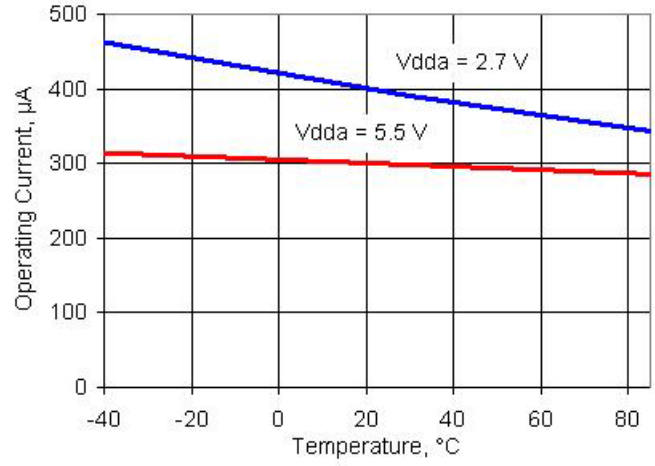


Table 11-26. VDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate	1 V scale	–	–	1000	ksps
		4 V scale	–	–	250	ksps
TsettleP	Settling time to 0.1%, step 25% to 75%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.8	4	µs
TsettleN	Settling time to 0.1%, step 75% to 25%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.7	4	µs
	Voltage noise	Range = 1 V, fast mode, Vdda = 5 V, 10 kHz	–	750	–	nV/sqrtHz

Figure 11-52. VDAC Step Response, Codes 0x40 - 0xC0, 1 V Mode, Fast Mode, Vdda = 5 V

Figure 11-53. VDAC PSRR vs Frequency

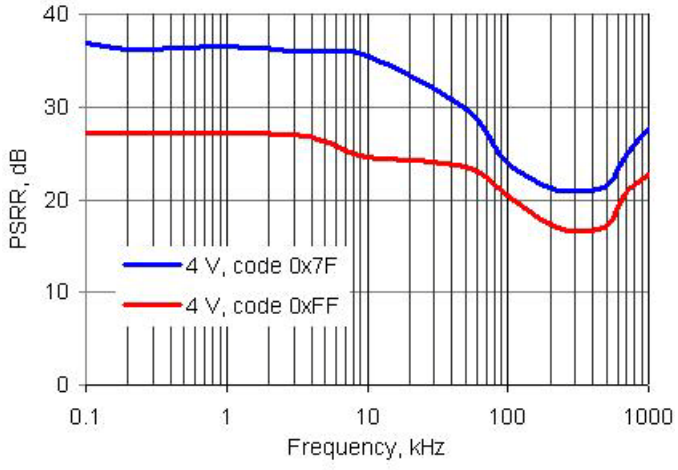


Figure 11-54. VDAC Glitch Response, Codes 0x7F - 0x80, 1 V Mode, Fast Mode, Vdda = 5 V

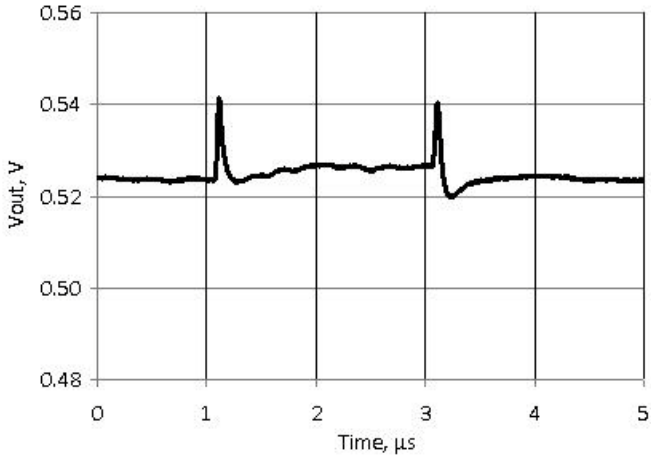
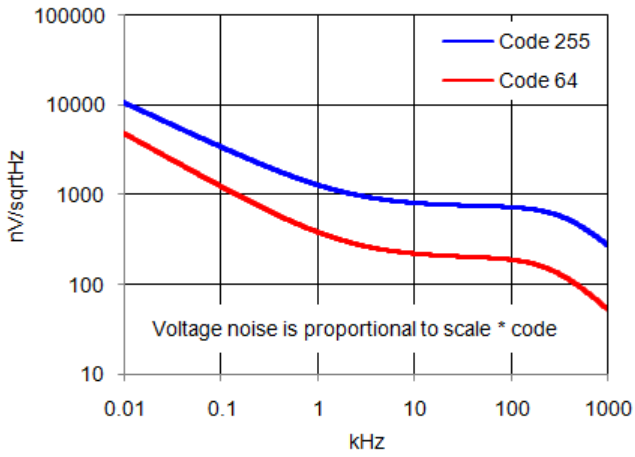


Figure 11-55. VDAC Voltage Noise, 1 V Mode, Fast Mode, V_{DDA} = 5 V



11.5.8 Mixer

The mixer is created using a SC/CT analog block; see the Mixer component data sheet in PSoC Creator for full electrical specifications and APIs.

Table 11-27. Mixer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage		–	–	26	mV
	Quiescent current		–	0.9	2	mA
G	Gain		–	0	–	dB

Table 11-28. Mixer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LO}	Local oscillator frequency	Down mixer mode	–	–	4	MHz
f_{in}	Input signal frequency	Down mixer mode	–	–	14	MHz
f_{LO}	Local oscillator frequency	Up mixer mode	–	–	1	MHz
f_{in}	Input signal frequency	Up mixer mode	–	–	1	MHz
SR	Slew rate		3	–	–	V/µs

11.5.9 Transimpedance Amplifier

The TIA is created using a SC/CT analog block; see the TIA component data sheet in PSoC Creator for full electrical specifications and APIs.

Table 11-29. Transimpedance Amplifier (TIA) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IOFF}	Input offset voltage		–	–	20	mV
Rconv	Conversion resistance[35]	R = 20K; 40 pF load	–25	–	+35	%
		R = 30K; 40 pF load	–25	–	+35	%
		R = 40K; 40 pF load	–25	–	+35	%
		R = 80K; 40 pF load	–25	–	+35	%
		R = 120K; 40 pF load	–25	–	+35	%
		R = 250K; 40 pF load	–25	–	+35	%
		R= 500K; 40 pF load	–25	–	+35	%
		R = 1M; 40 pF load	–25	–	+35	%
	Quiescent current		–	1.1	2	mA

Table 11-30. Transimpedance Amplifier (TIA) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW	Input bandwidth (–3 dB)	R = 20K; 40 pF load	1000	–	–	kHz
		R = 120K; 40 pF load	230	–	–	kHz
		R = 1M; 40 pF load	23	–	–	kHz

Note
35. Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component data sheets. External precision resistors can also be used.

11.5.10 Programmable Gain Amplifier

The PGA is created using a SC/CT analog block; see the PGA component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-31. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vin	Input voltage range	Power mode = minimum	Vssa	–	Vdda	V
Vos	Input offset voltage	Power mode = high, gain = 1	–	–	20	mV
TCVos	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
Ge1	Gain error, gain = 1		–	–	±2	%
Ge16	Gain error, gain = 16		–	–	±8	%
Ge50	Gain error, gain = 50		–	–	±10	%
Vonl	DC output nonlinearity	Gain = 1	–	–	±0.1	% of FSR
Cin	Input capacitance		–	–	7	pF
Voh	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	V_{DDA} – 0.15	–	–	V
Vol	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	–	–	V_{SSA} + 0.15	V
Vsrc	Output voltage under load	Iload = 250 µA, power mode = high	–	–	300	mV
Idd	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

Table 11-32. PGA AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1, noninverting mode, 300 mV ≤ VIN ≤ V_{DDA} – 1.2 V, CI ≤ 25 pF	6	8	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	–	–	V/µs
e_n	Input noise density	Power mode = high, Vdda = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

Figure 11-56. Bandwidth vs. Temperature, Gain = 1, Power Mode = High

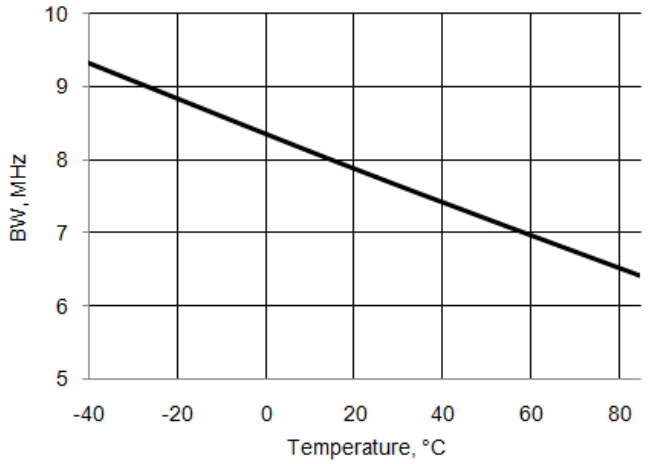
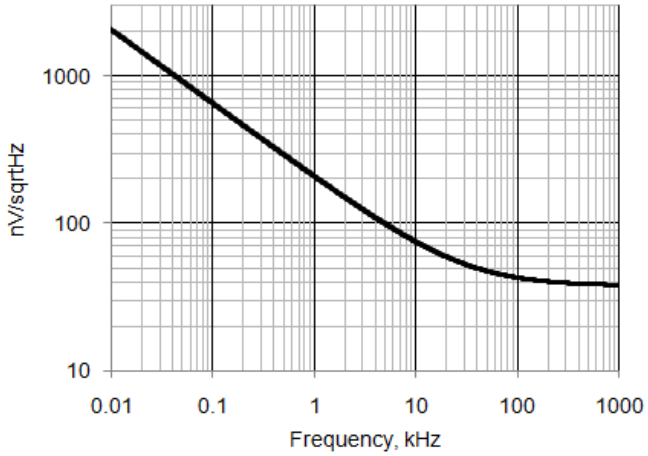


Figure 11-57. Noise vs. Frequency, V_{DDA} = 5 V, Power Mode = High



11.5.11 LCD Direct Drive

Table 11-33. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	LCD system operating current	Bus clock = 3 MHz, Vddio = Vdda = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	63	–	µA
I_{CC_SEG}	Current per segment driver		–	148	–	µA
V_{BIAS}	LCD bias range (V_{BIAS} refers to the main output voltage(V0) of LCD DAC)	3 V ≤ V_{BIAS} ≤ V_{DDIO} for the drive pin	2.09	–	5.2	V
	LCD bias step size	3 V ≤ V_{BIAS} ≤ V_{DDIO} for the drive pin	–	25.8	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset	V_{BIAS} ≤ V_{DDA} – 0.5 V	–	–	20	mV
I_{OUT}	Output drive current per segment driver)	Vddio = 5.5V	90	–	165	µA

Table 11-34. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LCD}	LCD frame rate		10	50	150	Hz

11.6 Digital Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.6.1 Timer

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component data sheet in PSoC Creator.

Table 11-35. Timer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	16-bit timer block current consumption	Input clock frequency – 3 MHz	–	65	–	µA
		Input clock frequency –12 MHz	–	170	–	µA
		Input clock frequency – 48 MHz	–	650	–	µA
		Input clock frequency – 67 MHz	–	900	–	µA

Table 11-36. Timer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Capture pulse width (Internal)		13	–	–	ns
	Capture pulse width (external)		30	–	–	ns
	Timer resolution		13	–	–	ns
	Enable pulse width		13	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		13	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component data sheet in PSoC Creator.

Table 11-37. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	48 MHz		–	260	–	µA
	67 MHz		–	350	–	µA

Table 11-38. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Capture pulse		13	–	–	ns
	Resolution		13	–	–	ns
	Pulse width		13	–	–	ns
	Pulse width (external)		30	–	–	ns
	Enable pulse width		13	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		13	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component data sheet in PSoC Creator.

Table 11-39. PWM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	16-bit PWM block current consumption	Input clock frequency – 3 MHz	–	65	–	µA
		Input clock frequency –12 MHz	–	170	–	µA
		Input clock frequency – 48 MHz	–	650	–	µA
		Input clock frequency – 67 MHz	–	900	–	µA

Table 11-40. PWM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Pulse width		13	–	–	ns
	Pulse width (external)		30	–	–	ns
	Kill pulse width		13	–	–	ns
	Kill pulse width (external)		30	–	–	ns
	Enable pulse width		13	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		13	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.4 I^2C

Table 11-41. Fixed I^2C DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	Enabled, configured for 100 kbps	–	90	250	µA
		Enabled, configured for 400 kbps	–	100	250	µA

Table 11-42. Fixed I^2C AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate		–	–	400	Kbps

11.6.5 USB

Table 11-43. USB DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{USB_5}	Device supply for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
$V_{USB_3.3}$		USB configured, USB regulator bypassed	3.15	–	3.6	V
$I_{USB_Configured}$	Device supply current in device active mode	V_{DDD} = 5 V, bus clock ≥ 33 MHz	–	55	–	mA
		V_{DDD} = 3.3 V, bus clock ≥ 33 MHz	–	40	–	mA
$I_{USB_Suspended}$	Device supply current in device sleep mode	V_{DDD} = 5 V, connected to USB host	–	0.5	–	mA
		V_{DDD} = 3.3 V, connected to USB host	–	0.5	–	mA

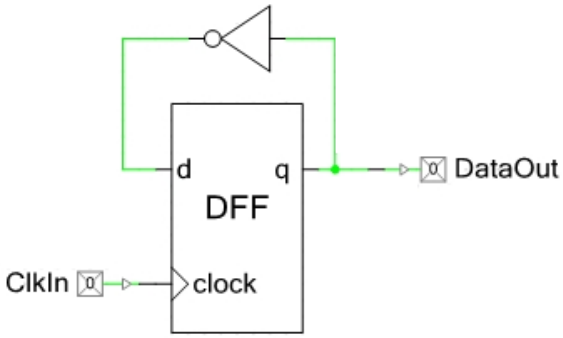
11.6.6 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component data sheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-44. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-58.	25 °C	–	20	28	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-58.	Worst-case placement, routing, and pin selection	–	–	55	ns

Figure 11-58. Clock to Output Performance



11.7 Memory

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-45. Flash DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	V_{DDD} pin	2.7	–	5.5	V

Table 11-46. Flash AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Row write time (erase + program)		–	8.3	32	ms
T_{BULK}	Bulk erase time (256 KB)	10 °C < average ambient temp. T_A < 40 °C	–	117	440	ms
	Sector erase time (16 KB)	10 °C < average ambient temp. T_A < 40 °C	–	6.3	26	ms
T_{PROG}	Total device programming time	No overhead[36]	–	9	32.5	seconds
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. T_A ≤ 55 °C, 100 K erase/program cycles	20	–	–	years
		Average ambient temp. T_A ≤ 70 °C, 10 K erase/program cycles	10	–	–	

Note
36. See application note AN64359 for a description of a low-overhead method of programming PSoC 5 flash.

11.7.2 EEPROM

Table 11-47. EEPROM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		2.7	–	5.5	V

Table 11-48. EEPROM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{WRITE}	Single row erase/write cycle time		–	8.3	32	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, $T_A \leq 55$ °C, 1M erase/program cycles	20	–	–	years

11.7.3 SRAM

Table 11-49. SRAM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{SRAM}	SRAM retention voltage		1.2	–	–	V

Table 11-50. SRAM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{SRAM}	SRAM operating frequency		DC	–	67.01	MHz

11.7.4 Write Once Latch (WOL)

Table 11-51. WOL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Program voltage	V_{DDD} pin	2.7	–	3.3	V
	Program temperature	T_J	10	25	40	°C

11.8 PSoC System Resources

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.8.1 Voltage Monitors

Table 11-52. Voltage Monitors DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

Table 11-53. Voltage Monitors AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Response time[37]		–	1	–	µs

11.8.2 Interrupt Controller

Table 11-54. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from interrupt signal input to ISR code execution from main line code[38]		–	–	12	Tcy CPU
	Delay from interrupt signal input to ISR code execution from ISR code (tail-chaining)[38]		–	–	6	Tcy CPU

Note
37. Based on device characterization (Not production tested).
38. ARM Cortex-M3 NVIC spec. Visit www.arm.com for detailed documentation about the Cortex-M3 CPU.

11.8.3 SWD Interface

Figure 11-59. SWD Interface Timing

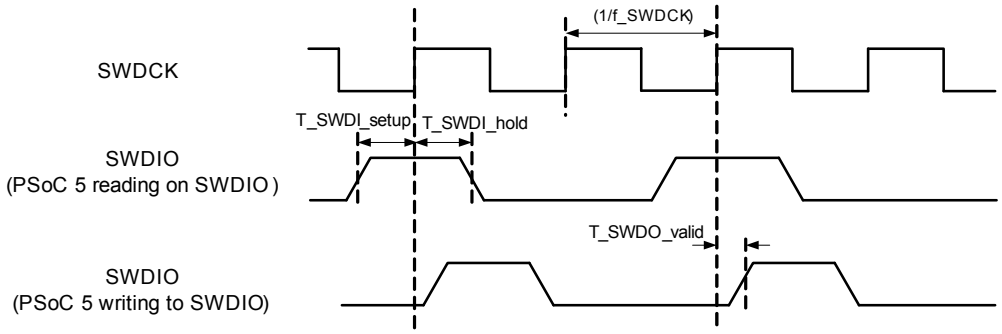


Table 11-55. SWD Interface AC Specifications[39]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_SWDCK	SWDCLK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	12[40]	MHz
		2.7 V ≤ V_{DDD} < 3.3 V	–	–	6.5[40]	MHz
		2.7 V ≤ V_{DDD} < 3.3 V, SWD over USBIO pins	–	–	5[40]	MHz
T_SWDI_setup	SWDIO input setup before SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDI_hold	SWDIO input hold after SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDO_valid	SWDCK high to SWDIO output	T = 1/f_SWDCK max	–	–	2T/5	

11.8.4 TPIU Interface

Table 11-56. TPIU Interface AC Specifications[41]

Parameter	Description	Conditions	Min	Typ	Max	Units
	SWV bit rate		–	–	33	Mbit

Notes
39. Based on device characterization (Not production tested).
40. f_SWDCK must also be no more than 1/3 CPU clock frequency.
41. SWV signal frequency and bit rate are limited by GPIO output frequency, see "GPIO AC Specifications" on page 62.

11.9 Clocking

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.9.1 kHz External Crystal Oscillator (kHzECO)

For more information on crystal selection for the kHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-57. kHz ECO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Oscillator operating current	Low power mode; CL = 6 pF	–	0.25	–	µA
C_{IN}	Capacitance at Pins kHz-XTAL:Xi and kHz-XTAL:Xo[42]		–	5	7	pF

Table 11-58. kHz ECO Crystal Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency		–	32.768	–	kHz
C_L	Crystal load capacitance	Recommended values	–	6 or 12.5	–	pF
D_L	Crystal drive level tolerance		1	–	–	µW

11.9.2 Internal Main Oscillator

Table 11-59. IMO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	48 MHz		–	465	850	µA
	24 MHz		–	195	500	µA
	12 MHz		–	150	450	µA
	6 MHz		–	120	400	µA
	3 MHz		–	105	300	µA

Note
42. Based on device characterization (Not production tested).

Figure 11-60. IMO Current vs. Frequency

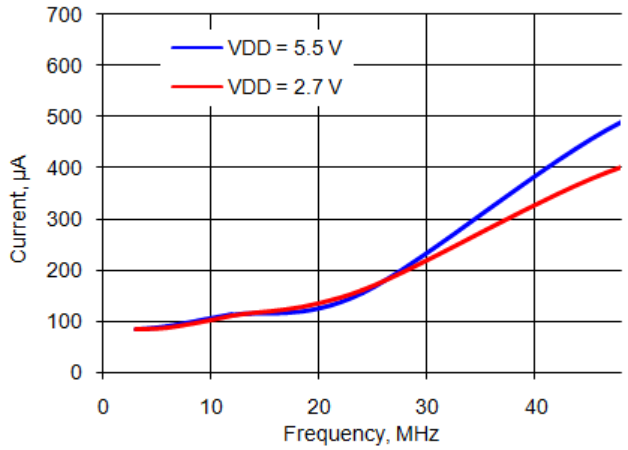


Table 11-60. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO}	IMO frequency stability (with factory trim)					
	48 MHz		–10	–	10	%
	24 MHz		–8	–	8	%
	12 MHz		–6.25	–	6.25	%
	6 MHz		–5.8	–	5.8	%
	3 MHz		–5	–	5	%
	Startup time[43]	From enable (during normal system operation) or wakeup from low power state	–	–	12	µs
Jp-p	Jitter (peak to peak)[43]					
	F = 24 MHz		–	0.5	–	ns
	F = 3 MHz		–	2.3	–	ns

Figure 11-61. IMO Frequency Variation vs. Temperature

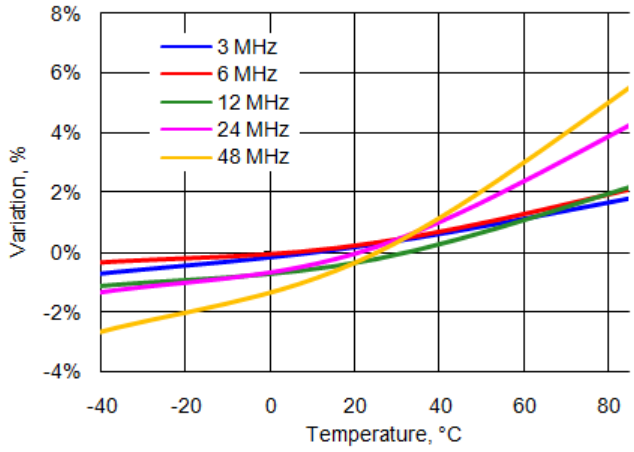
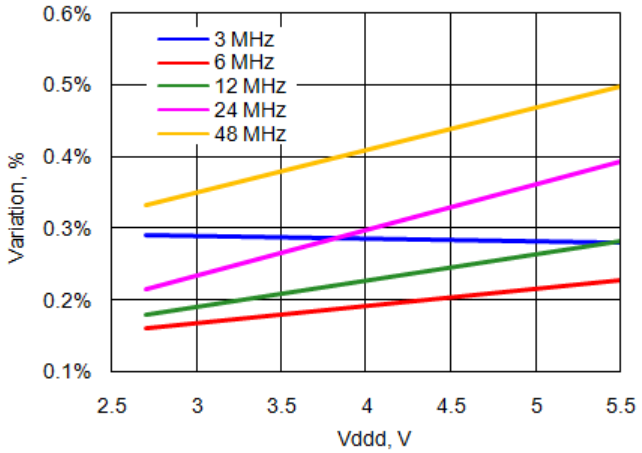


Figure 11-62. IMO Frequency Variation vs. V_{DDD}



Note
43. Based on device characterization (Not production tested).

11.9.3 Internal Low Speed Oscillator

Table 11-61. ILO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time, all frequencies	Turbo mode	–	–	2.5	ms
F_{ILO}	ILO frequencies (trimmed)					
	100 kHz		45	100	200	kHz
	1 kHz		0.5	1	2	kHz
	ILO frequencies (untrimmed)					
	100 kHz		30	100	300	kHz
	1 kHz		0.3	1	3.5	kHz

Figure 11-63. ILO Frequency Variation vs. Temperature

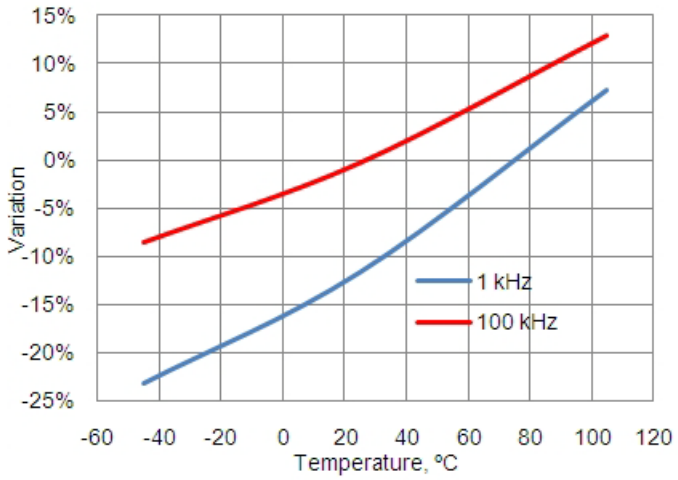
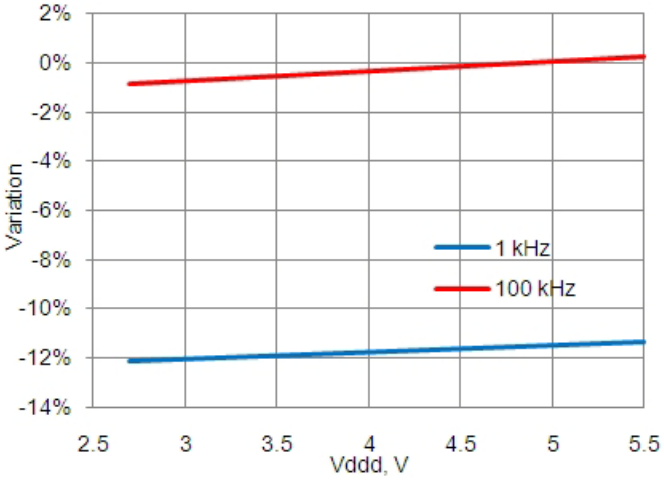


Figure 11-64. ILO Frequency Variation vs. V_{DD}



11.9.4 MHz External Crystal Oscillator (MHzECO)

For more information on crystal or ceramic resonator selection for the MHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-62. MHzECO Crystal Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency		4	–	25	MHz
C_L	Crystal load capacitance		–	–	20	pF
C0	Crystal shunt capacitance		–	–	7	pF
ESR	Crystal effective series resistance	4 MHz ≤ F < 8 MHz	–	–	125	Ω
		8 MHz ≤ F < 12 MHz	–	–	75	Ω
		12 MHz ≤ F ≤ 25 MHz	–	–	50	Ω
DL	Crystal drive level tolerance	No Rs, see AN54439	500	–	–	µW
C_{IN}	Capacitance at Pins MHz-XTAL:Xi and MHz-XTAL:Xo[44]		–	4	–	pF

11.9.5 External Clock Reference

Table 11-63. External Clock Reference AC Specifications[45]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase-Locked Loop

Table 11-64. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 67 MHz	–	400	–	µA
		In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-65. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[45]		1	–	48	MHz
	PLL intermediate frequency[46]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[45]		24	–	67	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[47]		–	–	400	ps

Notes
44. Based on device characterization (Not production tested).
45. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
46. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.
47. Based on device characterization (Not production tested).

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C53 device includes: up to 128 KB flash, 32 KB SRAM, 2 KB EEPROM, a precision on-chip voltage reference, precision oscillators, flash, DMA, a fixed function I^2C, SWD programming and debug, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C53 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C53 Family with ARM Cortex-M3 CPU

Part Number	MCU Core				Analog								Digital			I/O[50]				Package	Device ID[51]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparators	SC/CT Analog Blocks[48]	Opamps	DFB	CapSense	UDBs[49]	16-bit Timer/PWM	FS USB	Total I/O	GPIO	SIO	USBIO		
CY8C5368LTI-026	67	256	64	2	✔	1 × 12-bit SAR	2	4	2	2	–	✔	24	4	✔	46	36	8	2	68-pin QFN	0x0E11A069
CY8C5368AXI-106	67	256	64	2	✔	1 × 12-bit SAR	2	4	2	2	–	✔	24	4	✔	70	60	8	2	100-pin TQFP	0x0E16A069
CY8C5367LTI-003	67	128	32	2	✔	1 × 12-bit SAR	2	4	2	2	–	✔	24	4	✔	46	36	8	2	68-pin QFN	0x0E103069
CY8C5367AXI-108	67	128	32	2	✔	1 × 12-bit SAR	2	4	2	2	–	✔	24	4	✔	70	60	8	2	100-pin TQFP	0x0E16C069
CY8C5366LTI-053	67	64	16	2	✔	1 × 12-bit SAR	2	4	2	2	–	✔	24	4	✔	46	36	8	2	68-pin QFN	0x0E135069
CY8C5366AXI-001	67	64	16	2	✔	1 × 12-bit SAR	2	4	2	2	–	✔	24	4	✔	70	60	8	2	100-pin TQFP	0x0E101069
CY8C5365LTI-104	67	32	8	2	✔	1 × 12-bit SAR	2	4	2	2	–	✔	20	4	✔	46	36	8	2	68-pin QFN	0x0E168069
CY8C5365AXI-043	67	32	8	2	✔	1 × 12-bit SAR	2	4	2	2	–	✔	20	4	✔	70	60	8	2	100-pin TQFP	0x0E12B069

Notes

48. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See Example Peripherals on page 32 for more information on how analog blocks can be used.
49. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See Example Peripherals on page 32 for more information on how UDBs can be used.
50. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See I/O System and Routing on page 25 for details on the functionality of each of these types of I/O.
51. The device ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

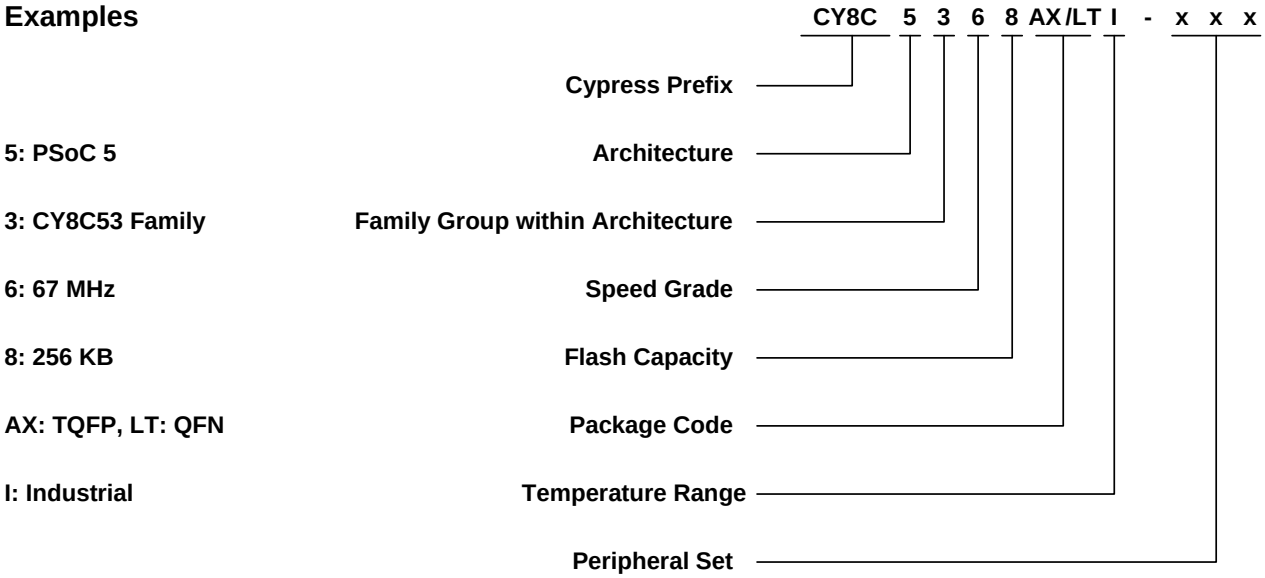
12.1 Part Numbering Conventions

PSoC 5 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, …, 9, A, B, …, Z) unless stated otherwise.

CY8Cabcdefg-xxx

- a: Architecture
  - 3: PSoC 3
  - 5: PSoC 5
- b: Family group within architecture
  - 2: CY8C52 family
  - 3: CY8C53 family
  - 4: CY8C54 family
  - 5: CY8C55 family
- c: Speed grade
  - 4: 40 MHz
  - 6: 67 MHz
- d: Flash capacity
  - 5: 32 KB
  - 6: 64 KB
  - 7: 128 KB
  - 8: 256 KB
- ef: Package code
  - Two character alphanumeric
  - AX: TQFP
  - LT: QFN
- g: Temperature range
  - C: commercial
  - I: industrial
  - A: automotive
- xxx: Peripheral set
  - Three character numeric
  - No meaning is associated with these three characters

Examples



All devices in the PSoC 5 CY8C53 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration data sheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25	85	°C
T_J	Operating junction temperature		–40	–	100	°C
Tja	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
Tja	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
Tjc	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
Tjc	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt

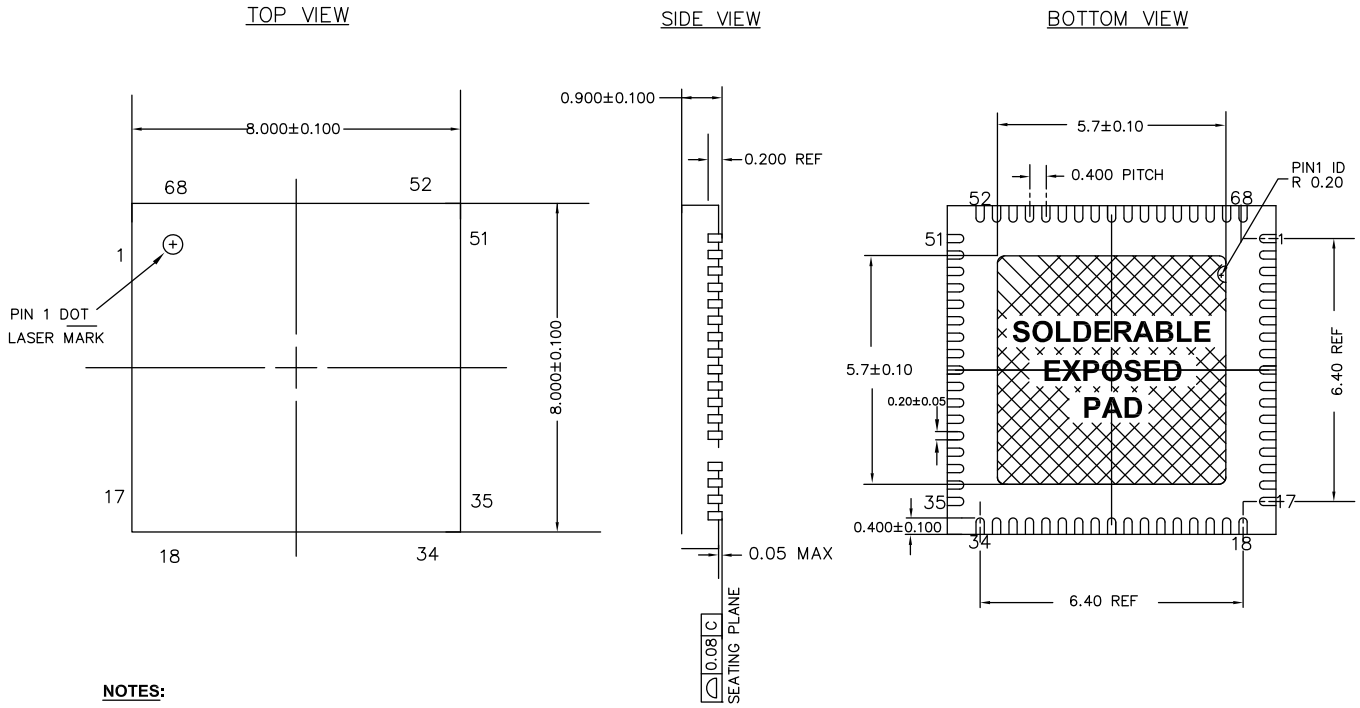
Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3
100-pin TQFP	MSL 3

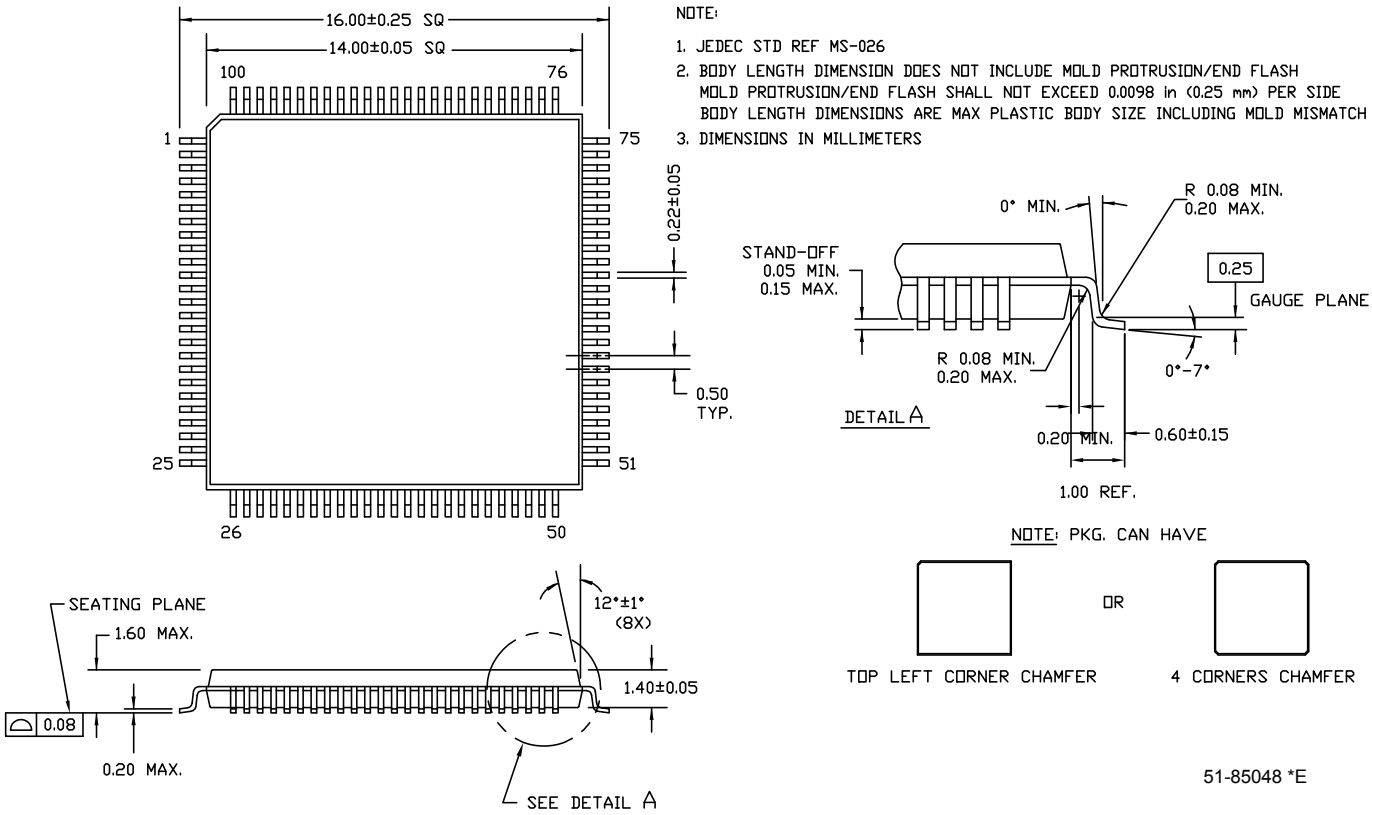
Figure 13-1. 68-Pin QFN 8x8 with 0.4 mm Pitch Package Outline (Sawn Version)



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.17g
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *D

Figure 13-2. 100-Pin TQFP (14 × 14 × 1.4 mm) Package Outline



14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RSVD	reserved
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SIO	special input/output, GPIO with advanced features. See GPIO.
SNR	signal-to-noise ratio
SOC	start of conversion
SOF	start of frame

Table 14-1. Acronyms Used in this Document (continued)

Acronym	Description
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

PSoC® 3, PSoC® 5 Architecture TRM

PSoC® 5 Registers TRM

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts

17. Revision History

Description Title: PSoC® 5: CY8C53 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-66237				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	3198501	03/17/2011	MKEA	New data sheet.
*A	3279676	06/10/2011	MKEA	Changed MHzECO range Updated Flash and EEPROM AC specs Added solder reflow peak temperature table Changed IDAC IDD numbers and VDAC Added flash retention specs Added JTAG and SWD interface diagrams Removed mention of comparator wakeup from sleep Updated PSoC Power system diagram Updated opamp dc specs table Updated SAR electrical specs Updated clocking sections Removed references to JTAG interface Updated and I/O graphs Added note that Interrupt Specs are ARM Specs Changed JTAG and SWD max speeds Modified ILO startup time Removed references to ETM and TRACEPORT Updated IDAC range limits Updated Vddio pin description Updated Power Modes section Added note on watchdog timer in the Reset section Updated ESD_{HBM} value Updated Boost Converter section
*B	3359654	09/01/2011	MKEA	Removed Boost regulator Removed Temperature Sensor specifications Updated device DC and AC specifications Updated Cortex-M3 bitband information Updated cache controller information Updated GPIO and SIO DC specifications Updated Opamp AC and DC specifications Updated IDAC AC specifications Updated comparator DC specifications Updated TIA AC specifications Updated Mixer DC specifications Updated Analog global specifications Updated Fixed function PWM and Timer DC specifications Changed fixed function I2C max bus speed Added note on undefined I2C bus conditions Updated USB DC specifications Updated USB driver AC specification Updated information to include 24 MHz ECO and 33 MHz bus clock for USB function Updated kHzECO and MHzECO Specifications Updated IMO AC specifications Updated PLL AC specifications Updated SWD interface section Updated Device IDs
*C	3422215	10/25/2011	MKEA	Changed ESD_{HBM} value to 750 Changed Min value of Input Edge Rate to 0.5 V/ns. Updated Low Power mode information throughout document

Description Title: PSoC® 5: CY8C53 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-66237				
*D	3428148	02/15/2012	WKA/MKEA	Moved status from Preliminary to Final. Changed pins 5, 7, and 8 to VSSD and pin 6 to DNU in 68-pin QFN pinout. Changed pins 10, 12, and 13 to VSSD and pin 11 to DNU in 100-pin TQFP pinout. Changed pins 10, 12, and 13 to VSSD and pin 11 to DNU in Typical Application Schematic. Updated latch up spec in Table 11-1. Updated I_{DD} parameter (Active mode) in Table 11-2. Updated sleep and hibernate current. Updated "DAC" section on page 51. Added note on strobing DAC twice. Updated "SIO" section on page 63. Added note on conditions for SIO to draw excess current. Updated pinout diagrams (Figure 2-1, Figure 2-2, and Figure 2-3) Updated Table 11-2 to include Power consumption details. Updated active, sleep and hibernate modes current specifications (Table 11-2, Table 6-3). Updated latch up current specification (Table 11-1) Updated ESD_{HBM} specification (Table 11-1) Updated "USB" section on page 41. Added note on required clock sources for using USB. Updated GPIO, SIO and USBIO graphs (Figure 11-5 to Figure 11-15) Added active mode current graph. (Figure 11-1). Updated LVI / HVI table in Section 6 (Table 6-4, Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt). Updated GPIO block diagram (Figure 6-7). Updated Table 11-1 IV_{DDIO} spec to have two sub-rows Updated note about max V_{DDIO} current sink capability Updated PGA graphs (Figure 11-55, Figure 11-56, and Figure 11-57). Updated SAR ADC graphs (Figure 11-24, Figure 11-25, Figure 11-27, Figure 11-28, and Figure 11-29) Updated Opamp graphs (Figure 11-17, Figure 11-18, Figure 11-19, Figure 11-20, Figure 11-20, Figure 11-21, Figure 11-22, and Figure 11-23). Updated Table 11-2 to include rows for I_{DDAR} and I_{DDDR}. Updated IDAC and VDAC graphs (Figure 11-30 to Figure 11-55). Updated "Reset" section on page 24. More details given to distinguish External Reset (XRES) from Power-on Reset Fixed typos: Replaced "CY8C38" with "PSoC 5" and "CY8C32" to "CY8C52". Updated the graphs under "Internal Main Oscillator" section on page 92 section. Updated and clarified specifications and conditions for sleep mode. Updated f_SWDCK, SWDCLK frequency max values Updated Table 11-3, T_{SLEEP} parameter

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