WINSOURCE ELECTRONICS

THE DATASHEET OF

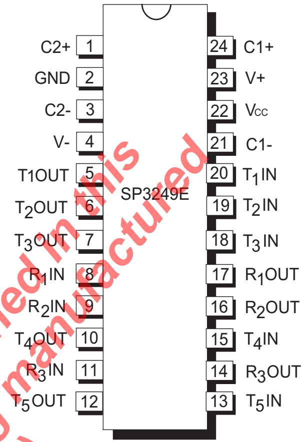
MCP23017T-E/ML

SP3249E

Intelligent +3.0V to +5.5V RS-232 Transceiver

FEATURES

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- Minimum 250Kbps data rate under load
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V_{CC} Variations
- Enhanced ESD Specifications:
  - $\pm$15kV Human Body Model
  - $\pm$15kV IEC61000-4-2 Air Discharge
  - $\pm$8kV IEC61000-4-2 Contact Discharge



Now Available in Lead Free Packaging

DESCRIPTION

The SP3249E device is an RS-232 transceiver solution intended for portable or hand-held applications such as notebook and palmtop computers. The SP3249E uses an internal high-efficiency, charge-pump power supply that requires only 0.1µF capacitors in 3.3V operation. This charge pump and Exar's driver architecture allow the SP3249E device to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.5V. The SP3249E is a 5-driver / 3-receiver device that is ideal for laptop / notebook computer and PDA applications.

SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Auto On-Line Circuitry	TTL 3-State	# of Pins
SP3223E	+3.0V to +5.5V	2	2	4 Capacitors	YES	YES	20
SP3243E	+3.0V to +5.5V	3	5	4 Capacitors	YES	YES	28
SP3238E	+3.0V to +5.5V	5	3	4 Capacitors	YES	YES	28
SP3239E	+3.0V to +5.5V	5	3	4 Capacitors	NO	YES	28
SP3249E	+3.0V to +5.5V	5	3	4 Capacitors	NO	NO	24

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}...-0.3V to +6.0V
V+ (NOTE 1).......................................-0.3V to +7.0V
V- (NOTE 1).......................................+0.3V to -7.0V
V+ + |V-| (NOTE 1)...+13V
I_{CC} (DC V_{CC} or GND current).........................±100mA

Input Voltages
TxIN, ...-0.3V to +6.0V
RxIN...±25V
Output Voltages
TxOUT...±13.2V
RxOUT......................................-0.3V to (V_{CC} +0.3V)
Short-Circuit Duration
TxOUT..Continuous
Storage Temperature......................-65°C to +150°C

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V to +5.5V, C1 - C4 = 0.1µF (tested at 3.3V +/-5%), C1 - C4 = 0.22µF (tested at 3.3V +/-10%), C1 = 0.047µF and C2 - C4 = 0.33µF (tested at 5.0V +/-10%), T_{AMB} = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current		0.3	1.0	mA	no load
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW HIGH	 2.4		0.8	V V	V_{CC} = +3.3V or +5.0V, TxIN
Input Leakage Current		±0.01	±1.0	µA	TxIN, T_{AMB} = +25°C
Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
Output Voltage HIGH	V_{CC} -0.6	V_{CC} -0.1		V	I_{OUT} = -1.0mA
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	All driver outputs loaded with 3KΩ to GND

V_{CC} = +3.0V to +5.5V, C1 - C4 = 0.1µF (tested at 3.3V +/-5%), C1 - C4 = 0.22µF (tested at 3.3V +/-10%), C1 = 0.047µF and C2 - C4 = 0.33µF (tested at 5.0V +/-10%), T_{AMB} = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS (continued)					
Output Resistance	300			Ω	V_{CC} = V+ = V- = 0V, V_{OUT}=±2V
Output Short-Circuit Current		±35	±60	mA	V_{OUT} = GND
RECEIVER INPUTS					
Input Voltage Range	-25		25	V	
Input Threshold LOW	0.6	1.2		V	Vcc = 3.3V
Input Threshold LOW	0.8	1.5		V	Vcc = 5.0V
Input Threshold HIGH		1.5	2.4	V	Vcc = 3.3V
Input Threshold HIGH		1.8	2.4	V	Vcc = 5.0V
Input Hysteresis		0.5		V	
Input Resistance	3	5	7	kΩ	
TIMING CHARACTERISTICS					
Maximum Data Rate	250			kbps	R_L = 3KΩ, C_L = 1000pF, one driver switching
Receiver Propagation Delay t_{PHL} t_{PLH}		 0.15 0.15		µs	Receiver input to Receiver output, C_L = 150pF
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		100		ns	$\| t_{PHL} - t_{PLH} \|$, T_{AMB} = 25°C
Receiver Skew		50		ns	$\| t_{PHL} - t_{PLH} \|$
Transition-Region Slew Rate			30	V/µs	Vcc = 3.3V, R_L = 3kΩ, T_{AMB} = 25°C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 250kbps data rate, all drivers loaded with 3kΩ, 0.1μF charge pump capacitors, and T_{AMB} = +25°C.

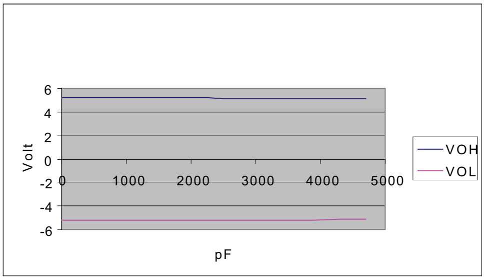


Figure 1. Transmitter Output Voltage VS. Load Capacitance

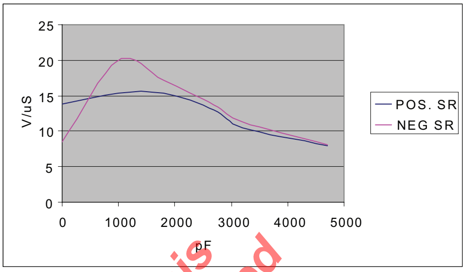


Figure 2. Slew Rate VS. Load Capacitance

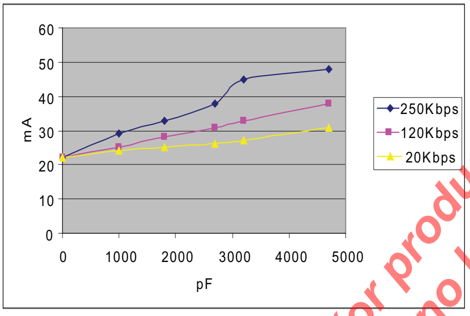


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data

NAME	FUNCTION	PIN NUMBER
C2+	Positive terminal of the symmetrical charge-pump capacitor C2.	1
GND	Ground.	2
C2-	Negative terminal of the symmetrical charge-pump capacitor C2.	3
V-	Regulated -5.5V output generated by the charge pump.	4
T_1OUT	RS-232 Driver Output.	5
T_2OUT	RS-232 Driver Output.	6
T_3OUT	RS-232 Driver Output.	7
R_1IN	RS-232 receiver input.	8
R_2IN	RS-232 receiver input.	9
T_4OUT	RS-232 Driver Output.	10
R_3IN	RS-232 receiver input.	11
T_5OUT	RS-232 Driver Output.	12
T_5IN	TTL/CMOS driver input.	13
R_3OUT	TTL/CMOS receiver output.	14
T_4IN	TTL/CMOS driver input.	15
R_2OUT	TTL/CMOS receiver output.	16
R_1OUT	TTL/CMOS receiver output.	17
T_3IN	TTL/CMOS driver input.	18
T_2IN	TTL/CMOS driver input.	19
T_1IN	TTL/CMOS driver input.	20
C1-	Negative terminal of the symmetrical charge-pump capacitor C1.	21
Vcc	+3.0V to +5.5V supply voltage.	22
V+	Regulated +5.5V output generated by the charge pump.	23
C1+	Positive terminal of the symmetrical charge-pump capacitor C1.	24

Table 1. Device Pin Description

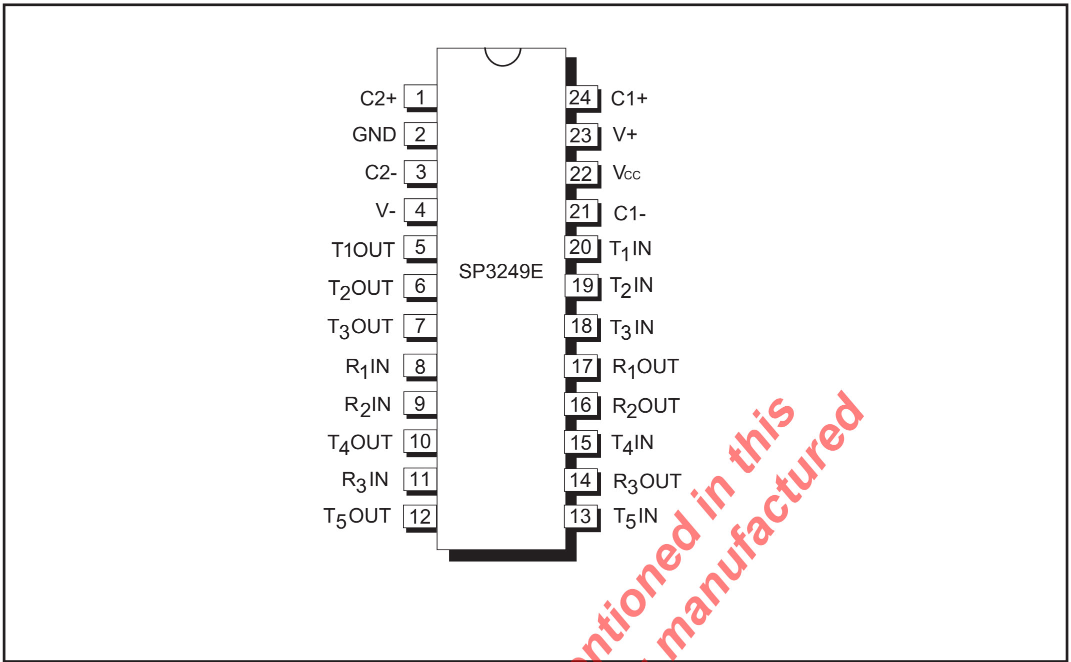


Figure 4. SP3249E Pinout Configuration

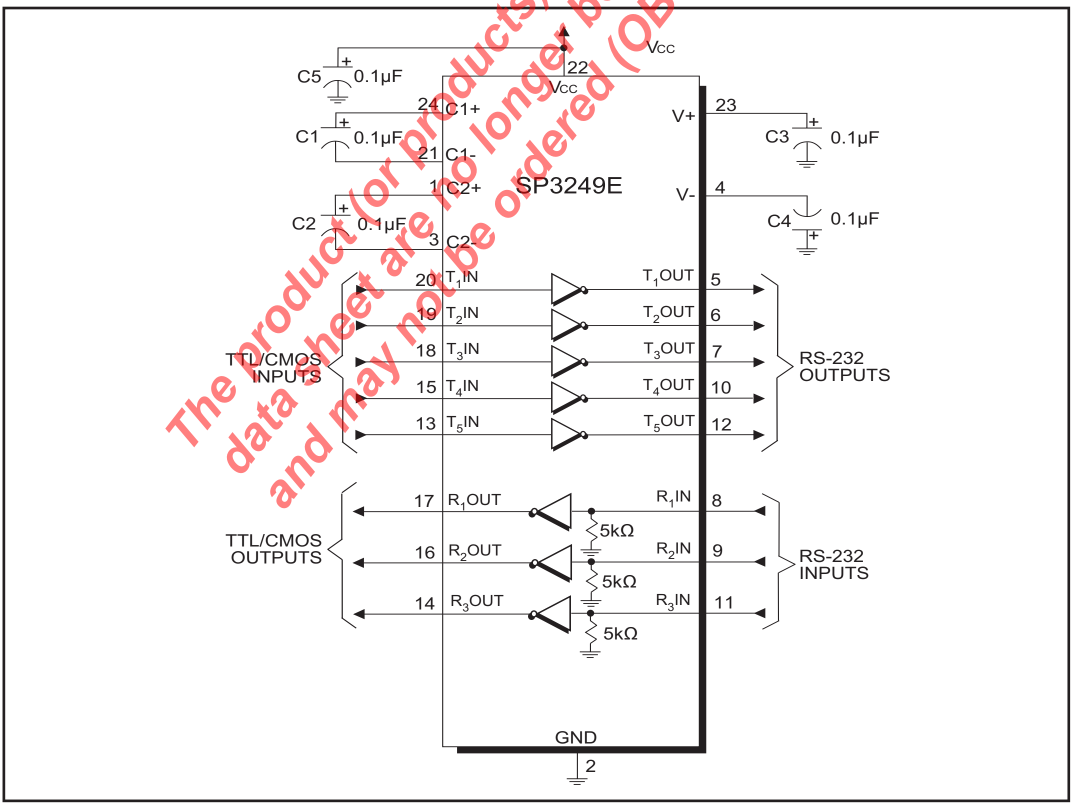


Figure 5. SP3249E Typical Operating Circuit

DESCRIPTION

The SP3249E device meets the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The SP3249E devices feature Exar's proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply. The SP3249E devices can guarantee a data rate of 250kbps fully loaded.

The SP3249E is a 5-driver/3-receiver device, ideal for portable or hand-held applications.

THEORY OF OPERATION

The SP3249E device is made up of three basic circuit blocks:

1. Drivers
2. Receivers
3. The Exar proprietary charge pump

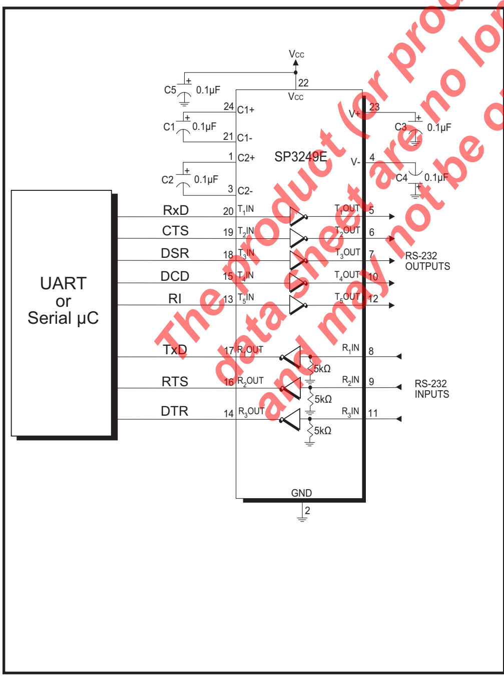


Figure 6. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232-F and all previous RS-232 versions.

The drivers can guarantee a data rate of 250kbps fully loaded with 3kΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software. All unused drivers inputs should be connected to GND or V_{CC}.

The slew rate of the driver output is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

Figure 7 shows a loopback test circuit used to test the RS-232 drivers. Figure 8 shows the test results of the loopback circuit with all five drivers active at 120kbps with typical RS-232 loads in parallel with 1000pF capacitors. Figure 9 shows the test results where one driver was active at 250kbps and all five drivers loaded with an RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data transmission rate of 120kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

Receivers

The receivers convert ±5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

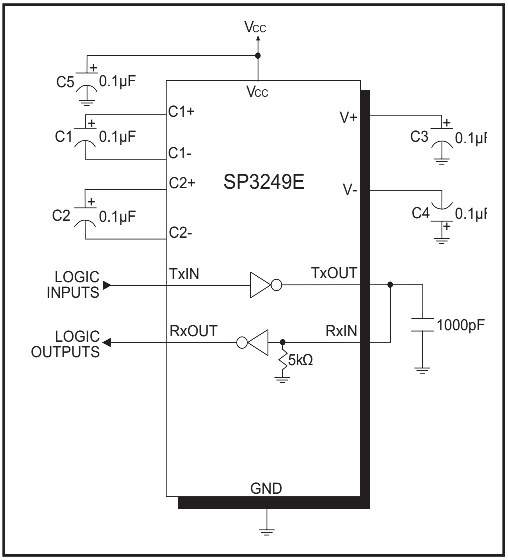


Figure 7. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

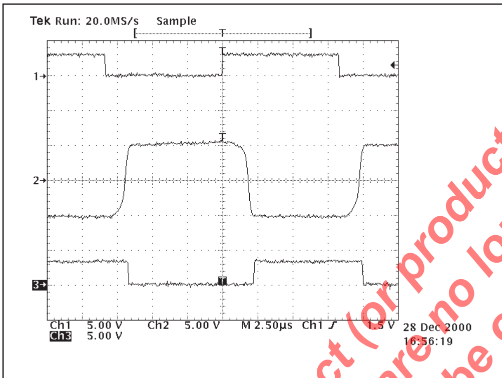


Figure 8. Loopback Test results at 120kbps (All Drivers Fully Loaded)

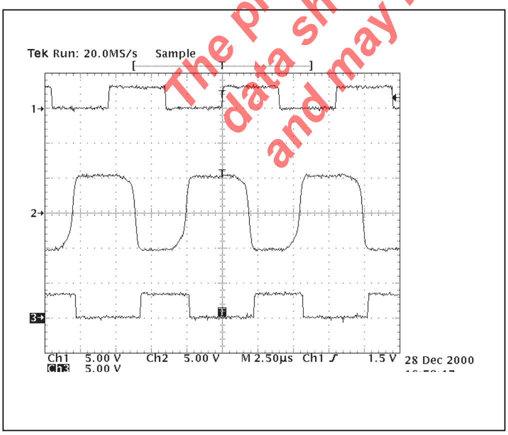


Figure 9. Loopback Test results at 250Kbps (All Drivers Fully Loaded)

Charge Pump

The charge pump is an Exar–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_l^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}, in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 500kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

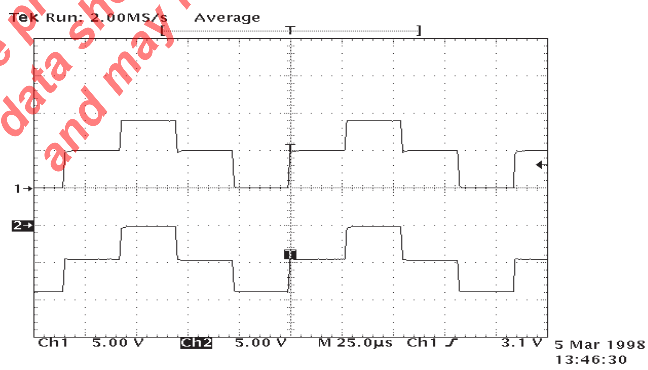


Figure 10. Charge Pump Waveform

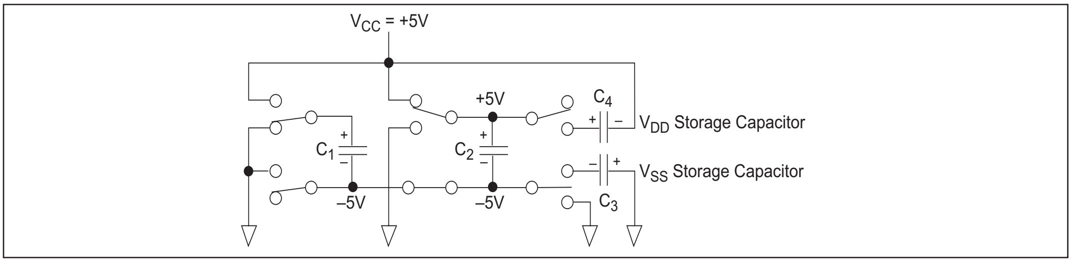


Figure 11. Charge Pump — Phase 1

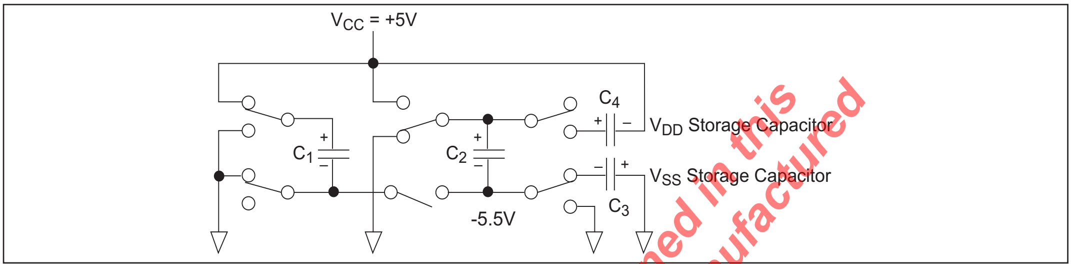


Figure 12. Charge Pump — Phase 2

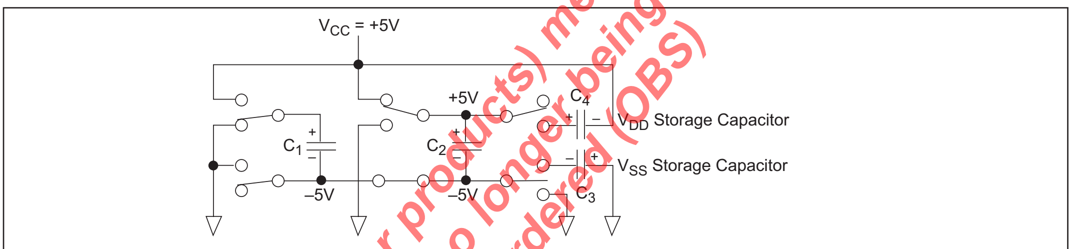


Figure 13. Charge Pump — Phase 3

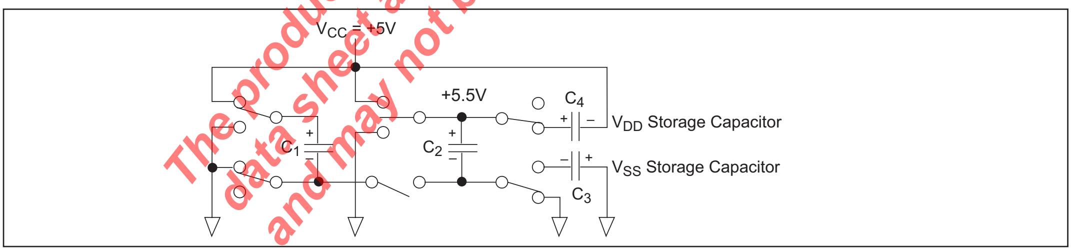


Figure 14. Charge Pump — Phase 4

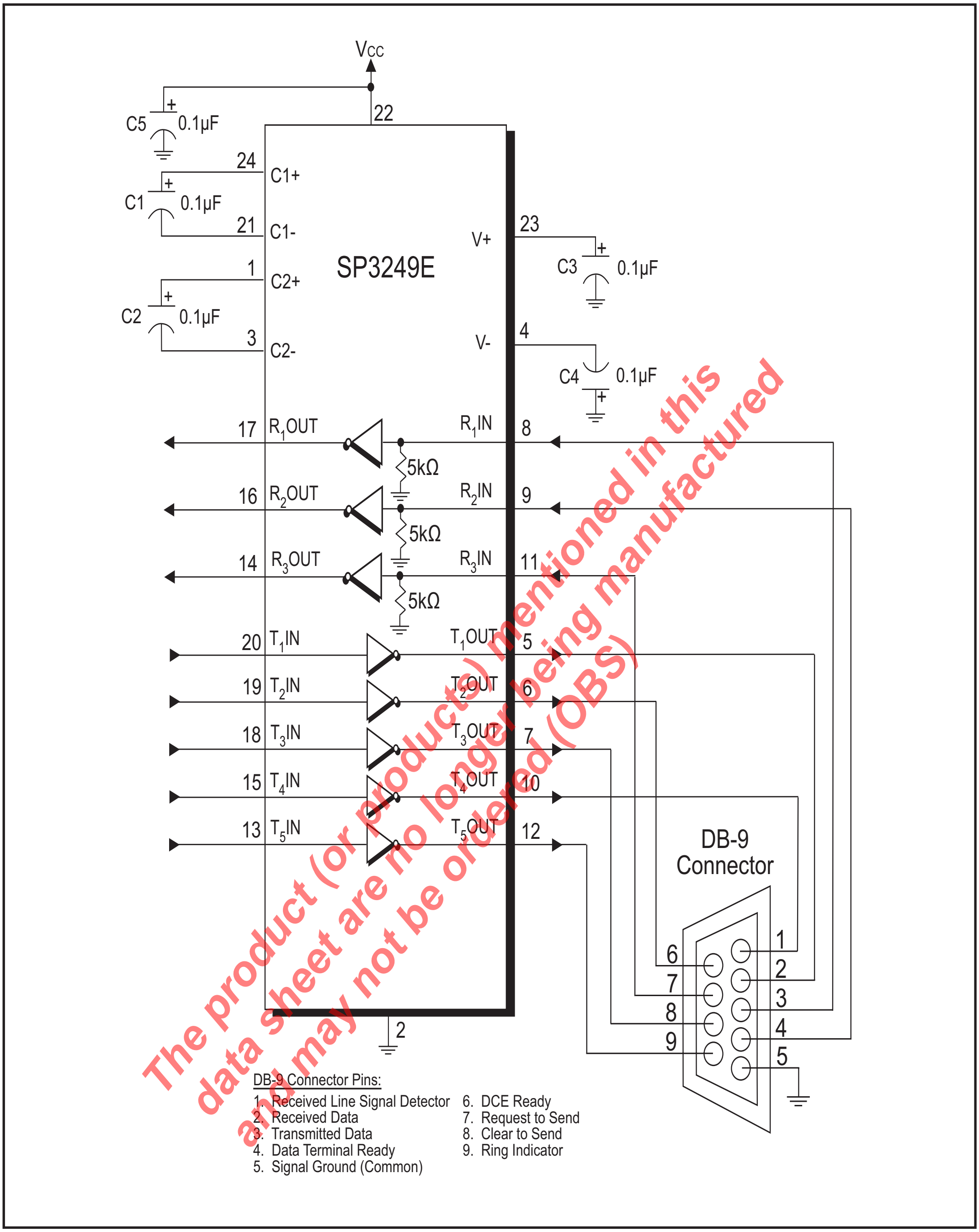


Figure 15. Circuit for the connectivity of the SP3249E with a DB-9 connector

ESD TOLERANCE

The SP3249E device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC61000-4-2 Air-Discharge
c) IEC61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 16. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the IC's tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC61000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC61000-4-2 is shown on Figure 17. There are two methods within IEC61000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

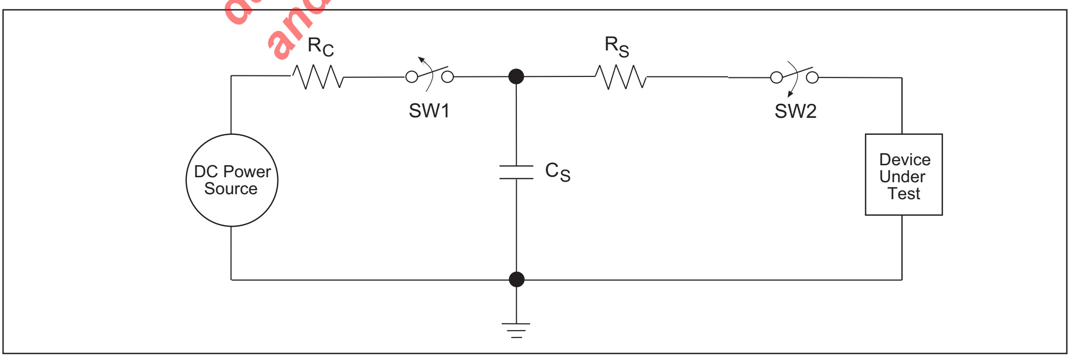


Figure 16. ESD Test Circuit for Human Body Model

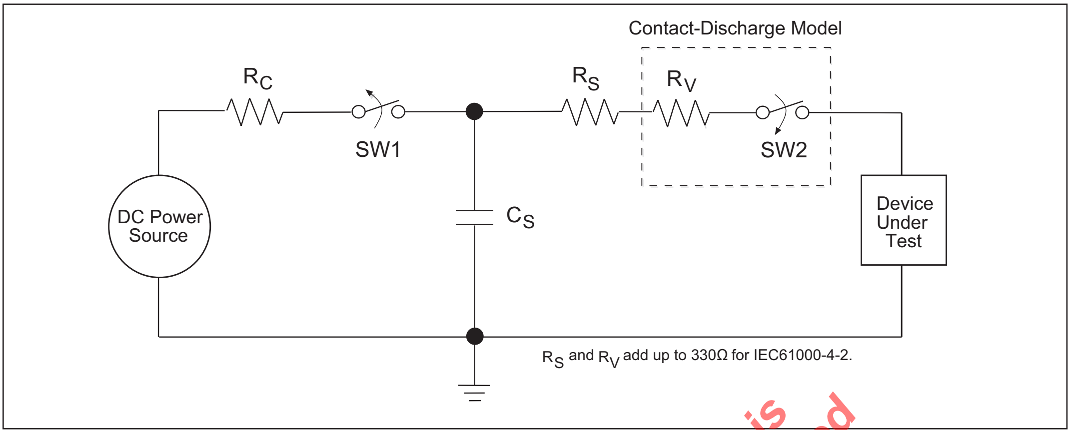


Figure 17. ESD Test Circuit for IEC61000-4-2

The circuit models in Figures 16 and 17 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

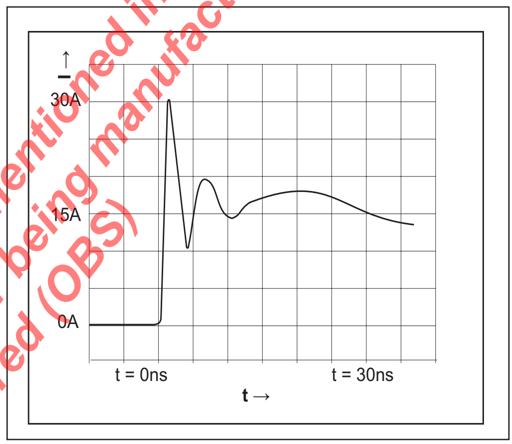
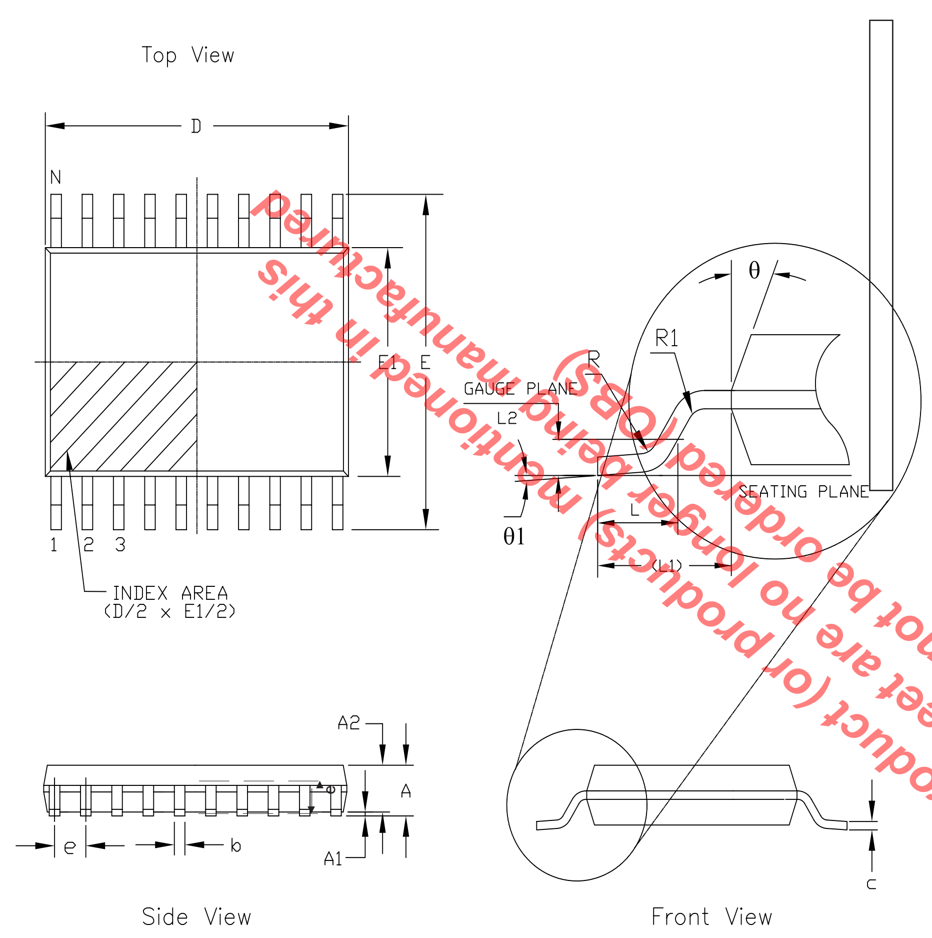


Figure 18. ESD Test Waveform for IEC61000-4-2

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC61000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs Receiver Inputs	±15kV ±15kV	±15kV ±15kV	±8kV ±8kV	4 4

Table 3. Transceiver ESD Tolerance Levels

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/19/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL



24 Pin TSSOP JEDEC MO-153 Variation AD

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R	0.09	—	—	0.035	—	—
R1	0.09	—	—	0.035	—	—
θ	12° REF			12° REF		
θ1	0°	—	8°	0°	—	8°
D	7.70	7.80	7.90	0.303	0.307	0.311
N	24			24		

EXAR	EXAR CORPORATION	
	24 PIN TSSOP PACKAGE OUTLINE	
Packaging Approval:	Drawing No:	24-PIN TSSOP
By: JL Date: 11/28/07	Revision: B	Sheet: 1 OF 1

ORDERING INFORMATION

Part Number	Temp. Range	Package
SP3249ECY-L	0C to +70C	24 Pin TSSOP
SP3249ECY-L/TR	0C to +70C	24 Pin TSSOP
SP3249EEY-L	-40C to +85C	24 Pin TSSOP
SP3249EEY-L/TR	-40C to +85C	24 Pin TSSOP

For Tape and Reel option add "/TR", Example: SP3249ECY-L/TR.

REVISION HISTORY

DATE	REVISION	DESCRIPTION
02/28/05	--	Legacy Sipex Datasheet
01/31/11	1.0.0	Convert to Exar Format, Update ordering information and change ESD specification to IEC61000-4-2

Notice

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Datasheet January 2011

For technical support please email Exar's Serial Technical Support group at : serialtechsupport@exar.com