



# THE DATASHEET OF LMV358QPWR



# LMV3xx Low-Voltage Rail-to-Rail Output Operational Amplifier

## 1 Features

- For an upgraded version - refer to [LMV321A](#), [LMV358A](#), and [LMV324A](#)
- 2.7-V and 5-V performance
- –40°C to +125°C operation
- No crossover distortion
- Low supply current
  - LMV321: 130  $\mu$ A (typical)
  - LMV358: 210  $\mu$ A (typical)
  - LMV324: 410  $\mu$ A (typical)
- Rail-to-rail output swing
- ESD protection exceeds JESD 22
  - 2000-V human-body model
  - 1000-V charged-device model

## 2 Applications

- [Desktop PCs](#)
- [HVAC: heating, ventilating, and air conditioning](#)
- [Motor control: AC induction](#)
- [Net-books](#)
- [Portable media players](#)
- [Power: telecom DC/DC module: digital](#)
- [Professional audio mixers](#)
- [Refrigerators](#)
- [Washing machines: high-end and low-end](#)

## 3 Description

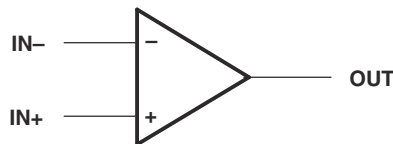
For an upgraded version with enhanced performance, please refer to [LMV321A](#), [LMV358A](#), and [LMV324A](#).

The LMV321, LMV358, and LMV324 devices are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing. These devices are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. With package sizes down to one-half the size of the DBV (SOT-23) package, these devices can be used for a variety of applications.

### Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
LMV321	Single	DBV (SOT-23, 5)	2.90 mm × 2.80 mm
		DCK (SC-70, 5)	2.00 mm × 2.10 mm
LMV358	Dual	D (SOIC, 8)	4.90 mm × 6.00 mm
		DDU (VSSOP, 8)	2.00 mm × 3.10 mm
		DGK (VSSOP, 8)	3.00 mm × 4.90 mm
		PW (TSSOP, 8)	3.00 mm × 6.40 mm
LMV324	Quad	D (SOIC, 14)	8.65 mm × 6.00 mm
		PW (TSSOP, 14)	5.00 mm × 6.40 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Simplified Schematic**



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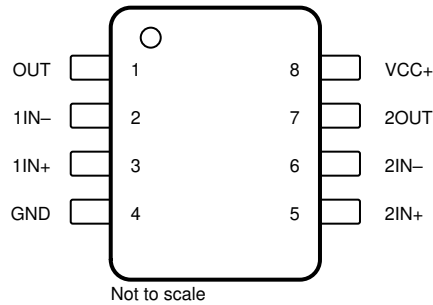
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision X (May 2020) to Revision Y (August 2023)	Page
• Updated the <i>Device Information</i> table to include channel count and package lead size.....	1

Changes from Revision W (October 2014) to Revision X (May 2020)	Page
• Deleted LMV324S mentions on the front page of the data sheet .....	1
• Added recommended device notice for LMV321A, LMV358A, and LMV324A.....	1
• Changed <i>Device Information</i> table to sort devices by channel count in ascending order.....	1
• Changed <i>Pin Configuration and Functions</i> section by dividing the Pin Functions table into separate tables per device.....	3
• Deleted LMV324S pinout information .....	3
• Changed HBM ESD voltage from 2500 V to 2000 V.....	5
• Changed CDM ESD voltage from 1500 V to 1000 V.....	5
• Deleted Shutdown voltage threshold for LMV324S.....	5
• Changed <i>Thermal Information</i> section by dividing the <i>Thermal Information</i> table into separate tables per device.....	5
• Changed Thermal Information for LMV321 .....	5
• Deleted LMV324S Thermal Information .....	5
• Changed Thermal Information for LMV324 .....	5
• Changed Thermal Information for LMV358 .....	6
• Deleted LMV324S test condition for supply current .....	6
• Changed output short-circuit current for sourcing from 60 mA to 40 mA .....	7
• Changed output short-circuit current for sinking from 160 mA to 40 mA .....	7
• Added specified by characterization table notes to output short-circuit current, output swing, and input bias current specifications .....	7

## 5 Pin Configuration and Functions

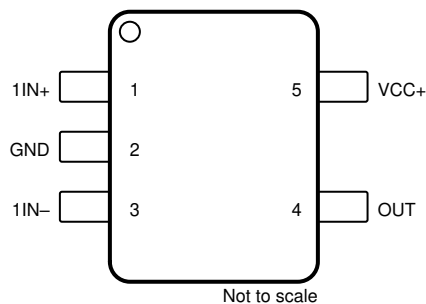


**Figure 5-1. D, DDU, DGK, and PW Packages, 8-Pin SOIC, VSSOP, and TSSOP (Top View)**

**Table 5-1. Pin Functions: LMV358**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN–	2	I	Inverting input
2IN+	5	I	Noninverting input
2IN–	6	I	Inverting input
2OUT	7	O	Output
GND	4	—	Negative supply
OUT	1	O	Output
VCC+	8	—	Positive supply

(1) I = input, O = output

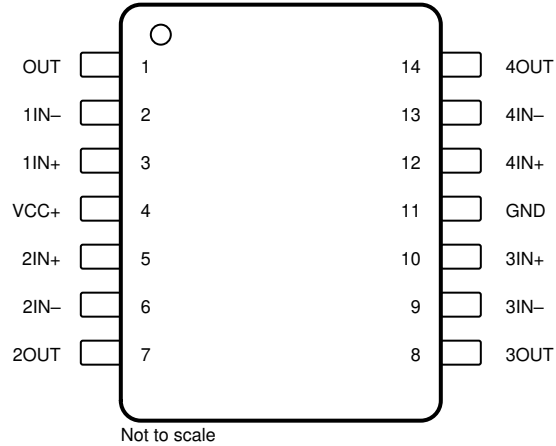


**Figure 5-2. DBV and DCK Packages, 5-Pin SOT-23 and SC-70 (Top View)**

**Table 5-2. Pin Functions: LMV321**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1IN+	1	I	Noninverting input
1IN–	3	I	Inverting input
GND	2	—	Negative supply
OUT	4	O	Output
VCC+	5	—	Positive supply

(1) I = input, O = output



**Figure 5-3. D and PW Packages, 14-Pin SOIC and TSSOP (Top View)**

**Table 5-3. Pin Functions: LMV324**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
3/4 SHDN	—	I	Shutdown (logic low ) / enable (logic high)
1/2 SHDN	—	I	Shutdown (logic low) / enable (logic high)
1IN+	3	I	Noninverting input
1IN–	2	I	Inverting input
2IN+	5	I	Noninverting input
2IN–	6	I	Inverting input
2OUT	7	O	Output
3IN+	10	I	Noninverting input
3IN–	9	I	Inverting input
3OUT	8	O	Output
4IN+	12	I	Noninverting input
4IN–	13	I	Inverting input
4OUT	14	O	Output
GND	11	—	Negative supply
OUT	1	O	OUT
VCC+	4	—	Positive supply

(1) I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		5.5	V
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>		±5.5	V
V <sub>I</sub>	Input voltage range (either input)	-0.2	5.7	V
	Duration of output short circuit (one amplifier) to ground <sup>(4)</sup>	At or below T <sub>A</sub> = 25°C, V <sub>CC</sub> ≤ 5.5 V		Unlimited
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V<sub>CC</sub> specified for the measurement of I<sub>OS</sub>) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V<sub>CC</sub> can cause excessive heating and eventual destruction.

### 6.2 ESD Ratings

		MIN	MAX	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge			V
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage (single-supply operation)	2.7	5.5	V	
T <sub>A</sub>	Operating free-air temperature	I temperature (LMV321, LMV358, LMV324, LMV321IDCK)	-40	125	°C
		Q temperature	-40	125	

### 6.4 Thermal Information: LMV321

THERMAL METRIC <sup>(1)</sup>	LMV321		UNIT	
	DBV (SOT-23)	DCK (SC-70)		
	5 PINS	5 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	232.9	239.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.5 Thermal Information: LMV324

THERMAL METRIC <sup>(1)</sup>	LMV324		UNIT	
	D (SOIC)	PW (TSSOP)		
	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	102.1	148.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Thermal Information: LMV358

THERMAL METRIC <sup>(1)</sup>	LMV358				UNIT
	D (SOIC)	DGK (VSSOP)	DDU (VSSOP)	PW (TSSOP)	
	8 PINS	8 PINS	8 PINS	8 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	207.9	201.2	210	200.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.7 Electrical Characteristics: V<sub>CC+</sub> = 2.7 V

V<sub>CC+</sub> = 2.7 V, T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IO</sub> Input offset voltage			1.7	7	mV
α <sub>VIO</sub> Average temperature coefficient of input offset voltage			5		μV/°C
I <sub>IB</sub> Input bias current			11	250	nA
I <sub>IO</sub> Input offset current			5	50	nA
CMRR Common-mode rejection ratio	V <sub>CM</sub> = 0 to 1.7 V	50	63		dB
k <sub>SVR</sub> Supply-voltage rejection ratio	V <sub>CC</sub> = 2.7 V to 5 V, V <sub>O</sub> = 1 V	50	60		dB
V <sub>ICR</sub> Common-mode input voltage range	CMRR ≥ 50 dB	0	-0.2		V
			1.9	1.7	
V <sub>O</sub> Output swing	R <sub>L</sub> = 10 kΩ to 1.35 V	High level	V <sub>CC</sub> - 100	V <sub>CC</sub> - 10	mV
		Low level		60	
I <sub>CC</sub> Supply current	LMV321I		80	170	μA
	LMV358I (both amplifiers)		140	340	
	LMV324I (all four amplifiers)		260	680	
B <sub>1</sub> Unity-gain bandwidth	C <sub>L</sub> = 200 pF		1		MHz
Φ <sub>m</sub> Phase margin			60		deg
G <sub>m</sub> Gain margin			10		dB
V <sub>n</sub> Equivalent input noise voltage	f = 1 kHz		46		nV/√Hz
I <sub>n</sub> Equivalent input noise current	f = 1 kHz		0.17		pA/√Hz

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

## 6.8 Electrical Characteristics: $V_{CC+} = 5\text{ V}$

$V_{CC+} = 5\text{ V}$ , at specified free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT		
$V_{IO}$	Input offset voltage	$T_A = 25^\circ\text{C}$		1.7	7	mV	
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			9		
$\alpha_{VIO}$	Average temperature coefficient of input offset voltage	$T_A = 25^\circ\text{C}$		5		$\mu\text{V}/^\circ\text{C}$	
$I_{IB}$	Input bias current	$T_A = 25^\circ\text{C}$		15	250 <sup>(1)</sup>	nA	
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			500 <sup>(1)</sup>		
$I_{IO}$	Input offset current	$T_A = 25^\circ\text{C}$		5	50 <sup>(1)</sup>	nA	
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$			150 <sup>(1)</sup>		
CMRR	Common-mode rejection ratio	$V_{CM} = 0\text{ to } 4\text{ V}$ $T_A = 25^\circ\text{C}$		50	65	dB	
$k_{SVR}$	Supply-voltage rejection ratio	$V_{CC} = 2.7\text{ V to } 5\text{ V}$ , $V_O = 1\text{ V}$ , $V_{CM} = 1\text{ V}$ $T_A = 25^\circ\text{C}$		50	60	dB	
$V_{ICR}$	Common-mode input voltage range	CMRR $\geq 50\text{ dB}$ , $T_A = 25^\circ\text{C}$		0	-0.2	V	
					4.2		4
$V_O$	Output swing	$R_L = 2\text{ k}\Omega\text{ to } 2.5\text{ V}$ , high level, $T_A = 25^\circ\text{C}$		$V_{CC} - 300$	$V_{CC} - 40$	mV	
		$R_L = 2\text{ k}\Omega\text{ to } 2.5\text{ V}$ , high level, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$		$V_{CC} - 400$ <sup>(1)</sup>			
		$T_A = 25^\circ\text{C}$ , low level			120		300
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$ , low level					400 <sup>(1)</sup>
		$R_L = 10\text{ k}\Omega\text{ to } 2.5\text{ V}$ , high level, $T_A = 25^\circ\text{C}$		$V_{CC} - 100$	$V_{CC} - 10$		
		$R_L = 10\text{ k}\Omega\text{ to } 2.5\text{ V}$ , high level, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$		$V_{CC} - 200$ <sup>(1)</sup>			
		$T_A = 25^\circ\text{C}$ , low level			65		180
$A_{VD}$	Large-signal differential voltage gain	$R_L = 2\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$		15	100	V/mV	
		$R_L = 2\text{ k}\Omega$ , $T_A = -40^\circ\text{C to } +125^\circ\text{C}$		10 <sup>(1)</sup>			
$I_{OS}$	Output short-circuit current	Sourcing, $V_O = 0\text{ V}$ , $T_A = 25^\circ\text{C}$		5 <sup>(1)</sup>	40	mA	
		Sinking, $V_O = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		10 <sup>(1)</sup>	40		
$I_{CC}$	Supply current	LMV321I, $T_A = 25^\circ\text{C}$		130	250	$\mu\text{A}$	
		LMV321I, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$			350		
		LMV358I (both amplifiers), $T_A = 25^\circ\text{C}$		210	440		
		LMV358I (both amplifiers), $T_A = -40^\circ\text{C to } +125^\circ\text{C}$			615		
		LMV324I (all four amplifiers), $T_A = 25^\circ\text{C}$		410	830		
		LMV324I (all four amplifiers), $T_A = -40^\circ\text{C to } +125^\circ\text{C}$			1160		
$B_1$	Unity-gain bandwidth	$C_L = 200\text{ pF}$ , $T_A = 25^\circ\text{C}$		1		MHz	
$\Phi_m$	Phase margin	$T_A = 25^\circ\text{C}$		60		deg	
$G_m$	Gain margin	$T_A = 25^\circ\text{C}$		10		dB	
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$ , $T_A = 25^\circ\text{C}$		39		$\text{nV}/\sqrt{\text{Hz}}$	
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$ , $T_A = 25^\circ\text{C}$		0.21		$\text{pA}/\sqrt{\text{Hz}}$	
SR	Slew rate	$T_A = 25^\circ\text{C}$		1		$\text{V}/\mu\text{s}$	

(1) Specified by characterization. Not production tested.

## 6.9 Typical Characteristics

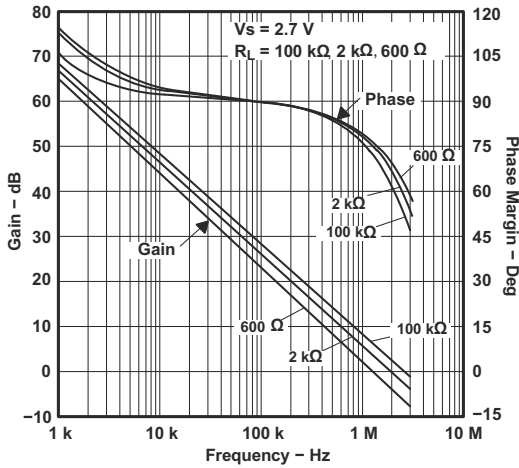


Figure 6-1. LMV321 Frequency Response vs Resistive Load

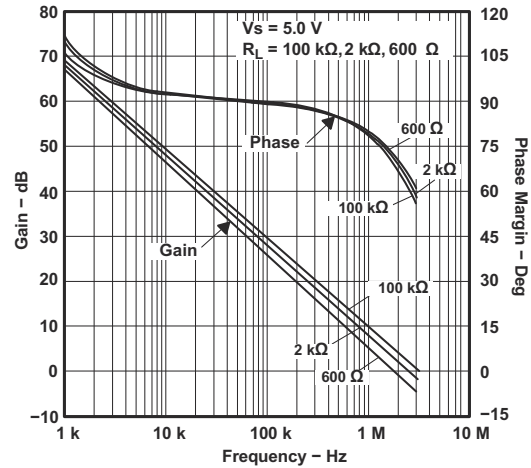


Figure 6-2. LMV321 Frequency Response vs Resistive Load

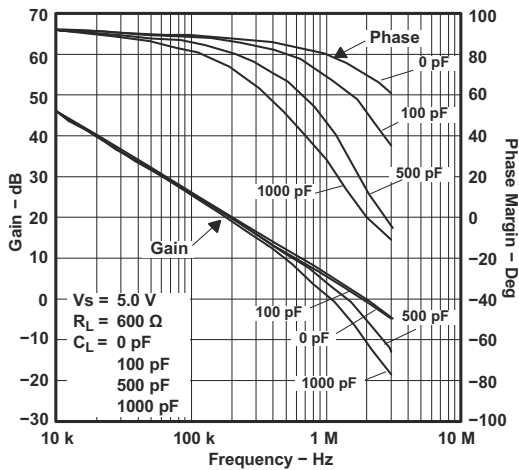


Figure 6-3. LMV321 Frequency Response vs Capacitive Load

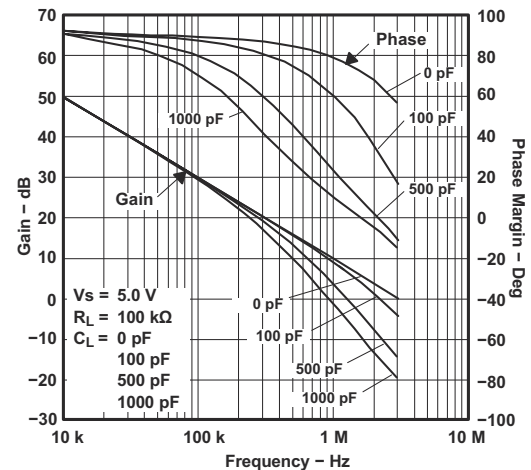


Figure 6-4. LMV321 Frequency Response vs Capacitive Load

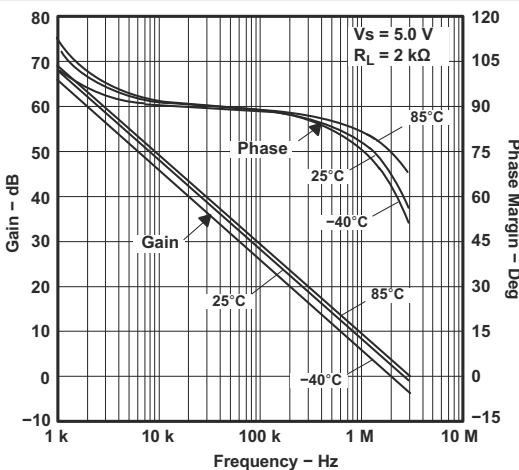


Figure 6-5. LMV321 Frequency Response vs Temperature

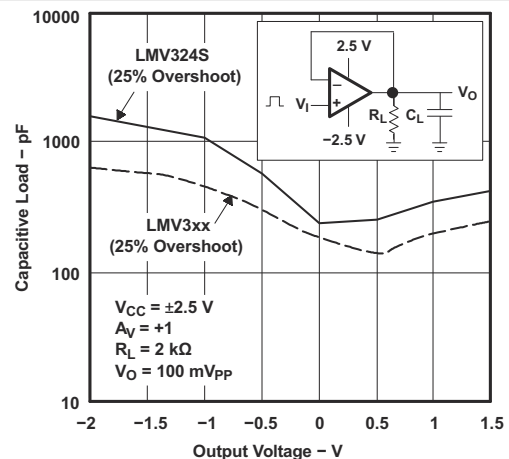


Figure 6-6. Stability vs Capacitive Load

### 6.9 Typical Characteristics (continued)

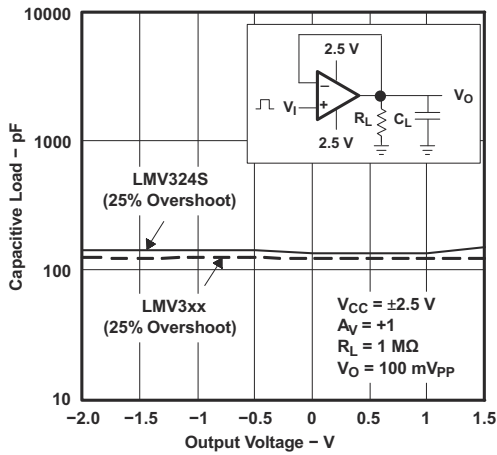


Figure 6-7. Stability vs Capacitive Load

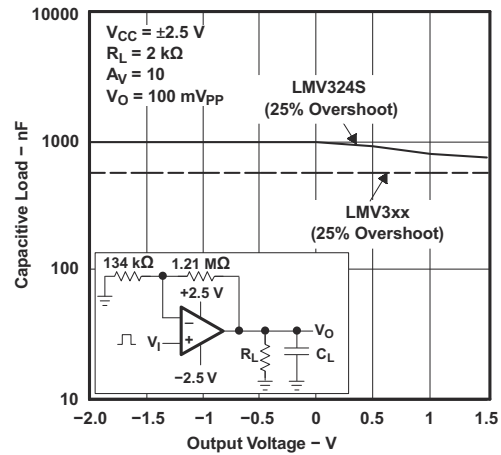


Figure 6-8. Stability vs Capacitive Load

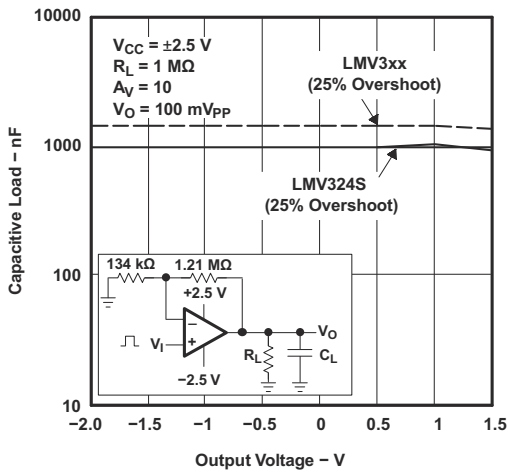


Figure 6-9. Stability vs Capacitive Load

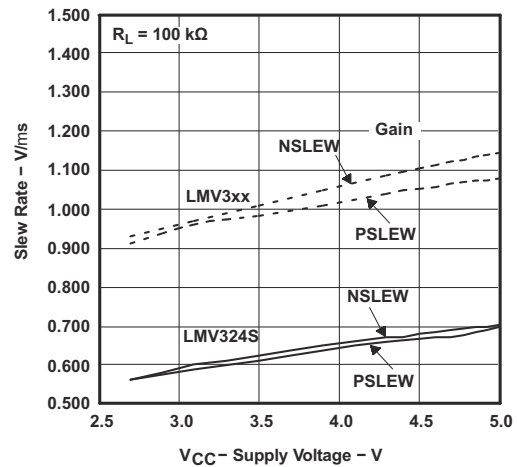


Figure 6-10. Slew Rate vs Supply Voltage

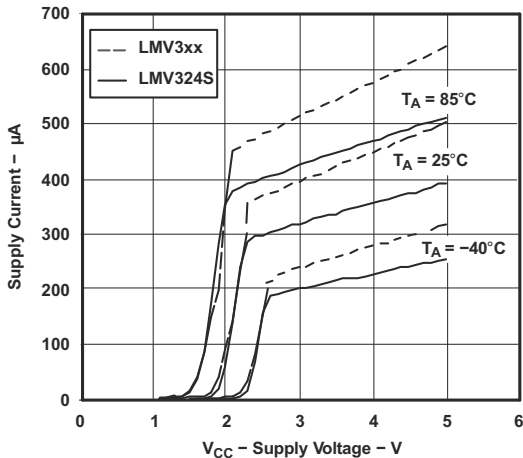


Figure 6-11. Supply Current vs Supply Voltage: Quad Amplifier

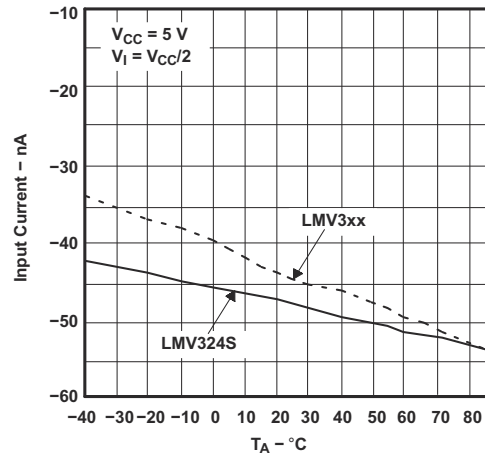


Figure 6-12. Input Current vs Temperature

## 6.9 Typical Characteristics (continued)

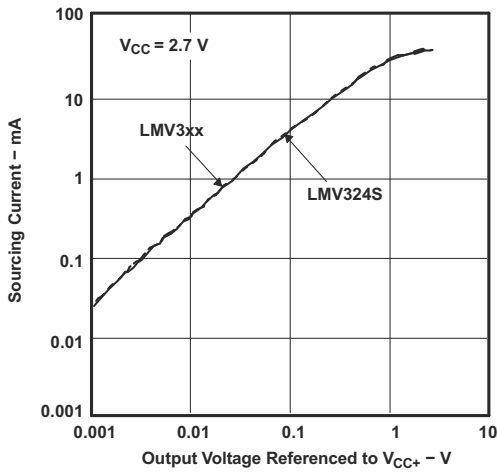


Figure 6-13. Source Current vs Output Voltage

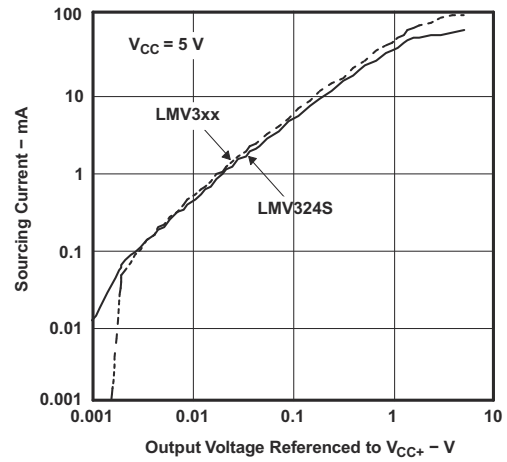


Figure 6-14. Source Current vs Output Voltage

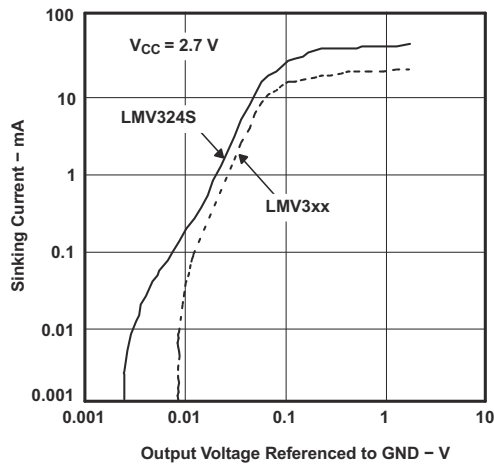


Figure 6-15. Sinking Current vs Output Voltage

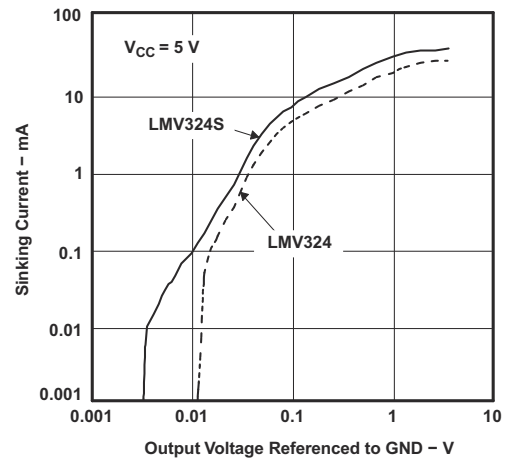


Figure 6-16. Sinking Current vs Output Voltage

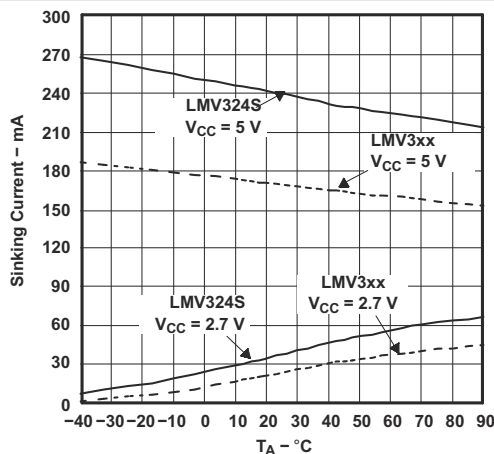


Figure 6-17. Short-Circuit Current vs Temperature

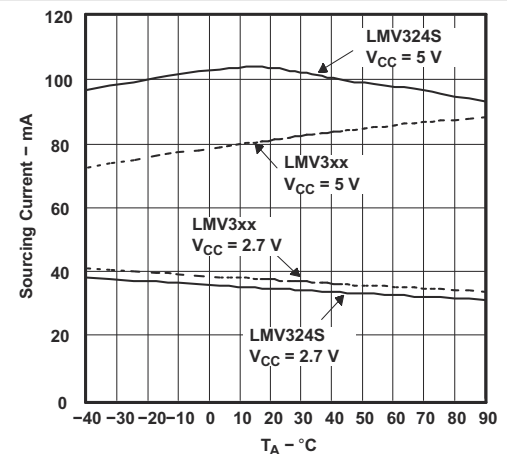


Figure 6-18. Short-Circuit Current vs Temperature

### 6.9 Typical Characteristics (continued)

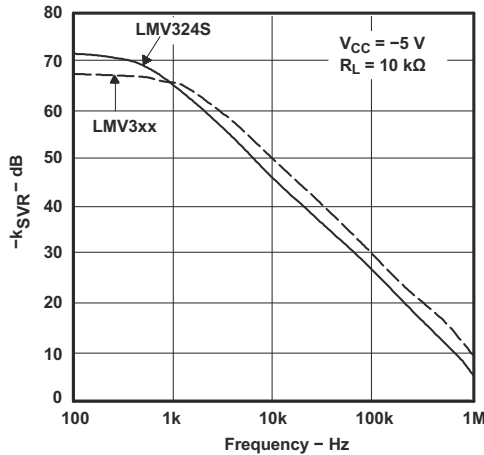


Figure 6-19.  $-k_{SVR}$  vs Frequency

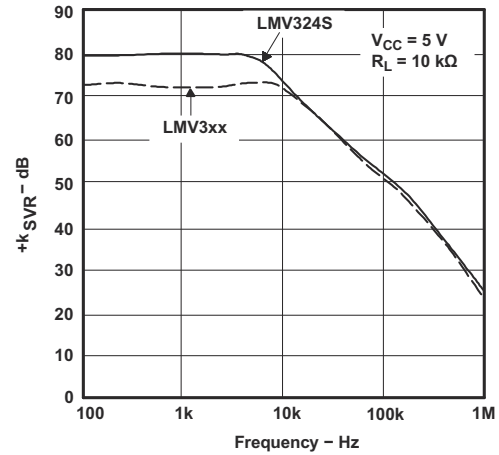


Figure 6-20.  $+k_{SVR}$  vs Frequency

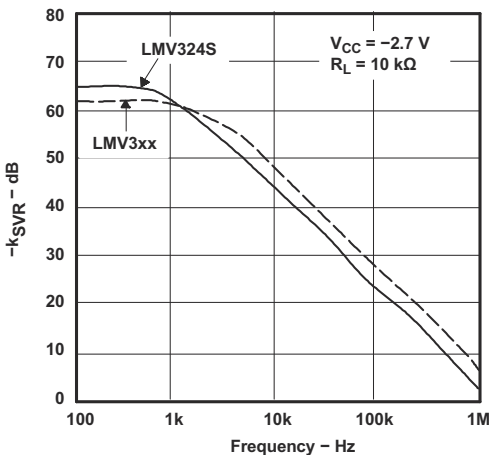


Figure 6-21.  $-k_{SVR}$  vs Frequency

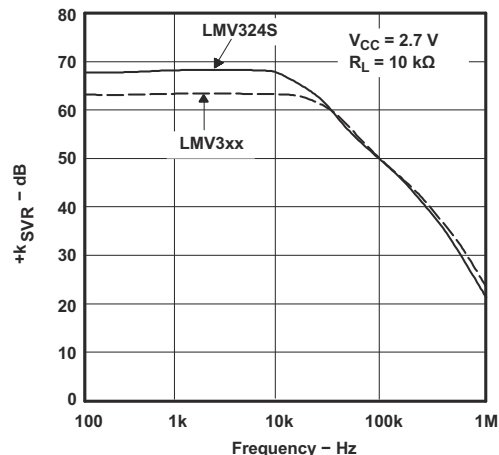


Figure 6-22.  $+k_{SVR}$  vs Frequency

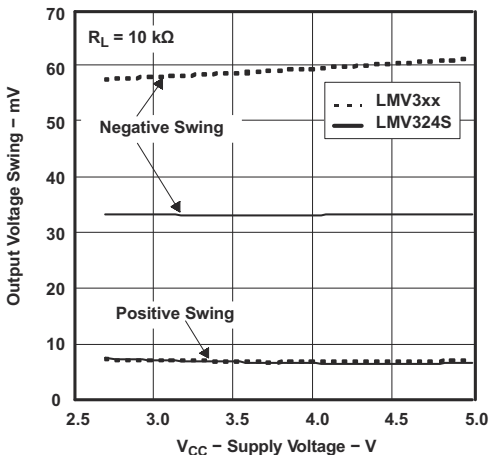


Figure 6-23. Output Voltage Swing From Rails vs Supply Voltage

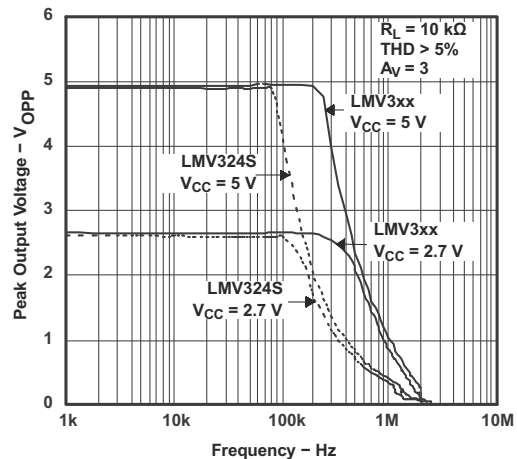


Figure 6-24. Output Voltage vs Frequency

## 6.9 Typical Characteristics (continued)

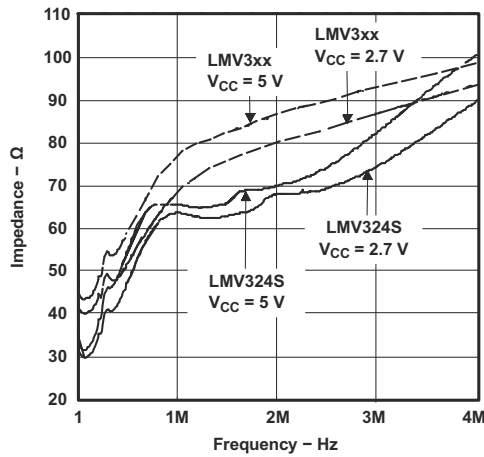


Figure 6-25. Open-Loop Output Impedance vs Frequency

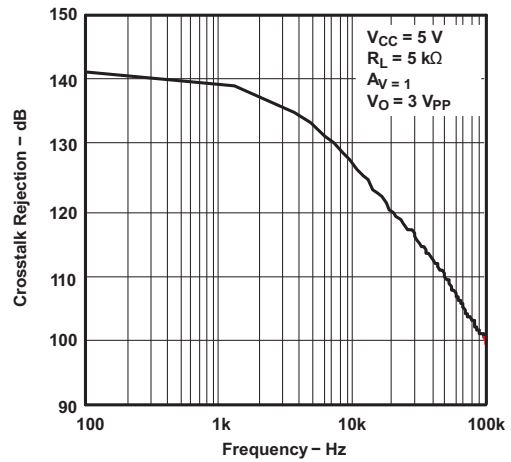


Figure 6-26. Cross-Talk Rejection vs Frequency

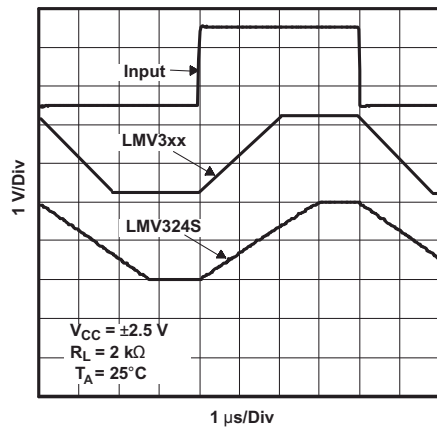


Figure 6-27. Noninverting Large-Signal Pulse Response

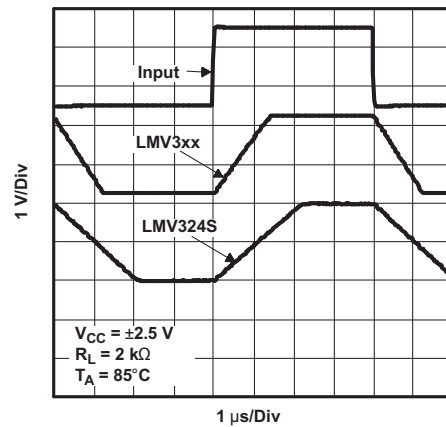


Figure 6-28. Noninverting Large-Signal Pulse Response

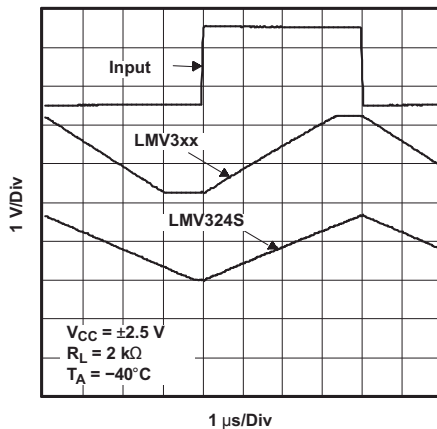


Figure 6-29. Noninverting Large-Signal Pulse Response

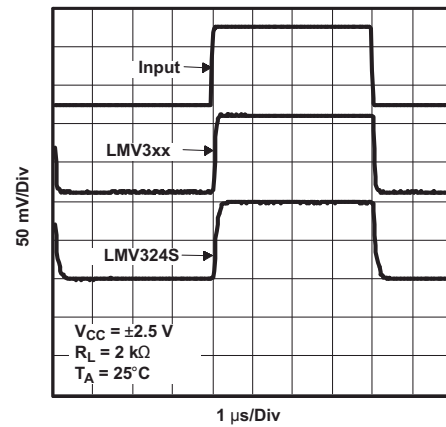


Figure 6-30. Noninverting Small-Signal Pulse Response

## 6.9 Typical Characteristics (continued)

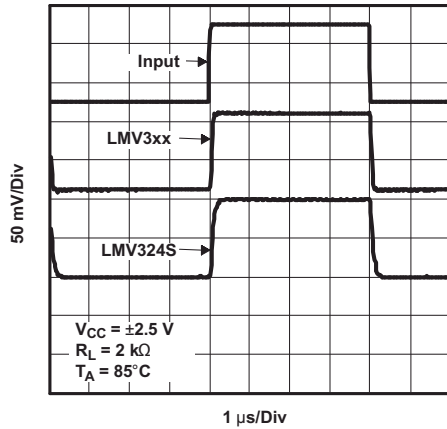


Figure 6-31. Noninverting Small-Signal Pulse Response

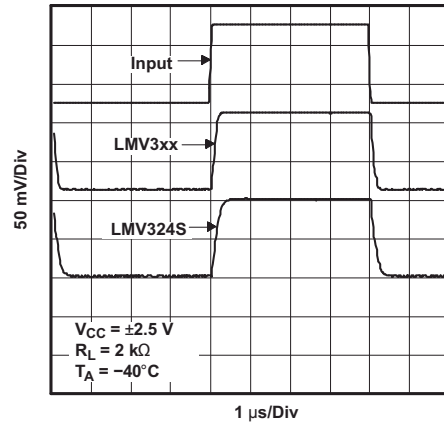


Figure 6-32. Noninverting Small-Signal Pulse Response

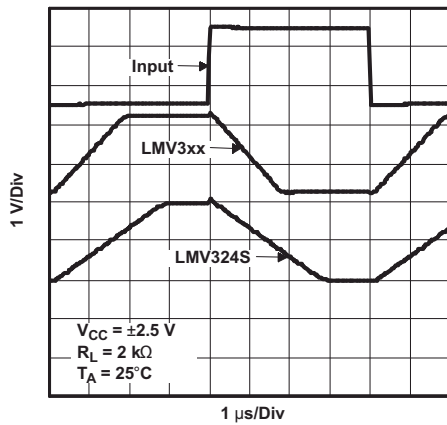


Figure 6-33. Inverting Large-Signal Pulse Response

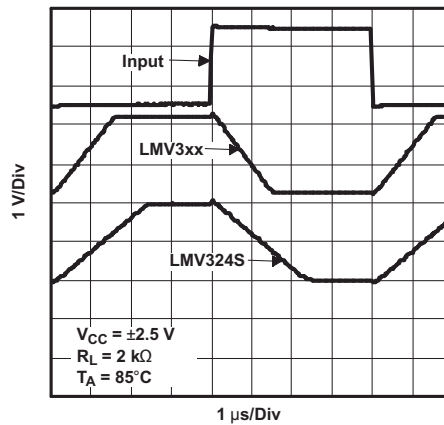


Figure 6-34. Inverting Large-Signal Pulse Response

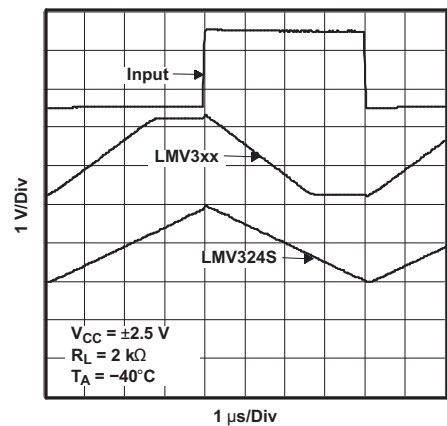


Figure 6-35. Inverting Large-Signal Pulse Response

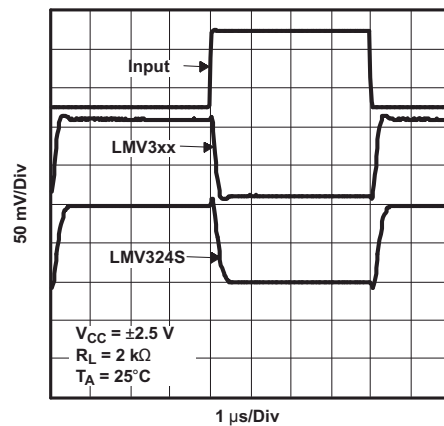


Figure 6-36. Inverting Small-Signal Pulse Response

## 6.9 Typical Characteristics (continued)

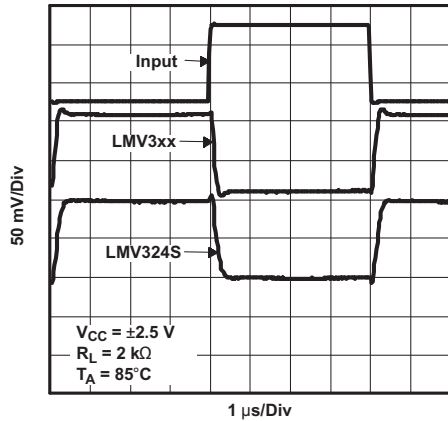


Figure 6-37. Inverting Small-Signal Pulse Response

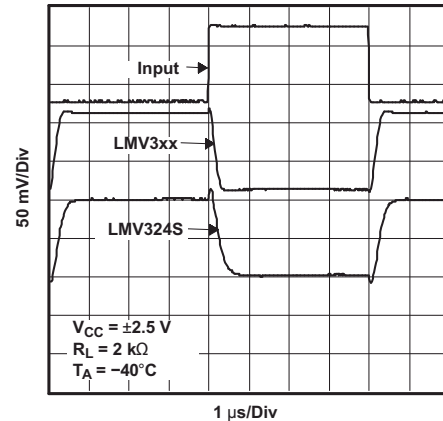


Figure 6-38. Inverting Small-Signal Pulse Response

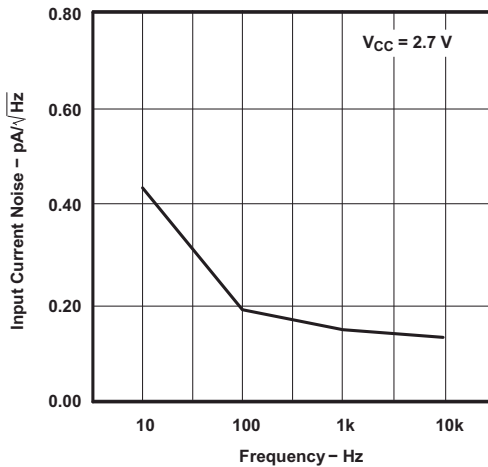


Figure 6-39. Input Current Noise vs Frequency

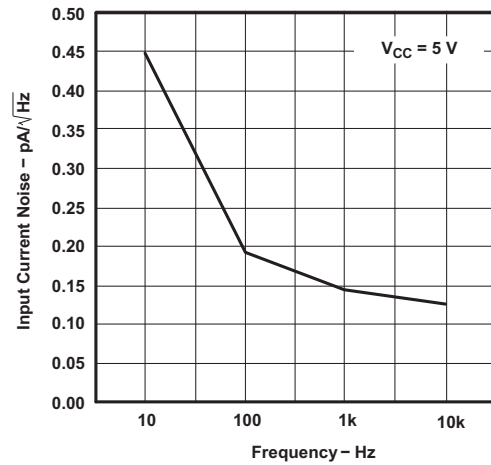


Figure 6-40. Input Current Noise vs Frequency

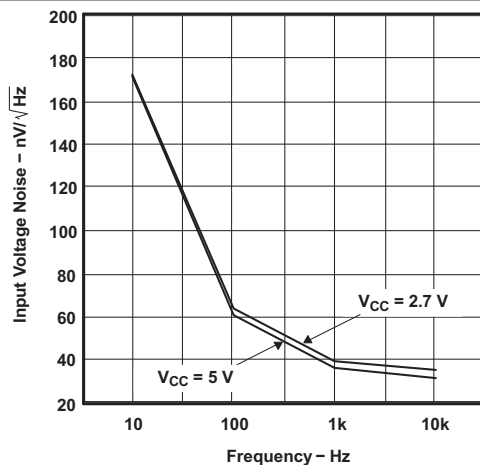


Figure 6-41. Input Voltage Noise vs Frequency

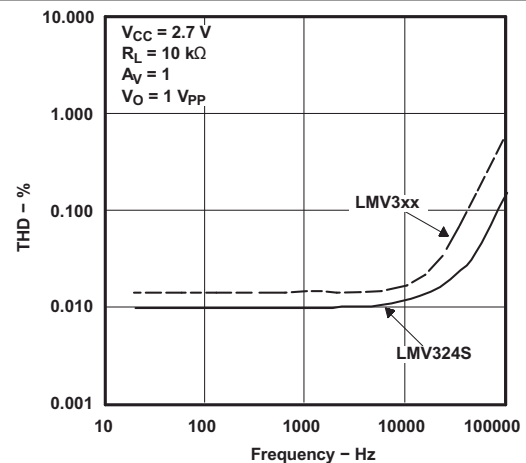


Figure 6-42. THD + N vs Frequency

## 6.9 Typical Characteristics (continued)

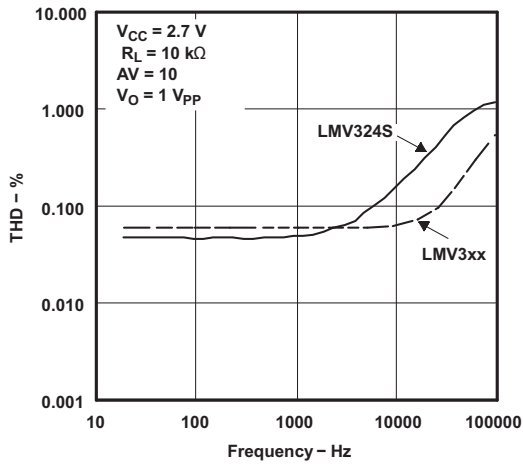


Figure 6-43. THD + N vs Frequency

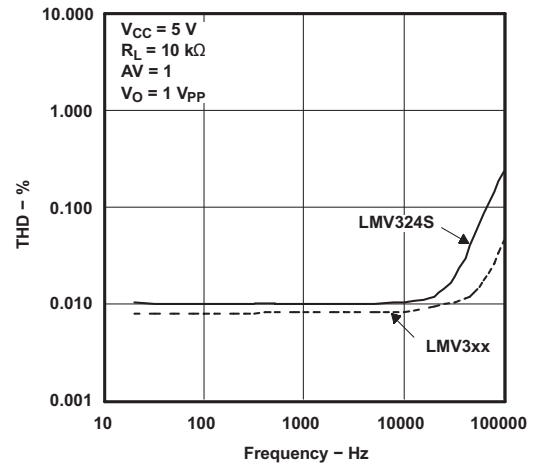


Figure 6-44. THD + N vs Frequency

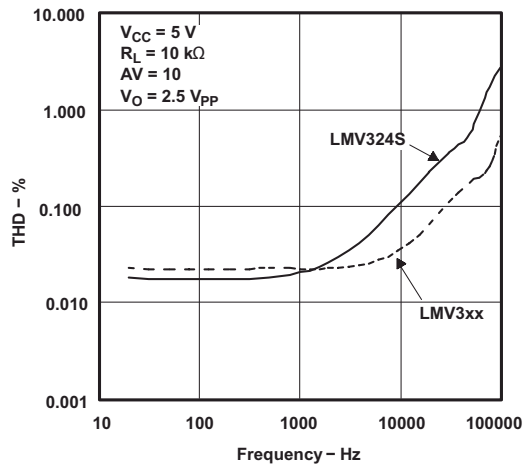


Figure 6-45. THD + N vs Frequency



## 7.3 Feature Description

### 7.3.1 Operating Voltage

The LMV321, LMV358, and LMV324 devices are fully specified and ensured for operation from 2.7 V to 5 V. In addition, many specifications apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* graphs.

### 7.3.2 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The LMV321, LMV358, LMV324 devices have a 1-MHz unity-gain bandwidth.

### 7.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The LMV321, LMV358, LMV324 devices have a 1-V/ $\mu\text{s}$  slew rate.

## 7.4 Device Functional Modes

The LMV321, LMV358, LMV324 devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

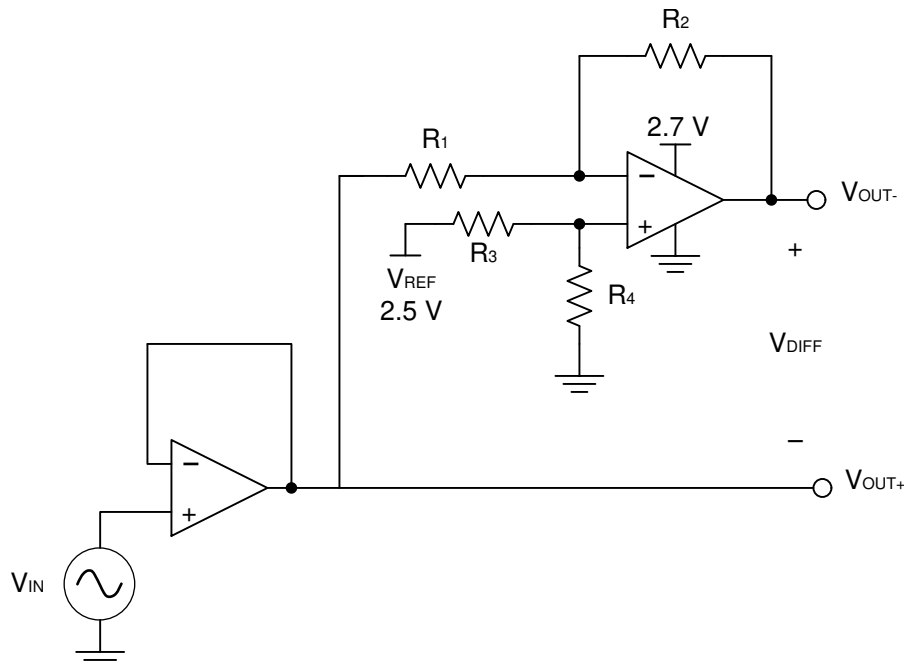
## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Typical Application

Some applications require differential signals. [Figure 8-1](#) shows a simple circuit to convert a single-ended input of 0.5 to 2 V into differential output of  $\pm 1.5$  V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage,  $V_{OUT+}$ . The second amplifier inverts the input and adds a reference voltage to generate  $V_{OUT-}$ . Both  $V_{OUT+}$  and  $V_{OUT-}$  range from 0.5 to 2 V. The difference,  $V_{DIFF}$ , is the difference between  $V_{OUT+}$  and  $V_{OUT-}$ . The LMV358 was used to build this circuit.



**Figure 8-1. Schematic for Single-Ended Input to Differential Output Conversion**

### 8.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 2.7 V
- Reference voltage: 2.5 V
- Input: 0.5 to 2 V
- Output differential:  $\pm 1.5$  V

### 8.1.2 Detailed Design Procedure

The circuit in [Figure 8-1](#) takes a single-ended input signal,  $V_{IN}$ , and generates two output signals,  $V_{OUT+}$  and  $V_{OUT-}$  using two amplifiers and a reference voltage,  $V_{REF}$ .  $V_{OUT+}$  is the output of the first amplifier and is a buffered version of the input signal,  $V_{IN}$  (see [Equation 1](#)).  $V_{OUT-}$  is the output of the second amplifier which uses  $V_{REF}$  to add an offset voltage to  $V_{IN}$  and feedback to add inverting gain. The transfer function for  $V_{OUT-}$  is [Equation 2](#).

$$V_{OUT+} = V_{IN} \quad (1)$$

$$V_{OUT-} = V_{REF} \times \left( \frac{R_4}{R_3 + R_4} \right) \times \left( 1 + \frac{R_2}{R_1} \right) - V_{IN} \times \frac{R_2}{R_1} \quad (2)$$

The differential output signal,  $V_{DIFF}$ , is the difference between the two single-ended output signals,  $V_{OUT+}$  and  $V_{OUT-}$ . [Equation 3](#) shows the transfer function for  $V_{DIFF}$ . By applying the conditions that  $R_1 = R_2$  and  $R_3 = R_4$ , the transfer function is simplified into [Equation 6](#). Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the  $V_{REF}$ . The differential output range is  $2 \times V_{REF}$ . Furthermore, the common mode voltage will be one half of  $V_{REF}$  (see [Equation 7](#)).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left( 1 + \frac{R_2}{R_1} \right) - V_{REF} \times \left( \frac{R_4}{R_3 + R_4} \right) \left( 1 + \frac{R_2}{R_1} \right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{cm} = \left( \frac{V_{OUT+} + V_{OUT-}}{2} \right) = \frac{1}{2} V_{REF} \quad (7)$$

#### 8.1.2.1 Amplifier Selection

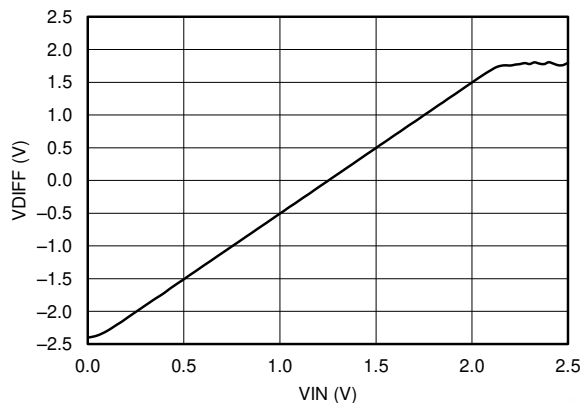
Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because LMV358 has a bandwidth of 1 MHz, this circuit will only be able to process signals with frequencies of less than 1 MHz.

#### 8.1.2.2 Passive Component Selection

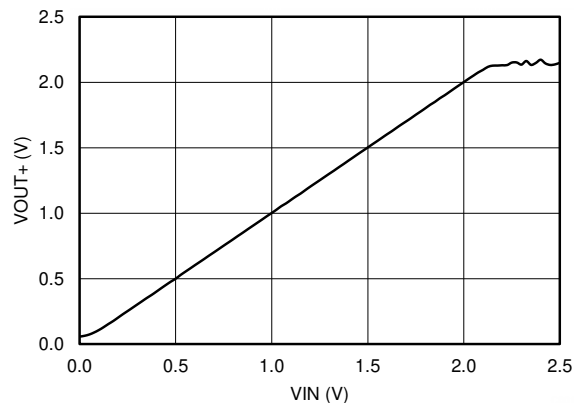
Because the transfer function of  $V_{OUT-}$  is heavily reliant on resistors ( $R_1$ ,  $R_2$ ,  $R_3$ , and  $R_4$ ), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 k $\Omega$  with tolerances measured to be within 2%. If the noise of the system is a key parameter, the user can select smaller resistance values (6 k $\Omega$  or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

### 8.1.3 Application Curves

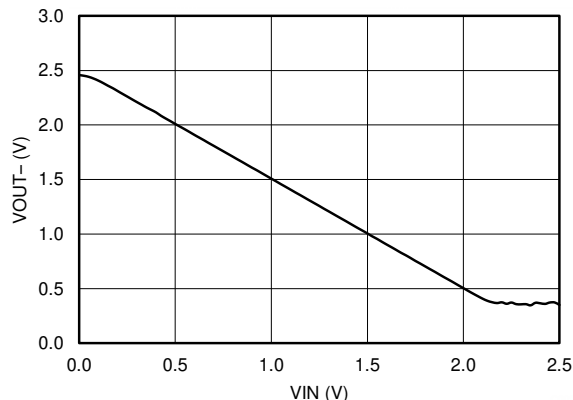
The measured transfer functions in [Figure 8-2](#), [Figure 8-3](#), and [Figure 8-4](#) were generated by sweeping the input voltage from 0 V to 2.5 V. However, this design should only be used between 0.5 V and 2 V for optimum linearity.



**Figure 8-2. Differential Output Voltage vs Input Voltage**



**Figure 8-3. Positive Output Voltage Node vs Input Voltage**



**Figure 8-4. Positive Output Voltage Node vs Input Voltage**

### 8.2 Power Supply Recommendations

The LMV321, LMV358, LMV324 devices are specified for operation from 2.7 to 5 V; many specifications apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

#### CAUTION

Supply voltages larger than 5.5 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout section](#).

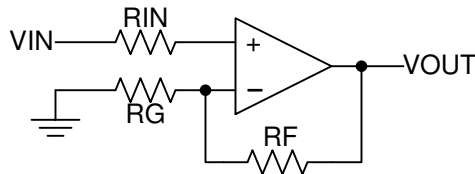
## 8.3 Layout

### 8.3.1 Layout Guidelines

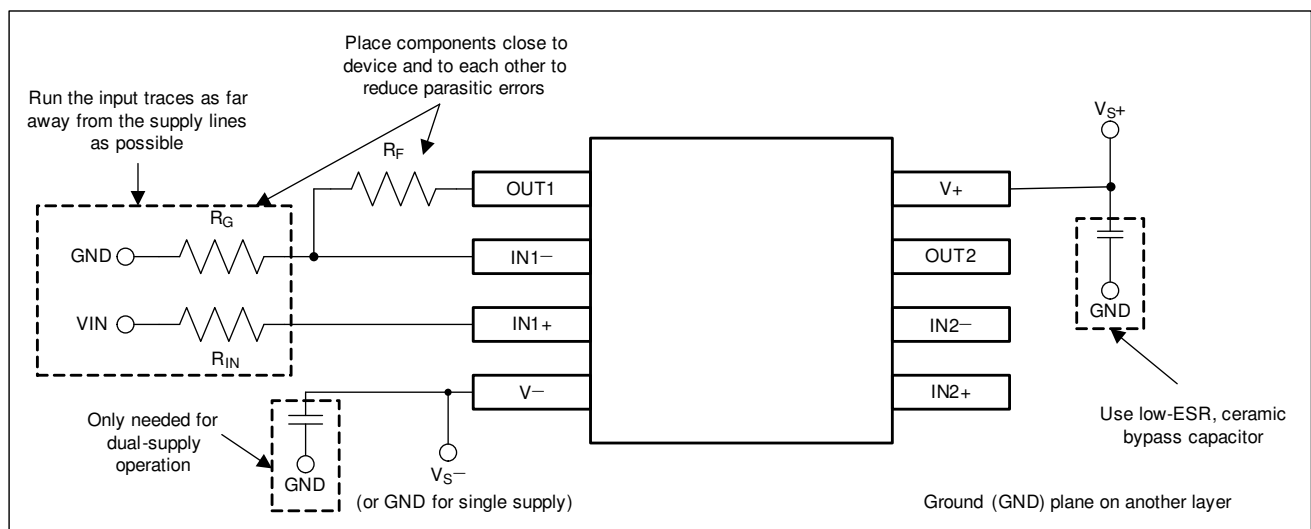
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V+$  to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Ensure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping  $R_F$  and  $R_G$  close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 8.3.2 Layout Example



**Figure 8-5. Operational Amplifier Schematic for Noninverting Configuration**



**Figure 8-6. Operational Amplifier Board Layout for Noninverting Configuration**

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV321IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RC1F	<a href="#">Samples</a>
LMV321IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RC1F	<a href="#">Samples</a>
LMV321IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RC1F	<a href="#">Samples</a>
LMV321IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RC1F	<a href="#">Samples</a>
LMV321IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU   SN   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(R3F, R3K, R3O, R3 R, R3Z)	<a href="#">Samples</a>
LMV321IDCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	(R3F, R3K, R3O, R3 R, R3Z)	<a href="#">Samples</a>
LMV321IDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU   SN   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(R3C, R3F, R3R)	<a href="#">Samples</a>
LMV324IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LMV324I	<a href="#">Samples</a>
LMV324IDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324I	<a href="#">Samples</a>
LMV324IDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324I	<a href="#">Samples</a>
LMV324IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	MV324I	<a href="#">Samples</a>
LMV324IPWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324I	<a href="#">Samples</a>
LMV324IPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324I	<a href="#">Samples</a>
LMV324QDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	<a href="#">Samples</a>
LMV324QDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	<a href="#">Samples</a>
LMV324QPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	MV324Q	<a href="#">Samples</a>
LMV324QPWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	MV324Q	<a href="#">Samples</a>
LMV358IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(R5B, R5Q, R5R)	<a href="#">Samples</a>
LMV358IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(R5B, R5Q, R5R)	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV358IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	MV358I	<a href="#">Samples</a>
LMV358IDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	<a href="#">Samples</a>
LMV358IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	<a href="#">Samples</a>
LMV358IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	MV358I	<a href="#">Samples</a>
LMV358IPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	<a href="#">Samples</a>
LMV358QDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(RHO, RHR)	<a href="#">Samples</a>
LMV358QDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(RHO, RHR)	<a href="#">Samples</a>
LMV358QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358Q	<a href="#">Samples</a>
LMV358QPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	MV358Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

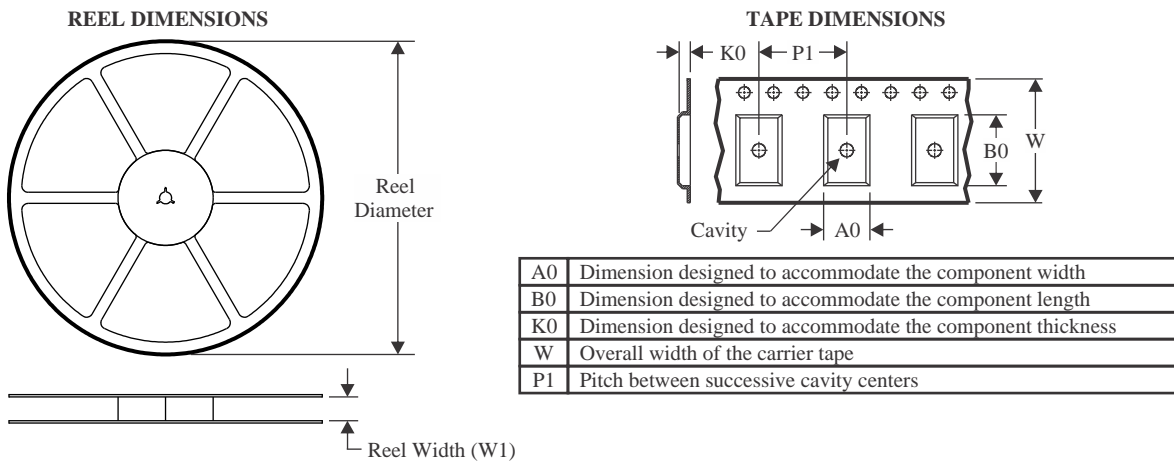
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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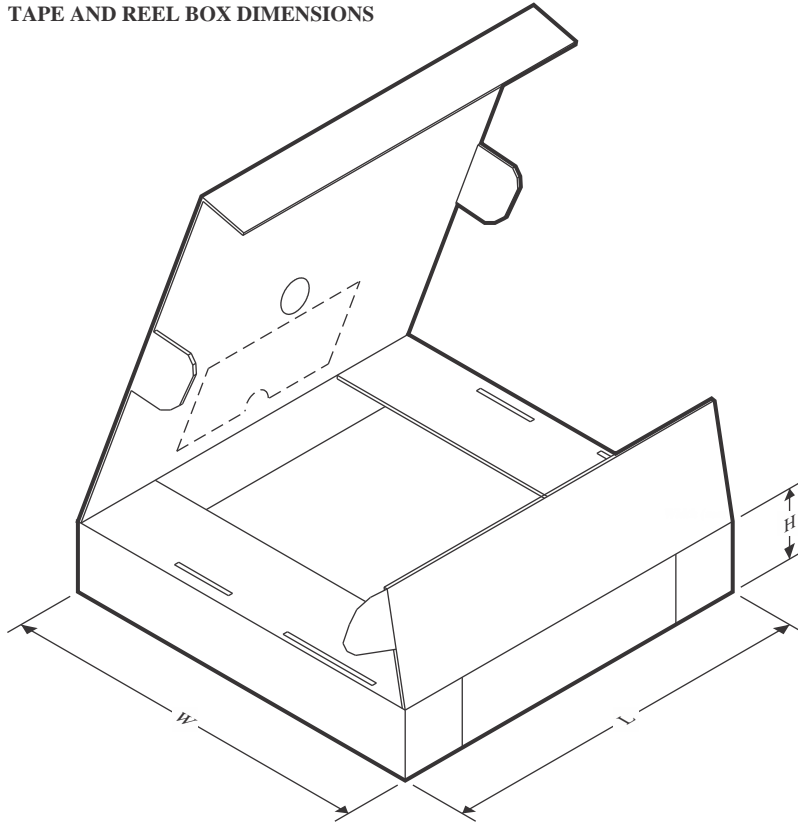
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV321IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV321IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV321IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
LMV321IDCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
LMV324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324QPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324QPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV358IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LMV358IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358IPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358IPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358QDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358QDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358QDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LMV358QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV321IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV321IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LMV321IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
LMV321IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV321IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
LMV321IDCKT	SC70	DCK	5	250	210.0	185.0	35.0
LMV324IDR	SOIC	D	14	2500	333.2	345.9	28.6
LMV324IDRG4	SOIC	D	14	2500	356.0	356.0	35.0
LMV324IDRG4	SOIC	D	14	2500	356.0	356.0	35.0
LMV324IDRG4	SOIC	D	14	2500	340.5	336.1	32.0
LMV324IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LMV324IPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LMV324QDR	SOIC	D	14	2500	356.0	356.0	35.0
LMV324QDR	SOIC	D	14	2500	356.0	356.0	35.0
LMV324QPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LMV324QPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
LMV358IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LMV358IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV358IDGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
LMV358IDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV358IDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LMV358IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LMV358IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LMV358IPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LMV358IPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LMV358QDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LMV358QDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LMV358QDGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
LMV358QDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV358QDR	SOIC	D	8	2500	356.0	356.0	35.0
LMV358QPWR	TSSOP	PW	8	2000	366.0	364.0	50.0



# EXAMPLE BOARD LAYOUT

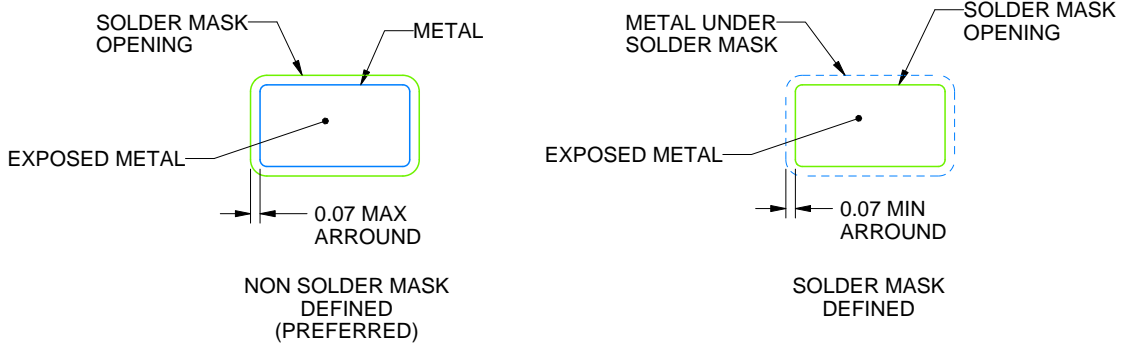
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

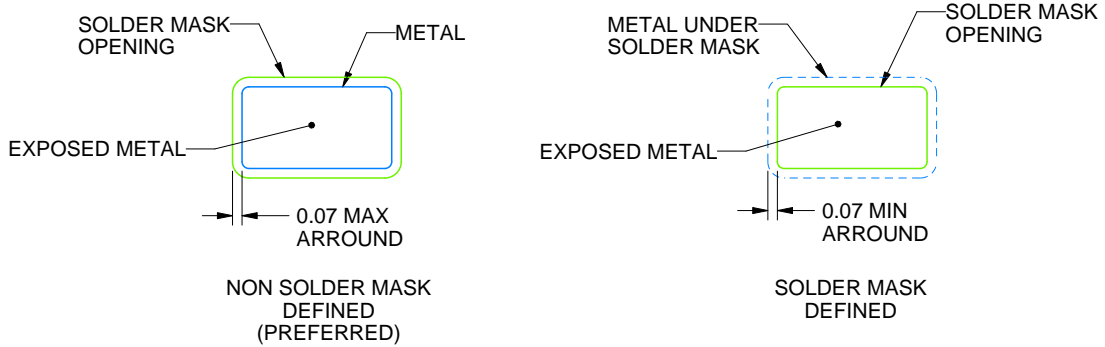
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

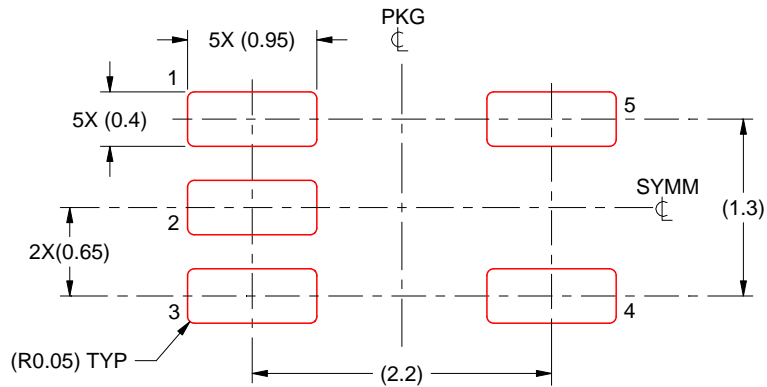
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

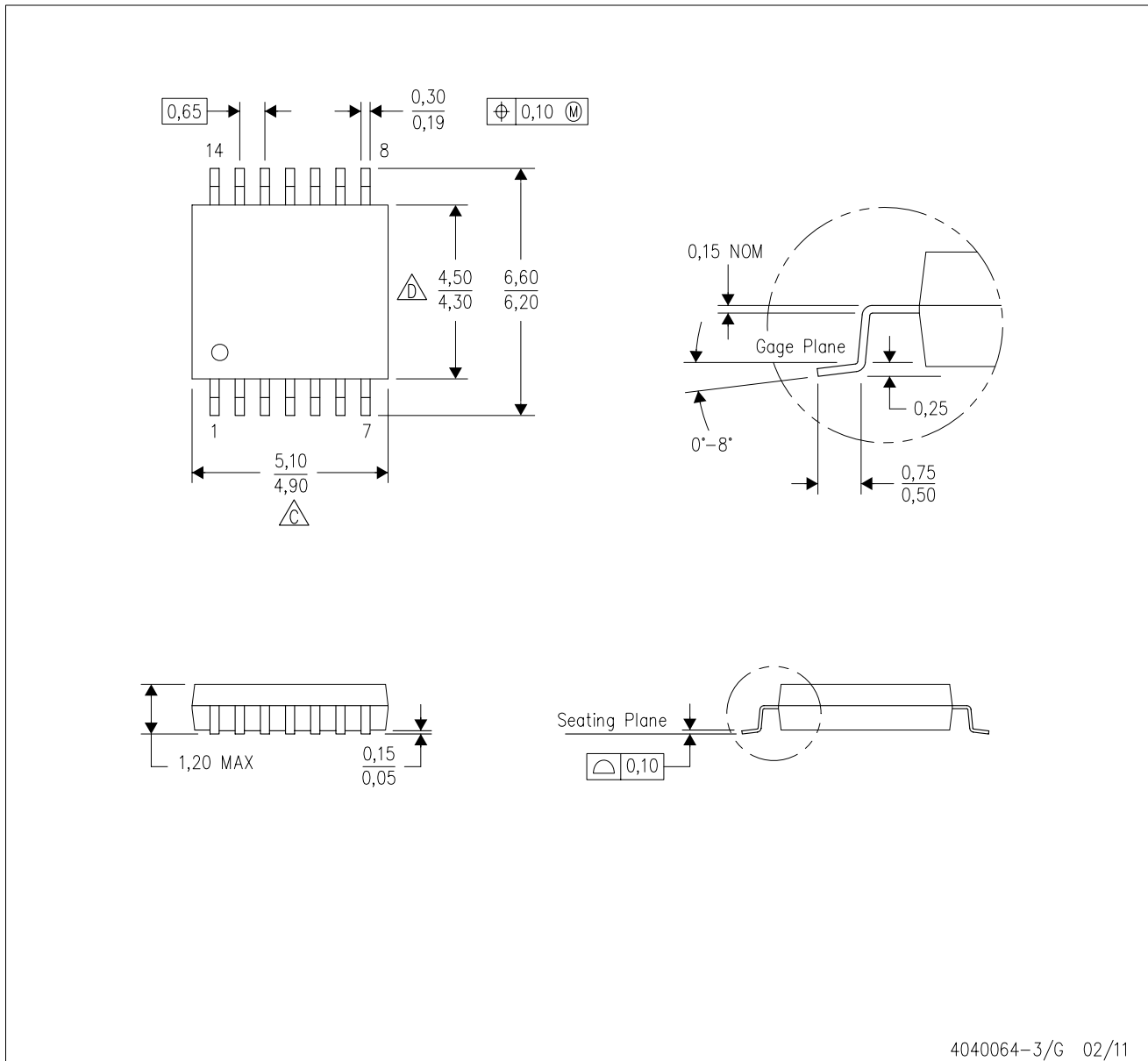


4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

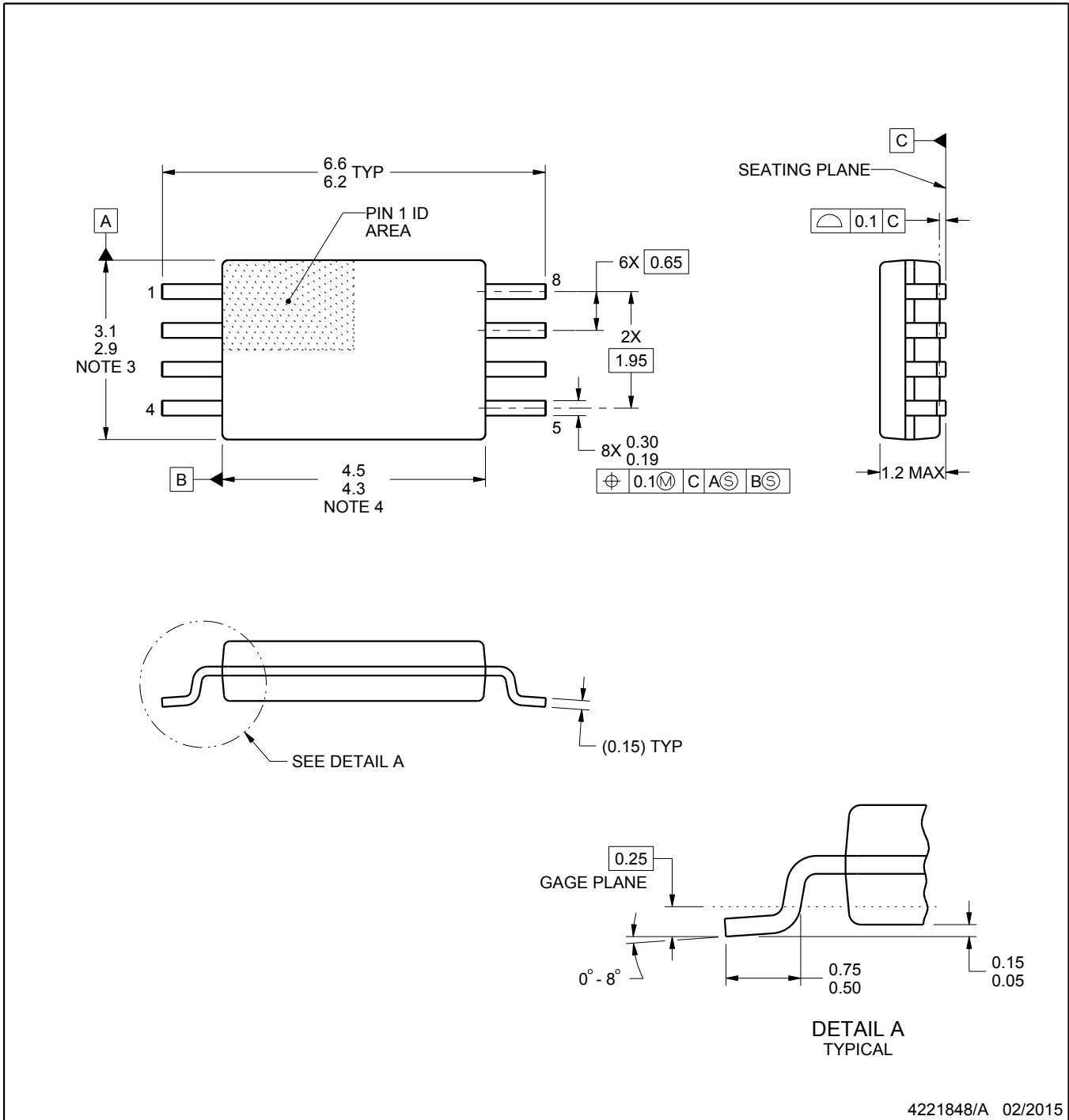
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



PACKAGE OUTLINE  
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

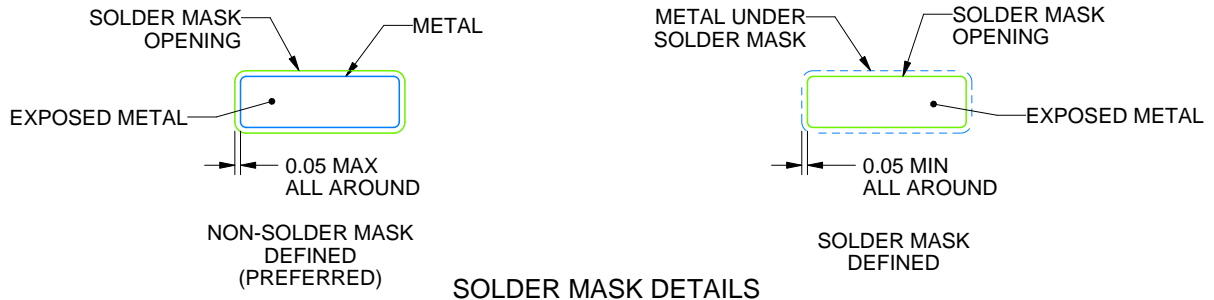
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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