



**THE DATASHEET OF  
SN74BCT245DBR**



# SN54BCT245, SN74BCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

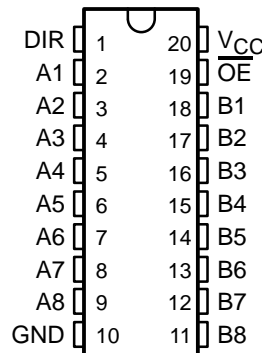
SCBS013H – SEPTEMBER 1998 – REVISED MAY 2002

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)

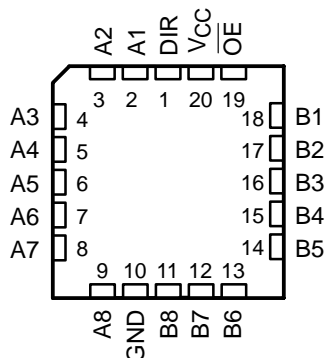
## description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

SN54BCT245 . . . J OR W PACKAGE  
SN74BCT245 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54BCT245 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

| TA             | PACKAGE†      |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|---------------|-----------------------|------------------|
| 0°C to 70°C    | PDIP – N      | Tube          | SN74BCT245N           | SN74BCT245N      |
|                | SOIC – DW     | Tube          | SN74BCT245DW          | BCT245           |
|                |               | Tape and reel | SN74BVT245DWR         |                  |
|                | SOP – NS      | Tape and reel | SN74BCT245NSR         | BCT245           |
|                | SSOP – DB     | Tape and reel | SN74BCT245DBR         | BT245            |
| TSSOP – PW     | Tape and reel | SN74BCT245PWR | BT245                 |                  |
| –55°C to 125°C | CDIP – J      | Tube          | SNJ54BCT245J          | SNJ54BCT245J     |
|                | CFP – W       | Tube          | SNJ54BCT245W          | SNJ54BCT245W     |
|                | LCCC – FK     | Tube          | SNJ54BCT245FK         | SNJ54BCT245FK    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.



# SN54BCT245, SN74BCT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

|          |                                | SN54BCT245 |     |     | SN74BCT245 |     |     | UNIT |
|----------|--------------------------------|------------|-----|-----|------------|-----|-----|------|
|          |                                | MIN        | NOM | MAX | MIN        | NOM | MAX |      |
| $V_{CC}$ | Supply voltage                 | 4.5        | 5   | 5.5 | 4.5        | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       | 2          |     |     | 2          |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |            |     | 0.8 |            |     | 0.8 | V    |
| $I_{IK}$ | Input clamp current            |            |     | -18 |            |     | -18 | mA   |
| $I_{OH}$ | High-level output current      | A port     |     | -3  | B port     |     | -3  | mA   |
|          |                                | B port     |     | -12 | A port     |     | -15 |      |
| $I_{OL}$ | Low-level output current       | A port     |     | 20  | B port     |     | 24  | mA   |
|          |                                | B port     |     | 48  | A port     |     | 64  |      |
| $T_A$    | Operating free-air temperature | -55        |     | 125 | 0          |     | 70  | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |               | TEST CONDITIONS           |                                        | SN54BCT245 |      | SN74BCT245 |       | UNIT |
|-----------|---------------|---------------------------|----------------------------------------|------------|------|------------|-------|------|
|           |               |                           |                                        | MIN        | TYP† | MAX        | MIN   |      |
| $V_{IK}$  |               | $V_{CC} = 4.5\text{ V}$ , | $I_I = -18\text{ mA}$                  |            |      | -1.2       | -1.2  | V    |
| $V_{OH}$  | A port        | $V_{CC} = 4.5\text{ V}$   | $I_{OH} = -1\text{ mA}$                | 2.5        | 3.4  | 2.5        | 3.4   | V    |
|           |               |                           | $I_{OH} = -3\text{ mA}$                | 2.4        | 3.3  | 2.4        | 3.3   |      |
|           | B port        | $V_{CC} = 4.5\text{ V}$   | $I_{OH} = -3\text{ mA}$                | 2.4        | 3.3  | 2.4        | 3.3   |      |
|           |               |                           | $I_{OH} = -12\text{ mA}$               | 2          | 3.2  |            |       |      |
|           |               |                           |                                        |            |      | 2          | 3.1   |      |
| $V_{OL}$  | A port        | $V_{CC} = 4.5\text{ V}$   | $I_{OL} = 20\text{ mA}$                |            | 0.3  | 0.5        |       | V    |
|           |               |                           | $I_{OL} = 24\text{ mA}$                |            |      |            | 0.35  |      |
|           | B port        | $V_{CC} = 4.5\text{ V}$   | $I_{OL} = 48\text{ mA}$                |            | 0.38 | 0.55       |       |      |
|           |               |                           | $I_{OL} = 64\text{ mA}$                |            |      |            | 0.42  |      |
|           |               |                           |                                        |            |      |            |       |      |
| $I_I$     | A or B port   | $V_{CC} = 5.5\text{ V}$ , | $V_I = 5.5\text{ V}$                   |            |      | 1          | 1     | mA   |
|           | Control input |                           |                                        |            |      | 0.1        | 0.1   |      |
| $I_{IH}‡$ | A or B port   | $V_{CC} = 5.5\text{ V}$ , | $V_I = 2.7\text{ V}$                   |            |      | 70         | 70    | µA   |
|           | Control input |                           |                                        |            |      | 20         | 20    |      |
| $I_{IL}‡$ | A or B port   | $V_{CC} = 5.5\text{ V}$ , | $V_I = 0.5\text{ V}$                   |            |      | -0.65      | -0.65 | mA   |
|           | Control input |                           |                                        |            |      | -1.2       | -1.2  |      |
| $I_{OS}§$ | A port        | $V_{CC} = 5.5\text{ V}$ , | $V_O = 0$                              | -60        | -150 | -60        | -150  | mA   |
|           | B port        |                           |                                        | -100       | -225 | -100       | -225  |      |
| $I_{CCL}$ | A to B        | $V_{CC} = 5.5\text{ V}$   |                                        | 57         | 90   | 57         | 90    | mA   |
| $I_{CCH}$ | A to B        | $V_{CC} = 5.5\text{ V}$   |                                        | 36         | 57   | 36         | 57    | mA   |
| $I_{CCZ}$ |               | $V_{CC} = 5.5\text{ V}$   |                                        | 10         | 15   | 10         | 15    | mA   |
| $C_i$     | Control input | $V_{CC} = 5\text{ V}$ ,   | $V_I = 2.5\text{ V}$ or $0.5\text{ V}$ |            | 7    |            | 7     | pF   |
| $C_{io}$  | A to B        | $V_{CC} = 5\text{ V}$ ,   | $V_O = 2.5\text{ V}$ or $0.5\text{ V}$ |            | 9    |            | 9     | pF   |
|           | B to A        |                           |                                        |            | 12   |            | 12    |      |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



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OCTAL BUS TRANSCEIVERS  
WITH 3-STATE OUTPUTS**

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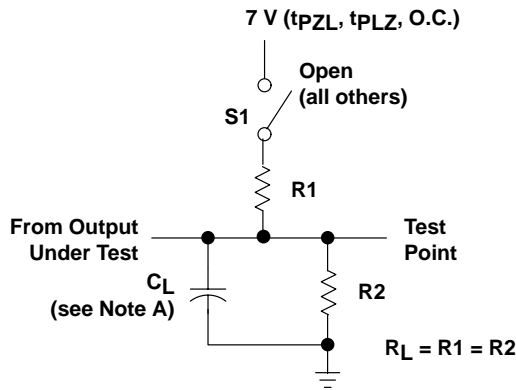
**switching characteristics (see Figure 1)**

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = 500 Ω,<br>R <sub>2</sub> = 500 Ω,<br>T <sub>A</sub> = 25°C |     |      | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>1</sub> = 500 Ω,<br>R <sub>2</sub> = 500 Ω,<br>T <sub>A</sub> = MIN to MAX <sup>†</sup> |      |            | UNIT |     |
|------------------|-----------------|----------------|----------------------------------------------------------------------------------------------------------------------------------|-----|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------------|------|-----|
|                  |                 |                | BCT245                                                                                                                           |     |      | SN54BCT245                                                                                                                                                     |      | SN74BCT245 |      |     |
|                  |                 |                | MIN                                                                                                                              | TYP | MAX  | MIN                                                                                                                                                            | MAX  | MIN        |      | MAX |
| t <sub>PLH</sub> | A or B          | B or A         | 1                                                                                                                                | 4.4 | 6    | 1                                                                                                                                                              | 7.2  | 1          | 7    | ns  |
| t <sub>PHL</sub> |                 |                | 1.5                                                                                                                              | 4.8 | 6.6  | 1.5                                                                                                                                                            | 7.6  | 1.5        | 7    |     |
| t <sub>PZH</sub> | $\overline{OE}$ | A or B         | 1.5                                                                                                                              | 8   | 9.4  | 1.5                                                                                                                                                            | 11.2 | 1.5        | 10.9 | ns  |
| t <sub>PZL</sub> |                 |                | 1.5                                                                                                                              | 8   | 10.2 | 1.5                                                                                                                                                            | 11.8 | 1.5        | 11.6 |     |
| t <sub>PHZ</sub> | $\overline{OE}$ | A or B         | 1.5                                                                                                                              | 5.8 | 8.3  | 1.5                                                                                                                                                            | 9.7  | 1.5        | 9.3  | ns  |
| t <sub>PLZ</sub> |                 |                | 1.5                                                                                                                              | 5.1 | 7.8  | 1.5                                                                                                                                                            | 9.6  | 1.5        | 9.1  |     |

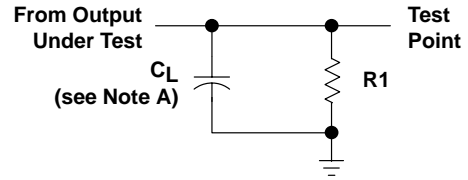
<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



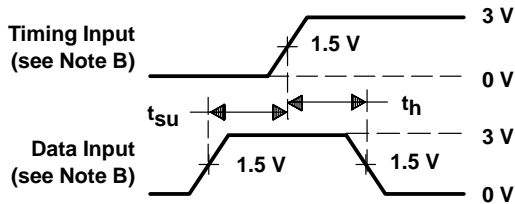
PARAMETER MEASUREMENT INFORMATION



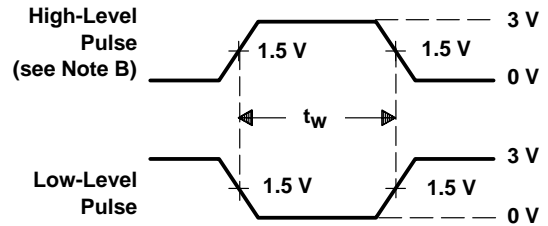
LOAD CIRCUIT FOR  
3-STATE AND OPEN-COLLECTOR OUTPUTS



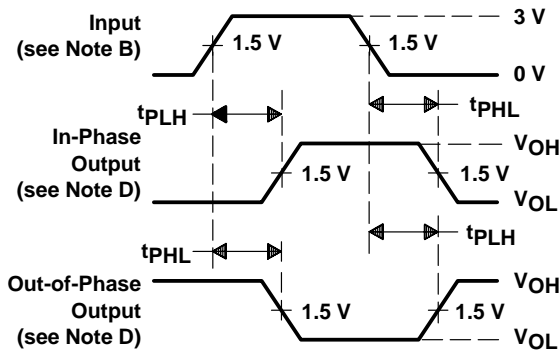
LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS



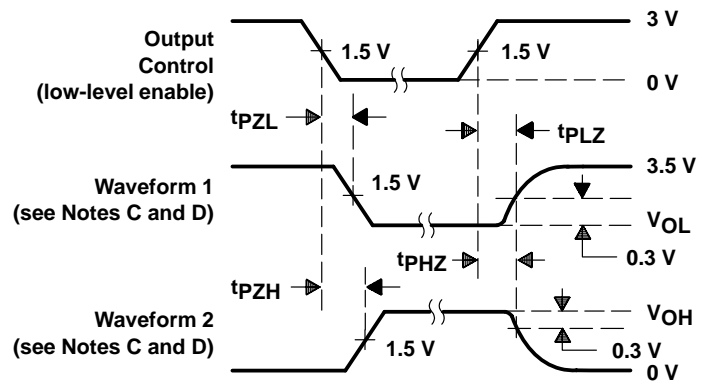
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. The outputs are measured one at a time with one transition per measurement.  
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 1. Load Circuit and Voltage Waveforms

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## TYPICAL CHARACTERISTICS†

Figures 2 through 5 show the typical power dissipation for an SN74BCT245 over variations in outputs switching, output frequency, and capacitive load.

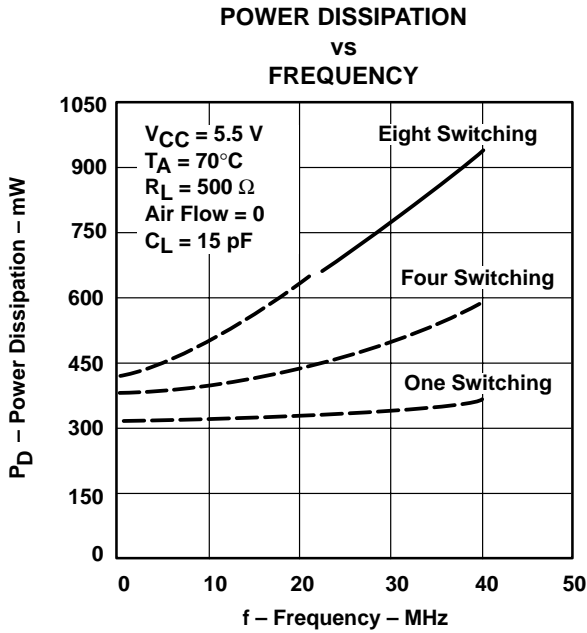


Figure 2

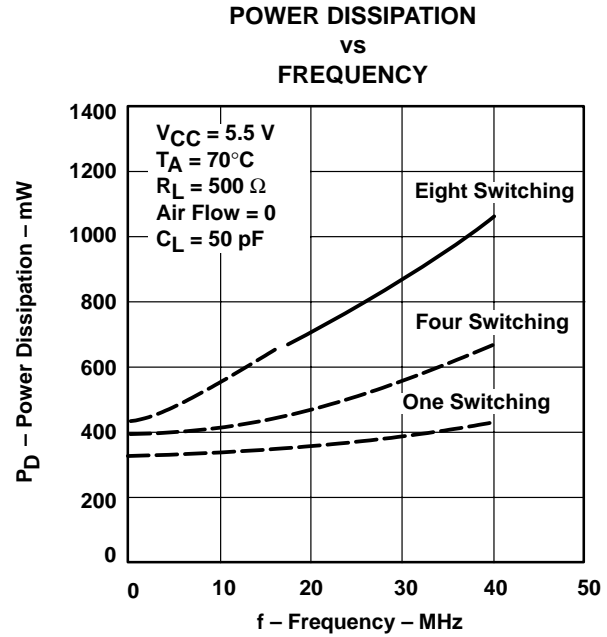


Figure 3

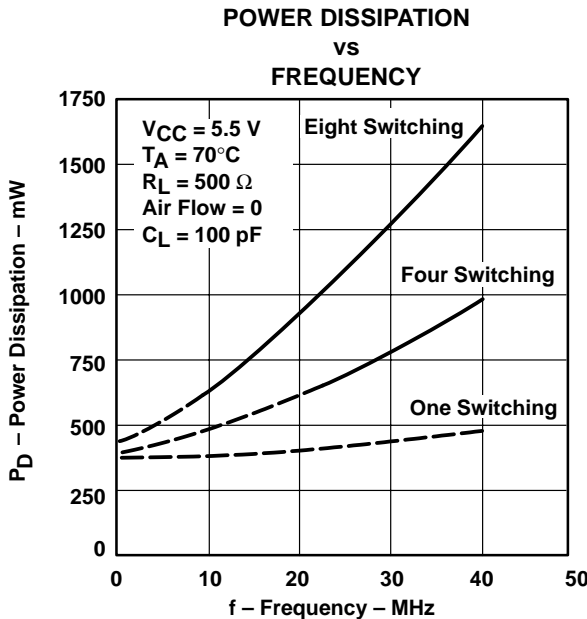


Figure 4

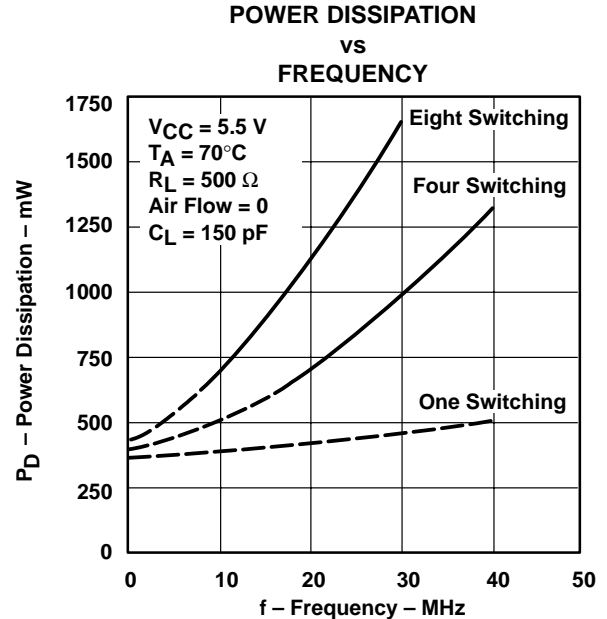


Figure 5

† The dashed lines are for the DB package only.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)              | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------------------|-------------------------|
| 5962-9051401M2A  | ACTIVE        | LCCC         | FK              | 20   | 55          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9051401M2A<br>SNJ54<br>BCT245FK | <a href="#">Samples</a> |
| 5962-9051401MRA  | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9051401MR<br>A<br>SNJ54BCT245J  | <a href="#">Samples</a> |
| 5962-9051401MSA  | ACTIVE        | CFP          | W               | 20   | 25          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9051401MS<br>A<br>SNJ54BCT245W  | <a href="#">Samples</a> |
| SN74BCT245DBR    | ACTIVE        | SSOP         | DB              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | BT245                                | <a href="#">Samples</a> |
| SN74BCT245DWR    | ACTIVE        | SOIC         | DW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | BCT245                               | <a href="#">Samples</a> |
| SN74BCT245N      | ACTIVE        | PDIP         | N               | 20   | 20          | RoHS & Non-Green | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74BCT245N                          | <a href="#">Samples</a> |
| SN74BCT245NSR    | ACTIVE        | SO           | NS              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | BCT245                               | <a href="#">Samples</a> |
| SN74BCT245PWR    | ACTIVE        | TSSOP        | PW              | 20   | 2000        | RoHS & Green     | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | BT245                                | <a href="#">Samples</a> |
| SNJ54BCT245FK    | ACTIVE        | LCCC         | FK              | 20   | 55          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9051401M2A<br>SNJ54<br>BCT245FK | <a href="#">Samples</a> |
| SNJ54BCT245J     | ACTIVE        | CDIP         | J               | 20   | 20          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9051401MR<br>A<br>SNJ54BCT245J  | <a href="#">Samples</a> |
| SNJ54BCT245W     | ACTIVE        | CFP          | W               | 20   | 25          | Non-RoHS & Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9051401MS<br>A<br>SNJ54BCT245W  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54BCT245, SN74BCT245 :**

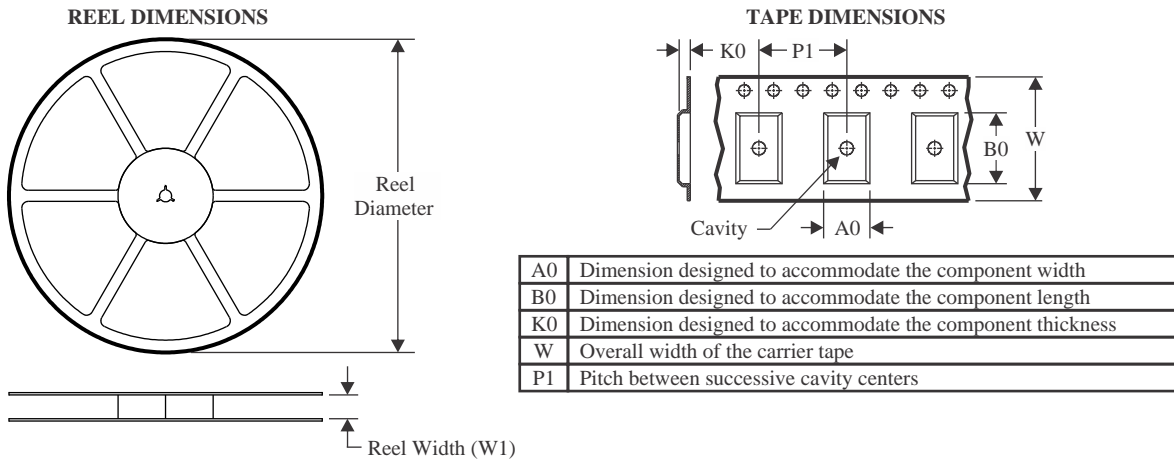
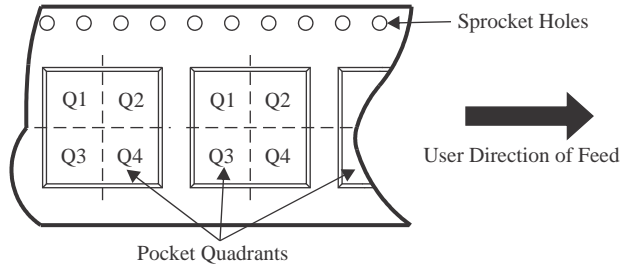
● Catalog : [SN74BCT245](#)

● Military : [SN54BCT245](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74BCT245DBR | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74BCT245DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74BCT245NSR | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74BCT245PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74BCT245DBR | SSOP         | DB              | 20   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74BCT245DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74BCT245NSR | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74BCT245PWR | TSSOP        | PW              | 20   | 2000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9051401M2A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-9051401MSA | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74BCT245N     | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54BCT245FK   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54BCT245W    | W            | CFP          | 20   | 25  | 506.98 | 26.16  | 6220   | NA     |

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

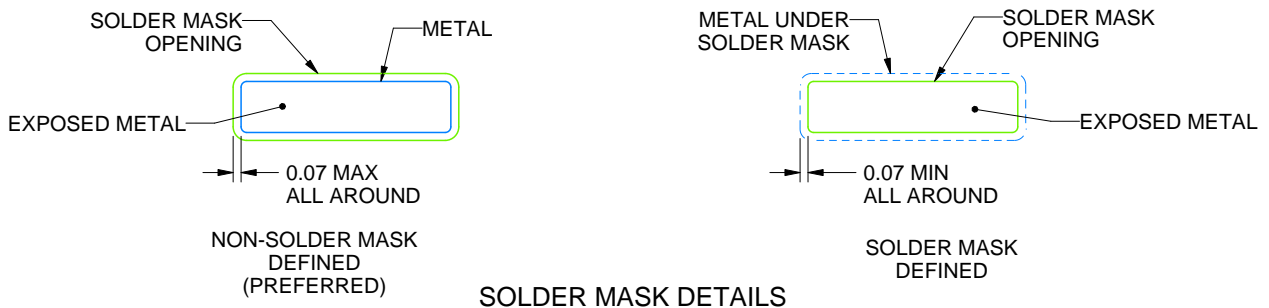
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

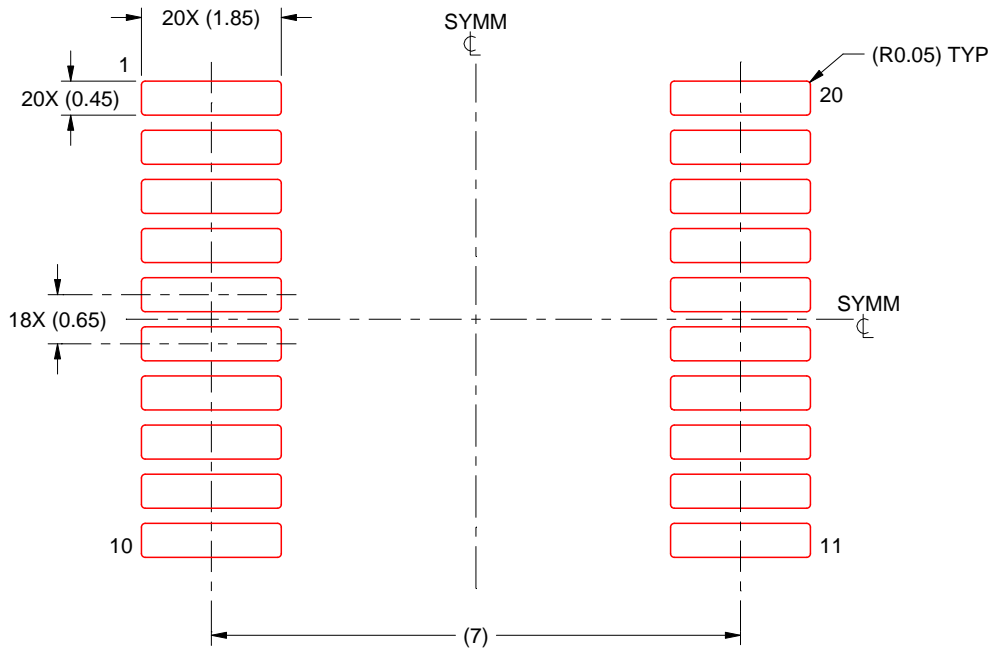
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

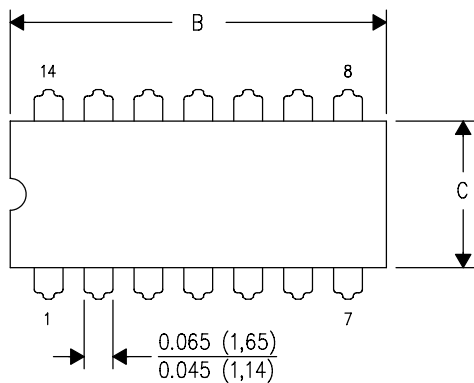


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20



# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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