



**THE DATASHEET OF
SN75157DG4**



SN75157 Dual Differential Line Receiver

1 Features

- Meets or exceeds the requirements of ANSI standards EIA/TIA-422-B and EIA/TIA-423-B and ITU recommendation V.10 and V.11
- Operates from single 5V power supply
- Wide common-mode voltage range
- High input impedance
- TTL-compatible outputs
- High-speed schottky circuitry
- 8-Pin dual-in-line package

2 Applications

- [Factory automation](#)
- [AC and servo motor drives](#)

3 Description

The SN75157 is a dual differential line receiver designed to meet standards EIA/TIA-422-B and EIA/TIA-423-B and ITU V.10 and V.11. The device uses Schottky circuitry, and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. The device operates from a single 5V power supply and is supplied in 8-pin dual-in-line and small-outline packages.

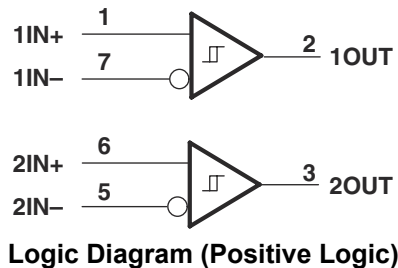
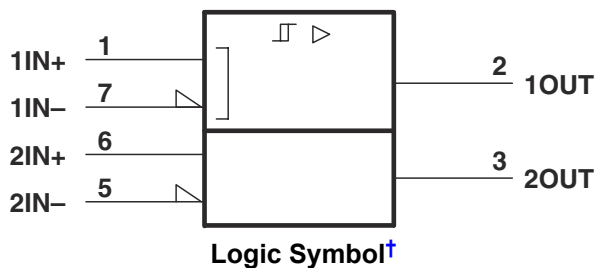
The SN75157 is characterized for operation from 0°C to 70°C.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN75157	SOIC (D, 8)	4.9mm × 6mm
	PDIP (P, 8)	9.81mm × 9.43mm
	SOP (PS, 8)	6.2mm × 7.8mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



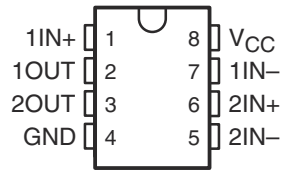
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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4 Pin Configuration and Functions



**Figure 4-1. D, P, OR PS Package
(Top View)**

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1IN+	1	I	Non-Inverting Differential Input for Channel 1's Differential Receiver
1OUT	2	O	Single Ended Output for Channel 1 Differential Receiver
2OUT	3	O	Single Ended Output for Channel 2 Differential Receiver
GND	4	GND	Device Ground
2IN-	5	I	Inverting Differential Input for Channel 2's Differential Receiver
2IN+	6	I	Non-Inverting Differential Input for Channel 2's Differential Receiver
1IN-	7	I	Inverting Differential Input for Channel 1's Differential Receiver
V _{CC}	8	POW	5V (+/-5%) Positive Supply Connection Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, POW = Power, GND = Ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾	-0.5	7	V
V _I	Input voltage range		±15	V
V _{ID}	Differential input voltage ⁽³⁾		±15	v
V _O	Output voltage range ⁽²⁾	-0.5	5.5	V
I _{OL}	Low-level output current		50	mA
	Continuous total dissipation	See Dissipation Ratings		
T _J	Operating free-air temperature range	0	70	°C
T _{stg}	Storage temperature range	-65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 s		260	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential input voltage, are with respect to the network ground terminal.
- (3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Ratings

PACKAGE	T _A ≤ 25°C POWER RATING	OPERATING FACTOR ABOVE T _A = 25°C	T _A ≤ 70°C POWER RATING
D	725mW	5.8mW/°C	464mW
P	1000mW	8.0mW/°C	640mW
PS	450mW	3.6mW/°C	288mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IC}	Common-mode input voltage			±7	V
T _A	Operating free-air temperature	0	25	70	°C

5.4 Thermal Resistance Characteristics

THERMAL METRIC ⁽¹⁾		D (SOIC)	P (PIDP)	PS (SOP)	UNIT
		8 Pins	8 Pins	8 Pins	
R _{θJA}	Junction-to-ambient thermal resistance	116.7	84.3	89.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	56.3	65.4	46.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	63.4	62.1	50.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	8.8	31.3	23.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	62.6	60.4	60.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)⁽⁴⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽⁵⁾	MAX	UNIT
V _{IT}	Input threshold voltage (V _{IT+} and V _{IT-}) ⁽²⁾			-0.2		0.2	V
				-0.4		0.4	
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT-})				70		mV
V _{OH}	High-level output voltage	V _{ID} = 0.2V,	I _O = -1mA	2.5	3.5		V
V _{OL}	Low-level output voltage	V _{ID} = -0.2V,	I _O = 20mA		0.35	0.5	V
I _I	Input current ⁽³⁾	V _{CC} = 0 to 5.5V,	V _I = 10V		1.1	3.25	mA
			V _I = -1 V		-1.6	-3.25	
I _{OS}	Short-circuit output current ⁽¹⁾	V _O = 0V,	V _{ID} = 0.2V	-40	-75	-100	mA
I _{CC}	Supply current	V _{ID} = -0.5V,	No load		35	50	mA

- (1) Only one output should be shorted at a time and duration of the short circuit should not exceed one second.
- (2) The expanded threshold parameter is tested with a 500-W resistor in series with each input.
- (3) The input not under test is grounded.
- (4) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
- (5) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.6 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 15pF, see Figure 6-1			15	25	ns
t _{PHL}	Propagation delay time, high- to low-level output				13	25	

5.7 Typical Characteristics

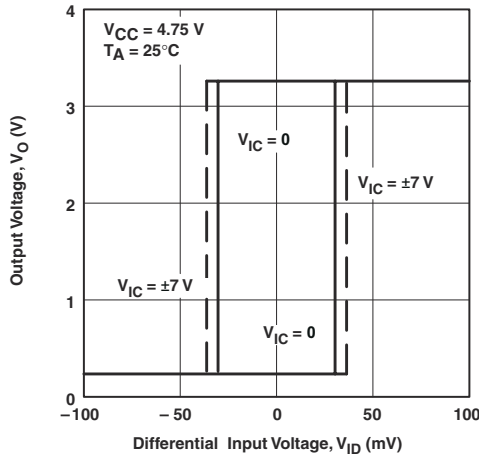


Figure 5-1. Output Voltage vs Differential Input Voltage

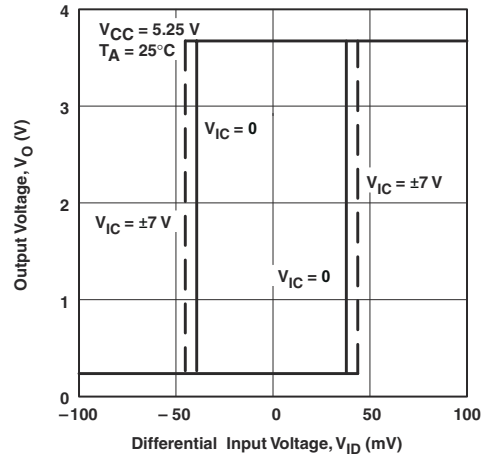


Figure 5-2. Output Voltage vs Differential Input Voltage

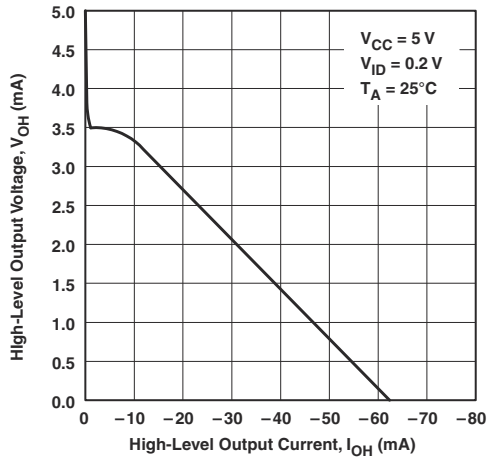


Figure 5-3. High-Level Output Voltage vs High-Level Output Current

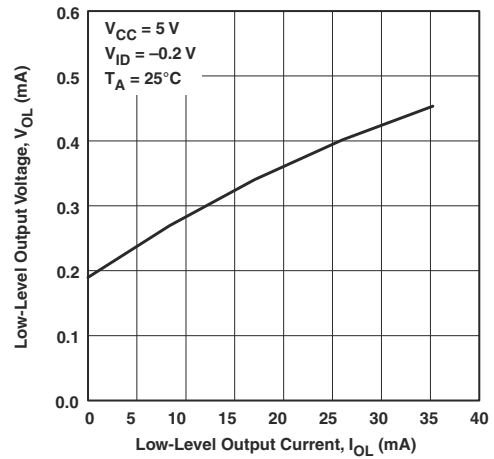


Figure 5-4. Low-Level Output Voltage vs Low-Level Output Current

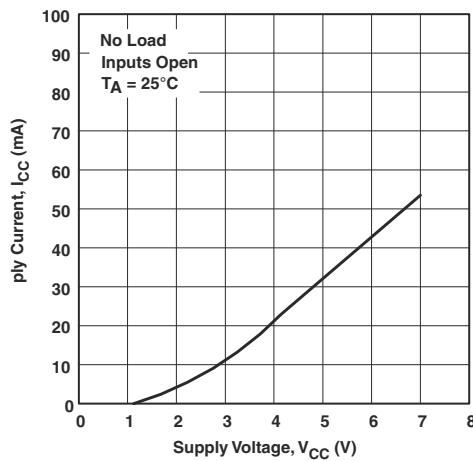
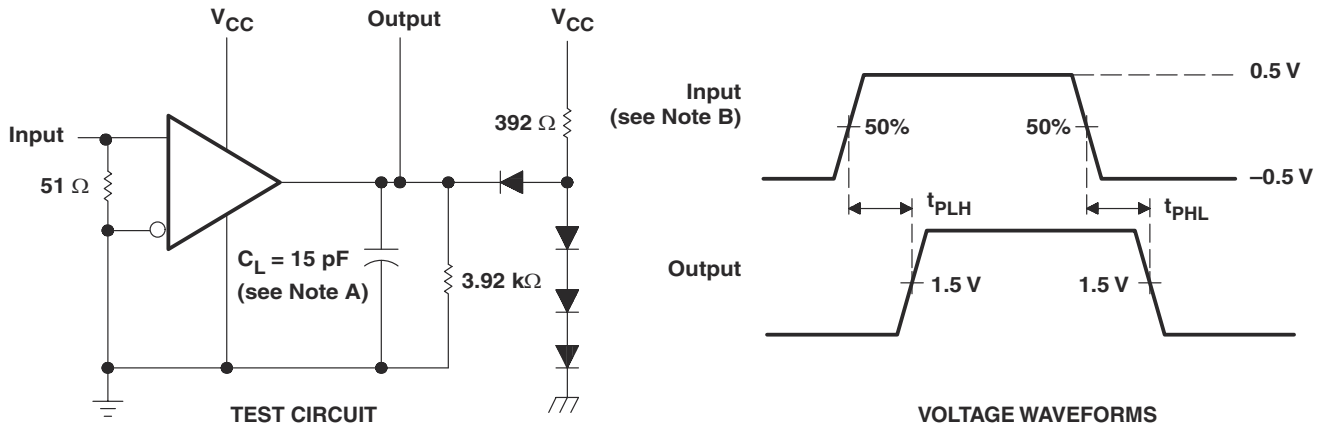


Figure 5-5. Supply Current vs Supply Voltage

Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5\ \text{ns}$, $t_f \leq 5\ \text{ns}$, $\text{PRR} \leq 5\ \text{MHz}$, duty cycle = 50%.

Figure 6-1. Test Circuit and Voltage Waveforms

6 Detailed Description

6.1 Device Functional Modes

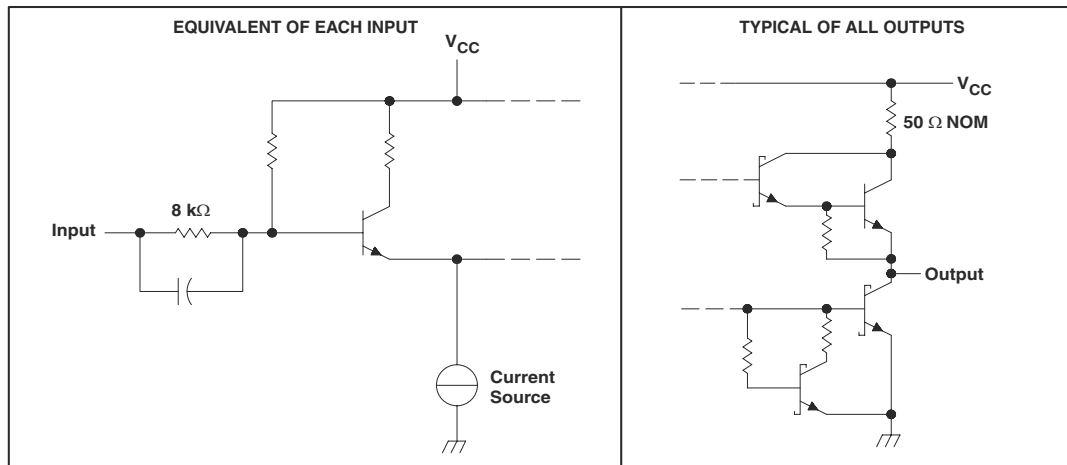


Figure 6-1. Schematics of Inputs and Outputs

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application

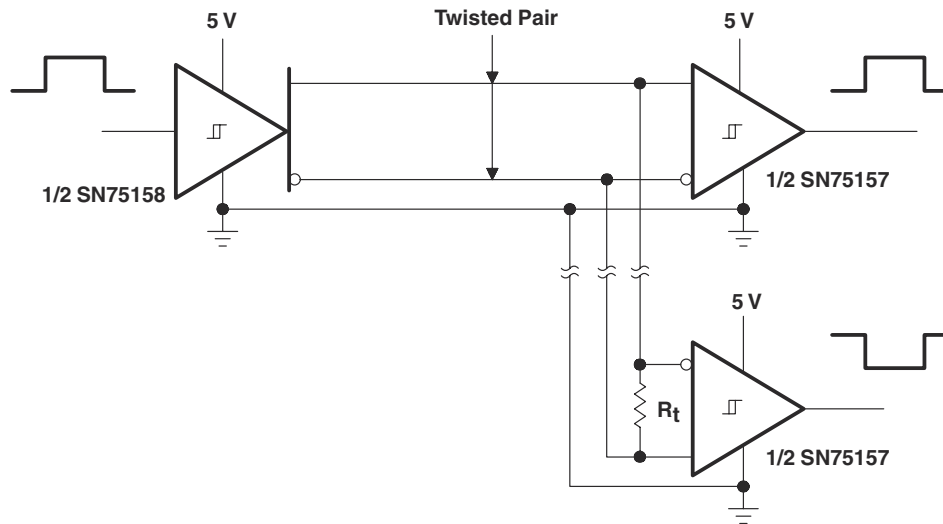


Figure 7-1. EIA/TIA-422-B System Application

8 Device and Documentation Support

8.1 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.2 Trademarks

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All trademarks are the property of their respective owners.

8.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 1997) to Revision D (January 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75157D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75157	
SN75157DE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75157	
SN75157DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75157	
SN75157DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		75157	Samples
SN75157P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75157P	Samples
SN75157PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A157	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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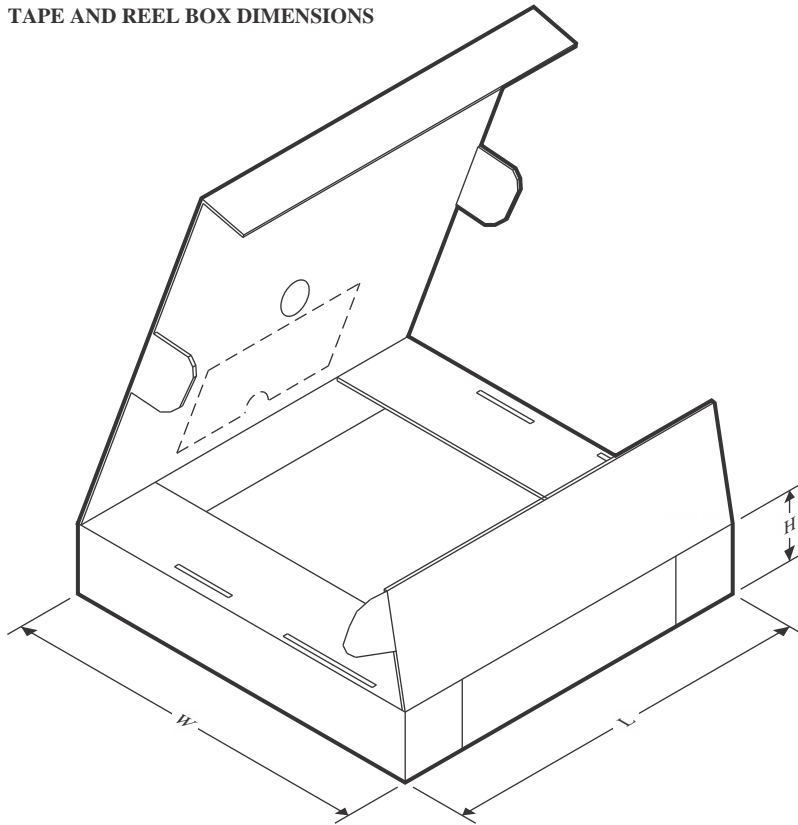
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75157DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75157PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75157DR	SOIC	D	8	2500	353.0	353.0	32.0
SN75157PSR	SO	PS	8	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75157D	D	SOIC	8	75	507	8	3940	4.32
SN75157DE4	D	SOIC	8	75	507	8	3940	4.32
SN75157DG4	D	SOIC	8	75	507	8	3940	4.32
SN75157P	P	PDIP	8	50	506	13.97	11230	4.32

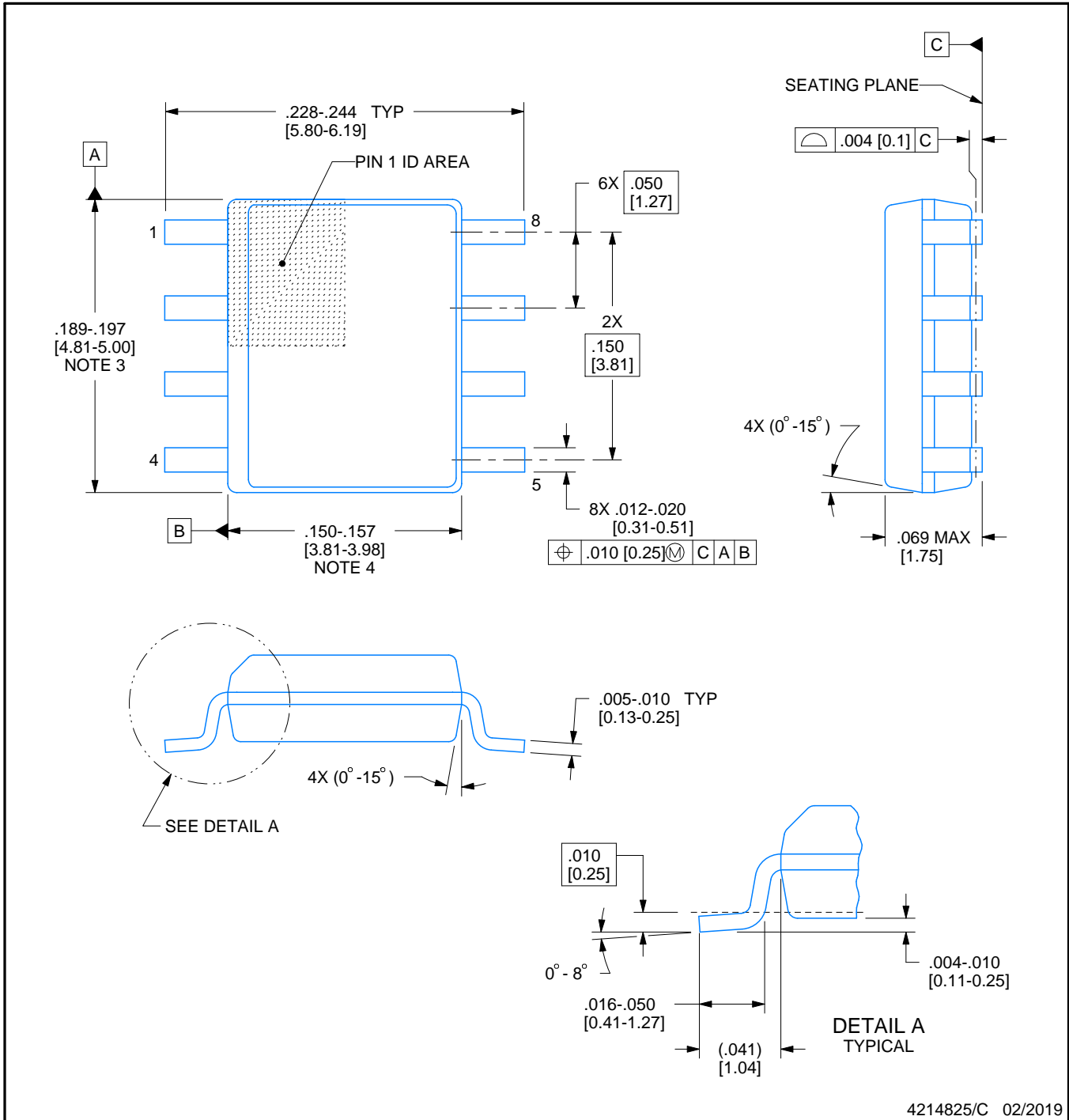


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

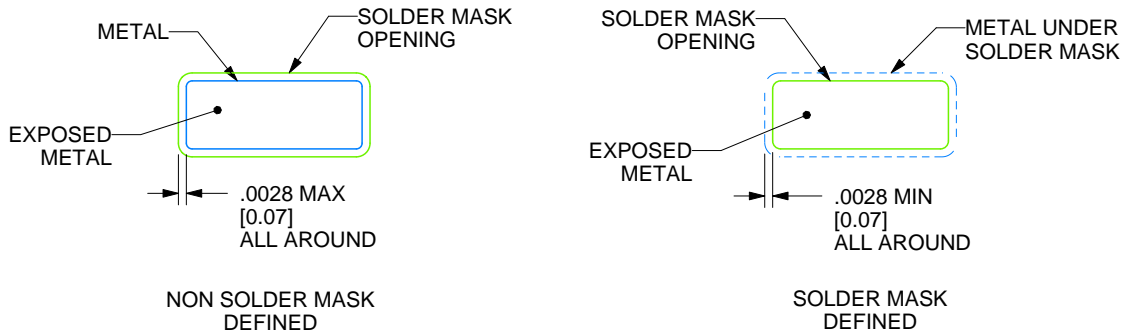
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

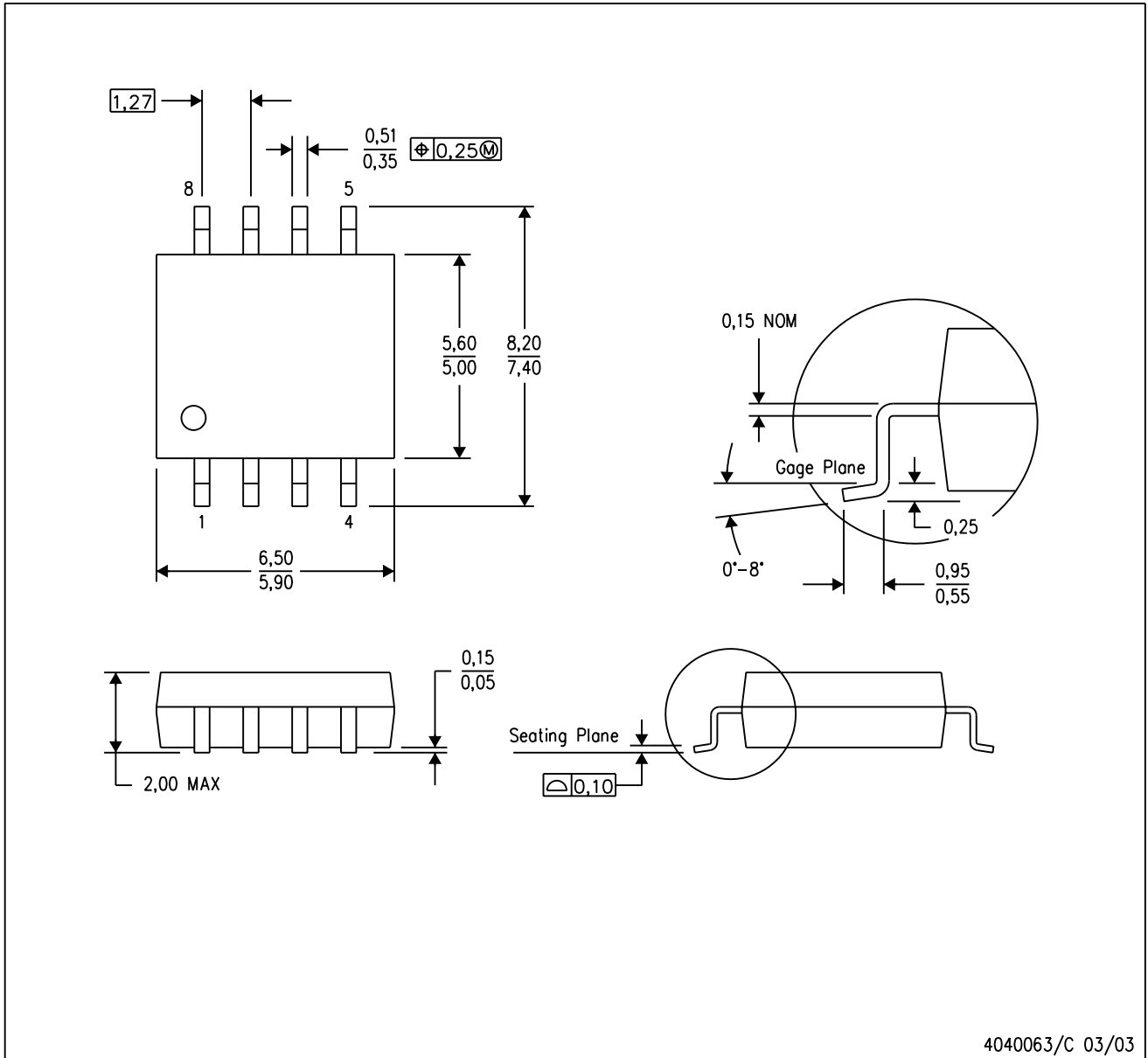
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

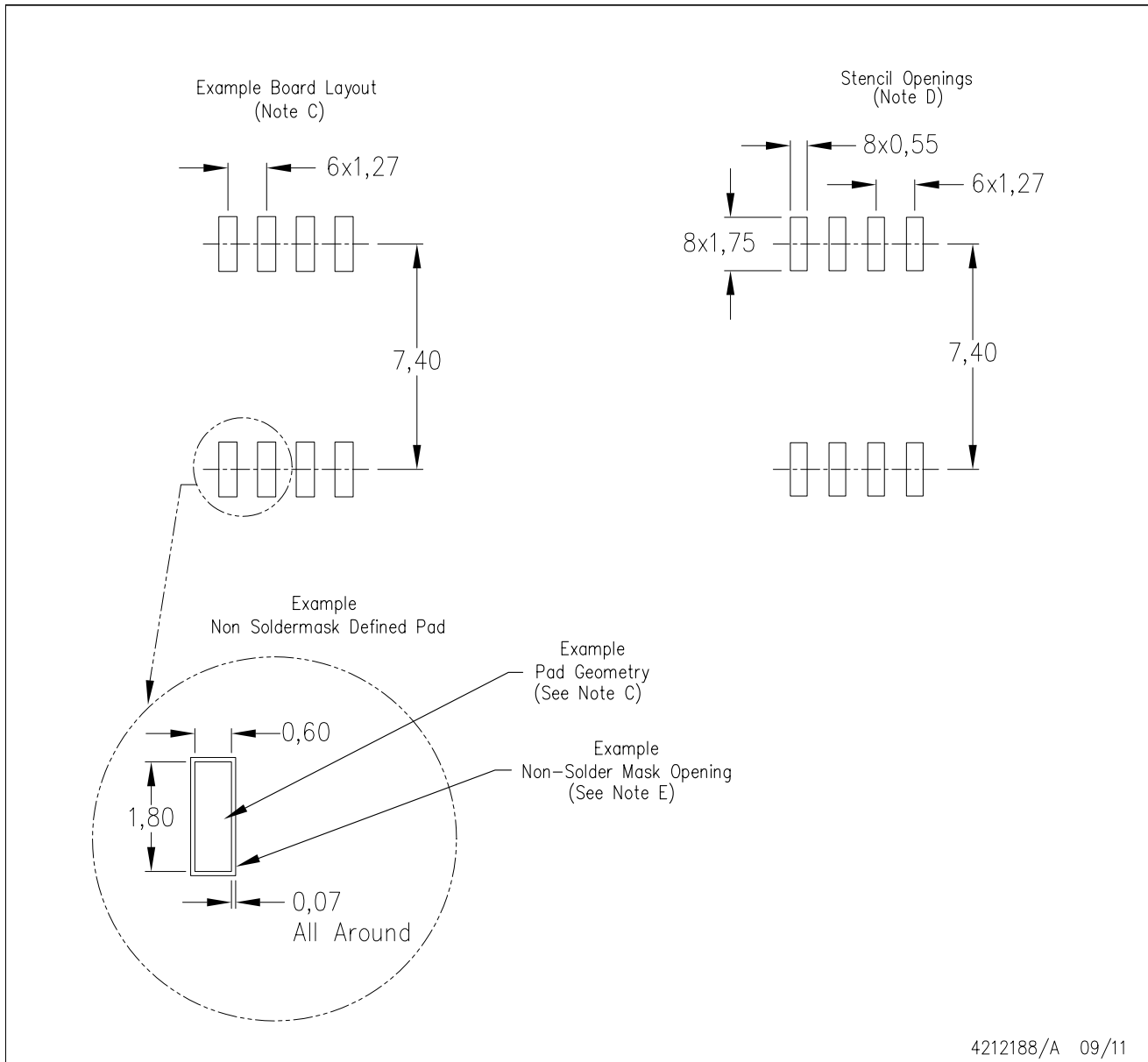
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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