



**THE DATASHEET OF
TPS61010DGSG4**



TPS6101x High-Efficiency, 1-Cell and 2-Cell Boost Converters

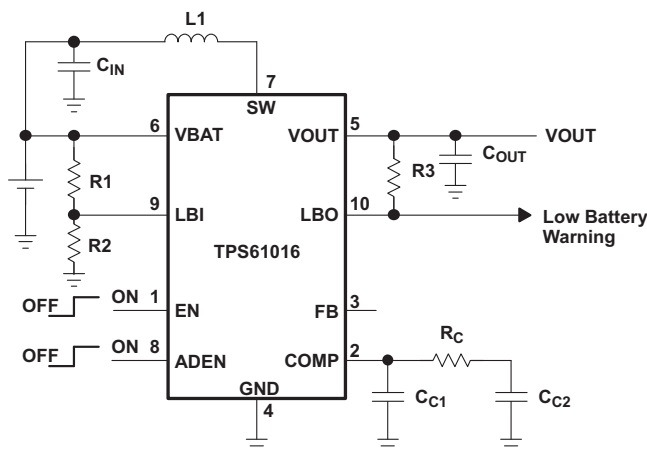
1 Features

- Integrated Synchronous Rectifier for Highest Power Conversion Efficiency (> 95%)
- Start-Up Into Full Load With Supply Voltages as Low as 0.9 V, Operating Down to 0.8 V
- 200-mA Output Current From 0.9-V Supply
- Powersave-Mode for Improved Efficiency at Low Output Currents
- Autodischarge Allows to Discharge Output Capacitor During Shutdown
- Device Quiescent Current Less Than 50 μ A
- Ease-of-Use Through Isolation of Load From Battery During Shutdown of Converter
- Integrated Antiringing Switch Across Inductor
- Integrated Low Battery Comparator
- Micro-Small 10-Pin MSOP or 3 mm x 3 mm QFN Package
- EVM Available (TPS6101xEVM-157)

2 Applications

- All Single- or Dual-Cell Battery Operated Products
 - Internet Audio Players
 - Pager
 - Portable Medical Diagnostic Equipment
 - Remote Control
 - Wireless Headsets

Simplified Application Circuit



3 Description

The TPS6101x devices are boost converters intended for systems that are typically operated from a single- or dual-cell nickel-cadmium (NiCd), nickel-metal hydride (NiMH), or alkaline battery.

The converter output voltage can be adjusted from 1.5 V to a maximum of 3.3 V, by an external resistor divider or, is fixed internally on the chip. The devices provide an output current of 200 mA with a supply voltage of only 0.9 V. The converter starts up into a full load with a supply voltage of only 0.9 V and stays in operation with supply voltages down to 0.8 V.

The converter is based on a fixed frequency, current mode, pulse-width-modulation (PWM) controller that goes automatically into power save mode at light load. It uses a built-in synchronous rectifier, so, no external Schottky diode is required and the system efficiency is improved. The current through the switch is limited to a maximum value of 1300 mA. The converter can be disabled to minimize battery drain. During shutdown, the load is completely isolated from the battery.

An autodischarge function allows discharging the output capacitor during shutdown mode. This is especially useful when a microcontroller or memory is supplied, where residual voltage across the output capacitor can cause malfunction of the applications. When programming the ADEN-pin, the autodischarge function can be disabled. A low-EMI mode is implemented to reduce interference and radiated electromagnetic energy when the converter enters the discontinuous conduction mode. The device is packaged in the micro-small space saving 10-pin MSOP package. The TPS61010 is also available in a 3 mm x 3 mm 10-pin QFN package.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| TPS61010 | VSSOP (10) | 3.00 mm x 3.00 mm |
| | VSON (10) | |
| TPS61011 | VSSOP (10) | 3.00 mm x 3.00 mm |
| TPS61012 | | |
| TPS61013 | | |
| TPS61014 | | |
| TPS61015 | | |
| TPS61016 | | |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Table of Contents

| | | | |
|--|----|--|----|
| 1 Features | 1 | 9.4 Device Functional Modes..... | 15 |
| 2 Applications | 1 | 10 Application and Implementation | 16 |
| 3 Description | 1 | 10.1 Application Information..... | 16 |
| 4 Revision History | 2 | 10.2 Typical Applications | 16 |
| 5 Device Comparison Table | 3 | 11 Power Supply Recommendations | 25 |
| 6 Pin Configuration and Functions | 3 | 12 Layout | 25 |
| 7 Specifications | 4 | 12.1 Layout Guidelines | 25 |
| 7.1 Absolute Maximum Ratings | 4 | 12.2 Layout Example | 25 |
| 7.2 ESD Ratings..... | 4 | 12.3 Thermal Considerations | 27 |
| 7.3 Recommended Operating Conditions..... | 4 | 13 Device and Documentation Support | 28 |
| 7.4 Thermal Information | 4 | 13.1 Device Support | 28 |
| 7.5 Electrical Characteristics | 5 | 13.2 Related Links | 28 |
| 7.6 Typical Characteristics | 7 | 13.3 Community Resources..... | 28 |
| 8 Parameter Measurement Information | 11 | 13.4 Trademarks | 28 |
| 9 Detailed Description | 12 | 13.5 Electrostatic Discharge Caution..... | 28 |
| 9.1 Overview | 12 | 13.6 Glossary | 28 |
| 9.2 Functional Block Diagram | 12 | 14 Mechanical, Packaging, and Orderable Information | 28 |
| 9.3 Feature Description..... | 13 | | |

4 Revision History

| Changes from Revision E (December 2014) to Revision F | Page |
|---|------|
| • Moved Storage temperature range, T_{stg} to the Absolute Maximum Ratings | 4 |
| • Changed <i>Handling Ratings</i> To ESD Ratings | 4 |
| • Changed $R_{\theta JA} = 294^{\circ}\text{C}/\text{W}$ To: $R_{\theta JA} = 161.8^{\circ}\text{C}/\text{W}$ in Thermal Considerations | 27 |
| • Changed text "maximum power dissipation is about 130 mW." To: "maximum power dissipation is about 247 mW." in Thermal Considerations | 27 |
| • Changed Equation 8 From: = 136 mW To: = 247 mW | 27 |

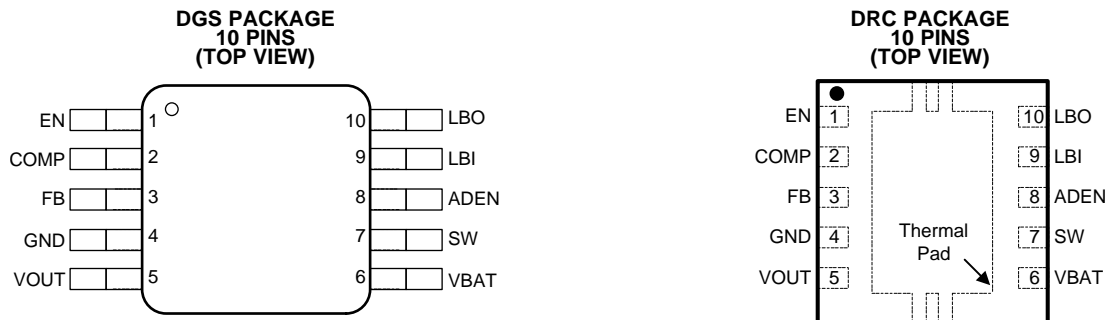
| Changes from Revision D (June 2005) to Revision E | Page |
|--|------|
| • Added <i>Pin Configuration and Functions</i> section, <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |

5 Device Comparison Table

| T _A | OUTPUT VOLTAGE (V) | PART NUMBER ⁽¹⁾ | MARKING DGS PACKAGE | PACKAGE ⁽²⁾ |
|----------------|----------------------------|----------------------------|---------------------|------------------------|
| –40°C to 85°C | Adjustable from 1.5 to 3.3 | TPS61010DGS | AIP | 10-Pin MSOP |
| | 1.5 | TPS61011DGS | AIQ | |
| | 1.8 | TPS61012DGS | AIR | |
| | 2.5 | TPS61013DGS | AIS | |
| | 2.8 | TPS61014DGS | AIT | |
| | 3.0 | TPS61015DGS | AIU | |
| | 3.3 | TPS61016DGS | AIV | |
| | Adjustable from 1.5 to 3.3 | TPS61010DRC | AYA | 10-Pin QFN |

- (1) The DGS package and the DRC package are available taped and reeled. Add a R suffix to device type (for example, TPS61010DGSR or TPS61010DRCR) to order quantities of 3000 devices per reel. The DRC package is also available in mini-reels. Add a T suffix to the device type (for example, TPS61010DRCT) to order quantities of 250 devices per reel.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

6 Pin Configuration and Functions



Pin Functions

| NAME | PIN | | I/O | DESCRIPTION |
|------|---------|---------|-----|---|
| | DRG NO. | DRC NO. | | |
| ADEN | 8 | 8 | I | Autodischarge output. The autodischarge function is enabled if this pin is connected to VBAT, it is disabled if ADEN is tied to GND. |
| COMP | 2 | 2 | I | Compensation of error amplifier. Connect an R/C/C network to set frequency response of control loop. |
| EN | 1 | 1 | I | Chip-enable input. The converter is switched on if this pin is set high, it is switched off if this pin is connected to GND. |
| FB | 3 | 3 | I | Feedback input for adjustable output voltage version TPS61010. Output voltage is programmed depending on the output voltage divider connected there. For the fixed output voltage versions, leave FB-pin unconnected. |
| GND | 4 | 4 | | Ground |
| LBI | 9 | 9 | I | Low-battery detector input. A low battery warning is generated at LBO when the voltage on LBI drops below the threshold of 500 mV. Connect LBI to GND or VBAT if the low-battery detector function is not used. Do not leave this pin floating. |
| LBO | 10 | 10 | O | Open-drain low-battery detector output. This pin is pulled low if the voltage on LBI drops below the threshold of 500 mV. A pullup resistor must be connected between LBO and VOUT. |
| SW | 7 | 7 | I | Switch input pin. The inductor is connected to this pin. |
| VBAT | 6 | 6 | I | Supply pin |
| VOUT | 5 | 5 | O | Output voltage. Internal resistor divider sets regulated output voltage in fixed output voltage versions. |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--|---|------|-----|------|
| Input voltage | V _{BAT} , V _{OUT} , EN, LBI, FB, ADEN | -0.3 | 3.6 | V |
| | SW | -0.3 | 7 | V |
| Voltage | LBO, COMP | -0.3 | 3.6 | V |
| Operating free-air temperature range, T _A | | -40 | 85 | °C |
| Maximum junction temperature, T _J | | | 150 | °C |
| Storage temperature range, T _{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | VALUE | MAX | UNIT |
|--------------------|-------------------------|--|-----|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | | ±2000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|----------------|---|-----|-----|------------------|------|
| V _I | Supply voltage at V _{BAT} | 0.8 | | V _{OUT} | V |
| I _O | Maximum output current at V _{IN} = 1.2 V | 100 | | | mA |
| I _O | Maximum output current at V _{IN} = 2.4 V | 200 | | | mA |
| L ₁ | Inductor | 10 | 33 | | μH |
| C _I | Input capacitor | | 10 | | μF |
| C _O | Output capacitor | 10 | 22 | 47 | μF |
| T _J | Operating virtual junction temperature | -40 | | 125 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS6101x | TPS61010 | UNIT |
|-------------------------------|--|----------|----------|------|
| | | DGS | DRC | |
| | | 10 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 161.8 | 43.1 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 36.3 | 67.4 | |
| R _{θJB} | Junction-to-board thermal resistance | 82.7 | 18.1 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 1.3 | 1.6 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 81.1 | 18.2 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | 5.2 | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

 over recommended operating free-air temperature range, $V_{BAT} = 1.2\text{ V}$, $EN = V_{BAT}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--|------|----------------------|------|---------------|
| V_I | Minimum input voltage for start-up | $R_L = 33\ \Omega$ | | 0.85 | 0.9 | V |
| | | $R_L = 3\ \text{k}\Omega$, $T_A = 25\ ^\circ\text{C}$ | 0.8 | | | |
| | Input voltage once started | $I_O = 100\ \text{mA}$ | 0.8 | | | |
| V_O | Programmable output voltage range | TPS61010, $I_{OUT} = 100\ \text{mA}$ | 1.5 | | 3.3 | V |
| | | TPS61011, $0.8\ \text{V} < V_I < V_O$, $I_O = 0$ to $100\ \text{mA}$ | 1.45 | 1.5 | 1.55 | V |
| | TPS61012, $0.8\ \text{V} < V_I < V_O$, $I_O = 0$ to $100\ \text{mA}$ | 1.74 | 1.8 | 1.86 | V | |
| | TPS61013, $0.8\ \text{V} < V_I < V_O$, $I_O = 0$ to $100\ \text{mA}$ | 2.42 | 2.5 | 2.58 | V | |
| | TPS61013, $1.6\ \text{V} < V_I < V_O$, $I_O = 0$ to $200\ \text{mA}$ | 2.42 | 2.5 | 2.58 | V | |
| | TPS61014, $0.8\ \text{V} < V_I < V_O$, $I_O = 0$ to $100\ \text{mA}$ | 2.72 | 2.8 | 2.88 | V | |
| | TPS61014, $1.6\ \text{V} < V_I < V_O$, $I_O = 0$ to $200\ \text{mA}$ | 2.72 | 2.8 | 2.88 | V | |
| | TPS61015, $0.8\ \text{V} < V_I < V_O$, $I_O = 0$ to $100\ \text{mA}$ | 2.9 | 3.0 | 3.1 | V | |
| | TPS61015, $1.6\ \text{V} < V_I < V_O$, $I_O = 0$ to $200\ \text{mA}$ | 2.9 | 3.0 | 3.1 | V | |
| | TPS61016, $0.8\ \text{V} < V_I < V_O$, $I_O = 0$ to $100\ \text{mA}$ | 3.2 | 3.3 | 3.4 | V | |
| TPS61016, $1.6\ \text{V} < V_I < V_O$, $I_O = 0$ to $200\ \text{mA}$ | 3.2 | 3.3 | 3.4 | V | | |
| I_O | Maximum continuous output current | $V_I > 0.8\ \text{V}$ | 100 | | | mA |
| | | $V_I > 1.8\ \text{V}$ | 250 | | | |
| $I_{(SW)}$ | Switch current limit | TPS61011, once started | 0.39 | 0.48 | | A |
| | | TPS61012, once started | 0.54 | 0.56 | | |
| | | TPS61013, once started | 0.85 | 0.93 | | |
| | | TPS61014, once started | 0.95 | 1.01 | | |
| | | TPS61015, once started | 1 | 1.06 | | |
| | | TPS61016, once started | 1.07 | 1.13 | | |
| $V_{(FB)}$ | Feedback voltage | | 480 | 500 | 520 | mV |
| f | Oscillator frequency | | 420 | 500 | 780 | kHz |
| D | Maximum duty cycle | | 85% | | | |
| $r_{DS(on)}$ | NMOS switch on-resistance | $V_O = 1.5\ \text{V}$ | | 0.37 | 0.51 | Ω |
| | PMOS switch on-resistance | | | 0.45 | 0.54 | |
| $r_{DS(on)}$ | NMOS switch on-resistance | $V_O = 3.3\ \text{V}$ | | 0.2 | 0.37 | Ω |
| | PMOS switch on-resistance | | | 0.3 | 0.45 | |
| | Line regulation ⁽¹⁾ | $V_I = 1.2\ \text{V}$ to $1.4\ \text{V}$, $I_O = 100\ \text{mA}$ | | 0.3 | | %V |
| | Load regulation ⁽¹⁾ | $V_I = 1.2\ \text{V}$; $I_O = 50\ \text{mA}$ to $100\ \text{mA}$ | | 0.1 | | |
| | Autodischarge switch resistance | | | 300 | 400 | Ω |
| | Residual output voltage after autodischarge | ADEN = V_{BAT} ; EN = GND | | | 0.4 | V |
| V_{IL} | LBI voltage threshold ⁽²⁾ | $V_{(LBI)}$ voltage decreasing | 480 | 500 | 520 | mV |
| | LBI input hysteresis | | | 10 | | mv |
| | LBI input current | | | 0.01 | 0.03 | |
| V_{OL} | LBO output low voltage | $V_{(LBI)} = 0\ \text{V}$, $V_O = 3.3\ \text{V}$, $I_{(OL)} = 10\ \mu\text{A}$ | | 0.04 | 0.2 | V |
| | LBO output leakage current | $V_{(LBI)} = 650\ \text{mV}$, $V_{(LBO)} = V_O$ | | | 0.03 | μA |
| $I_{(FB)}$ | FB input bias current (TPS61010 only) | $V_{(FB)} = 500\ \text{mV}$ | | 0.01 | 0.03 | |
| V_{IL} | EN and ADEN input low voltage | $0.8\ \text{V} < V_{BAT} < 3.3\ \text{V}$ | | $0.2 \times V_{BAT}$ | | V |

(1) Line and load regulation is measured as a percentage deviation from the nominal value (i.e., as percentage deviation from the nominal output voltage). For line regulation, x %/V stands for $\pm x\%$ change of the nominal output voltage per 1-V change on the input/supply voltage. For load regulation, y% stands for $\pm y\%$ change of the nominal output voltage per the specified current change.

(2) For proper operation the voltage at LBI may not exceed the voltage at V_{BAT} .

Electrical Characteristics (continued)

 over recommended operating free-air temperature range, V_{BAT} = 1.2 V, EN = V_{BAT} (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|--|------------------------|------|------|------|
| V _{IH} | EN and ADEN input high voltage | 0.8 V < V _{BAT} < 3.3 V | 0.8 × V _{BAT} | | | V |
| | EN and ADEN input current | EN and ADEN = GND or V _{BAT} | | 0.01 | 0.03 | μA |
| I _q | Quiescent current into pins V _{BAT} /SW and V _{OUT} | I _L = 0 mA, V _{EN} = V _I | V _{BAT} /SW | 31 | 46 | μA |
| | | | V _O | 5 | 8 | |
| I _{off} | Shutdown current from power source | V _{EN} = 0 V, ADEN = V _{BAT} , T _A = 25°C | | 1 | 3 | μA |

7.6 Typical Characteristics

7.6.1 Table of Graphs

| | | FIGURE |
|---------------------------------|---|---------------------------|
| Maximum output current | vs Input voltage for $V_O = 2.5\text{ V}, 3.3\text{ V}$ | Figure 1 |
| | vs Input voltage for $V_O = 1.5\text{ V}, 1.8\text{ V}$ | Figure 2 |
| Efficiency | vs Output current for $V_I = 1.2\text{ V}, V_O = 1.5\text{ V}, L1 = \text{Sumida CDR74} - 10\text{ }\mu\text{H}$ | Figure 3 |
| | vs Output current for $V_I = 1.2\text{ V}, V_O = 2.5\text{ V}, L1 = \text{Sumida CDR74} - 10\text{ }\mu\text{H}$ | Figure 4 |
| | vs Output current for $V_{IN} = 1.2\text{ V}, V_O = 3.3\text{ V}, L1 = \text{Sumida CDR74} - 10\text{ }\mu\text{H}$ | Figure 5 |
| | vs Output current for $V_I = 2.4\text{ V}, V_O = 3.3\text{ V}, L1 = \text{Sumida CDR74} - 10\text{ }\mu\text{H}$ | Figure 6 |
| | vs Input voltage for $I_O = 10\text{ mA}, I_O = 100\text{ mA}, I_O = 200\text{ mA}, V_O = 3.3\text{ V}, L1 = \text{Sumida CDR74} - 10\text{ }\mu\text{H}$ | Figure 7 |
| | TPS61016, $V_{BAT} = 1.2\text{ V}, I_O = 100\text{ mA}$ | Figure 8 |
| | Sumida CDRH6D38 - 10 μH | |
| | Sumida CDRH5D18 - 10 μH | |
| | Sumida CDRH74 - 10 μH | |
| | Sumida CDRH74B - 10 μH | |
| | Coilcraft DS 1608C - 10 μH | |
| | Coilcraft DO 1608C - 10 μH | |
| | Coilcraft DO 3308P - 10 μH | |
| | Coilcraft DS 3316 - 10 μH | |
| | Coiltronics UP1B - 10 μH | |
| | Coiltronics UP2B - 10 μH | |
| | Murata LQS66C - 10 μH | |
| Murata LQN6C - 10 μH | | |
| TDK SLF 7045 - 10 μH | | |
| TDK SLF 7032 - 10 μH | | |
| Output voltage | vs Output current TPS61011 | Figure 9 |
| | vs Output current TPS61013 | Figure 10 |
| | vs Output current TPS61016 | Figure 11 |
| Minimum supply start-up voltage | vs Load resistance | Figure 12 |
| No-load supply current | vs Input voltage | Figure 13 |
| Shutdown supply current | vs Input voltage | Figure 14 |
| Switch current limit | vs Output voltage | Figure 15 |

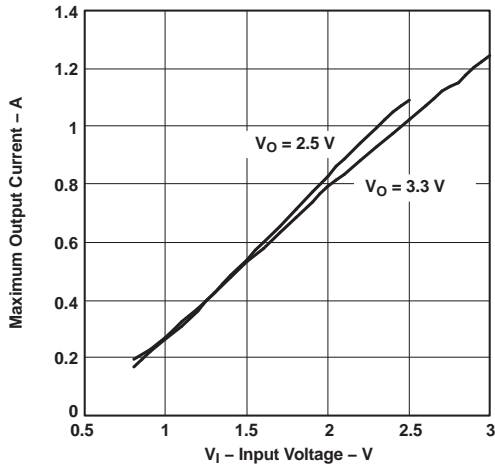


Figure 1. Maximum Output Current vs Input Voltage

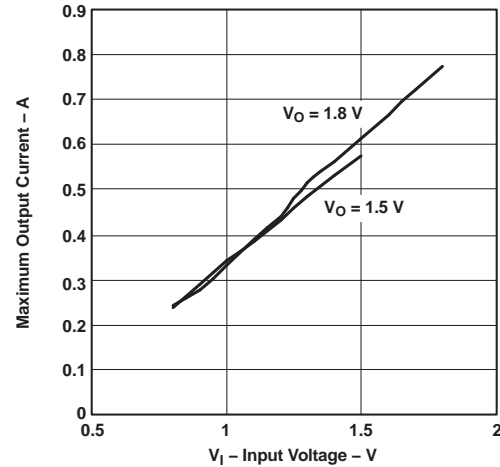


Figure 2. Maximum Output Current vs Input Voltage

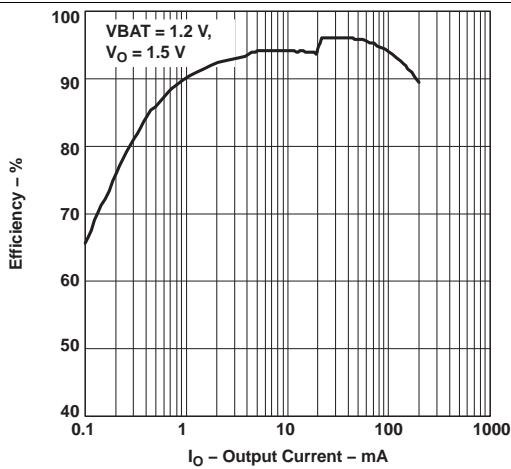


Figure 3. Efficiency vs Output Current

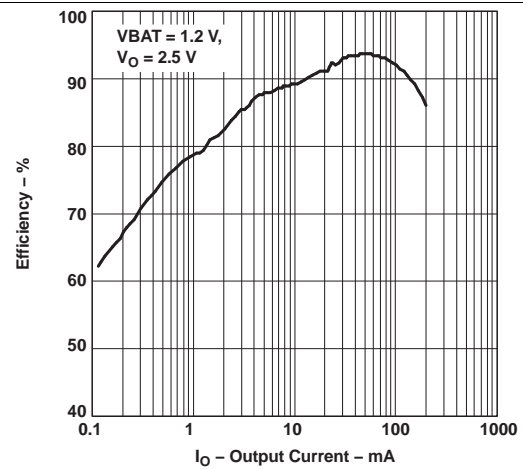


Figure 4. Efficiency vs Output Current

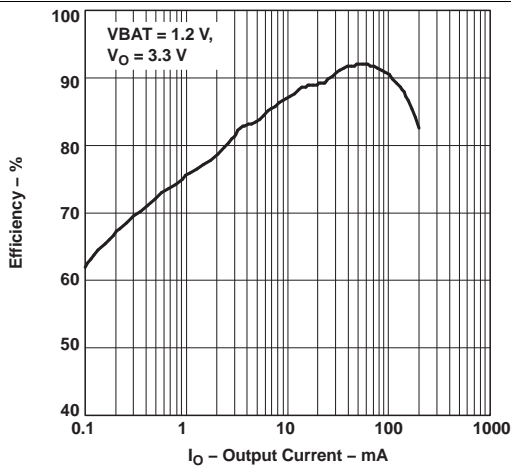


Figure 5. Efficiency vs Output Current

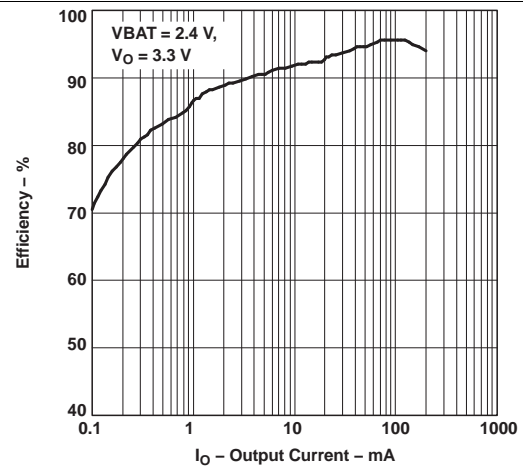


Figure 6. Efficiency vs Output Current

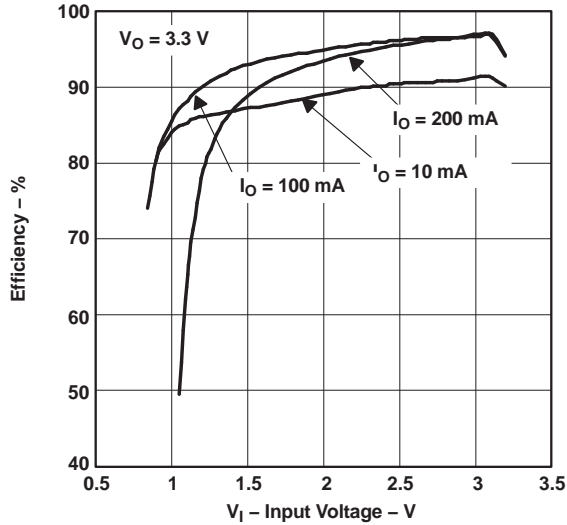


Figure 7. Efficiency vs Input Voltage

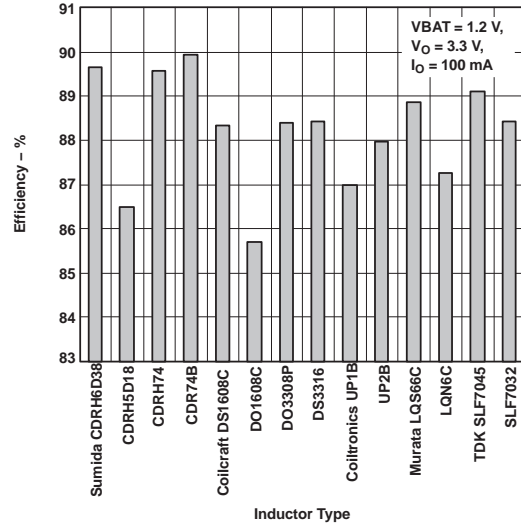


Figure 8. Efficiency vs Inductor Type

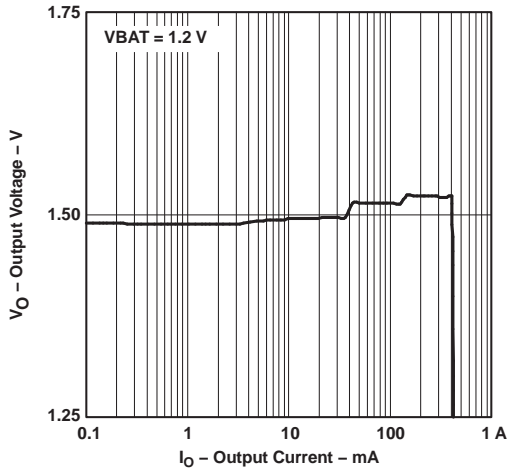


Figure 9. Output Voltage vs Output Current

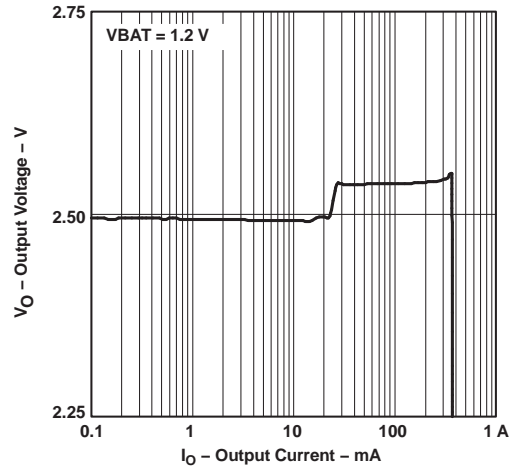


Figure 10. Output Voltage vs Output Current

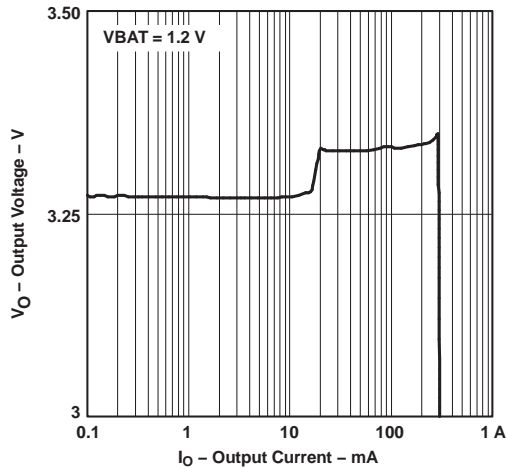


Figure 11. Output Voltage vs Output Current

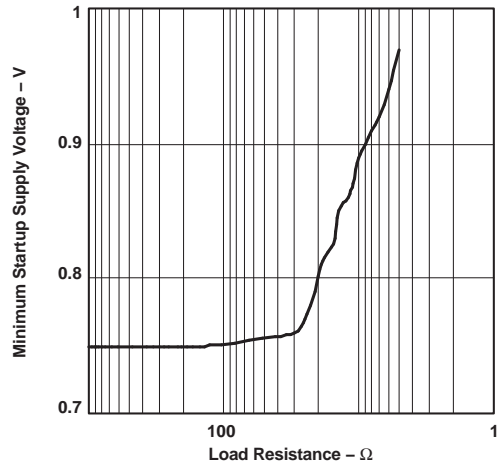


Figure 12. Minimum Start-Up Supply Voltage vs Load Resistance

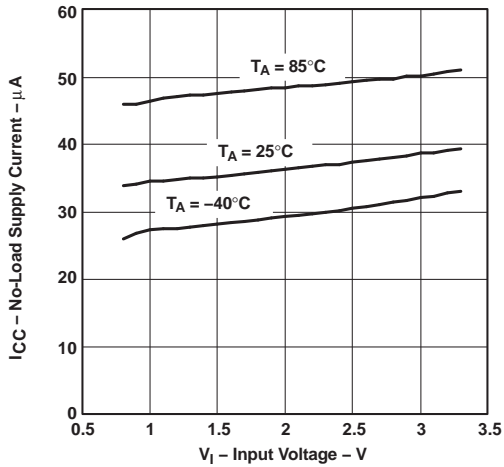


Figure 13. No-Load Supply Current vs Input Voltage

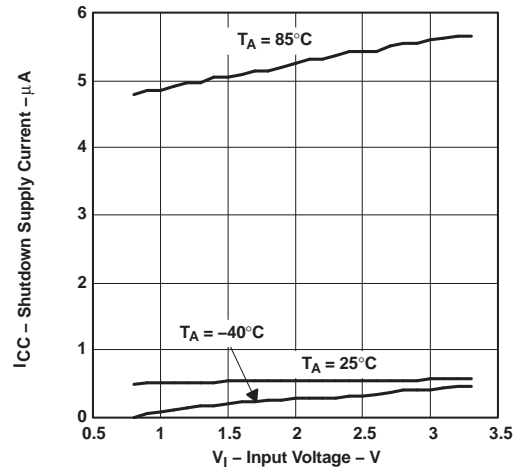


Figure 14. Shutdown Supply Current vs Input Voltage

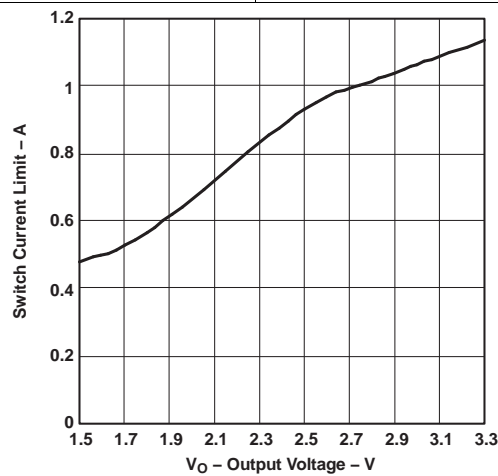
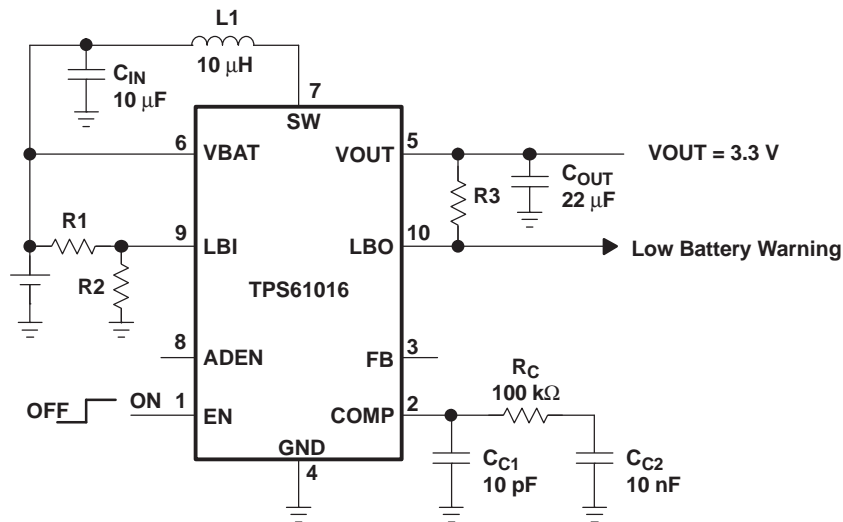


Figure 15. Switch Current Limit vs Output Voltage

8 Parameter Measurement Information



List of Components:

IC1: Only Fixed Output Versions
(Unless Otherwise Noted)

L1: SUMIDA CDRH6D38 – 100

C_{IN}: X7R/X5R Ceramic

C_{OUT}: X7R/X5R Ceramic

Figure 16. Circuit Used for Typical Characteristics Measurements

9 Detailed Description

9.1 Overview

The converter is based on a fixed frequency, current mode, pulse-width-modulation (PWM) Boost converter with the synchronous rectifier built in. The device limits the current through the power switch on a pulse by pulse basis. TPS6101x enters a power save-mode at light load. In this mode, TPS6101x only switches if the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses, and goes again into power save-mode once the output voltage exceeds a set threshold voltage. The load is completely isolated from the battery when the device shutdown. An auto-discharge function allows discharging the output capacitor during shutdown. The auto-discharge function is enabled if this pin is connected to VBAT, and it is disabled if ADEN is tied to GND.

9.2 Functional Block Diagram

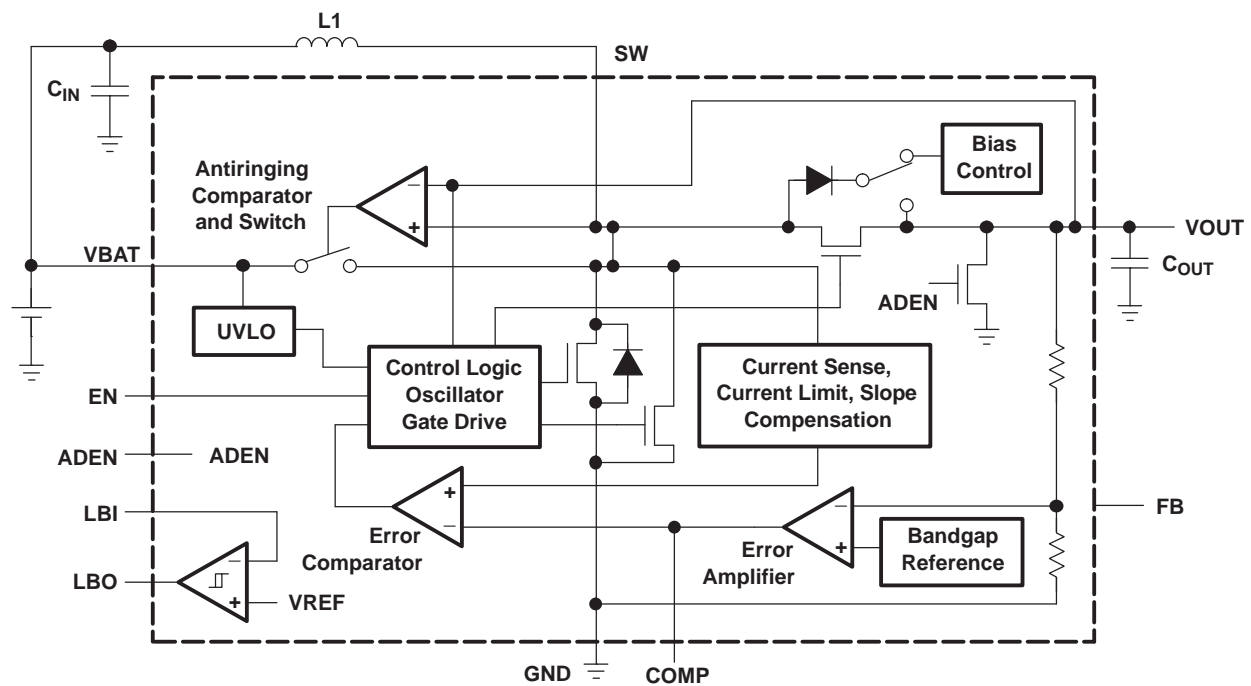
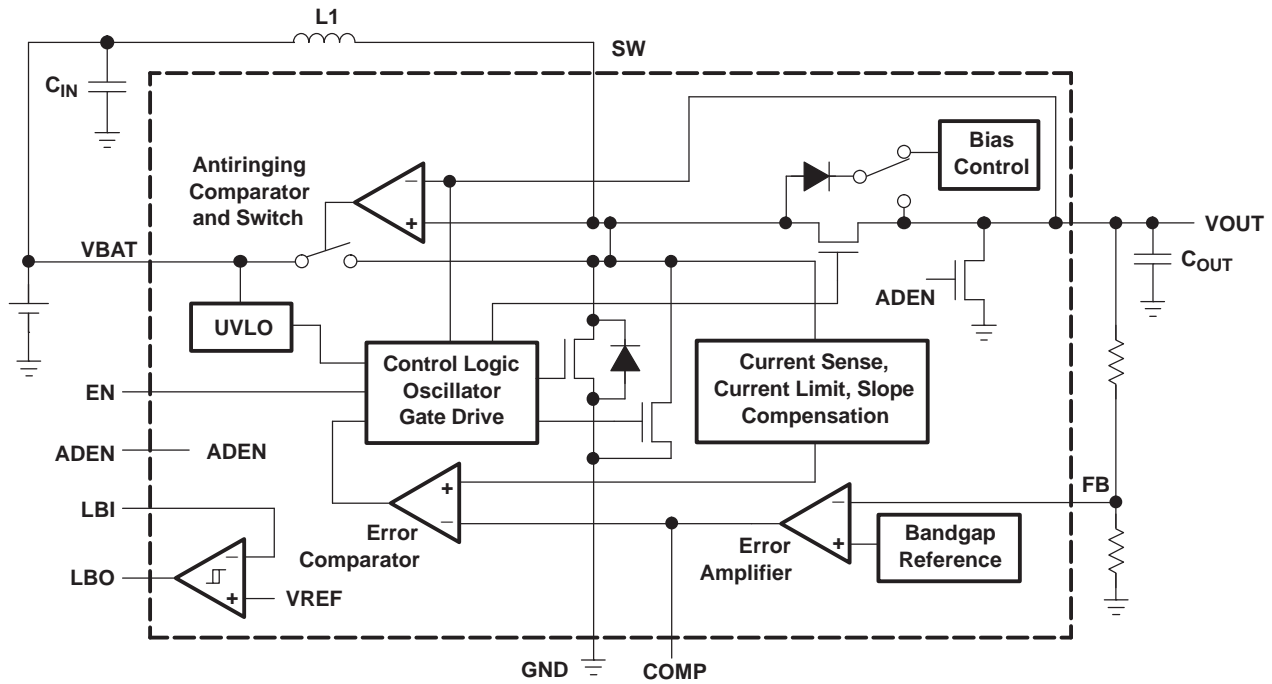


Figure 17. Fixed Output Voltage Versions TPS61011 to TPS61016

Functional Block Diagram (continued)

Figure 18. Adjustable Output Voltage Version TPS61010

9.3 Feature Description

9.3.1 Controller Circuit

The device is based on a current-mode control topology using a constant frequency pulse-width modulator to regulate the output voltage. The controller limits the current through the power switch on a pulse by pulse basis. The current-sensing circuit is integrated in the device, therefore, no additional components are required. Due to the nature of the boost converter topology used here, the peak switch current is the same as the peak inductor current, which will be limited by the integrated current limiting circuits under normal operating conditions.

The control loop must be externally compensated with an R-C-C network connected to the COMP-pin.

9.3.2 Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. There is no additional Schottky diode required. Because the device uses an integrated low $r_{DS(on)}$ PMOS switch for rectification, the power conversion efficiency reaches 95%.

A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device, however, uses a special circuit to disconnect the backgate diode of the high-side PMOS and so, disconnects the output circuitry from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer, is that the battery is not depleted during shutdown of the converter. So, no additional effort has to be made by the system designer to ensure disconnection of the battery from the output of the converter. Therefore, design performance will be increased without additional costs and board space.

Feature Description (continued)

9.3.3 Power-Save Mode

The TPS61010 is designed for high efficiency over a wide output current range. Even at light loads, the efficiency stays high because the switching losses of the converter are minimized by effectively reducing the switching frequency. The controller enters a powersave-mode if certain conditions are met. In this mode, the controller only switches on the transistor if the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses, and goes again into powersave-mode once the output voltage exceeds a set threshold voltage.

9.3.4 Device Enable

The device is shut down when EN is set to GND. In this mode, the regulator stops switching, all internal control circuitry including the low-battery comparator, is switched off, and the load is disconnected from the input (as described above in the synchronous rectifier section). This also means that the output voltage may drop below the input voltage during shutdown.

The device is put into operation when EN is set high. During start-up of the converter, the duty cycle is limited in order to avoid high peak currents drawn from the battery. The limit is set internally by the current limit circuit and is proportional to the voltage on the COMP-pin.

9.3.5 Undervoltage Lockout (UVLO)

The UVLO function prevents the device from starting up if the supply voltage on VBAT is lower than approximately 0.7 V. This UVLO function is implemented in order to prevent the malfunctioning of the converter. When in operation and the battery is being discharged, the device will automatically enter the shutdown mode if the voltage on VBAT drops below approximately 0.7 V.

9.3.6 Autodischarge

The autodischarge function is useful for applications where the supply voltage of a μC , μP , or memory has to be removed during shutdown in order to ensure a defined state of the system.

The autodischarge function is enabled when the ADEN is set high, and is disabled when the ADEN is set to GND. When the autodischarge function is enabled, the output capacitor will be discharged after the device is shut down by setting EN to GND. The capacitors connected to the output are discharged by an integrated switch of 300 Ω , hence the discharge time depends on the total output capacitance. The residual voltage on VOUT is less than 0.4 V after autodischarge.

9.3.7 Low-Battery Detector Circuit (LBI and LBO)

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO-pin is high impedance. The LBO-pin goes active low when the voltage on the LBI-pin decreases below the set threshold voltage of 500 mV \pm 15 mV, which is equal to the internal reference voltage. The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI-pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI-pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI-threshold.

If the low-battery detection circuit is not used, the LBI-pin should be connected to GND (or to VBAT) and the LBO-pin can be left unconnected. Do not let the LBI-pin float.

9.3.8 Antiringing Switch

The device integrates a circuit that removes the ringing that typically appears on the SW-node when the converter enters the discontinuous current mode. In this case, the current through the inductor ramps to zero and the integrated PMOS switch turns off to prevent a reverse current from the output capacitors back to the battery. Due to remaining energy that is stored in parasitic components of the semiconductors and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage internally to V_{BAT} and therefore, dampens this ringing.

Feature Description (continued)

9.3.9 Adjustable Output Voltage

The devices with fixed output voltages are trimmed to operate with an output voltage accuracy of $\pm 3\%$.

The accuracy of the adjustable version is determined by the accuracy of the internal voltage reference, the controller topology, and the accuracy of the external resistor. The reference voltage has an accuracy of $\pm 4\%$ over line, load, and temperature. The controller switches between fixed frequency and pulse-skip mode, depending on load current. This adds an offset to the output voltage that is equivalent to 1% of V_O . The tolerance of the resistors in the feedback divider determine the total system accuracy.

9.4 Device Functional Modes

Table 1. TPS6101x Operation Modes

| MODE | DESCRIPTION | CONDITION |
|------|-------------------------------------|------------|
| PWM | Boost in normal switching operation | Heavy load |
| PFM | Boost in power save operation | Light load |

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The devices are designed to operate from an input voltage supply range between 0.9 V and 3.3 V with a maximum switch current limit up to 1300mA. The devices operate in PWM mode from the medium to heavy load conditions and in power save mode at light load condition. In PWM mode the TPS6101x converter operates with the nominal switching frequency of 500kHz. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range.

10.2 Typical Applications

10.2.1 1.8-mm Maximum Height Power Supply With Single Battery Cell Input Using Low Profile Components

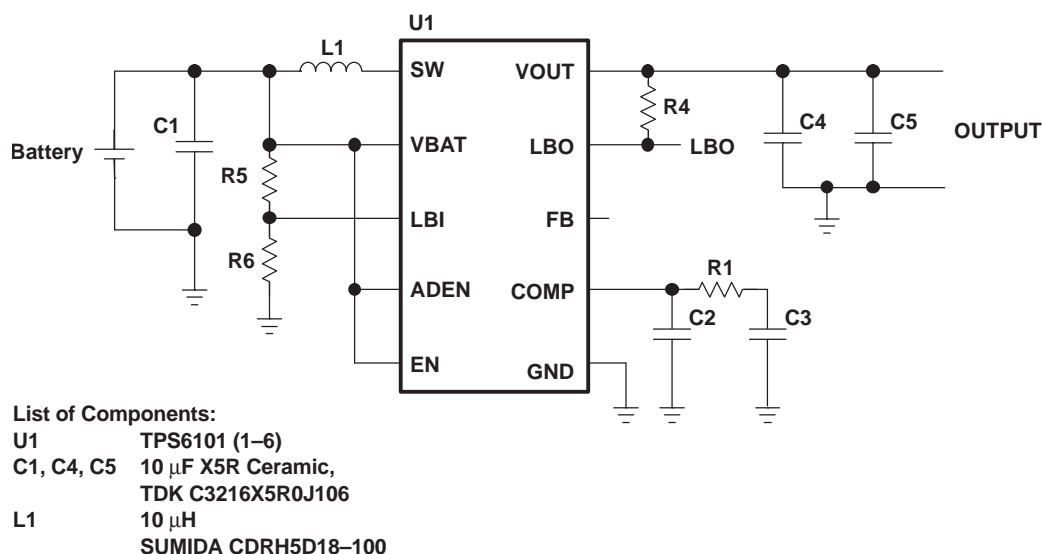


Figure 19. 1.8-mm Maximum Height Power Supply With Single Battery Cell Input Using Low Profile Components Schematic

10.2.1.1 Design Requirements

Use the following typical application design procedure to select external components values for the TPS6101x device.

The output voltage of the adjustable output voltage version changes with the output current. Due to device-internal ground shift, which is caused by the high switch current, the internal reference voltage and the voltage on the FB pin increases with increasing output current. Since the output voltage follows the voltage on the FB pin, the output voltage rises as well with a rate of 1 mV per 1-mA output current increase. Additionally, when the converter goes into pulse-skip mode at output currents around 5 mA and lower, the output voltage drops due to the hysteresis of the controller. This hysteresis is about 15 mV, measured on the FB pin.

10.2.1.2.2 Programming the Low Battery Comparator Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 μ A, the voltage across R2 is equal to the reference voltage that is generated on-chip, which has a value of 500 mV \pm 15 mV. The recommended value for R2 is therefore in the range of 500 k Ω . From that, the value of resistor R1, depending on the desired minimum battery voltage V_{BAT} , can be calculated using [Equation 2](#).

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{REF}} - 1 \right) = 500k\Omega \times \left(\frac{V_{BAT}}{500mV} - 1 \right) \quad (2)$$

For example, if the low-battery detection circuit should flag an error condition on the LBO output pin at a battery voltage of 1 V, a resistor in the range of 500 k Ω should be chosen for R1. The output of the low battery comparator is a simple open-drain output that goes active low if the battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 M Ω , and should only be pulled up to the V_O . If not used, the LBO pin can be left floating or tied to GND.

10.2.1.2.3 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor is required and a storage capacitor at the output. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS61010's switch is 1100 mA at an output voltage of 3.3 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_O). Estimation of the maximum average inductor current can be done using [Equation 3](#).

$$I_L = I_{OUT} \times \frac{V_O}{V_{BAT} \times 0.8} \quad (3)$$

For example, for an output current of 100 mA at 3.3 V, at least 515-mA of current flows through the inductor at a minimum input voltage of 0.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs.

With those parameters, it is possible to calculate the value for the inductor by using [Equation 4](#).

$$L = \frac{V_{BAT} \times (V_{OUT} - V_{BAT})}{\Delta I_L \times f \times V_{OUT}} \quad (4)$$

Parameter 7 is the switching frequency and ΔI_L is the ripple current in the inductor, that is, $20\% \times I_L$.

In this example, the desired inductor has the value of 12 μ H. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. Care must be taken that load transients and losses in the circuit can lead to higher currents as estimated in [Equation 3](#). Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers were tested. All work with the TPS6101x converter within their specified parameters:

Table 3. Recommended Inductors

| VENDOR | RECOMMENDED INDUCTOR SERIES |
|-------------|-----------------------------|
| Sumida | Sumida CDR74B |
| | Sumida CDRH74 |
| | Sumida CDRH5D18 |
| | Sumida CDRH6D38 |
| Coilcraft | Coilcraft DO 1608C |
| | Coilcraft DS 1608C |
| | Coilcraft DS 3316 |
| | Coilcraft DT D03308P |
| Coiltronics | Coiltronics UP1B |
| | Coiltronics UP2B |
| Murata | Murata LQS66C |
| | Murata LQN6C |
| TDK | TDK SLF 7045 |
| | TDK SLF 7032 |

10.2.1.2.4 Capacitor Selection

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using [Equation 5](#).

$$C_{\min} = \frac{I_{\text{OUT}} \times (V_{\text{OUT}} - V_{\text{BAT}})}{f \times \Delta V \times V_{\text{OUT}}} \quad (5)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 15 mV, a minimum capacitance of 10 μF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using [Equation 6](#).

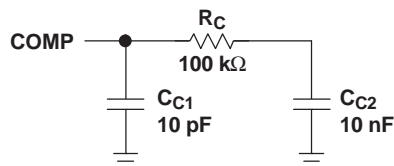
$$\Delta V_{\text{ESR}} = I_{\text{OUT}} \times R_{\text{ESR}} \quad (6)$$

An additional ripple of 30 mV is the result of using a tantalum capacitor with a low ESR of 300 m Ω . The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 45 mV. It is possible to improve the design by enlarging the capacitor or using smaller capacitors in parallel to reduce the ESR or by using better capacitors with lower ESR, like ceramics. For example, a 10 μF ceramic capacitor with an ESR of 50 m Ω is used on the evaluation module (EVM). Tradeoffs must be made between performance and costs of the converter circuit.

A 10- μF input capacitor is recommended to improve transient behavior of the regulator. A ceramic capacitor or a tantalum capacitor with a 100 nF ceramic capacitor in parallel placed close to the IC is recommended.

10.2.1.2.5 Compensation of the Control Loop

An R/C/C network must be connected to the COMP pin in order to stabilize the control loop of the converter. Both the pole generated by the inductor L1 and the zero caused by the ESR and capacitance of the output capacitor must be compensated. The network shown in [Figure 21](#) satisfies these requirements.


Figure 21. Compensation of Control Loop

Resistor R_C and capacitor C_{C2} depend on the chosen inductance. For a 10 μH inductor, the capacitance of C_{C2} should be chosen to 10 nF, or in other words, if the inductor is **XX** μH , the chosen compensation capacitor should be **XX** nF, the same number value. The value of the compensation resistor is then chosen based on the requirement to have a time constant of 1 ms, for the R/C network R_C and C_{C2} , hence for a 33 nF capacitor, a 33 k Ω resistor should be chosen for R_C .

Capacitor C_{C1} depends on the ESR and capacitance value of the output capacitor, and on the value chosen for R_C . Its value is calculated using [Equation 7](#).

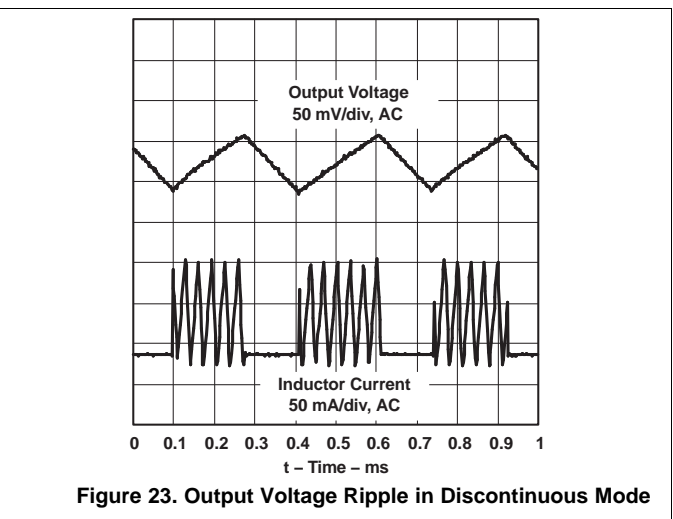
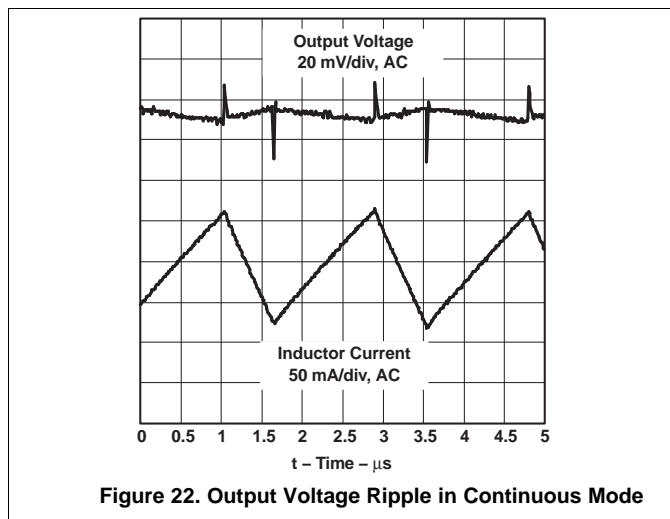
$$C_{C1} = \frac{C_{\text{OUT}} \times \text{ESR}_{\text{COUT}}}{R_C} \quad (7)$$

For a selected output capacitor of 22 μF with an ESR of 0.2 Ω , an R_C of 33 k Ω , the value of C_{C1} is in the range of 100 pF.

Table 4. Recommended Compensation Components

| INDUCTOR [μH] | OUTPUT CAPACITOR | | RC [k Ω] | CC1 [pF] | CC2 [nF] |
|----------------------------|-------------------------------|------------------|------------------|----------|----------|
| | CAPACITANCE [μF] | ESR [Ω] | | | |
| 33 | 22 | 0.2 | 33 | 120 | 33 |
| 22 | 22 | 0.3 | 47 | 150 | 22 |
| 10 | 22 | 0.4 | 100 | 100 | 10 |
| 10 | 10 | 0.1 | 100 | 10 | 10 |

10.2.1.3 Application Curves



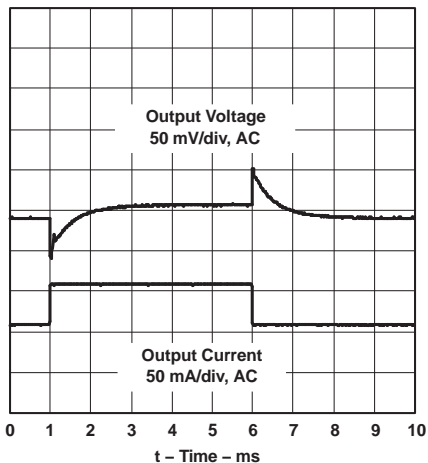


Figure 24. Load Transient Response

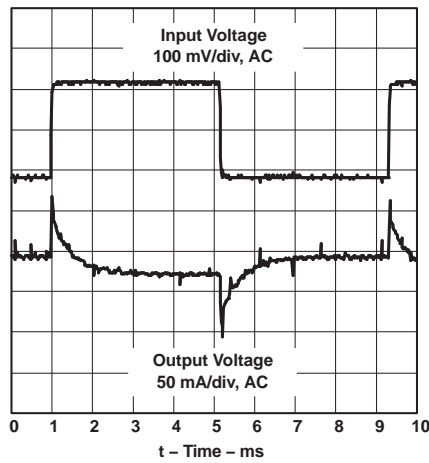


Figure 25. Line Transient Response

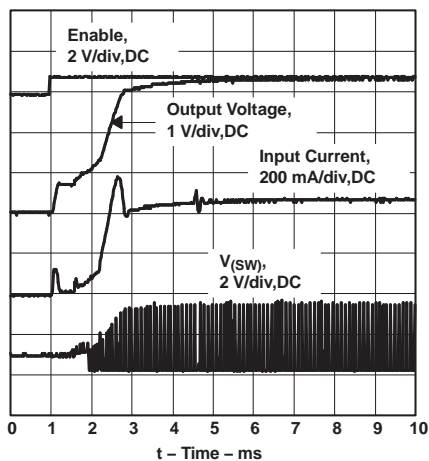


Figure 26. Converter Start-Up Time After Enable

10.2.2 250-mA Power Supply With Two Battery Cell Input

TPS6101x application schematic of 2 Cell AA Battery Input and >250-mA output current.

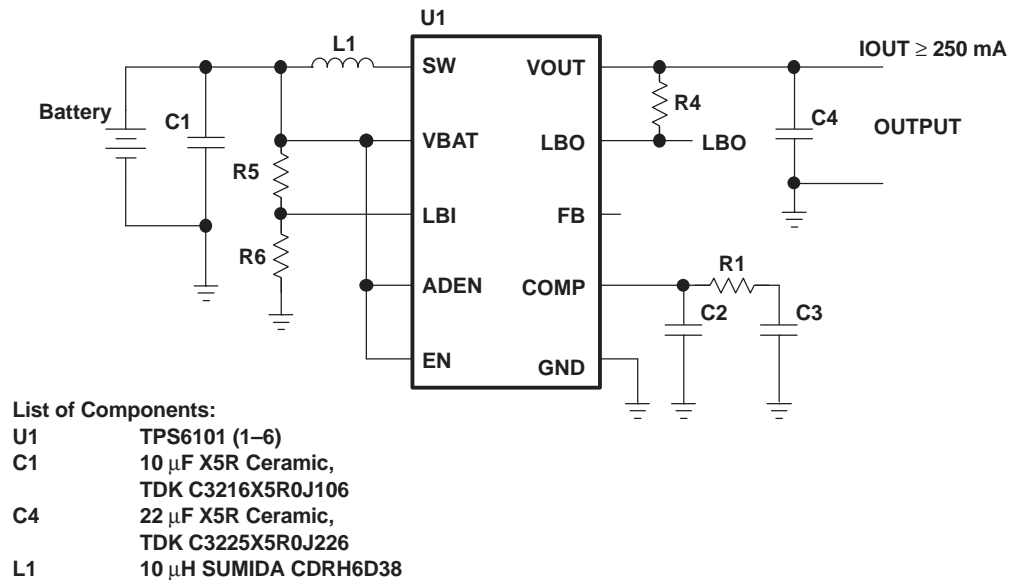
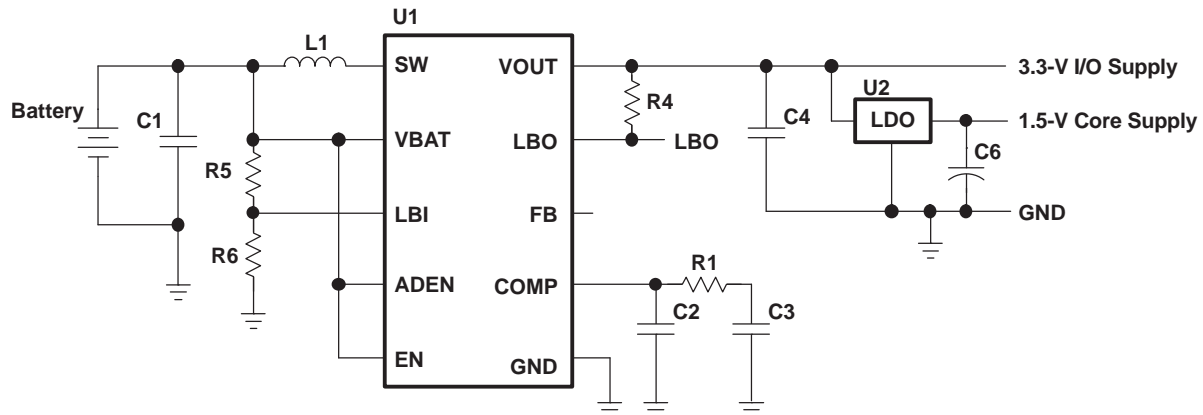


Figure 27. 250-mA Power Supply With Two Battery Cell Input

10.2.3 Dual Output Voltage Power Supply for DSPs

TPS6101x application schematic with 3.3V_{out} of I/O supply and post LDO 1.5V_{out} of DSP core supply.



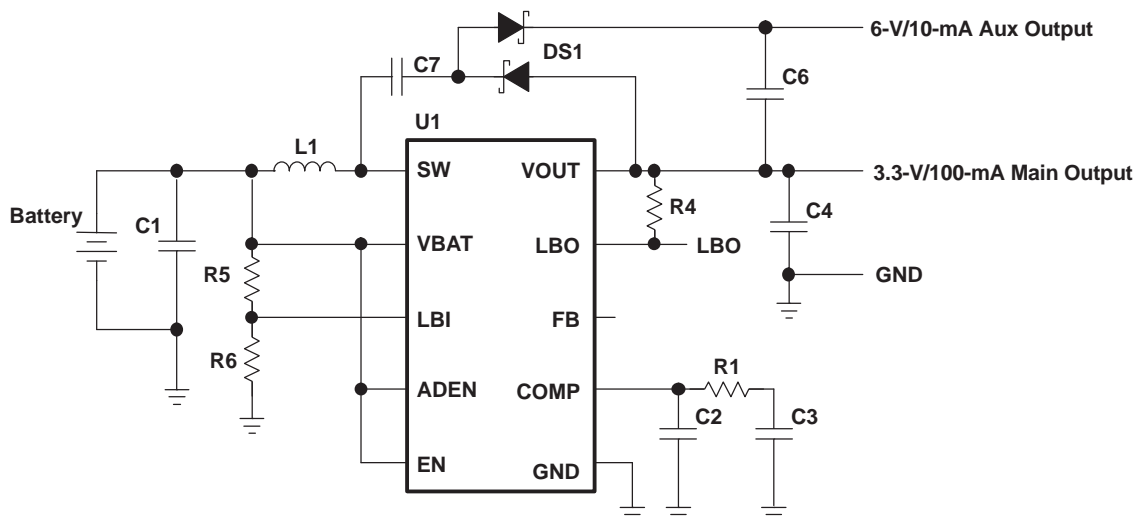
List of Components:

| | |
|----|---|
| U1 | TPS61016 |
| U2 | TPS76915 |
| C1 | 10 µF X5R Ceramic, TDK C3216X5R0J106 |
| C4 | 22 µF X5R Ceramic, TDK C3225X5R0J226 |
| L1 | 10 µH SUMIDA CDRH6D38 |

Figure 28. Dual Output Voltage Power Supply for DSPs

10.2.4 Power Supply With Auxiliary Positive Output Voltage

TPS6101x application schematic of 3.3V_{out} and 6V_{out} with charge pump.



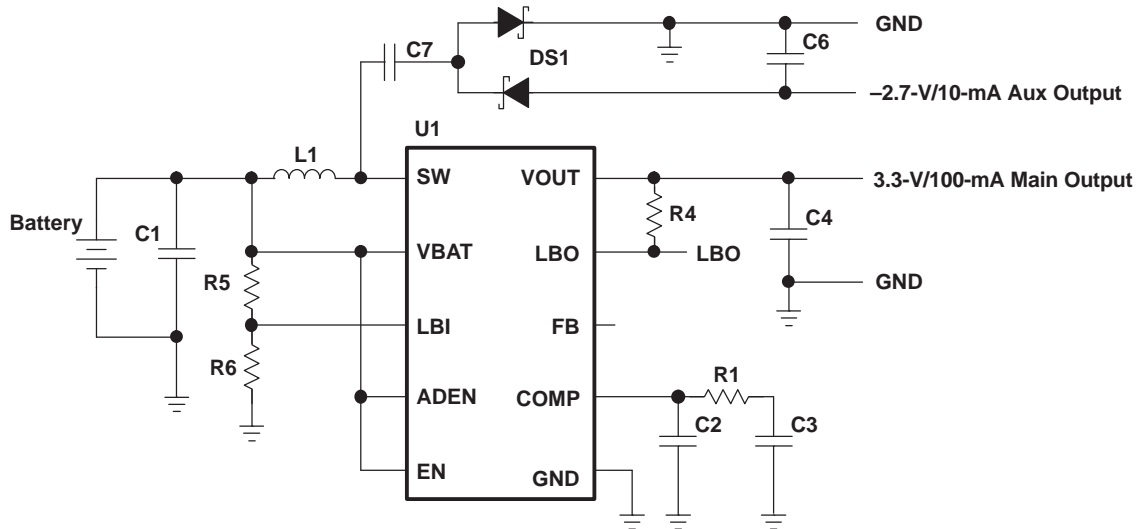
List of Components:

| | |
|-----|--|
| U1 | TPS61016 |
| DS1 | BAT54S |
| C1 | 10 µF X5R Ceramic, TDK C3216X5R0J106 |
| C4 | 22 µF X5R Ceramic, TDK C3225X5R0J226, |
| C6 | 1 µF X5R Ceramic, |
| C7 | 0.1 µF X5R Ceramic, |
| L1 | 10 µH SUMIDA CDRH6D38–100 |

Figure 29. Power Supply With Auxiliary Positive Output Voltage

10.2.5 Power Supply With Auxiliary Negative Output Voltage

TPS6101x application schematic of 3.3V_{out} and -2.7V_{out} with charge pump.



List of Components:

| | |
|-----|---|
| U1 | TPS61016 |
| DS1 | BAT54S |
| C1 | 10 μ F X5R Ceramic, TDK C3216X5R0J106 |
| C4 | 22 μ F X5R Ceramic, TDK C3225X5R0J226, |
| C6 | 1 μ F X5R Ceramic, |
| C7 | 0.1 μ F X5R Ceramic, |
| L1 | 10 μ H SUMIDA CDRH6D38-100 |

Figure 30. Power Supply With Auxiliary Negative Output Voltage

10.2.6 TPS6101x EVM Circuit Diagram

TPS6101x application schematic of the standard EVM configuration.

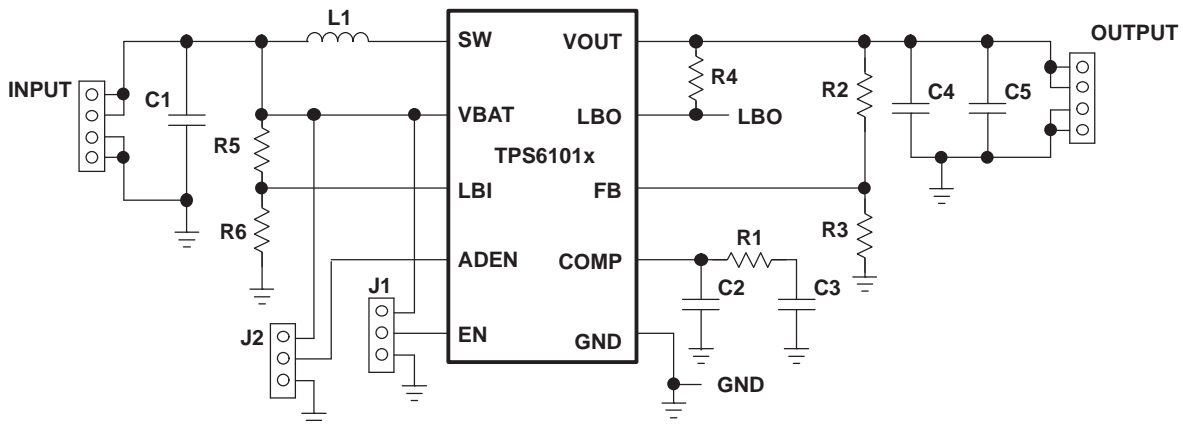


Figure 31. TPS6101x EVM Circuit Diagram

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 0.9 V and 3.3 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 μF is a typical choice.

12 Layout

12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems.

Therefore, use wide and short traces for the main current path as indicated in **bold** in Figure 32. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node as shown in Figure 32 to minimize the effects of ground noise. The compensation circuit and the feedback divider should be placed as close as possible to the IC. To layout the control ground, it is recommended to use short traces as well, separated from the power ground traces. Connect both grounds close to the ground pin of the IC as indicated in the layout diagram in Figure 32. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

12.2 Layout Example

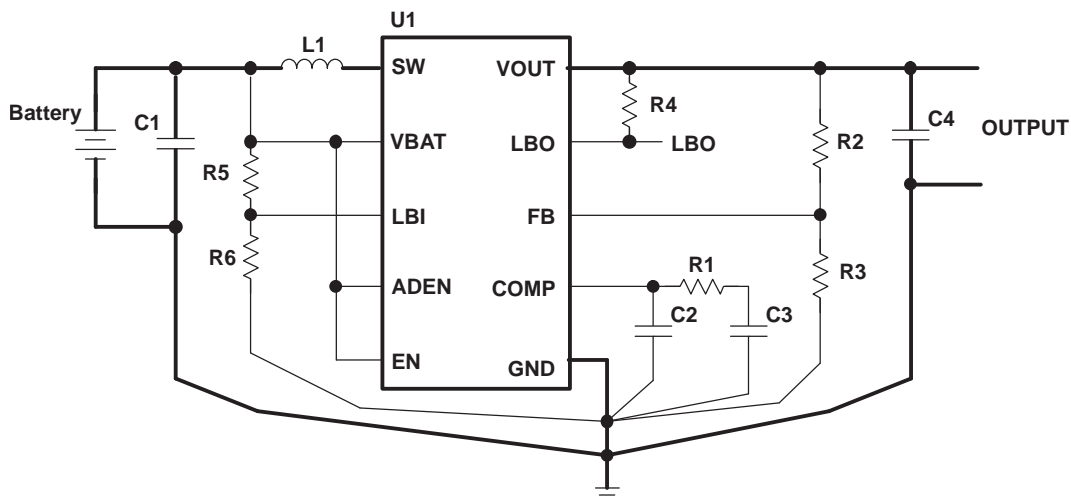


Figure 32. Layout Diagram

Layout Example (continued)

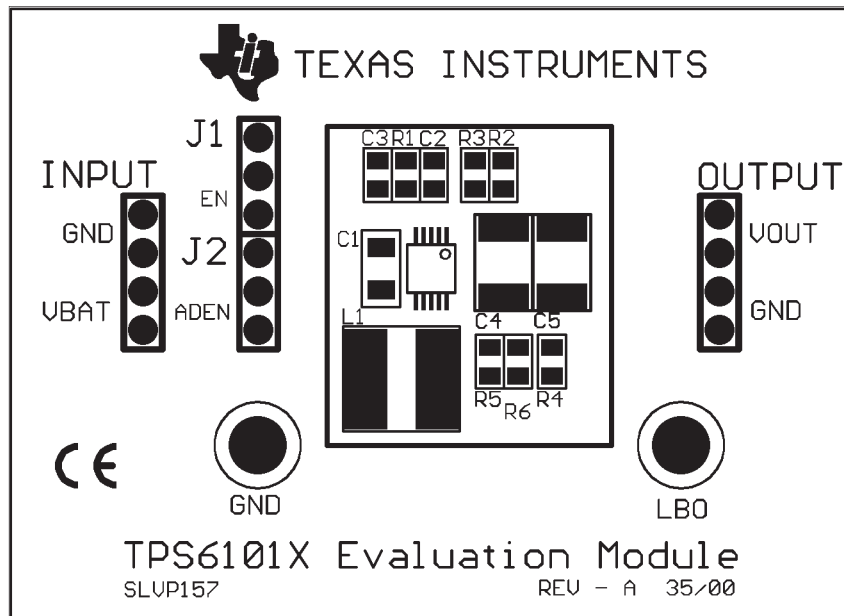


Figure 33. TPS6101x EVM Component Placement (Actual Size: 55.9 mm x 40.6 mm)

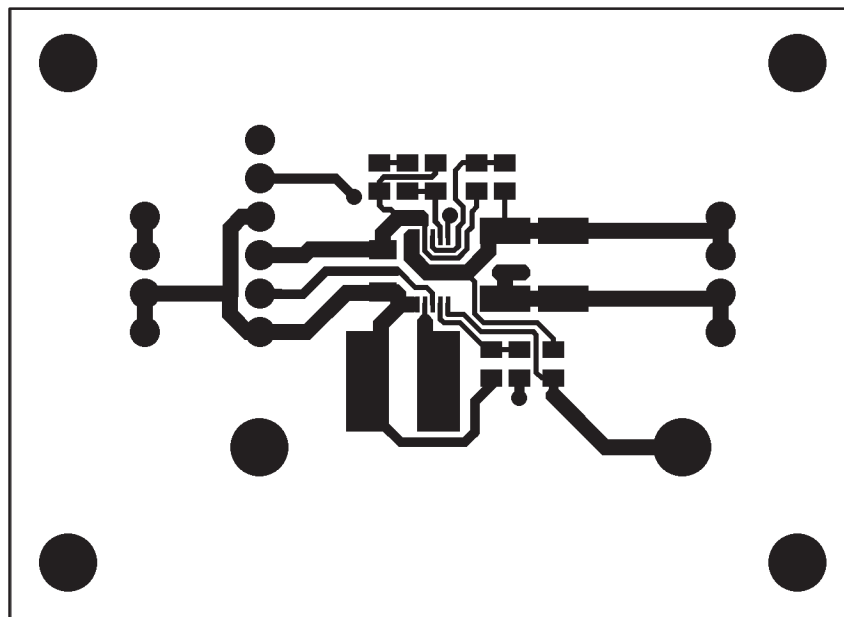


Figure 34. TPS6101x EVM Top Layer Layout (Actual Size: 55.9 mm x 40.6 mm)

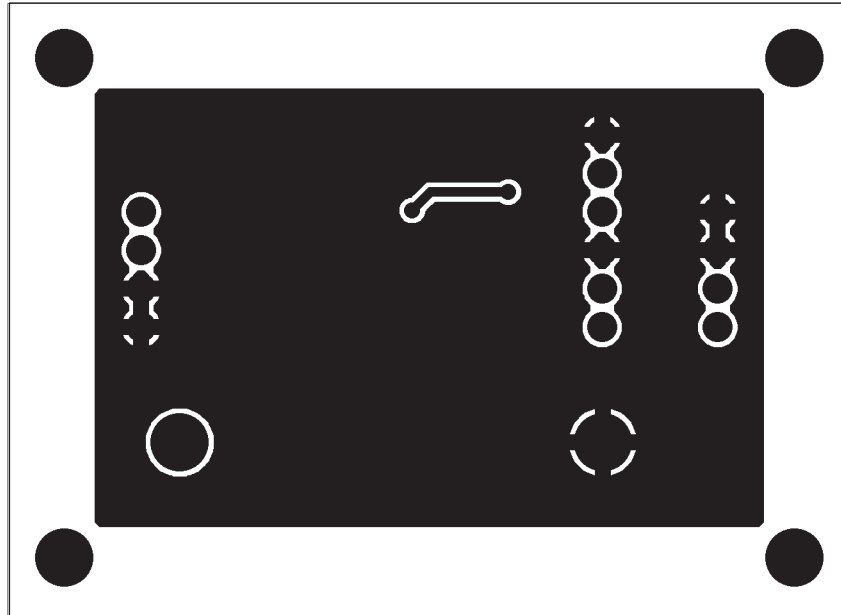
Layout Example (continued)


Figure 35. TPS6101x EVM Bottom Layer Layout (Actual Size: 55.9 mm x 40.6 mm)

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PWB design
- Improving the thermal coupling of the component to the PWB
- Introducing airflow in the system

The maximum junction temperature (T_J) of the TPS6101x devices is 125°C. The thermal resistance of the 10-pin MSOP package (DGS) is $R_{\theta JA} = 161.8^\circ\text{C}/\text{W}$. Specified regulator operation is assured to a maximum ambient temperature (T_A) of 85°C. Therefore, the maximum power dissipation is about 247 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(\text{MAX})} = \frac{T_{J(\text{MAX})} - T_A}{R_{\theta JA}} = \frac{125^\circ\text{C} - 85^\circ\text{C}}{161.8^\circ\text{C}/\text{W}} = 247 \text{ mW} \quad (8)$$

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TPS61010 | Click here | Click here | Click here | Click here | Click here |
| TPS61011 | Click here | Click here | Click here | Click here | Click here |
| TPS61012 | Click here | Click here | Click here | Click here | Click here |
| TPS61013 | Click here | Click here | Click here | Click here | Click here |
| TPS61014 | Click here | Click here | Click here | Click here | Click here |
| TPS61015 | Click here | Click here | Click here | Click here | Click here |
| TPS61016 | Click here | Click here | Click here | Click here | Click here |

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS61010DGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AIP | Samples |
| TPS61010DGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AIP | Samples |
| TPS61010DGSRG4 | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AIP | Samples |
| TPS61012DGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AIR | Samples |
| TPS61012DGSG4 | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AIR | Samples |
| TPS61013DGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AIS | Samples |
| TPS61014DGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AIT | Samples |
| TPS61015DGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AIU | Samples |
| TPS61015DGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AIU | Samples |
| TPS61016DGS | ACTIVE | VSSOP | DGS | 10 | 80 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AIV | Samples |
| TPS61016DGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AIV | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

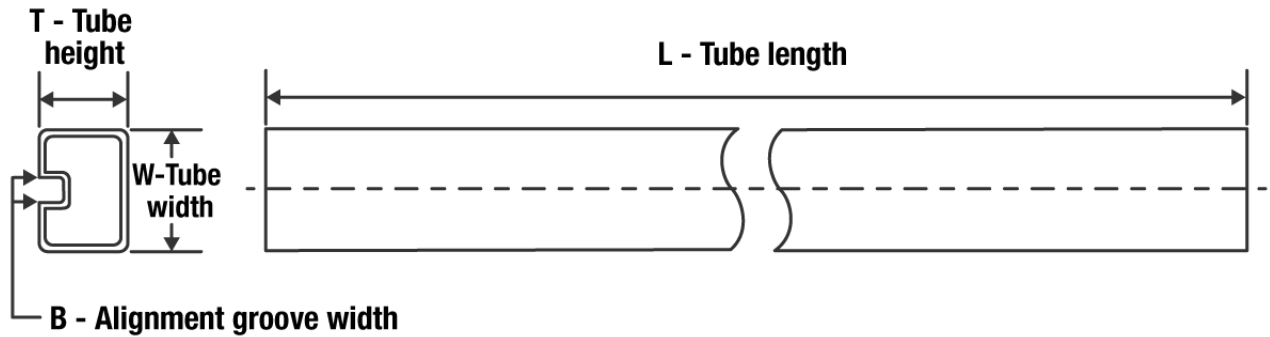

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS61010DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS61010DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS61015DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS61016DGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

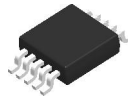
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS61010DGSR | VSSOP | DGS | 10 | 2500 | 358.0 | 335.0 | 35.0 |
| TPS61010DGSR | VSSOP | DGS | 10 | 2500 | 364.0 | 364.0 | 27.0 |
| TPS61015DGSR | VSSOP | DGS | 10 | 2500 | 364.0 | 364.0 | 27.0 |
| TPS61016DGSR | VSSOP | DGS | 10 | 2500 | 364.0 | 364.0 | 27.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS61010DGS | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS61012DGS | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS61012DGSG4 | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS61013DGS | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS61014DGS | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS61015DGS | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |
| TPS61016DGS | DGS | VSSOP | 10 | 80 | 330 | 6.55 | 500 | 2.88 |

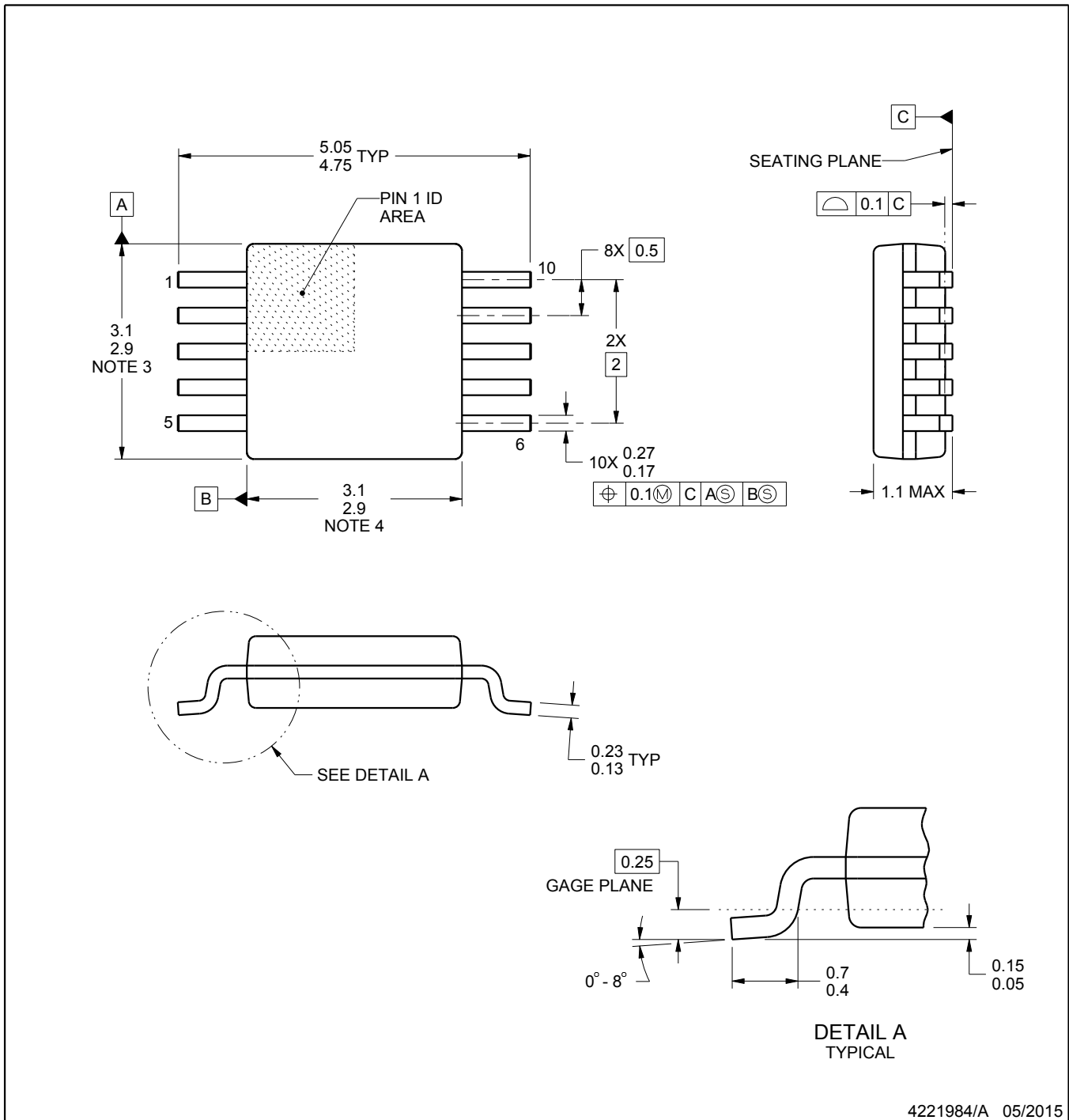
DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

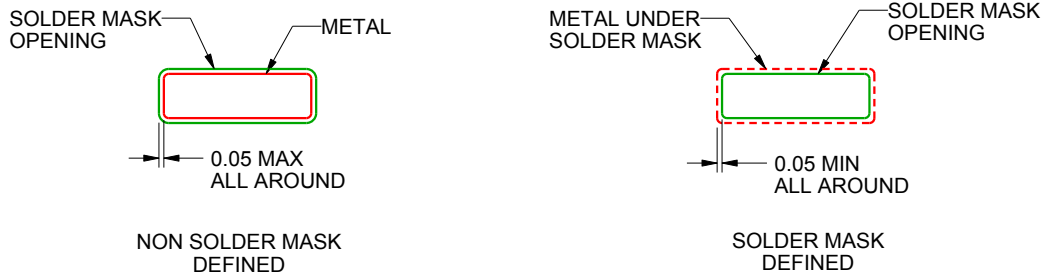
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

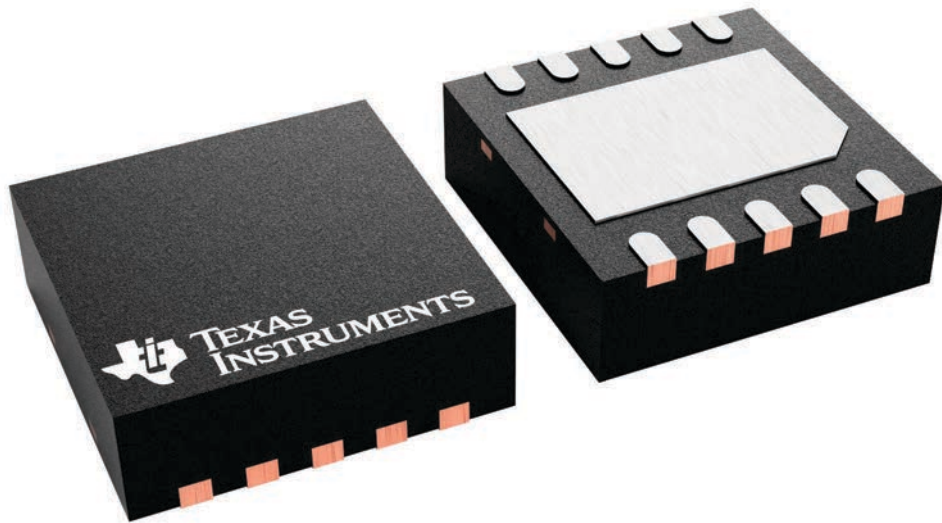
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226193/A

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