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# FDMS8320LDC

## N-Channel Dual Cool™ 56 Power Trench® MOSFET

40 V, 192 A, 1.1 mΩ

### Features

- Max  $r_{DS(on)}$  = 1.1 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 44\text{ A}$
- Max  $r_{DS(on)}$  = 1.5 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 37\text{ A}$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

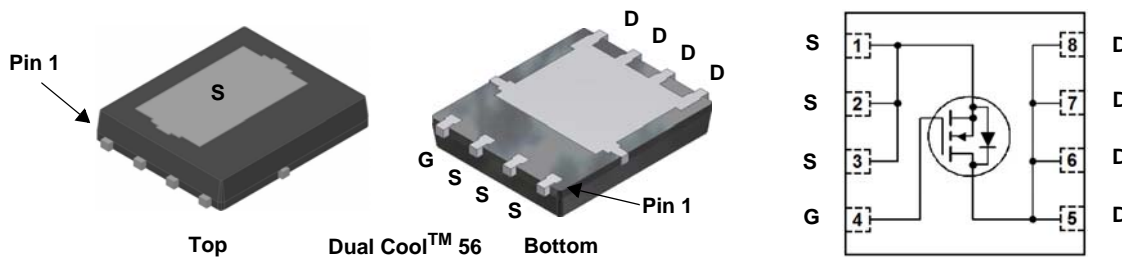


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

### Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$	192
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	44
	-Pulsed	(Note 4)	300
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	661
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	125
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	3.2
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	2.9	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8320L	FDMS8320LDC	Dual Cool™ 56	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		22		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 44\text{ A}$		0.8	1.1	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 37\text{ A}$		1.1	1.5	
		$V_{GS} = 10\text{ V}$ , $I_D = 44\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		1.2	1.7	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 44\text{ A}$		244		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		8310	11635	pF
$C_{oss}$	Output Capacitance			2255	3160	pF
$C_{rss}$	Reverse Transfer Capacitance			132	185	pF
$R_g$	Gate Resistance		0.1	1.4	2.6	$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{ V}$ , $I_D = 44\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		19	34	ns
$t_r$	Rise Time			15	27	ns
$t_{d(off)}$	Turn-Off Delay Time			69	110	ns
$t_f$	Fall Time			14	25	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 20\text{ V}$ , $I_D = 44\text{ A}$	121	170	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$		57	80	nC
$Q_{gs}$	Gate to Source Charge			21		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			16		nC

**Drain-Source Diode Characteristics**

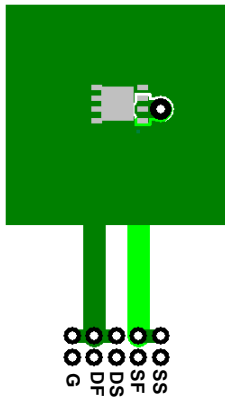
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.6\text{ A}$ (Note 2)		0.7	1.1	V
		$V_{GS} = 0\text{ V}$ , $I_S = 44\text{ A}$ (Note 2)		0.8	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 44\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		65	104	ns
$Q_{rr}$	Reverse Recovery Charge			57	91	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 44\text{ A}$ , $di/dt = 300\text{ A}/\mu\text{s}$		49	79	ns
$Q_{rr}$	Reverse Recovery Charge			89	143	nC

## Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	2.9	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1l)	13	

### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 38  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 81  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

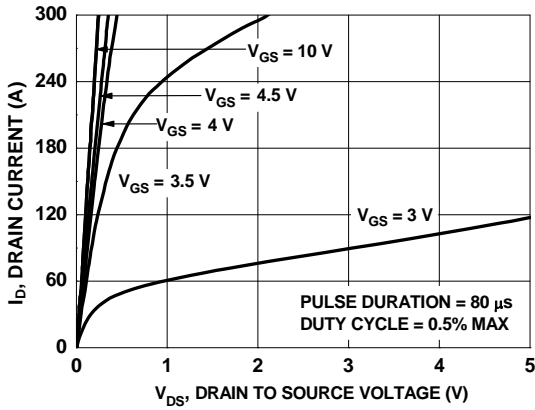
- c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g. 200FPM Airflow, No Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper
- l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

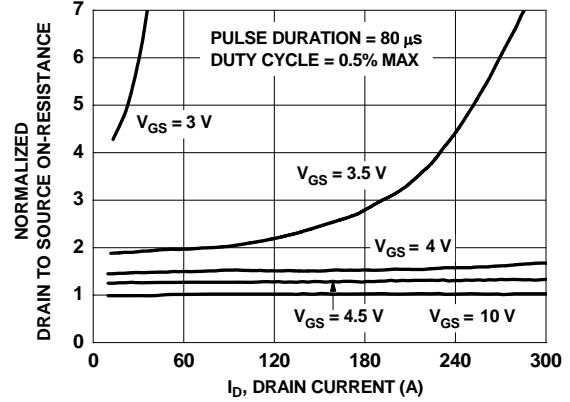
3.  $E_{AS}$  of 661 mJ is based on starting  $T_J = 25^{\circ}\text{C}$ ; N-ch: L = 3 mH,  $I_{AS} = 21\text{ A}$ ,  $V_{DD} = 40\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at L = 0.1 mH,  $I_{AS} = 66\text{ A}$ .

4. Pulse Id measured at 250 $\mu\text{s}$ , refer to Fig 11 SOA graph for more details.

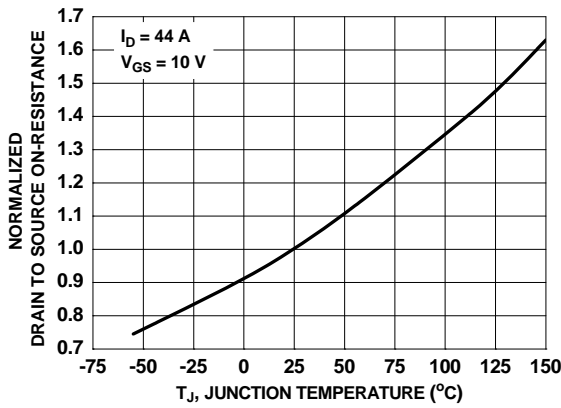
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



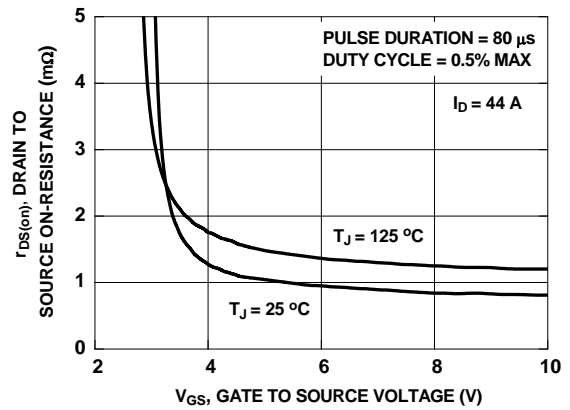
**Figure 1. On-Region Characteristics**



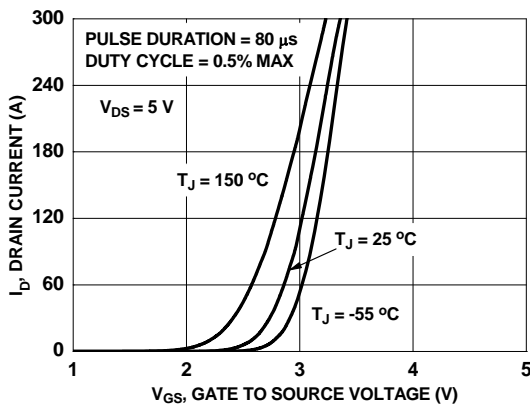
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



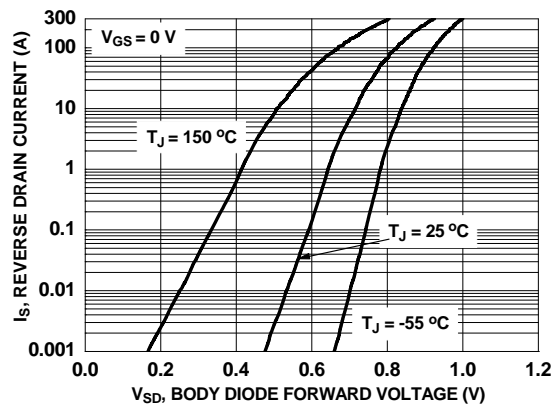
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

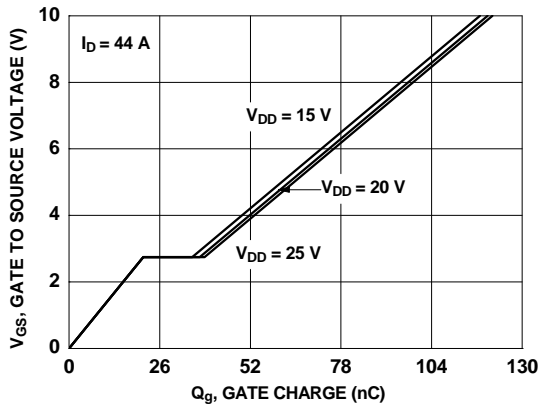


**Figure 5. Transfer Characteristics**

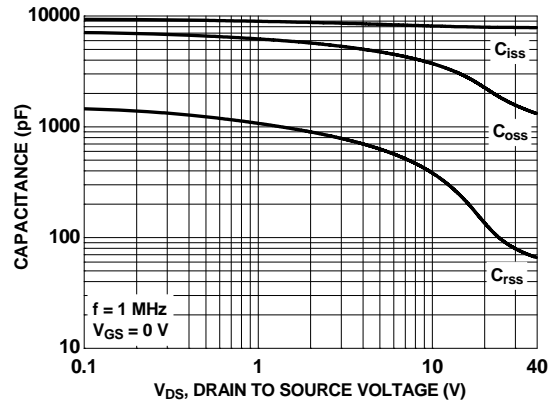


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

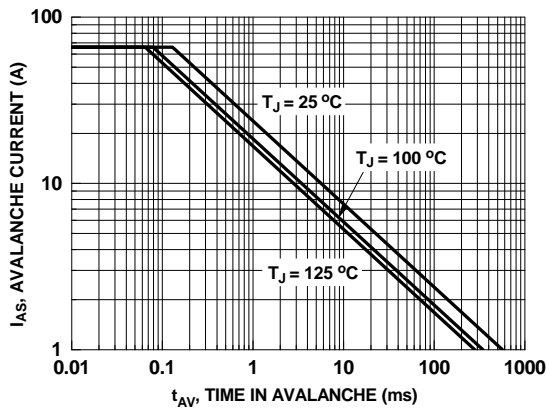
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



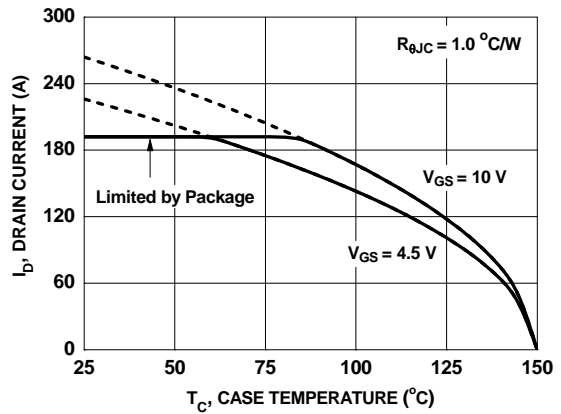
**Figure 7. Gate Charge Characteristics**



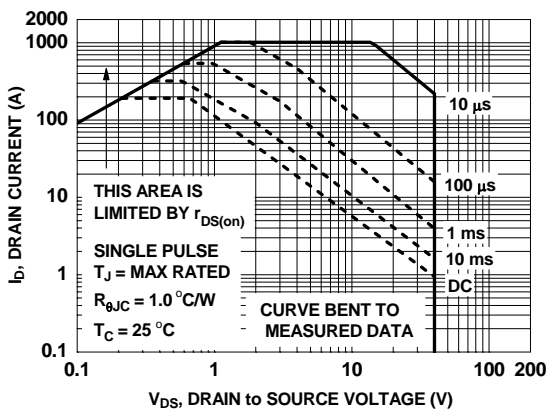
**Figure 8. Capacitance vs Drain to Source Voltage**



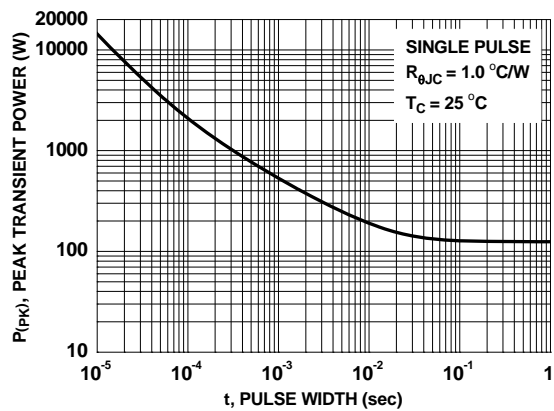
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

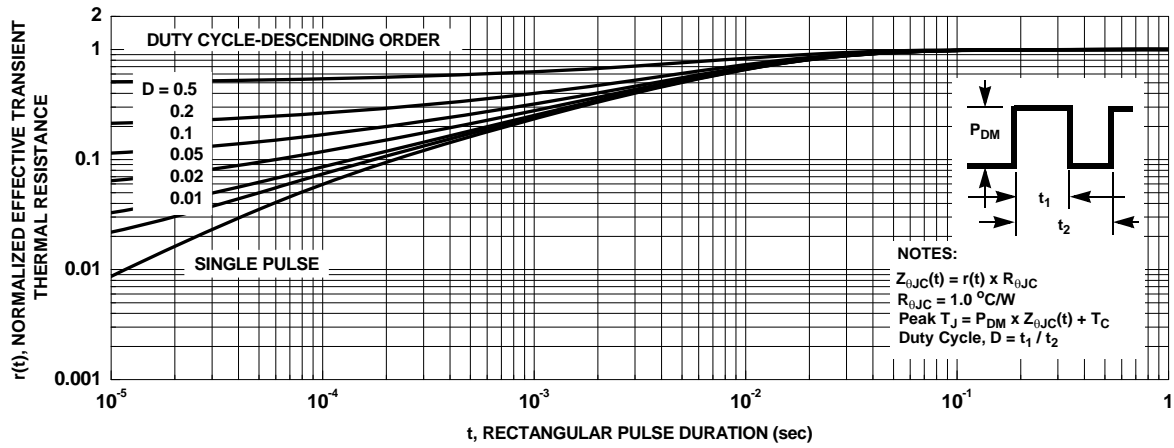


**Figure 11. Forward Bias Safe Operating Area**

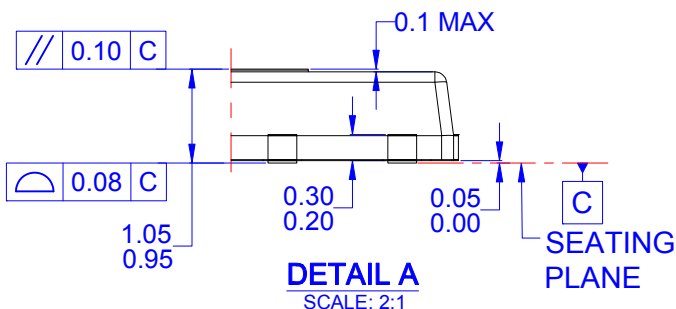
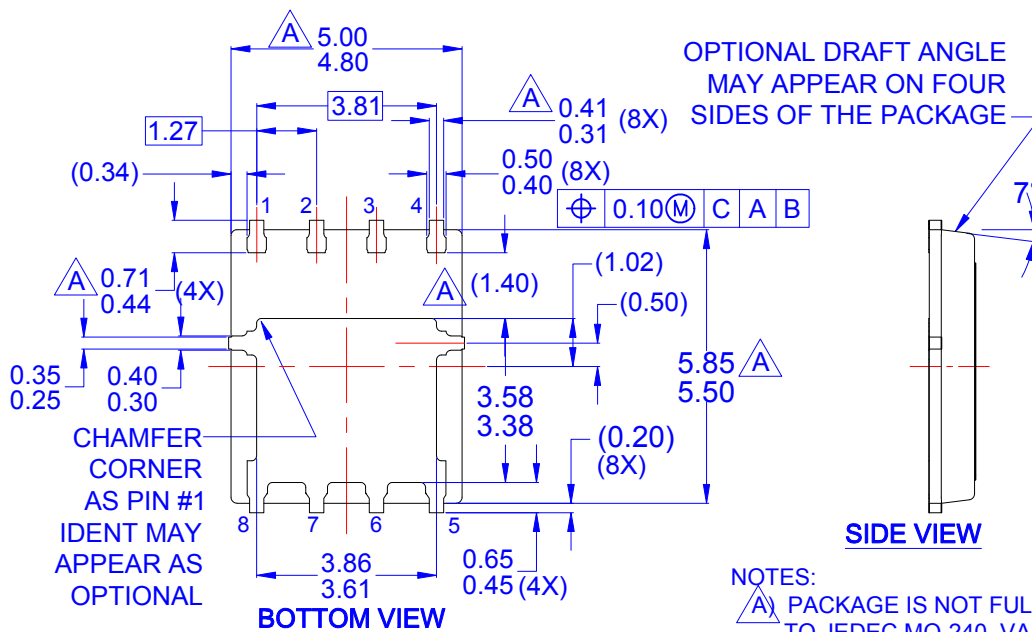
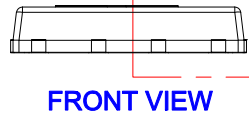
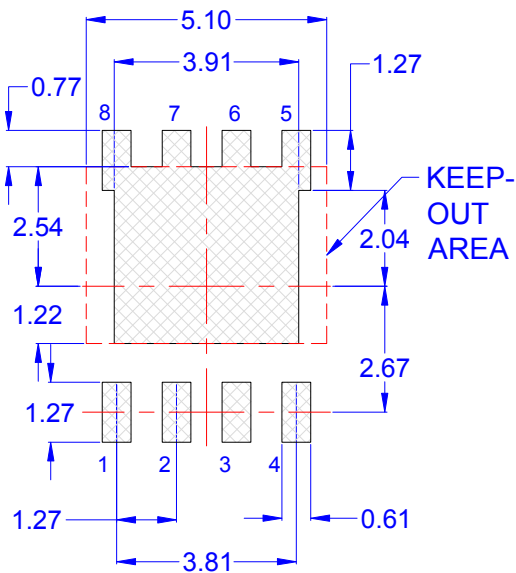
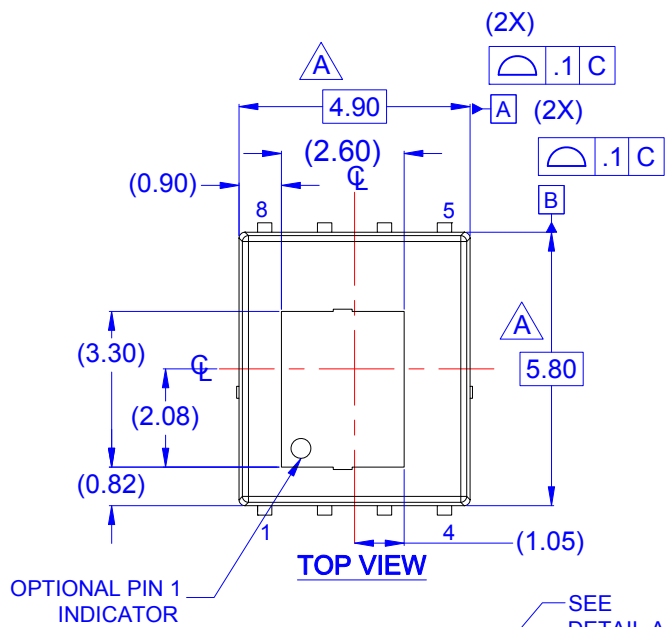


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**



- NOTES:
- A) PACKAGE IS NOT FULLY COMPLIANT TO JEDEC MO-240, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: PQFN08DREV4



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