



**THE DATASHEET OF
AP7217C-13**



Features

- Very Low Dropout Voltage
- Low Current Consumption: Typ. 40 μ A
- Output Voltage: 1.25V
- Guaranteed 600mA (min) Output
- Input Range up to 5.5V
- Current Limiting
- Stability with Low ESR Capacitors
- Thermal shutdown Protection
- Low Temperature Coefficient
- SOP-8L-EP: Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish / RoHS Compliant (Note 1)

General Description

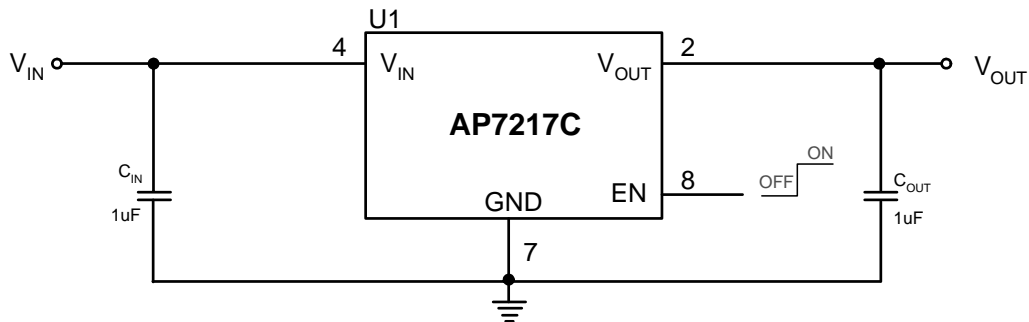
The AP7217C low-dropout linear regulator operates from a 2.5V to 5.5V supply and delivers a guaranteed 600mA (min) continuous load current.

The space-saving SOP-8L-EP package is suitable for "pocket" and hand-held applications.

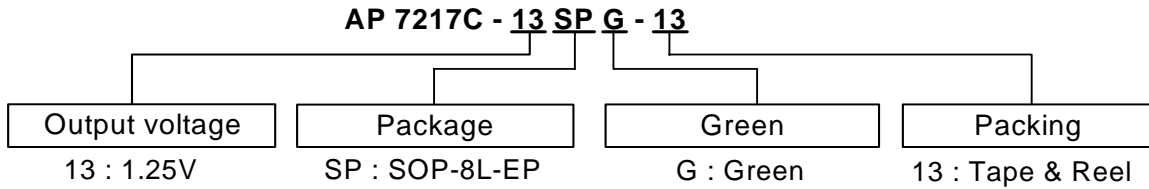
Applications

- CD and MP3 Players
- Cellular and PCS Phones
- Digital Still Camera
- Hand-Held Computers

Typical Application



Ordering Information

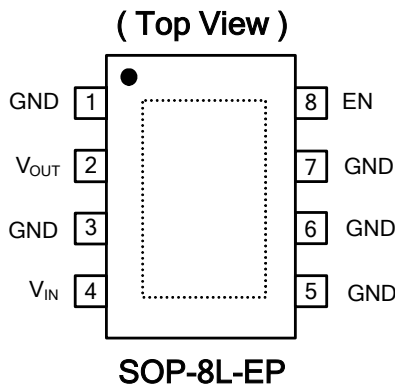


Device	Package Code	Packaging (Note 2)	13" Tape and Reel	
			Quantity	Part Number Suffix
AP7217C-13SPG-13	SP	SOP-8L-EP	2500/Tape & Reel	-13

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.
 2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

Pin Assignments

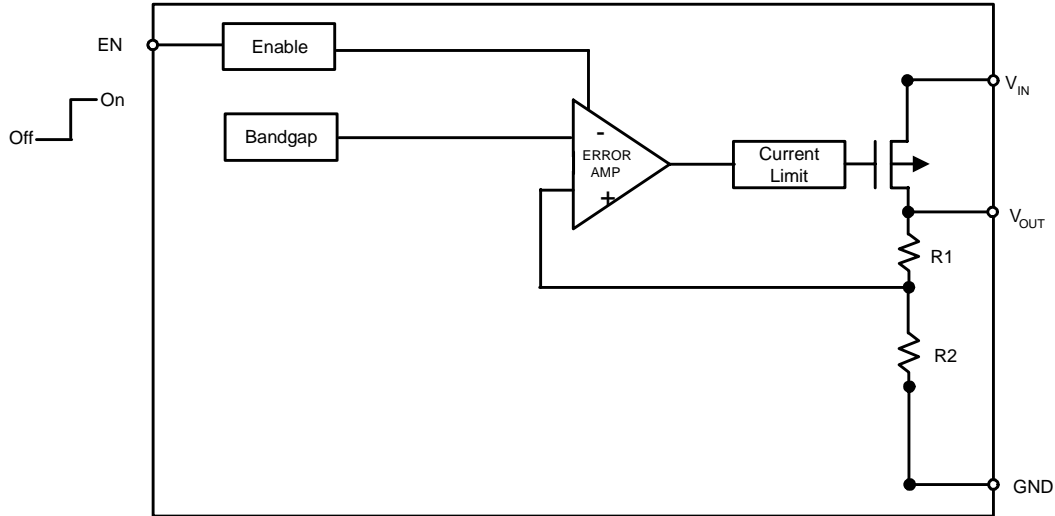
(1) SOP-8L-EP



Pin Descriptions

Pin Name	Pin No.	Description
GND	1, 3, 5, 6, 7	Ground
V _{OUT}	2	Voltage Output
V _{IN}	4	Supply Voltage
EN	8	High Enable

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit	
ESD HBM	Human Body Model ESD Protection	3.5	KV	
ESD MM	Machine Model ESD Protection	500	V	
V_{IN}	Input Voltage	+6	V	
I_{OUT}	Output Current	$P_D / (V_{IN} - V_O)$	mA	
P_D	Power Dissipation	SOP-8L-EP	1650	mW
T_J	Operating Junction Temperature Range	-40 to +125	°C	

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.5	5.5	V
I_{OUT}	Output Current	0	600	mA
T_A	Operating Ambient Temperature	-40	85	°C

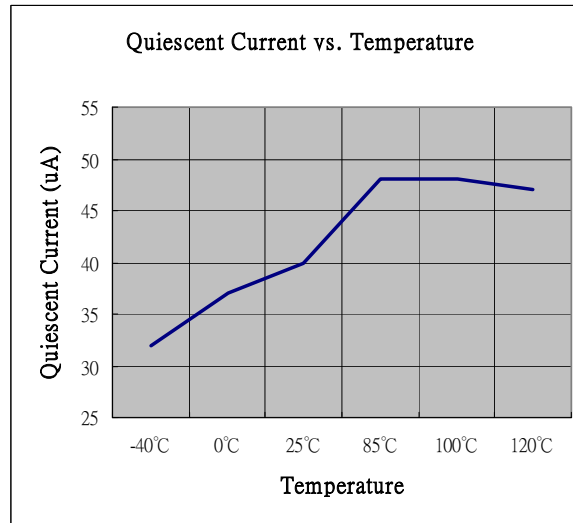
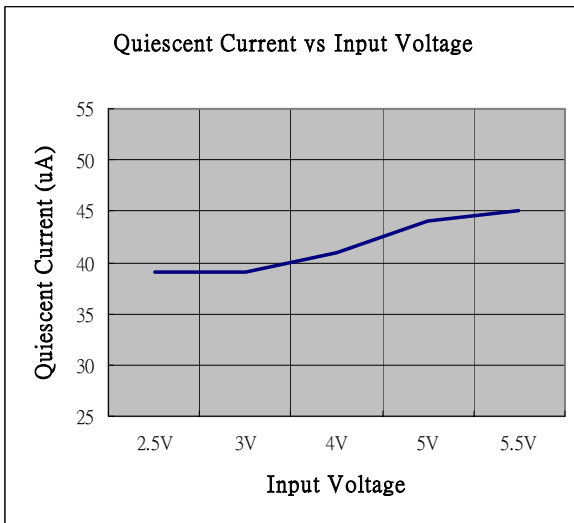
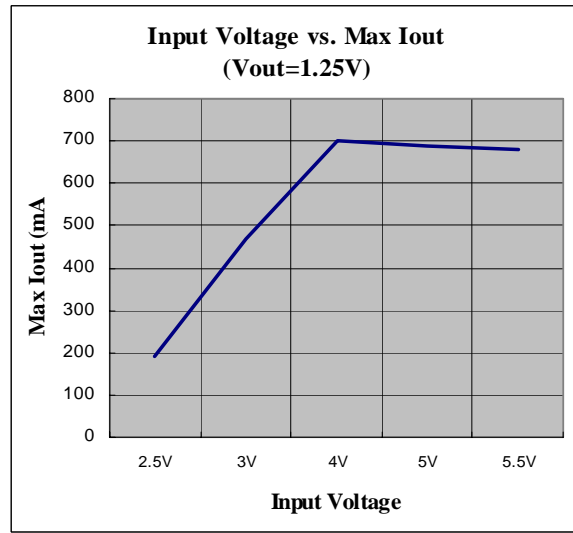
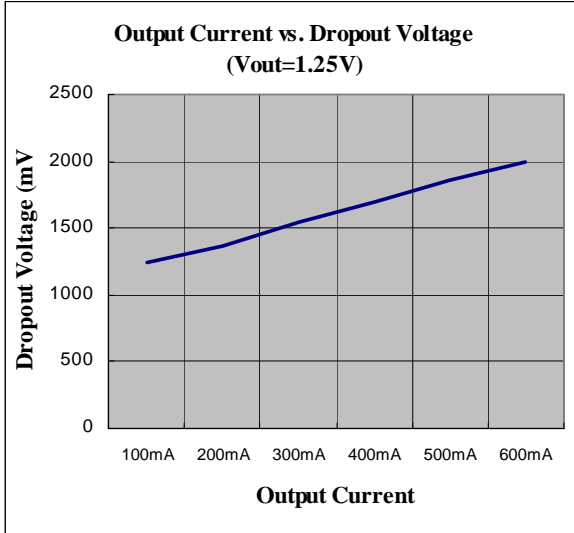
Electrical Characteristics

($T_A = 25^\circ\text{C}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 1\mu\text{F}$, $V_{EN} = V_{IN}$, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_Q	Quiescent Current	$I_O = 0\text{mA}$	-	40	60	μA
I_{STB}	Standby Current	$V_{EN} = \text{Off}$ $V_{IN} = 5.0\text{V}$		2	5	μA
V_{OUT}	Output Voltage Accuracy	$I_O = 30\text{mA}$, $V_{IN} = 5\text{V}$	1.225	1.25	1.275	V
	V_{OUT} Temperature Coefficient	-40°C to 85°C , $I_{OUT} = 30\text{mA}$		± 100		ppm / $^\circ\text{C}$
$V_{DROPOUT}$	Dropout Voltage	$I_{OUT} = 100\text{mA}$, $V_{OUT} = 1.25\text{V}$		1250		mV
		$I_{OUT} = 600\text{mA}$, $V_{OUT} = 1.25\text{V}$		2000		
I_{OUT}	Maximum Output Current	$V_{IN} = 5.3\text{V}$	600			mA
I_{LIMIT}	Current Limit	$V_{IN} = 5.3\text{V}$		750		mA
I_{SHORT}	Short Circuit Current	$V_{IN} = 5.3\text{V}$		70		mA
$\Delta V_{LINE}/\Delta V_{IN}/V_{OUT}$	Line Regulation	$4.3\text{V} \leq V_{IN} \leq 5.5\text{V}$; $I_{OUT} = 30\text{mA}$		0.01	± 0.2	%/V
ΔV_{OUT}	Load Regulation	$1\text{mA} \leq I_{OUT} \leq 100\text{mA}$, $V_{IN} = 5.3\text{V}$		10	20	mV
PSRR	Power Supply Rejection	$V_{IN} = 4.3\text{V} + 0.5\text{Vp-pAC}$, $I_{OUT} = 50\text{mA}$				dB
		$F = 1\text{KHz}$		55		
V_{EH}	EN Input Threshold	Output ON	1.6			V
V_{EL}		Output OFF			0.25	V
I_{EN}	Enable Pin Current		-0.1		0.1	μA
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOP-8L-EP (Note 3)		82		$^\circ\text{C}/\text{W}$
θ_{JC}	Thermal Resistance Junction-to-Case	SOP-8L-EP (Note 3)		12		$^\circ\text{C}/\text{W}$

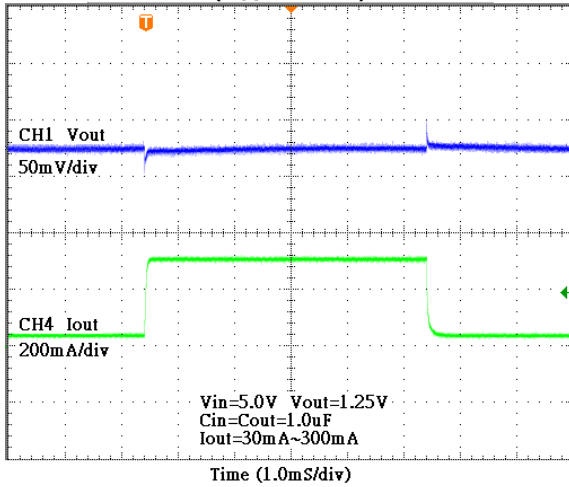
Notes: 3. Test condition for SOP-8L-EP: Device mounted on 2oz copper, minimum recommended pad layout on top & bottom layer with thermal vias, double sided FR-4 PCB.

Typical Performance Characteristics

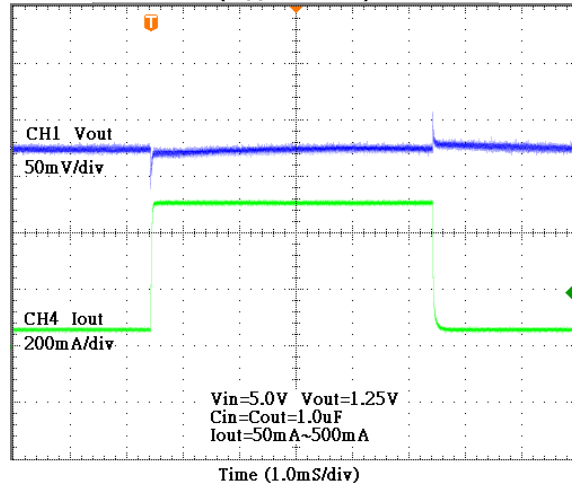


Typical Performance Characteristics (Continued)

Load Transient Response
($V_{OUT} = 1.25V$)



Load Transient Response
($V_{OUT} = 1.25V$)



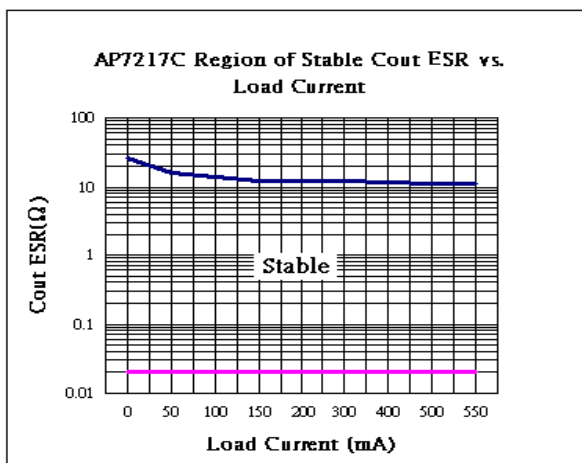
Application Note

Input Capacitor

A 1 μ F ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. A lower ESR (Equivalent Series Resistance) capacitor allows the use of less capacitance, while higher ESR type requires more capacitance. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

The output capacitor is required to stabilize and help the transient response of the LDO. The AP7217C is designed to have excellent transient response for most applications with a small amount of output capacitance. The AP7217C is stable with any small ceramic output capacitors of 1.0 μ F or higher value, and the temperature coefficients of X7R or X5R type. Additional capacitance helps to reduce undershoot and overshoot during transient. For PCB layout, the output capacitor must be placed as close as possible to OUT and GND pins, and keep the leads as short as possible.



ENABLE/SHUTDOWN Operation

The AP7217C (SOP-8L-EP) is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH} .

Thermal Considerations

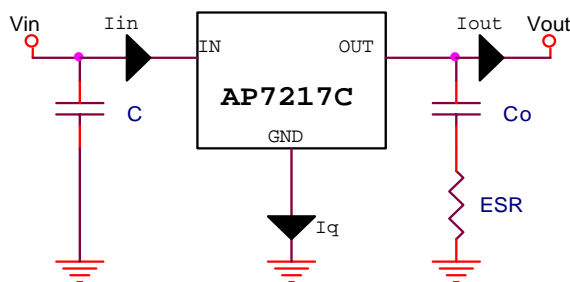
Thermal Shutdown Protection limits power dissipation in AP7217C. When the operation junction temperature exceeds 140°C, the Over Temperature Protection circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 30°C. For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junctions to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.



Current Limit Protection

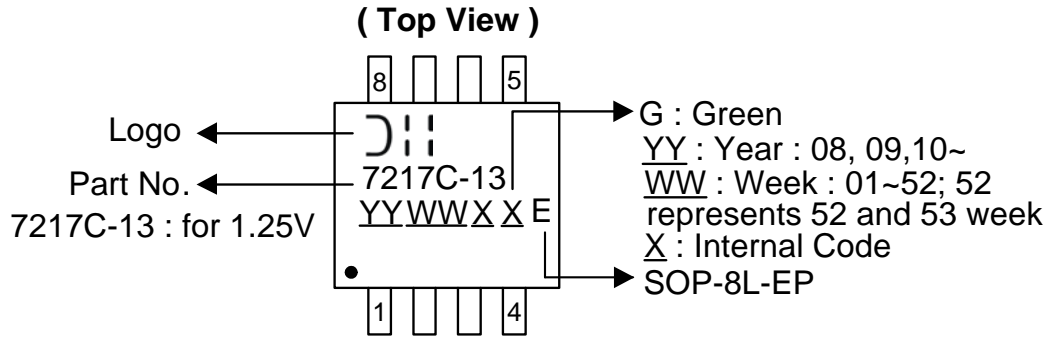
When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 750mA to prevent over-current and to protect the regulator from damage due to overheating.

Short circuit protection

When V_{OUT} pin is shorted to GND or V_{OUT} voltage is less than 200mV, short circuit protection will be triggered and clamp the output current to approximately 70mA.

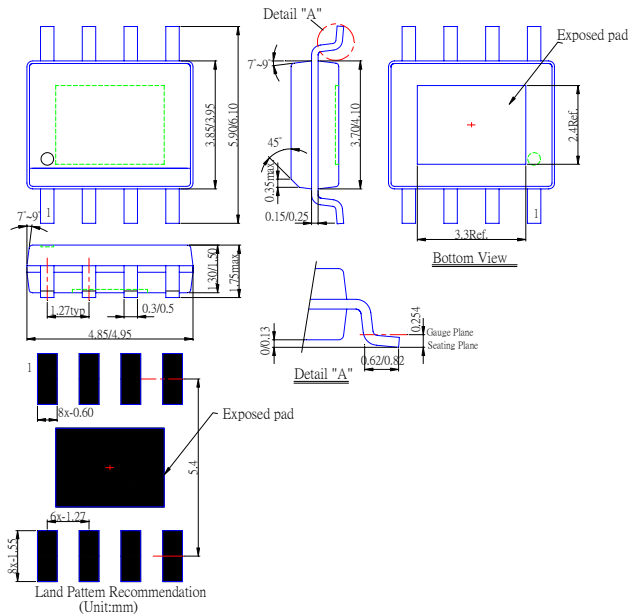
Marking Information

(1) SOP-8L-EP



Package Information (All Dimensions in mm)

(1) Package Type: SOP-8L-EP



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