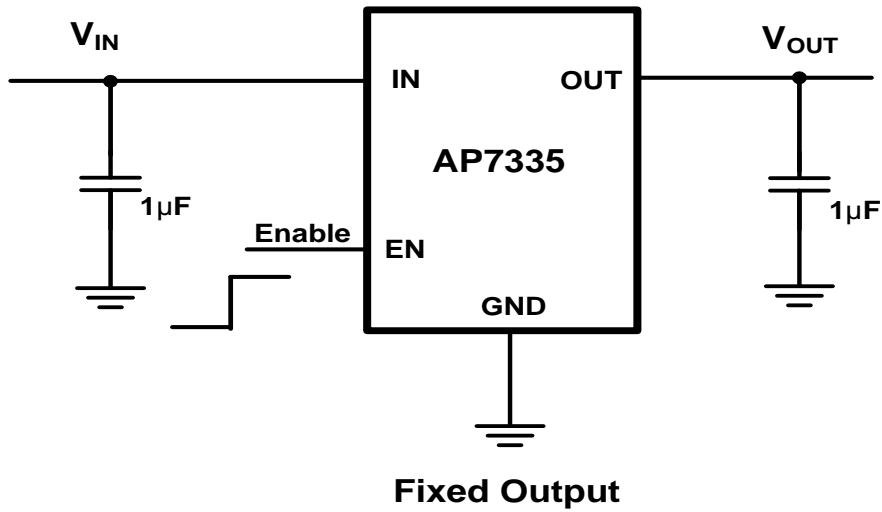




**THE DATASHEET OF
AP7335A-50SN-7**



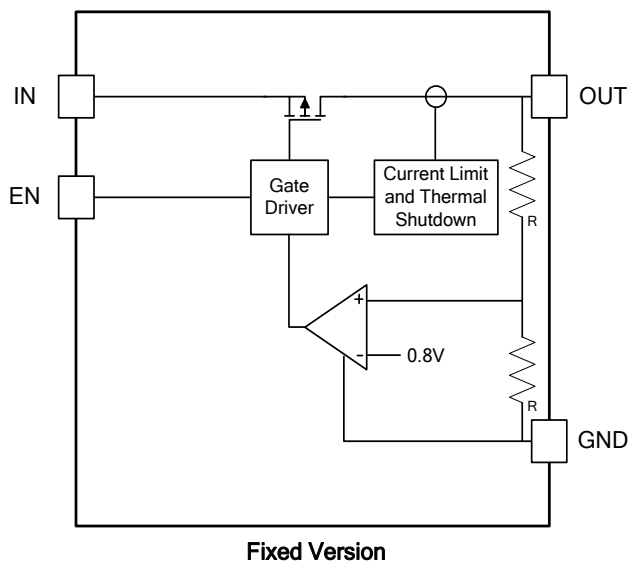
Typical Applications Circuit



Pin Descriptions

| Pin Number | Package Name | | Function |
|------------|------------------|------------------------|---|
| | SOT25 (Fixed) | U-DFN2020-6 (Fixed) | |
| IN | 1 | 3 | Voltage input pin. Bypass to ground through at least 1µF MLCC capacitor |
| GND | 2 | 2 | Ground |
| EN | 3 | 1 | Enable input, active high |
| NC | 4 | 5, 6 | No connection |
| OUT | 5 | 4 | Voltage output pin. Bypass to ground through 1µF MLCC capacitor |

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

| Symbol | Parameter | Rating | Unit |
|------------------------------------|-------------------------------------|-----------------------|------|
| V _{IN} | Input Voltage | 6.5 | V |
| V _{OUT} , V _{EN} | OUT, EN Voltage | V _{IN} + 0.3 | V |
| I _{LIMIT} | Continuous Load Current per Channel | Internal Limited | mA |
| T _{ST} | Storage Temperature Range | -65 to +150 | °C |
| ESD HBM | Human Body Model ESD Protection | 2,000 | V |
| ESD MM | Machine Model ESD Protection | 200 | V |

Note: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

| Symbol | Parameter | Min | Max | Unit |
|------------------|-------------------------------|--------------|-----|------|
| V _{IN} | Input voltage (Note 6) | 5.5 (Note 6) | 6 | V |
| I _{OUT} | Output Current (Note 5) | 0 | 300 | mA |
| T _A | Operating Ambient Temperature | -40 | +85 | °C |

Notes: 5. The device maintains a stable, regulated output voltage without a load current.
 6. V_{IN(MIN)} = 5.5V for 5.0V, V_{OUT} at 300mA I_{OUT}.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

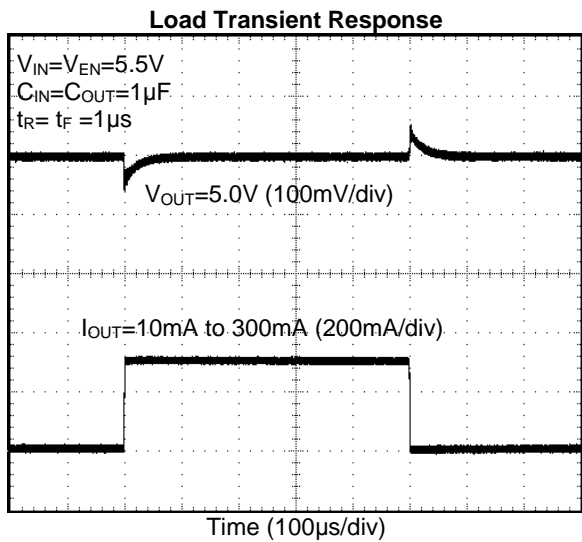
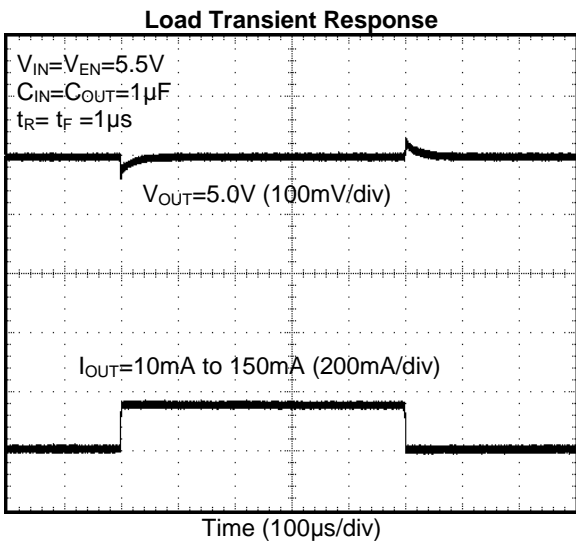
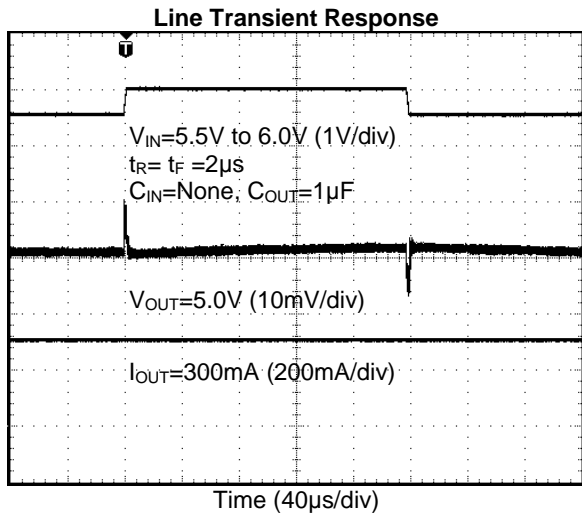
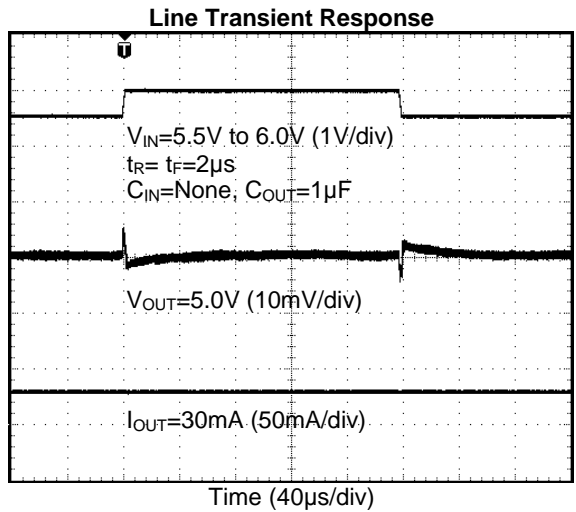
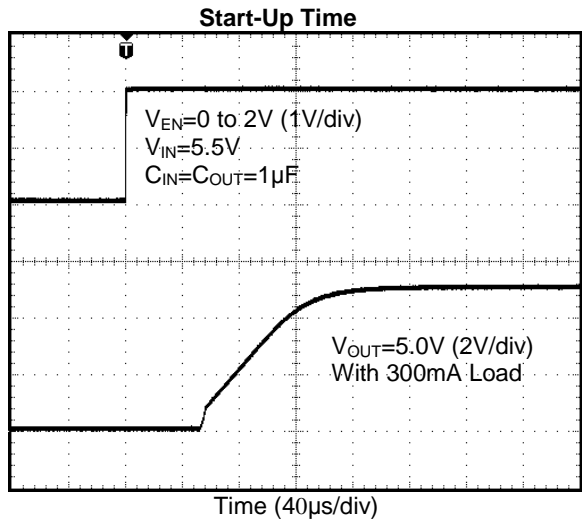
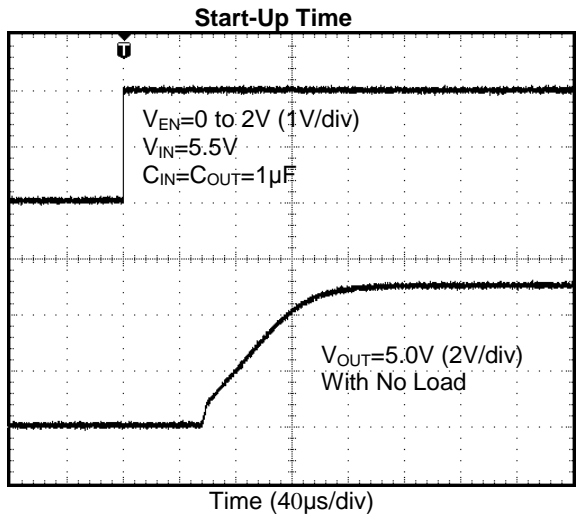
(T_A = +25°C, V_{IN} = 5.5 to 6V, C_{IN} = 1μF, C_{OUT} = 1μF, V_{EN} = 2V, unless otherwise stated)

| Symbol | Parameter | Test Conditions | Min | Typ. | Max | Unit |
|--|--|---|------|------|------|------|
| V _{OUT} | Output Voltage Accuracy | T _A = -40°C to +85°C, I _{OUT} = 10% of I _{OUT-Max} | -1 | - | 1 | % |
| $\frac{\Delta V_{OUT}}{\Delta V_{IN}/V_{OUT}}$ | Line Regulation | V _{IN} = 5.5V to 6V, V _{EN} = V _{IN} , I _{OUT} = 1mA | - | 0.02 | 0.20 | %/V |
| $\frac{\Delta V_{OUT}}{I_{OUT}}$ | Load Regulation | V _{IN} = 5.5V to 6V, I _{OUT} = 1mA to 300mA | -0.6 | - | 0.6 | % |
| V _{DROPOUT} | Dropout Voltage (Note 7) | I _{OUT} = 300mA | - | 150 | 200 | mV |
| I _Q | Input Quiescent Current | V _{EN} = V _{IN} , I _{OUT} = 0mA | - | 35 | 80 | μA |
| I _{SHDN} | Input Shutdown Current | V _{EN} = 0V, I _{OUT} = 0mA | - | 0.1 | 1 | μA |
| I _{LEAK} | Input Leakage Current | V _{EN} = 0V, OUT Grounded | - | 0.1 | 1 | μA |
| T _{ST} | Start-up Time | V _{EN} = 0V to 2.0V in 1μs, I _{OUT} = 300mA | - | 220 | - | μs |
| PSRR | PSRR | V _{IN} = 5.5V _{DC} + 0.5V _{PPAC} , f = 1kHz, I _{OUT} = 50mA | - | 65 | - | dB |
| I _{SHORT} | Short-circuit Current | V _{IN} = V _{IN-Min} to V _{IN-Max} , V _{OUT} < 0.2V (Fixed) | - | 160 | - | mA |
| I _{LIMIT} | Current limit | V _{IN} = V _{IN-Min} to V _{IN-Max} , V _{OUT} /R _{OUT} = 1.2A | 400 | 650 | - | mA |
| V _{IL} | En Input Logic Low Voltage | V _{IN} = V _{IN-Min} to V _{IN-Max} | - | - | 0.4 | V |
| V _{IH} | En Input Logic High Voltage | V _{IN} = V _{IN-Min} to V _{IN-Max} | 1.4 | - | - | V |
| I _{EN} | En Input Current | V _{IN} = 0V or V _{IN-Max} | -1 | - | 1 | μA |
| T _{SHDN} | Thermal Shutdown Threshold | - | - | +145 | - | °C |
| T _{HYS} | Thermal Shutdown Hysteresis | - | - | +15 | - | °C |
| θ _{JA} | Thermal Resistance Junction-to-Ambient | SOT25 (Note 8) | - | 187 | - | °C/W |
| | | U-DFN2020-6 (Note 8) | - | 251 | - | |

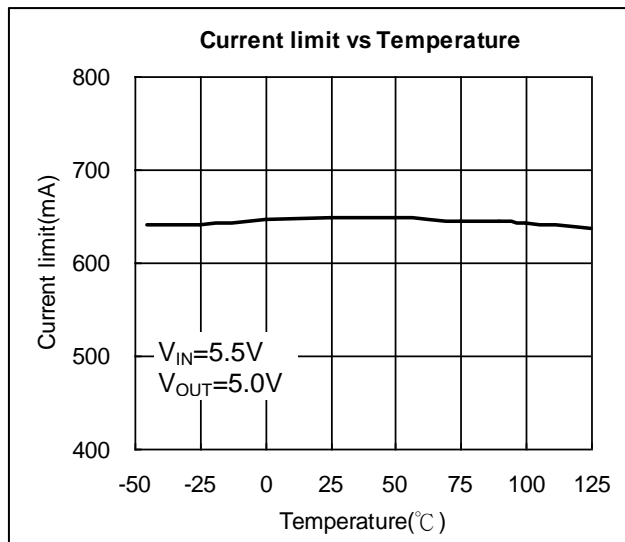
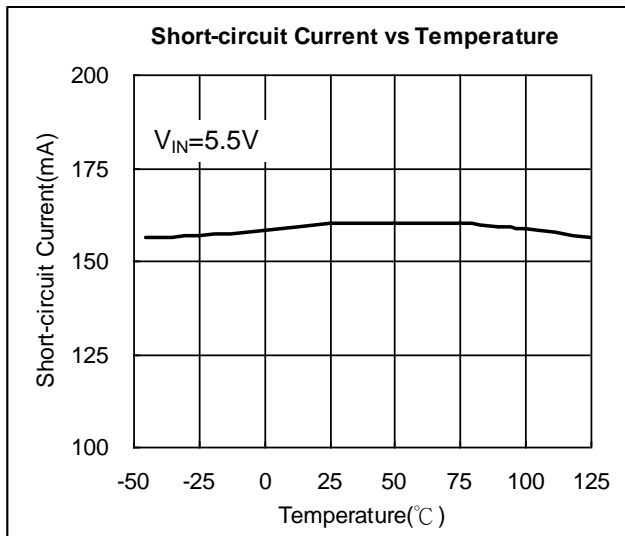
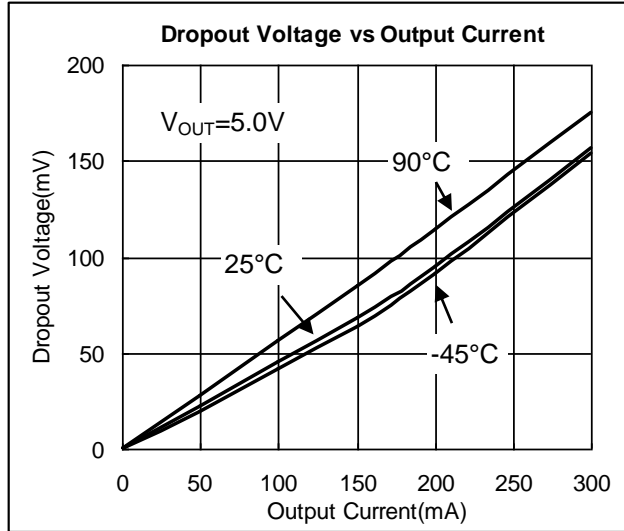
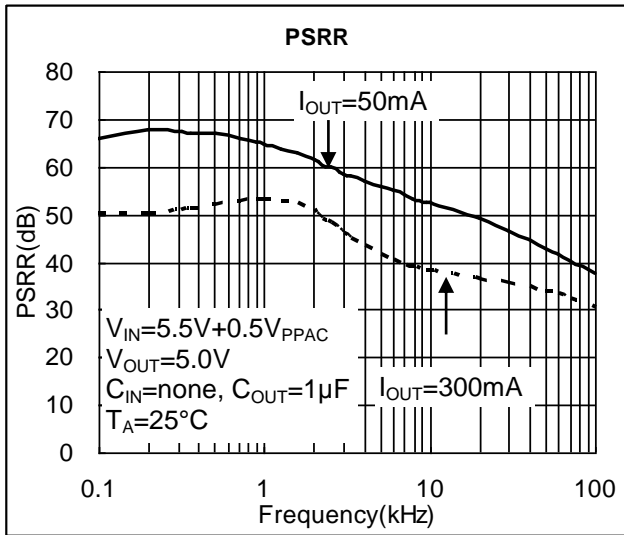
Notes: 7. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
8. Test condition for all packages: Device mounted on FR-4 substrate PC board, 1oz copper, with minimum recommended pad layout.

Performance Characteristics

NEW PRODUCT



Performance Characteristics (Cont.)



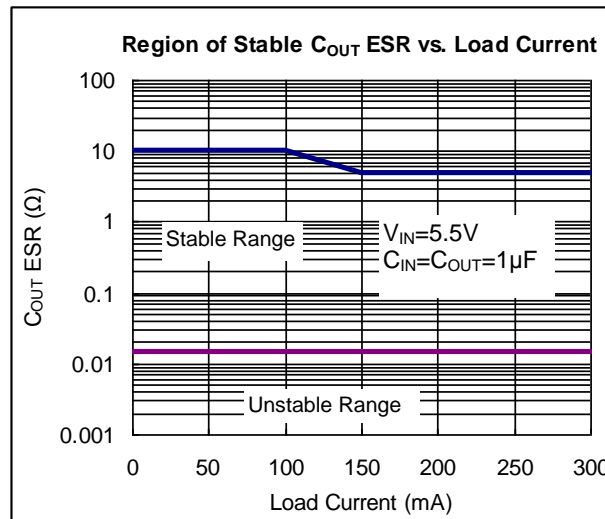
Application Note

Input Capacitor

A 1 μ F ceramic capacitor is recommended between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while higher ESR type requires more capacitance.

Output Capacitor

The output capacitor is required to stabilize and improve the transient response of the LDO. The AP7335A-50 is stable with very small ceramic output capacitors. Using a ceramic capacitor value that is at least 1 μ F with ESR > 15m Ω on the output ensures stability. Higher capacitance values help to improve line and load transient response. The output capacitance may be increased to keep low undershoot and overshoot. Output capacitor must be placed as close as possible to OUT and GND pins.



No Load Stability

No minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

ON/OFF Input Operation

The AP7335A-50 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

Current Limit Protection

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 650mA to prevent overcurrent and to protect the regulator from damage due to overheating.

Short Circuit Protection

When OUT pin is short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 160mA. This feature protects the regulator from overcurrent and damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +145 $^{\circ}$ C, allowing the device to cool down. When the junction temperature reduces to approximately +130 $^{\circ}$ C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Ultra Fast Start-Up

After enabled, the AP7335A-50 is able to provide full power in as little as tens of microseconds, typically 220 μ s, without sacrificing low ground current. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

Application Note

Fast Transient Response

Fast transient response LDO can extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100µA to 100mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDO.

The AP7335A-50's fast transient response from 0 to 300mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Low Quiescent Current

The AP7335A-50, consuming only around 35µA for all input range, provides great power saving in portable and low power applications.

Power Dissipation

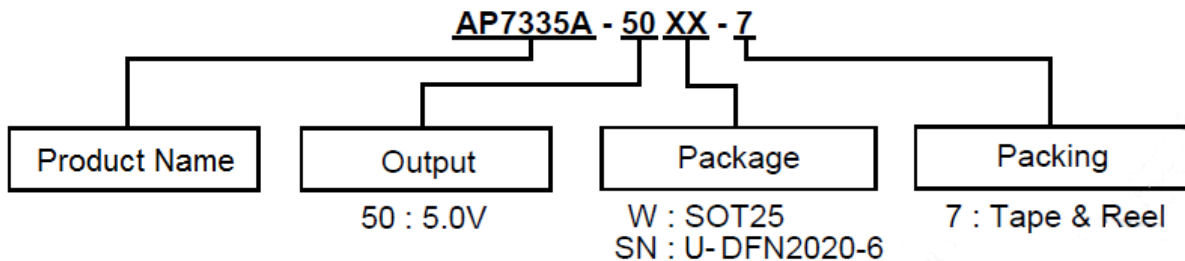
The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The maximum power dissipation, handled by the device, depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the following equation:

$$P_D (\text{max@}T_A) = \frac{(+145^\circ\text{C} - T_A)}{R_{\theta JA}}$$

Ordering Information

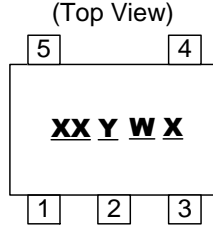


| Device | Package Code | Packaging (Note 9) | 7" Tape and Reel | |
|----------------|--------------|-----------------------|-------------------|--------------------|
| | | | Quantity | Part Number Suffix |
| AP7335A-50W-7 | W | SOT25 | 3,000/Tape & Reel | -7 |
| AP7335A-50SN-7 | SN | U-DFN2020-6 | 3,000/Tape & Reel | -7 |

Note: 9. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

Marking Information

(1) SOT25

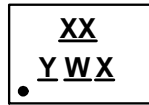


XX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : A~Z : G = Green

| Device | Package | Identification Code |
|---------------|---------|---------------------|
| AP7335A-50W-7 | SOT25 | TP |

(2) U-DFN2020-6

(Top View)



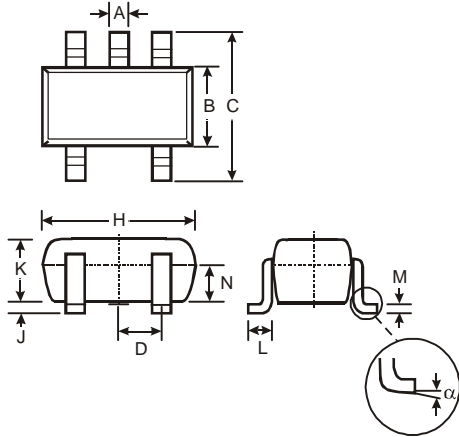
XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : A~Z : G = Green

| Device | Package | Identification Code |
|----------------|-------------|---------------------|
| AP7335A-50SN-7 | U-DFN2020-6 | TP |

Package Outline Dimensions (All dimensions in mm.)

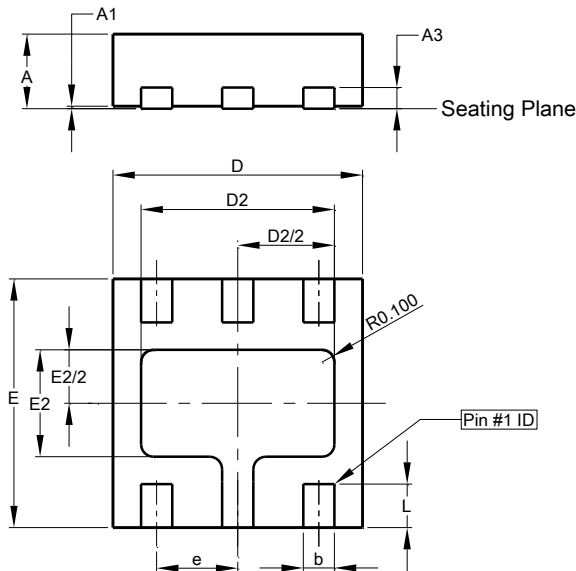
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) Package Type: SOT25



| SOT25 | | | |
|----------------------|-------|------|------|
| Dim | Min | Max | Typ |
| A | 0.35 | 0.50 | 0.38 |
| B | 1.50 | 1.70 | 1.60 |
| C | 2.70 | 3.00 | 2.80 |
| D | — | — | 0.95 |
| H | 2.90 | 3.10 | 3.00 |
| J | 0.013 | 0.10 | 0.05 |
| K | 1.00 | 1.30 | 1.10 |
| L | 0.35 | 0.55 | 0.40 |
| M | 0.10 | 0.20 | 0.15 |
| N | 0.70 | 0.80 | 0.75 |
| α | 0° | 8° | — |
| All Dimensions in mm | | | |

(2) Package Type: U-DFN2020-6

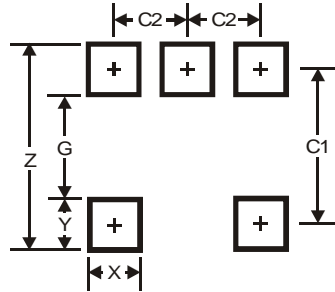


| U-DFN2020-6 | | | |
|----------------------|------|-------|------|
| Dim | Min | Max | Typ |
| A | 0.57 | 0.63 | 0.60 |
| A1 | 0 | 0.05 | 0.03 |
| A3 | - | - | 0.15 |
| b | 0.20 | 0.30 | 0.25 |
| D | 1.95 | 2.075 | 2.00 |
| D2 | 1.45 | 1.65 | 1.55 |
| e | - | - | 0.65 |
| E | 1.95 | 2.075 | 2.00 |
| E2 | 0.76 | 0.96 | 0.86 |
| L | 0.30 | 0.40 | 0.35 |
| All Dimensions in mm | | | |

Suggested Pad Layout

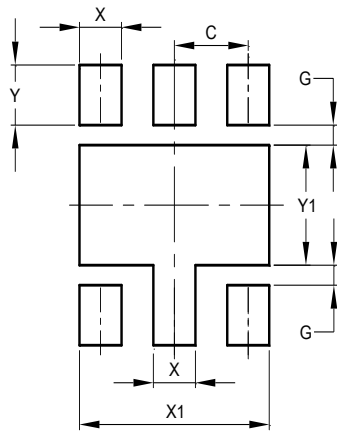
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) Package Type: SOT25



| Dimensions | Value (in mm) |
|------------|---------------|
| Z | 3.20 |
| G | 1.60 |
| X | 0.55 |
| Y | 0.80 |
| C1 | 2.40 |
| C2 | 0.95 |

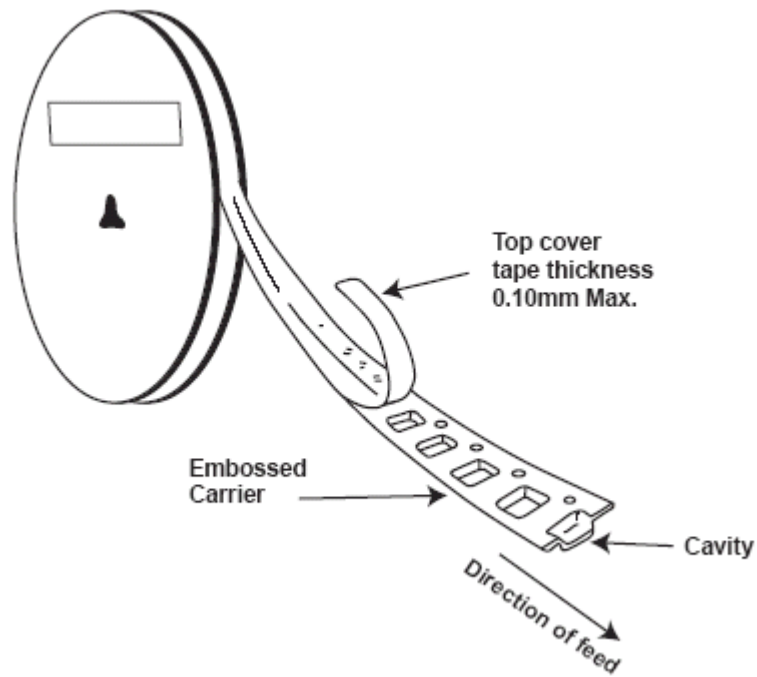
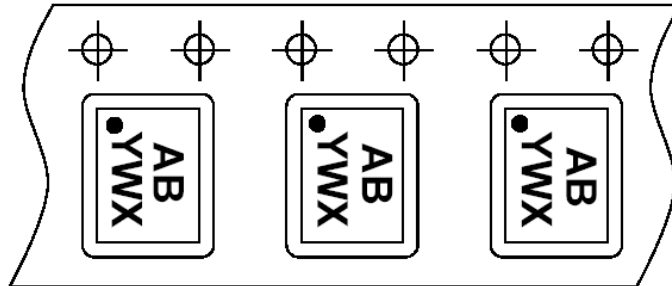
(2) Package Type: U-DFN2020-6



| Dimensions | Value (in mm) |
|------------|---------------|
| C | 0.65 |
| G | 0.15 |
| X | 0.37 |
| X1 | 1.67 |
| Y | 0.45 |
| Y1 | 0.90 |

Taping Orientation (Note 10)

For U-DFN2020-6



Note: 10. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

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