



**THE DATASHEET OF  
SN74LVTH16244ADGVR**



## 3.3-V ABT 16-Bit Buffers/Drivers With 3-State Outputs

Check for Samples: [SN54LVTH16244A](#), [SN74LVTH16244A](#)

### FEATURES

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **$I_{off}$  and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

### DESCRIPTION

The LVTH16244A devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



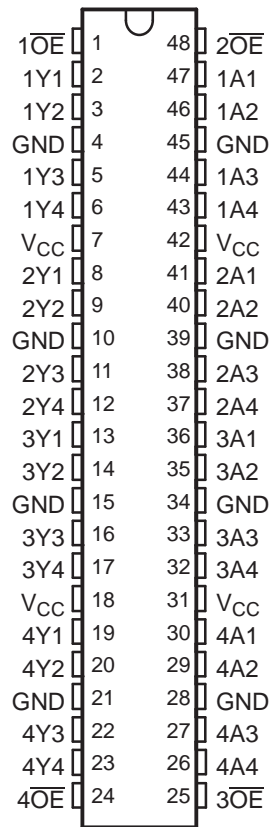
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

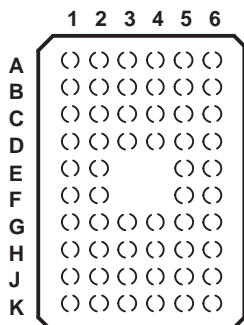
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992–2013, Texas Instruments Incorporated

SN54LVTH16244A . . . WD PACKAGE  
 SN74LVTH16244A . . . DGG, DGV, OR DL PACKAGE  
 (TOP VIEW)



**GQL OR ZQL PACKAGE  
(TOP VIEW)**

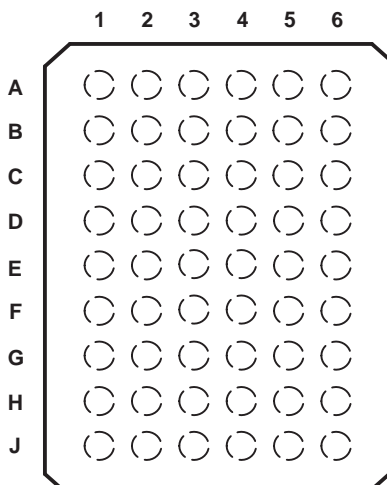


**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
<b>A</b>	$1\overline{OE}$	NC	NC	NC	NC	$2\overline{OE}$
<b>B</b>	1Y2	1Y1	GND	GND	1A1	1A2
<b>C</b>	1Y4	1Y3	V <sub>CC</sub>	V <sub>CC</sub>	1A3	1A4
<b>D</b>	2Y2	2Y1	GND	GND	2A1	2A2
<b>E</b>	2Y4	2Y3			2A3	2A4
<b>F</b>	3Y1	3Y2			3A2	3A1
<b>G</b>	3Y3	3Y4	GND	GND	3A4	3A3
<b>H</b>	4Y1	4Y2	V <sub>CC</sub>	V <sub>CC</sub>	4A2	4A1
<b>J</b>	4Y3	4Y4	GND	GND	4A4	4A3
<b>K</b>	$4\overline{OE}$	NC	NC	NC	NC	$3\overline{OE}$

(1) NC – No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)**

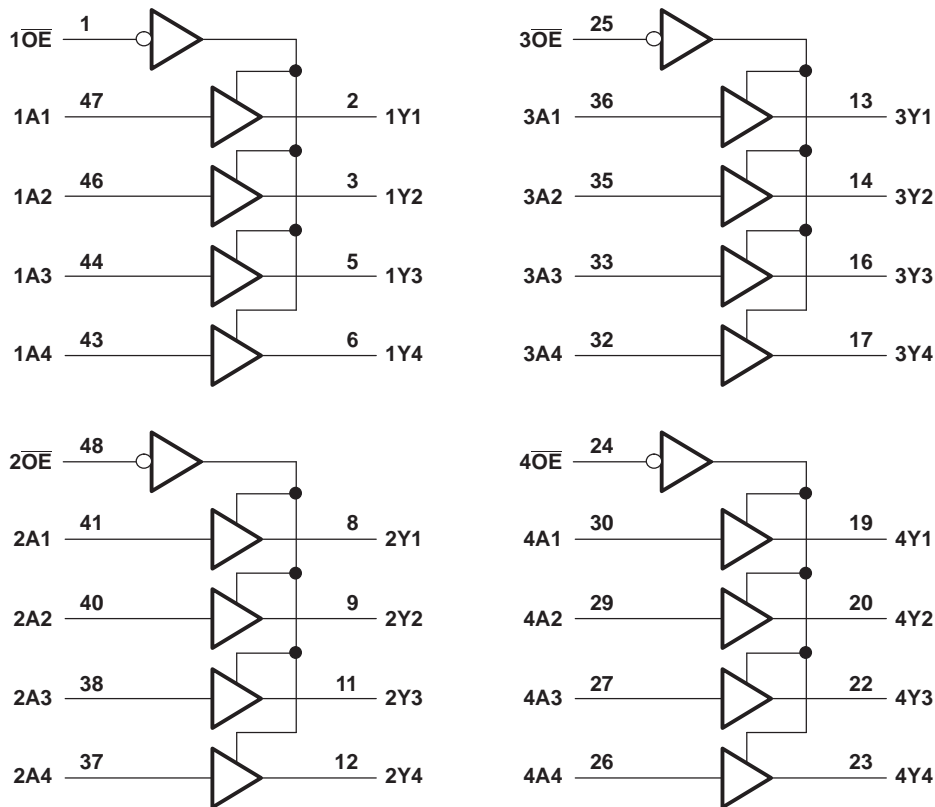
	1	2	3	4	5	6
<b>A</b>	1Y1	NC	$1\overline{OE}$	$2\overline{OE}$	NC	1A1
<b>B</b>	1Y3	1Y2	NC	NC	1A2	1A3
<b>C</b>	2Y1	1Y4	V <sub>CC</sub>	V <sub>CC</sub>	1A4	2A1
<b>D</b>	2Y3	2Y2	GND	GND	2A2	2A3
<b>E</b>	3Y1	2Y4	GND	GND	2A4	3A1
<b>F</b>	3Y3	3Y2	GND	GND	3A2	3A3
<b>G</b>	4Y1	3Y4	V <sub>CC</sub>	V <sub>CC</sub>	3A4	4A1
<b>H</b>	4Y3	4Y2	NC	NC	4A2	4A3
<b>J</b>	4Y4	NC	$4\overline{OE}$	$3\overline{OE}$	NC	4A4

(1) NC – No internal connection

**FUNCTION TABLE  
(EACH 4-BIT BUFFER)**

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high state <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	
I <sub>O</sub>	Current into any output in the low state	SN54LVTH16244A	96	V
		SN74LVTH16244A	128	
I <sub>O</sub>	Current into any output in the high state <sup>(3)</sup>	SN54LVTH16244A	48	V
		SN74LVTH16244A	64	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package	70	°C/W
		DGV package	58	
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The current flows only when the output is in the high state and V<sub>O</sub> > V<sub>CC</sub>.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		SN54LVTH16244A		SN74LVTH16244A		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage		5.5		5.5	V
I <sub>OH</sub>	High-level output current		-25		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate	200		200		μs/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS		SN54LVTH16244A			–40°C to 85°C SN74LVTH16244A			Recommended –40°C to 125°C SN74LVTH16244A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = –18 mA		–1.2			–1.2			–1.2			V
V <sub>OH</sub>	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OL</sub> = –100 μA		V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2			V
	V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = –8 mA		2.4			2.4			2.4			
	V <sub>CC</sub> = 3 V		2			2			2			
V <sub>OL</sub>	V <sub>CC</sub> = 2.7 V		0.2			0.2			0.2			V
			0.5			0.5			0.5			
			0.4			0.4			0.4			
	V <sub>CC</sub> = 3 V		0.5			0.5			0.5			
			0.55			0.55			0.55			
			0.55			0.55			0.55			
I <sub>I</sub>	V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V		50			10			10			μA
	Control inputs	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND	±1			±1			±1			
	Data inputs	V <sub>CC</sub> = 3.6 V	1			1			1			
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V					±100			±100			μA
I <sub>I(hold)</sub>	Data inputs	V <sub>CC</sub> = 3 V	75			75			75			μA
			–75			–75			–75			
		V <sub>CC</sub> = 3.6 V <sup>(2)</sup> , V <sub>I</sub> = 0 to 3.6 V				500 –750			500 –750			
I <sub>OZH</sub>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V		5			5			5			μA
I <sub>OZL</sub>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V		–5			–5			–5			μA
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, $\overline{OE}$ = don't care		±100 <sup>(3)</sup>			±100			±100			μA
I <sub>OZPD</sub>	V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, $\overline{OE}$ = don't care		±100 <sup>(3)</sup>			±100			±100			μA
I <sub>CC</sub>	V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND		0.19			0.19			0.19			mA
			5			5			5			
			0.19			0.19			0.19			
ΔI <sub>CC</sub> <sup>(4)</sup>	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND		0.2			0.2			0.2			mA
C <sub>i</sub>	V <sub>I</sub> = 3 V or 0 V		4			4			4			pF
C <sub>o</sub>	V <sub>O</sub> = 3 V or 0 V		9			9			9			pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) On products compliant to MIL-PRF-38535, this parameter does not apply.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

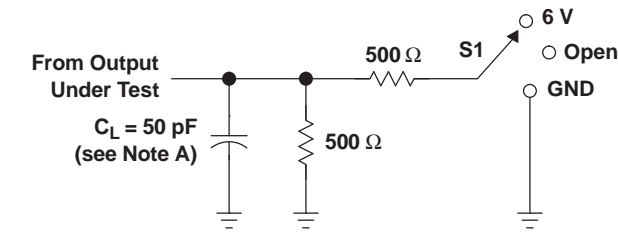
## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))<sup>(1)</sup>

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16244A				–40°C to 85°C SN74LVTH16244A				Recommended –40°C to 125°C SN74LVTH16244A				UNIT		
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$				
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	TYP	MAX		MIN	MAX
$t_{PLH}$	A	Y	1.1	4.4	4.6		1.2	2.3	3.2	3.7		1.2	2.3	4.4	4.6		ns
$t_{PHL}$			1.1	3.6	3.9		1.2	2	3.2	3.7		1.2	2	3.6	3.9		
$t_{PZH}$	$\overline{OE}$	Y	1.1	4.6	5.4		1.2	2.6	4	5		1.2	2.6	4.6	5.4		ns
$t_{PZL}$			1.1	5.4	6.2		1.2	2.7	4	5		1.2	2.7	5.4	6.2		
$t_{PHZ}$	$\overline{OE}$	Y	1.6	5.7	6.2		2.2	3.3	4.5	5		2.2	3.3	5.7	6.2		ns
$t_{PLZ}$			1.2	5	4.7		2	3.1	4.2	4.4		2	3.1	5	4.7		
$t_{sk(LH)}$									0.5			0.5				ns	
$t_{sk(HL)}$									0.5			0.5					

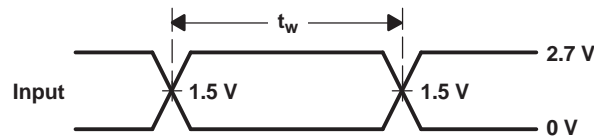
(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

PARAMETER MEASUREMENT INFORMATION

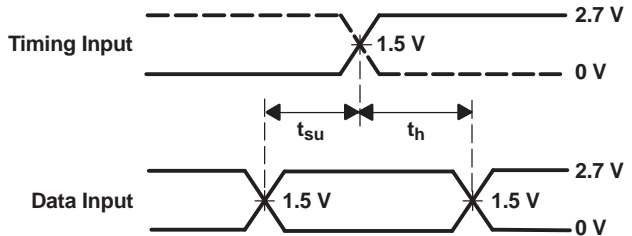


LOAD CIRCUIT

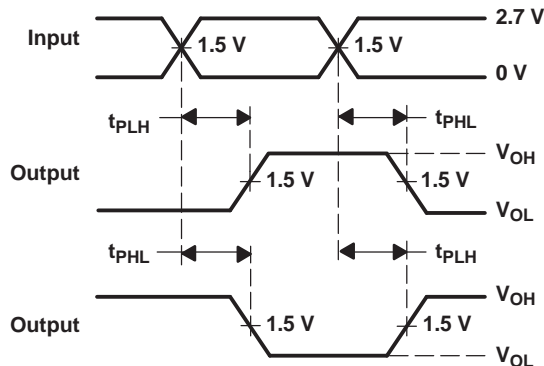
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



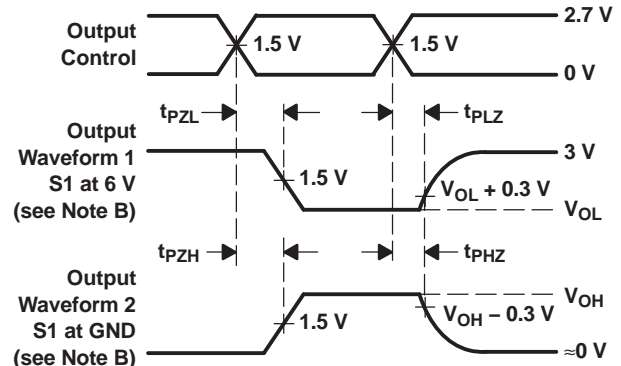
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

---

**REVISION HISTORY**

<b>Changes from Revision T (November 2006) to Revision U</b>	<b>Page</b>
• Updated document to new TI data sheet format - no specification changes. ....	1
• Removed ordering information. ....	1
• Updated operating temperature range. ....	5

---

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9668501QXA	ACTIVE	CFP	WD	48	15	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9668501QX A SNJ54LVTH16244 AWD	Samples
5962-9668501VXA	ACTIVE	CFP	WD	48	15	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9668501VX A SNV54LVTH16244 AWD	Samples
74LVTH16244ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A	Samples
74LVTH16244ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A	Samples
SN74LVTH16244ADGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A	Samples
SN74LVTH16244ADGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LL244A	Samples
SN74LVTH16244ADL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A	Samples
SN74LVTH16244ADLG4	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A	Samples
SN74LVTH16244ADLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A	Samples
SNJ54LVTH16244AWD	ACTIVE	CFP	WD	48	15	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9668501QX A SNJ54LVTH16244 AWD	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVTH16244A, SN54LVTH16244A-SP, SN74LVTH16244A :**

● Catalog : [SN74LVTH16244A](#), [SN54LVTH16244A](#)

● Enhanced Product : [SN74LVTH16244A-EP](#), [SN74LVTH16244A-EP](#)

● Military : [SN54LVTH16244A](#)

● Space : [SN54LVTH16244A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16244ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH16244ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVTH16244ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16244ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVTH16244ADGVR	TVSOP	DGV	48	2000	356.0	356.0	35.0
SN74LVTH16244ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

**TUBE**

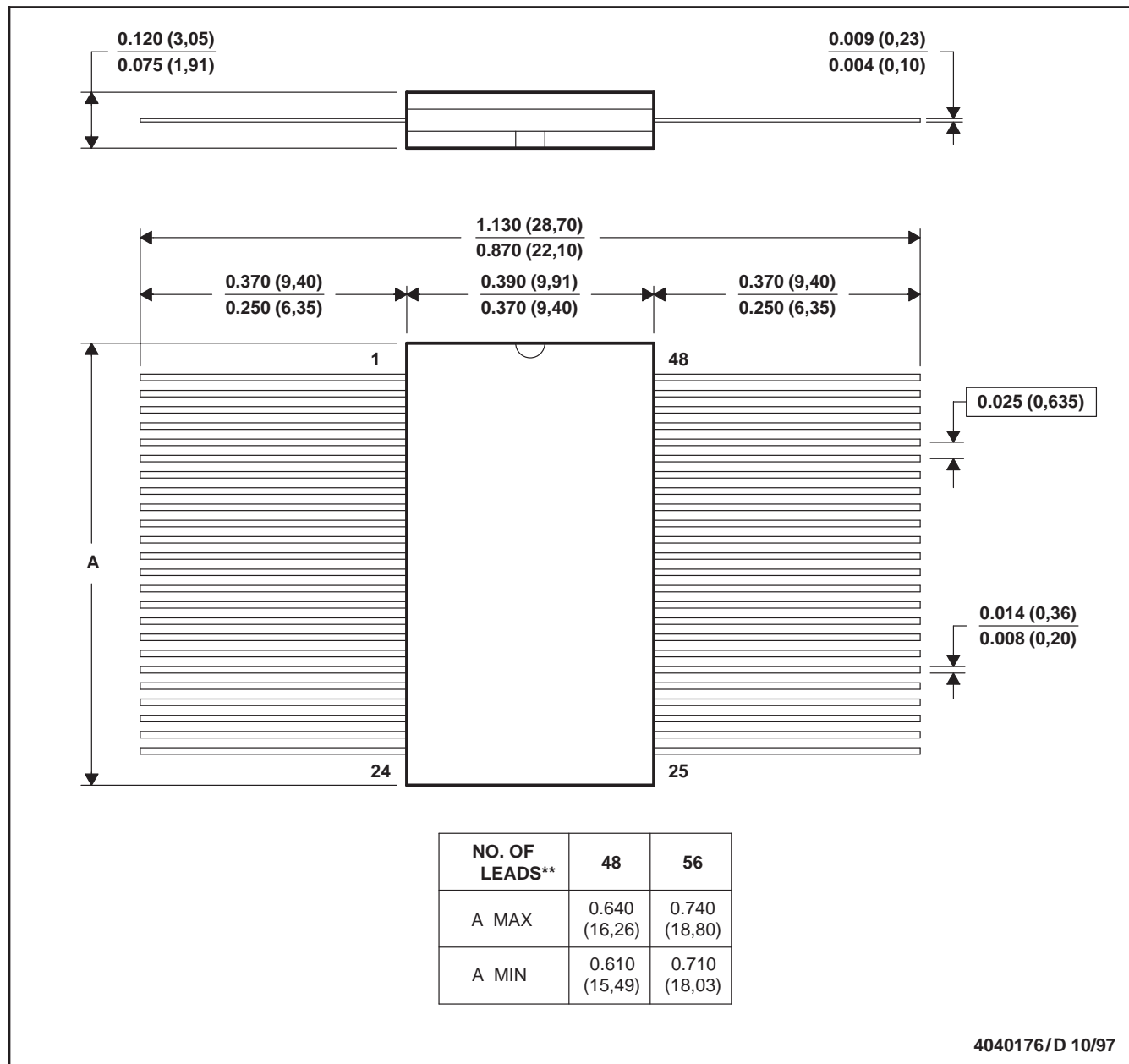

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVTH16244ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVTH16244ADLG4	DL	SSOP	48	25	473.7	14.24	5110	7.87

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN

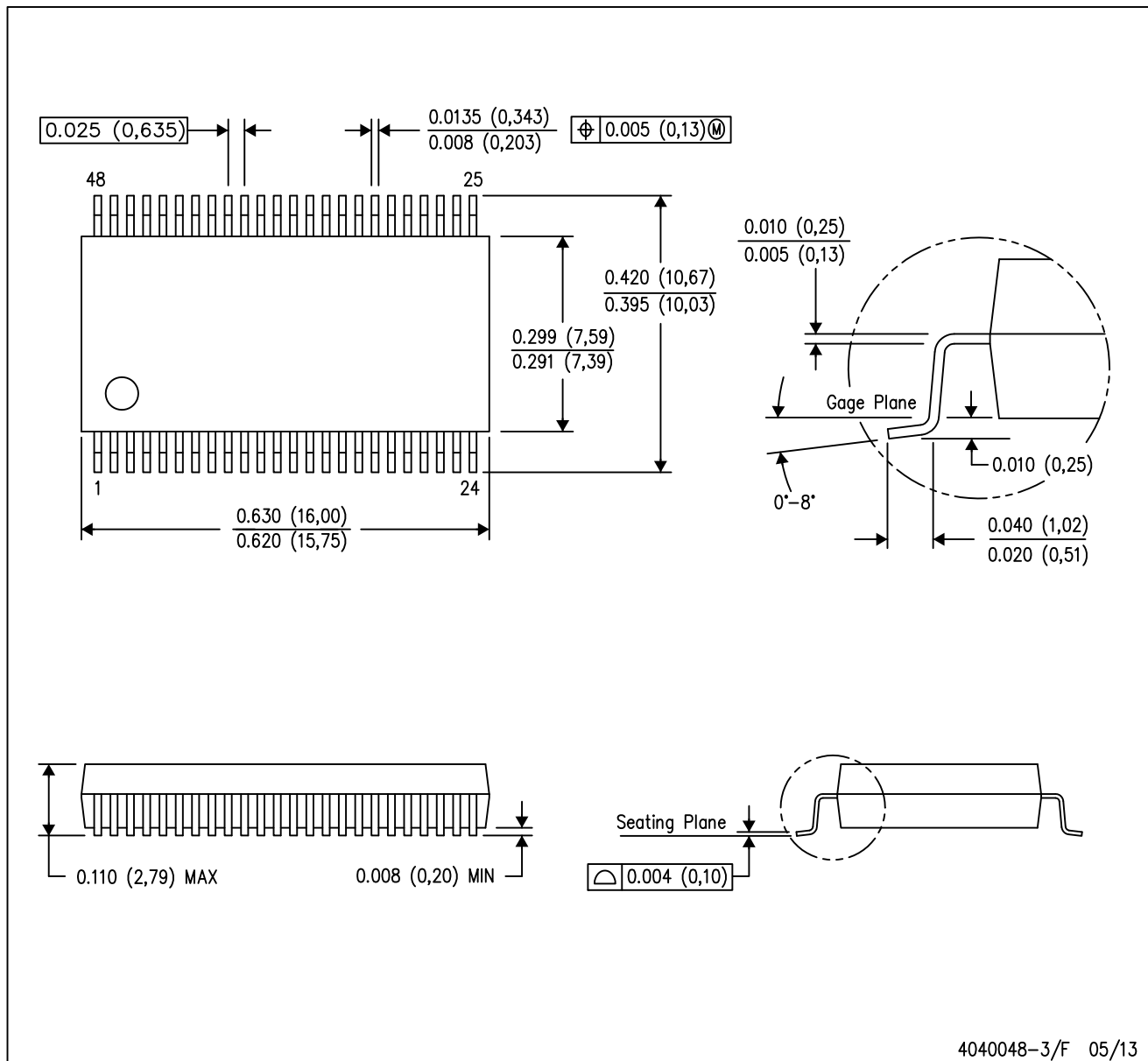


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

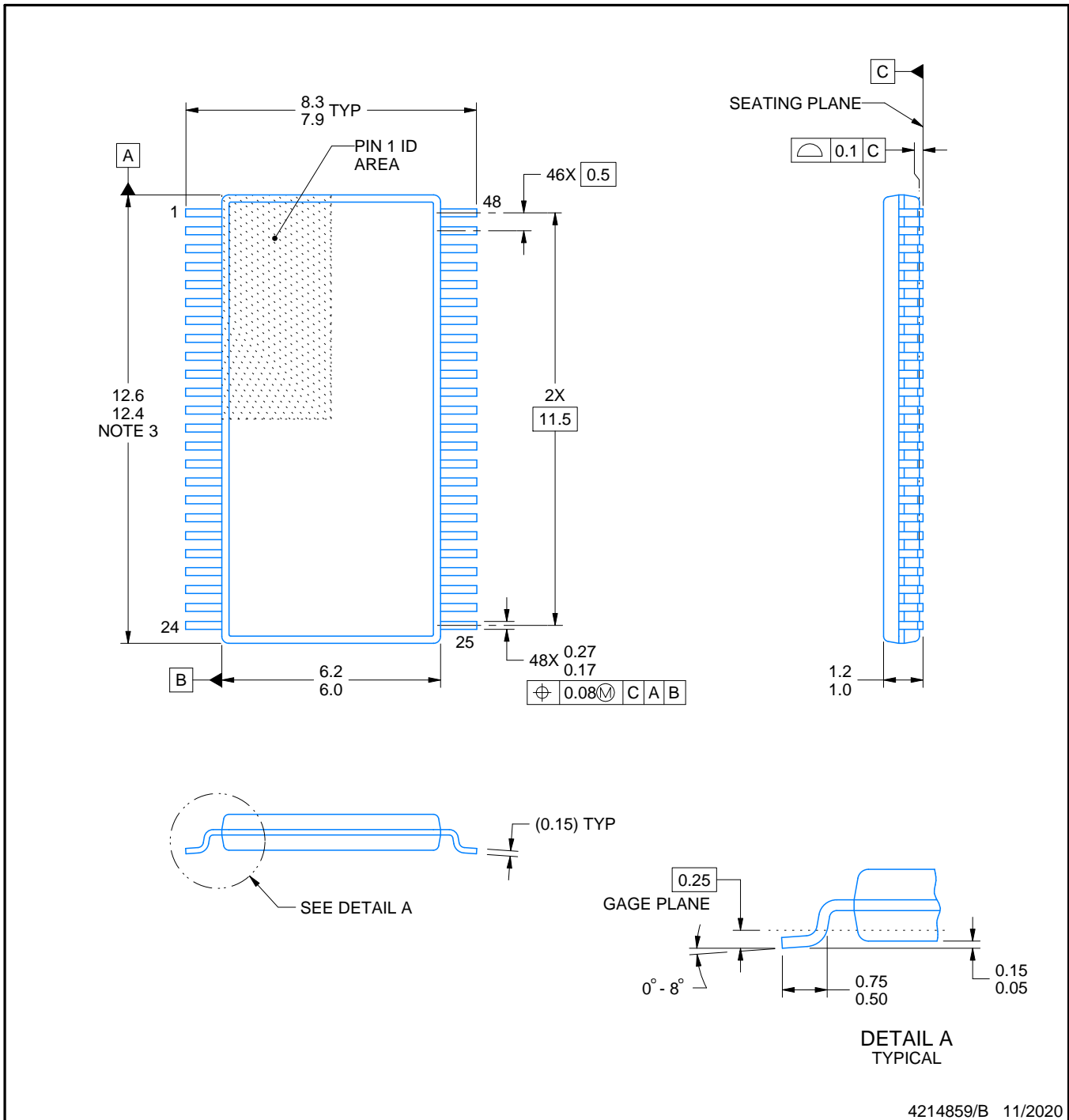
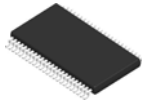
DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



4214859/B 11/2020

NOTES:

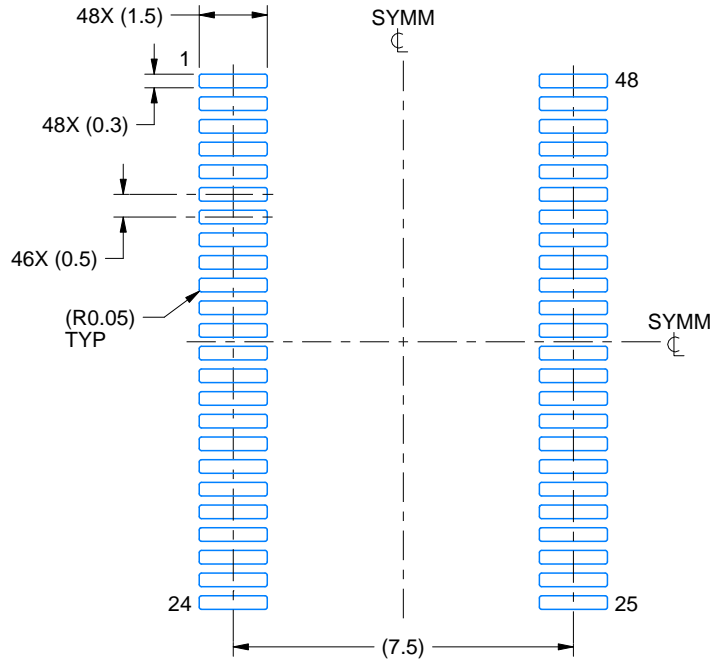
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

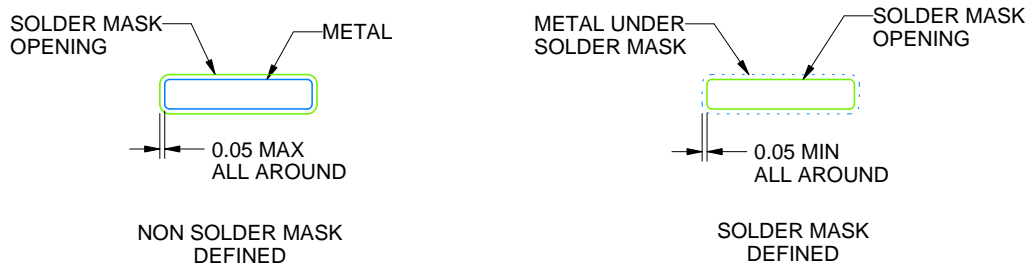
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

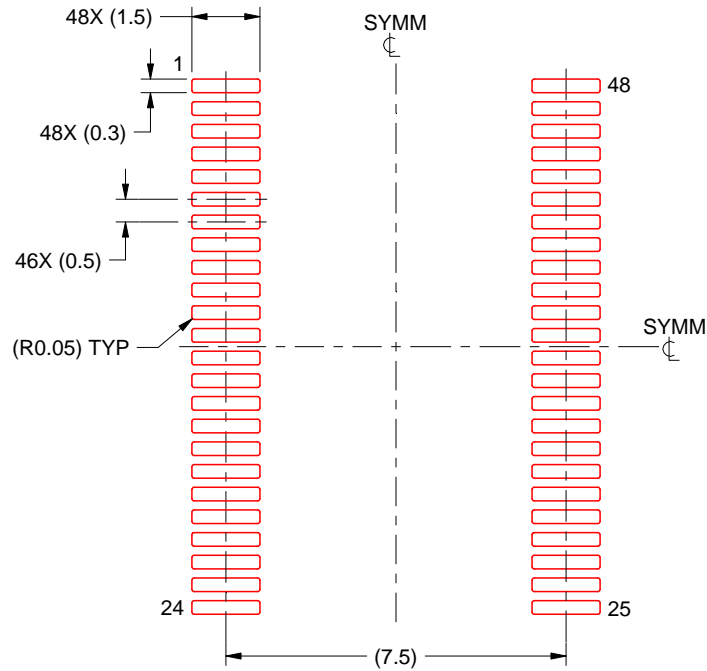
- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

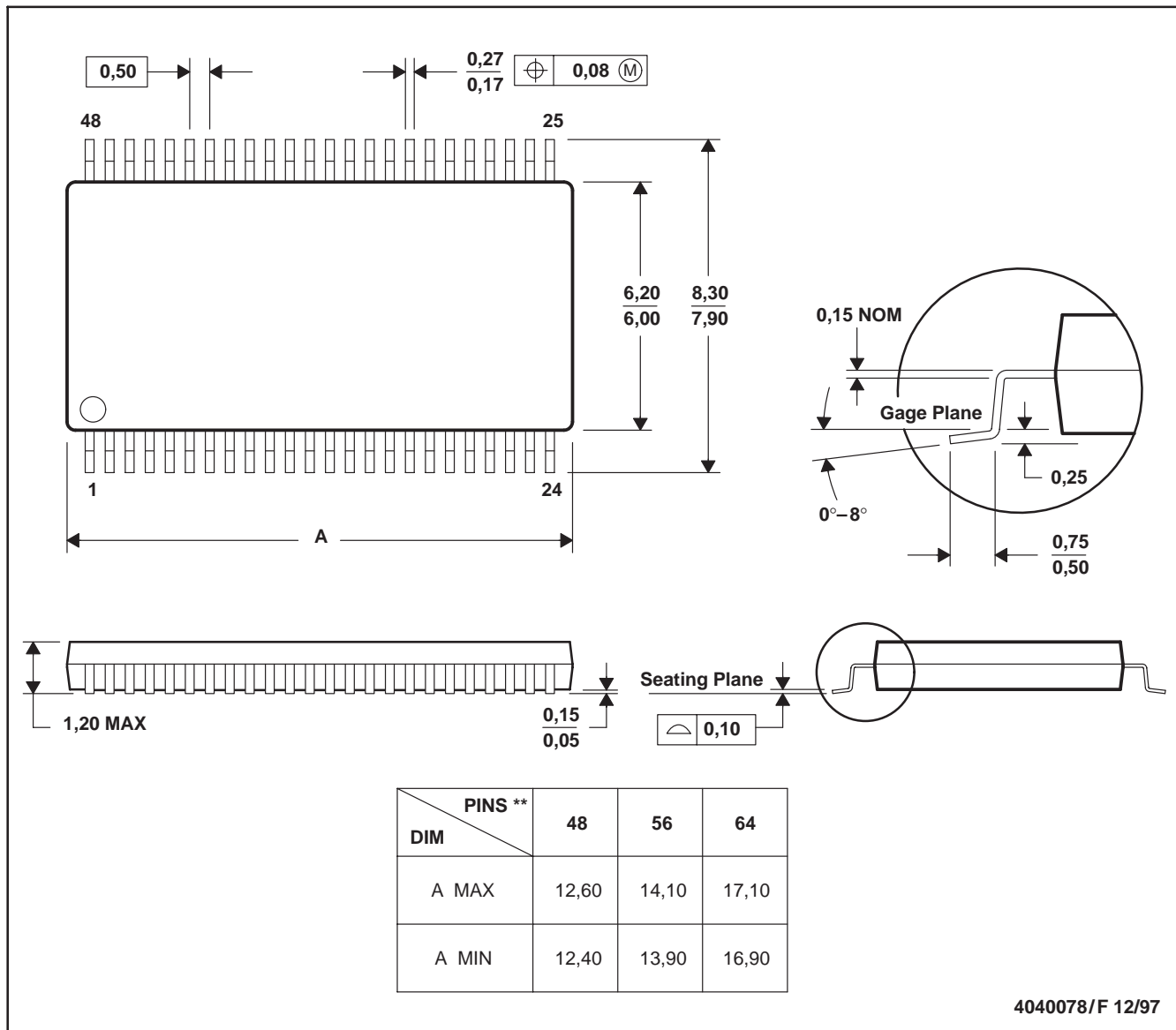
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

⊖ [View SN74LVTH16244ADGVR on WIN SOURCE](#)

⊖ [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management