THE DATASHEET OF

MAX14611ETD+T

EVALUATION KIT AVAILABLE

MAX14611

Quad Bidirectional Low-Voltage Logic-Level Translator

General Description

The MAX14611 is a quad bidirectional logic-level translator that provides the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. A low-voltage logic signal present on the V_L side of the device appears as a high-voltage logic signal on the V_{CC} side of the device, and vice-versa.

The device is ideal for I²C bus as well as MDIO bus applications where open-drain operation is often required. The device features a three-state output mode ($\overline{TS}$). Drive $\overline{TS}$ high to connect the pullup to the powered I/O port. This allows for continuous, undisrupted I²C operation on the powered side of the device while the level translation function is off. The MAX14611 is a pin-to-pin compatible upgrade to the MAX3378E in the TDFN package.

The MAX14611 features enhanced high-electrostatic-discharge (ESD) protection on all I/OVCC_ ports up to ±6kV HBM. The device operates over the -40°C to +85°C extended temperature range and is available in 3mm x 3mm, 14-pin TDFN and 4.9mm x 5.1mm, 14-pin TSSOP packages.

Applications

SPI, I²C, and MDIO Level Translation

Low-Voltage ASIC Level Translation

Portable Electronics

Mobile Phones

POS Systems

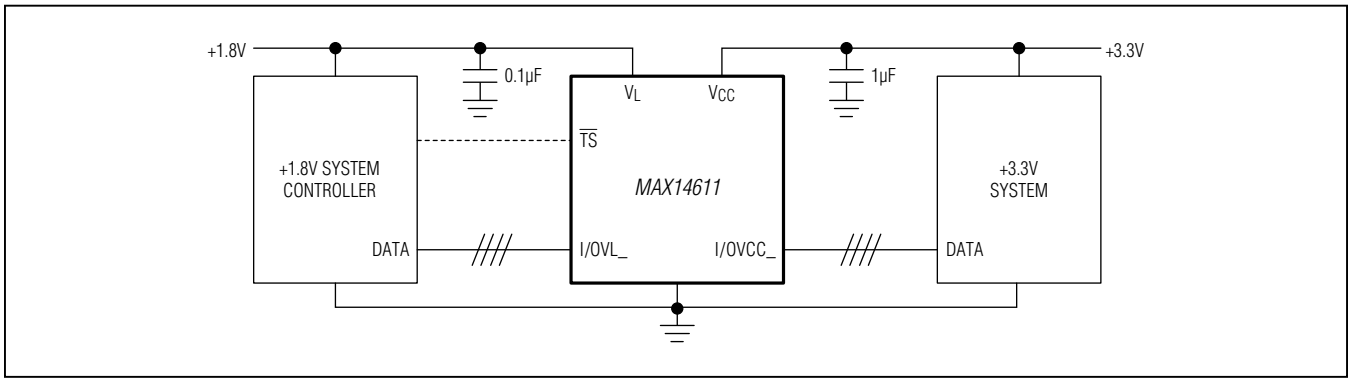
Telecommunications Equipment

Benefits and Features

- **Improved Interoperability**
  - **Meets I²C Specifications**
  - **10kΩ Internal Pullup Resistor**
  - **Pin-to-Pin Compatible with the MAX3377E and the MAX3378E**
  - **0.9V Operation on Low Voltage Supply**
- **Robust Logic-Level Translation**
  - **±0.5V Tolerances on All Pins**
  - **±6kV Human Body Model ESD Protection on I/OVCC_ Lines**
  - **Thermal Short-Circuit Protection**
  - **Short to Ground Fault Protection on All Pins**
  - **-40°C to +85°C Operating Temperature Range**
- **Increased Design Flexibility**
  - **Ultra-Low Supply Current**
  - **Pullup Resistor Enabled with a Single Power Supply when $\overline{TS}$ = High**
  - **10Ω (max) Transmission Gate FET**
  - **Small, 14-Pin, 3.0mm x 3.0mm TDFN Package and 14-Pin, 4.9mm x 5.1mm TSSOP Package**

Ordering Information appears at end of data sheet.

Typical Operating Circuit



For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX14611.related.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6276; Rev 0; 4/12

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V_{CC} ..... -0.5V to +6V
V_L ..... -0.5V to +5.5V
$\overline{TS}$ ..... -0.5V to +6V
I/OVCC_ ..... -0.5V to (V_{CC} + 0.5V)
I/OVL_ ..... -0.5V to (V_L + 0.5V)
Short-Circuit Duration I/OVL_, I/OVCC_ to GND ..... Continuous
Continuous Current ..... ±50mA

Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 24.4mW/°C above +70°C) 1951.2mW
TSSOP (derate 10mW/°C above +70°C) 796.8mW
Operating Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 8°C/W

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 100.4°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 30°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = 0.9V to the lesser of V_{CC} + 0.3V and 5V. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_L Supply Range	V_L		0.9		5	V
V_{CC} Supply Range	V_{CC}		1.65		5.5	V
V_L Supply Current	I_{VL}	I/OVCC_ = V_{CC}, I/OVL_ = V_L, $\overline{TS}$ = V_L			1	µA
V_{CC} Supply Current	I_{VCC}	I/OVCC_ = V_{CC}, I/OVL_ = V_L, $\overline{TS}$ = V_L			35	µA
V_{CC} Shutdown Mode Supply Current	I_{SHDN_VCC}	$\overline{TS}$ = GND, I/OVCC = unconnected		0.1	1	µA
		$\overline{TS}$ = V_{CC}, V_L = GND, I/OVCC = unconnected		0.1	1	
V_L Shutdown Mode Supply Current	I_{SHDN_VL}	$\overline{TS}$ = GND		0.1	1	µA
		$\overline{TS}$ = V_L, V_{CC} = GND, I/OVL_ = unconnected		0.1	1	
I/OVCC_, I/OVL_, $\overline{TS}$ Leakage Current	I_{LEAK}	T_A = +25°C, $\overline{TS}$ = GND		0.1	1	µA
$\overline{TS}$ Input Leakage Current	I_{LEAK_TS}	T_A = +25°C			1	µA
V_L Shutdown Threshold	V_{TH_VL}			0.3	0.85	V
V_{CC} Shutdown Threshold	V_{TH_VCC}			0.8	1.35	V
I/OVL_ Pullup Resistor	R_{VL_PU}			10		kΩ
I/OVCC_ Pullup Resistor	R_{VCC_PU}			10		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = 0.9V to the lesser of V_{CC} + 0.3V and 5V. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/OVL_ to I/OVCC_ DC Resistance	R_{IOVL_IOVCC}	Inferred from V_{OL} measurements		5	10	Ω
I/OVL_ Input-Voltage High	V_{IHL}		V_L - 0.2			V
I/OVL_ Input-Voltage Low	V_{ILL}				0.15	V
I/OVCC_ Input-Voltage High	V_{IHC}		V_{CC} - 0.4			V
I/OVCC_ Input-Voltage Low	V_{ILC}				0.2	V
I/OVL_ Output-Voltage High	V_{OHL}	I/OVL_ source current = 10µA	0.7 x V_L			V
I/OVL_ Output-Voltage Low	V_{OLL}	I/OVL_ sink current = 2mA, $V_{I/OVCC\_} \leq$ 50mV			0.4	V
I/OVCC_ Output-Voltage High	V_{OHC}	I/OVCC_ source current = 10µA	0.7 x V_{CC}			V
I/OVCC_ Output Voltage Low	V_{OLC}	I/OVCC_ sink current = 2mA, $V_{I/OVL\_} \leq$ 150mV			0.4	V
$\overline{TS}$ Input-Voltage High Threshold	V_{IH}		V_L - 0.2			V
$\overline{TS}$ Input-Voltage Low Threshold	V_{IL}	V_L > 1.3V			0.2	V
Accelerator Pulse Duration		Inferred from timing measurements			30	ns
V_L Output Accelerator Source Impedance		V_L = 0.9V		70		Ω
		V_L = 3.3V		15		
V_{CC} Output Accelerator Source Impedance		V_{CC} = 1.65V		50		Ω
		V_{CC} = 5.0V		10		
Thermal-Shutdown Threshold		20°C hysteresis		+150		°C
ESD PROTECTION						
I/OVCC_		Human Body Model, C_{VCC} = 1µF, C_{VL} = 0.1µF		±6		kV
All Other Pins		Human Body Model		±2		kV

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +0.9V to the lesser of V_{CC} + 0.3V and 5V, $\overline{TS}$ = V_L, R_L = 1MΩ, C_{VCC} = 1µF, C_{VL} = 0.1µF, $C_{I/OVCC\_}$ = 15pF, $C_{I/OVL\_}$ = 15pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are V_{CC} = +3.3V, V_L = +1.8V, and T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/OVCC_ Rise Time	t_{RVCC}	Push-pull driving (Figure 1)			40	ns
		Open-drain driving (Figure 2, Note 5)			100	
I/OVCC_ Fall Time	t_{FVCC}	Push-pull driving (Figure 1)			40	ns
		Open-drain driving (Figure 2, Note 5)			50	
I/OVL_ Rise Time	t_{RVL}	Push-pull driving (Figure 3)			30	ns
		Open-drain driving (Figure 4, Note 5)			105	
I/OVL_ Fall Time	t_{FVL}	Push-pull driving (Figure 3)			30	ns
		Open-drain driving (Figure 4, Note 5)			30	
Propagation Delay	I/O_{VL-VCC}	Push-pull driving (Figure 1)			40	ns
	I/O_{VL-VCC}	Open-drain driving (Figure 2, Note 5)			150	
Propagation Delay	I/O_{VCC-VL}	Push-pull driving (Figure 3)			30	ns
	I/O_{VCC-VL}	Open-drain driving (Figure 4, Note 5)			105	
Channel-to-Channel Skew	t_{SKEW}	Input rise time/fall time < 6ns, push-pull driving			20	ns
		Input rise time/fall time < 6ns, open-drain driving			50	
Maximum Data Rate		Push-pull operation			20	Mbps
		Open-drain operation (Notes 5, 6)			6	

Note 2: All units are 100% production tested at T_A = +25°C. Specifications over operating temperature range are guaranteed by design.

Note 3: V_L must be less than or equal to V_{CC} during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions.

Note 4: All timing is 10% to 90% for rise time and 90% to 10% for fall time.

Note 5: Not production tested; guaranteed by design.

Note 6: Requires the external pullup resistor.

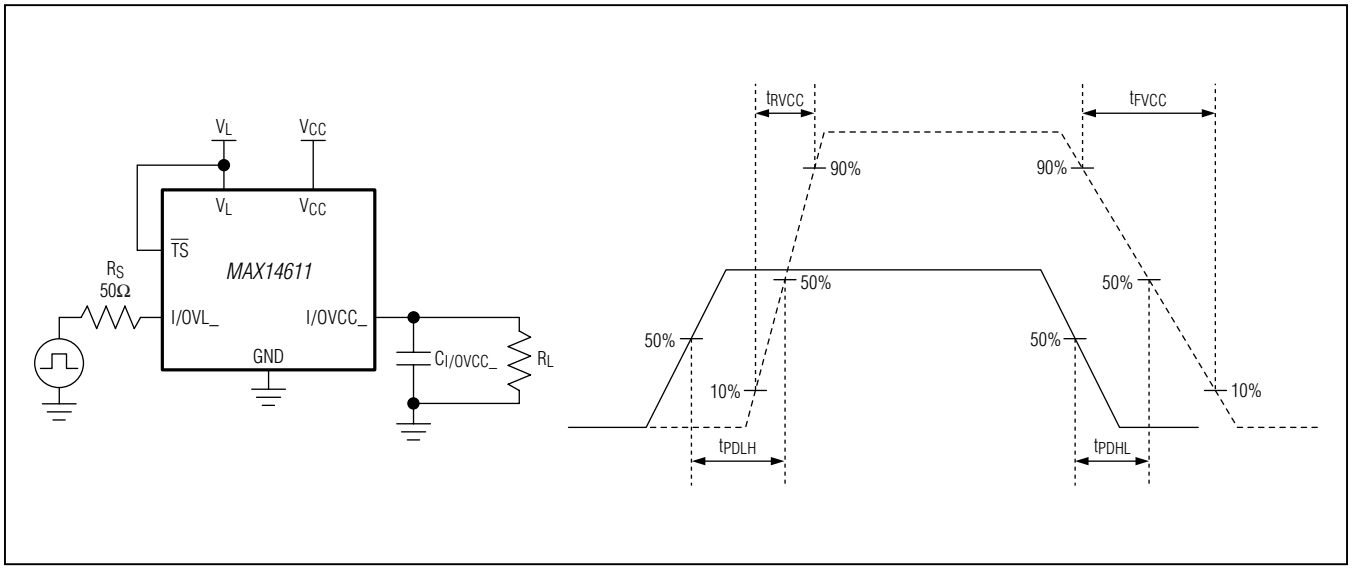


*Figure 1. Push-Pull Driving I/OVL_*

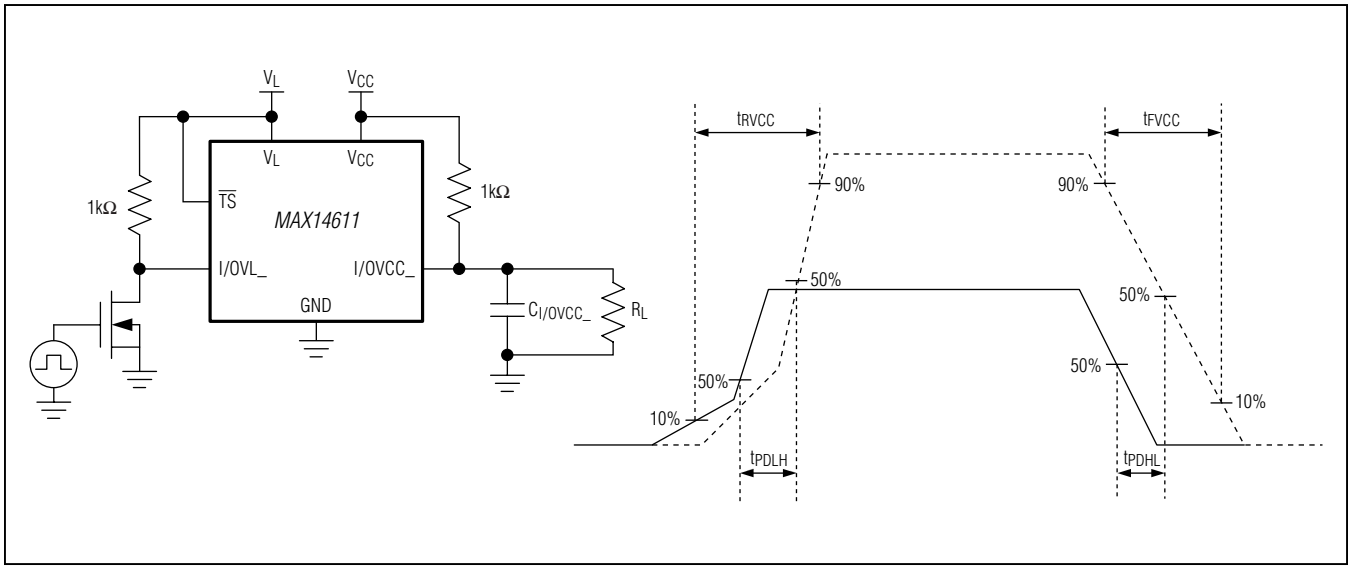


*Figure 2. Open-Drain Driving I/OVL_*

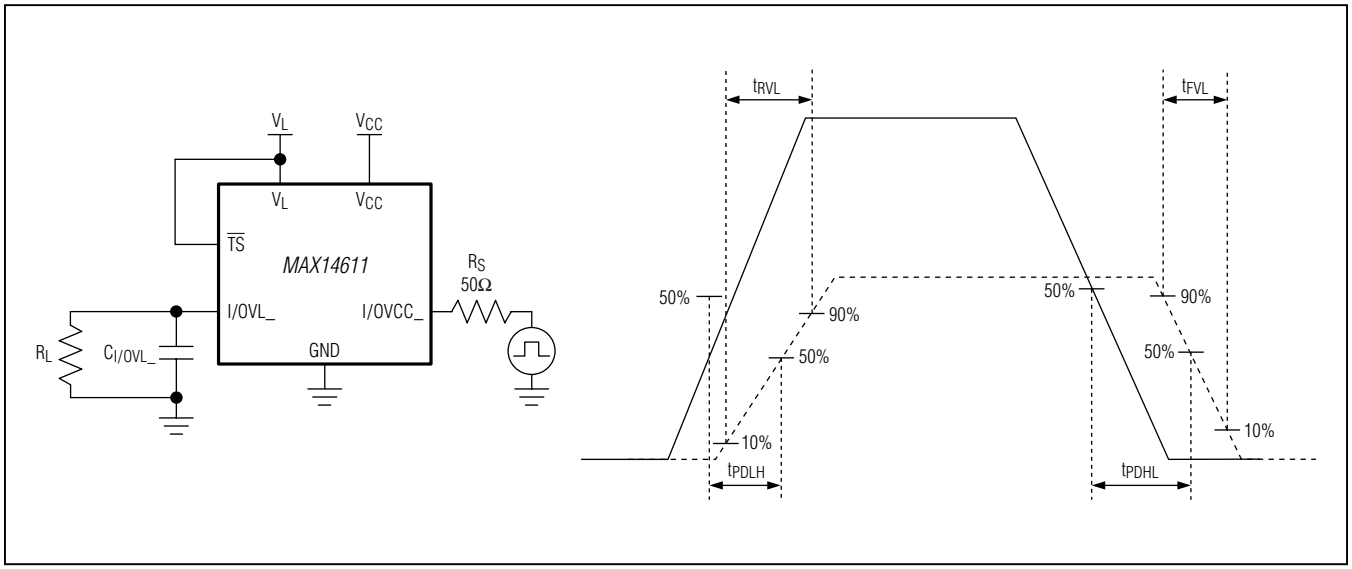


*Figure 3. Push-Pull Driving I/OVCC_*

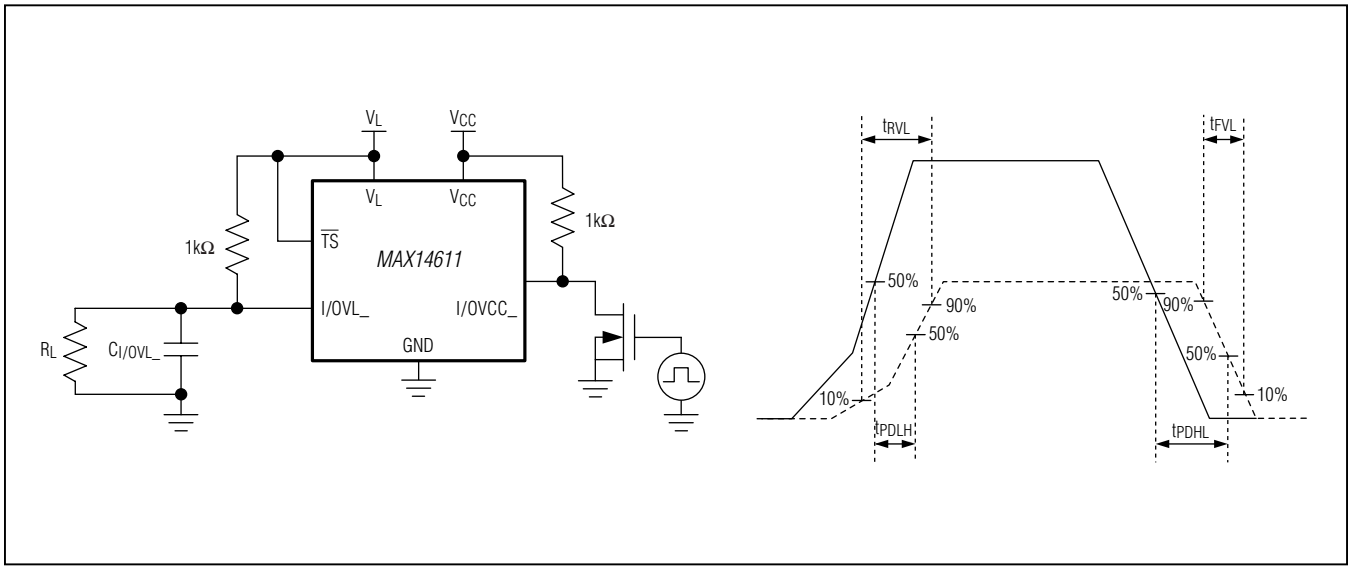
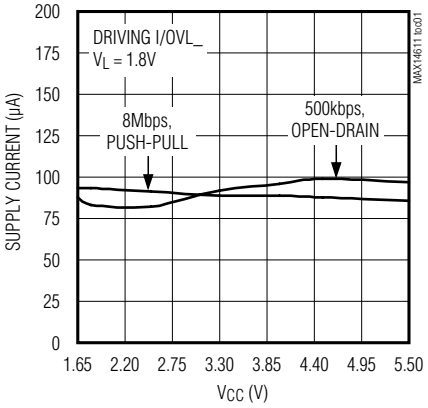


*Figure 4. Open-Drain Driving I/OVCC_*

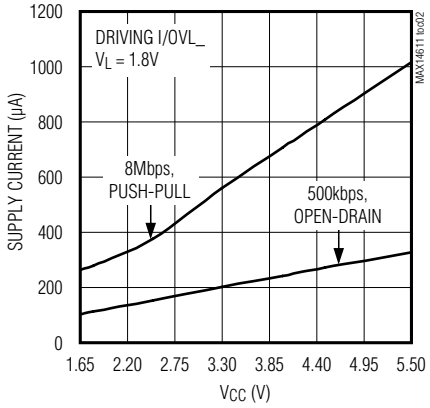
Typical Operating Characteristics

(V_{CC} = +3.3V, V_L = 1.8V, R_L = 1MΩ, C_L = 15pF, T_A = +25°C, data rate = 500kbps in open-drain operation and 8Mbps in push-pull operation, unless otherwise noted.)

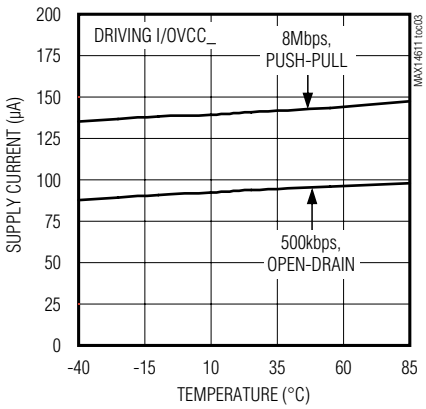
V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE



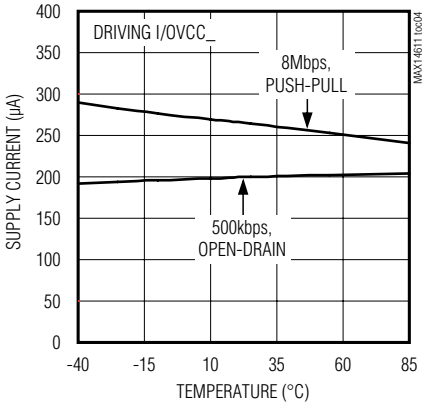
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE



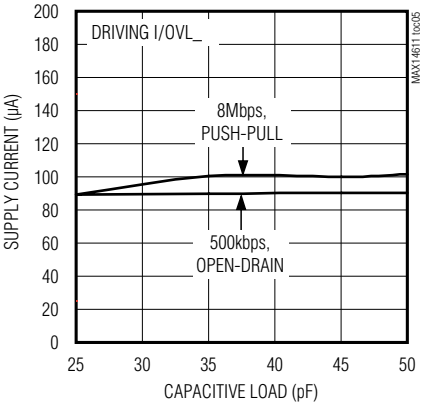
V_L SUPPLY CURRENT vs. TEMPERATURE



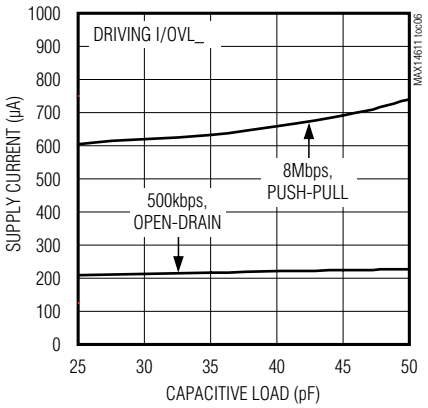
V_{CC} SUPPLY CURRENT vs. TEMPERATURE



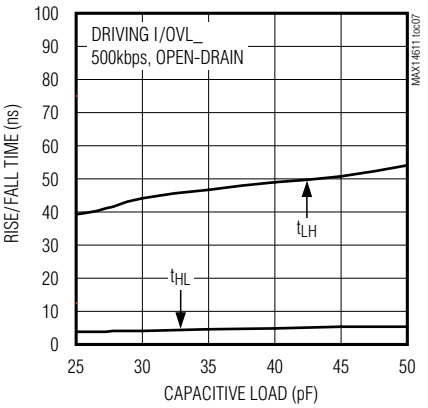
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD



V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD



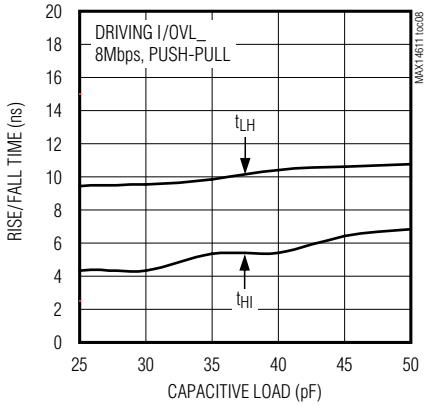
RISE/FALL TIME vs. CAPACITIVE LOAD



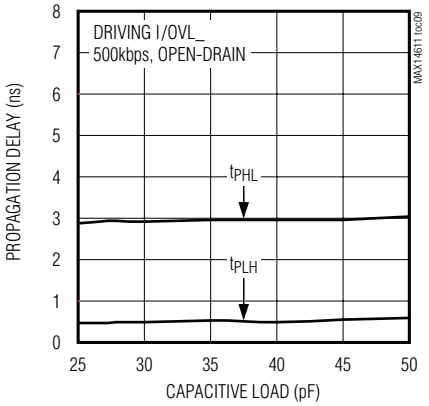
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = 1.8V, R_L = 1MΩ, C_L = 15pF, T_A = +25°C, data rate = 500kbps in open-drain operation and 8Mbps in push-pull operation, unless otherwise noted.)

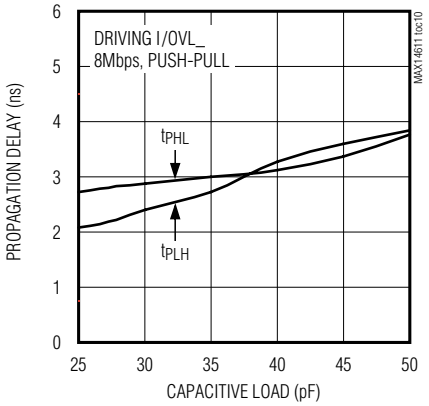
RISE/FALL TIME vs. CAPACITIVE LOAD



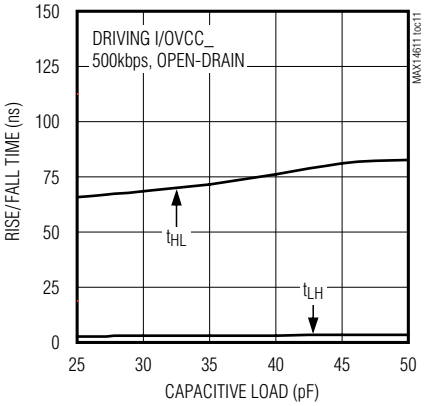
PROPAGATION DELAY vs. CAPACITIVE LOAD



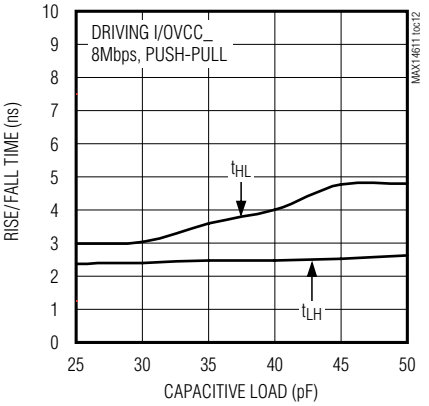
PROPAGATION DELAY vs. CAPACITIVE LOAD



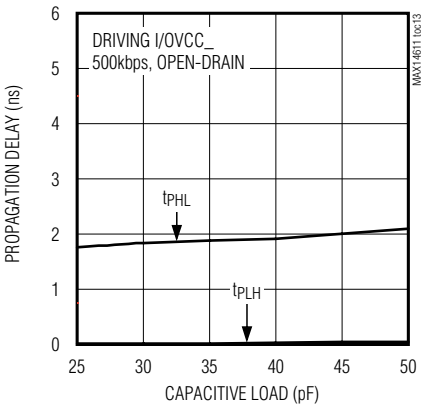
RISE/FALL TIME vs. CAPACITIVE LOAD



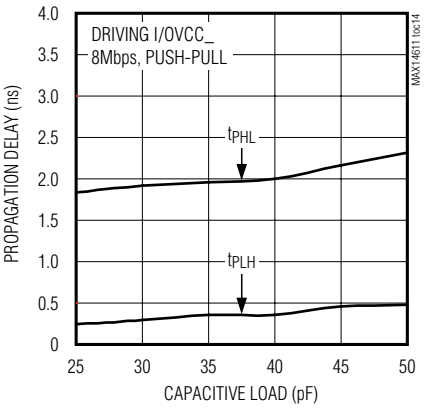
RISE/FALL TIME vs. CAPACITIVE LOAD



PROPAGATION DELAY vs. CAPACITIVE LOAD



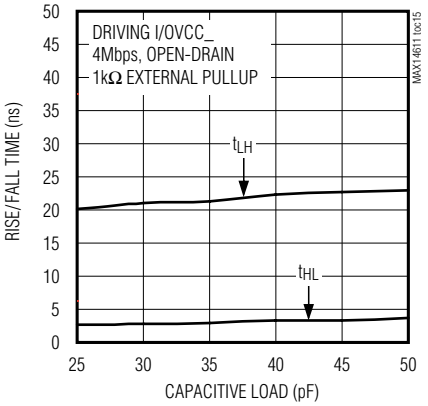
PROPAGATION DELAY vs. CAPACITIVE LOAD



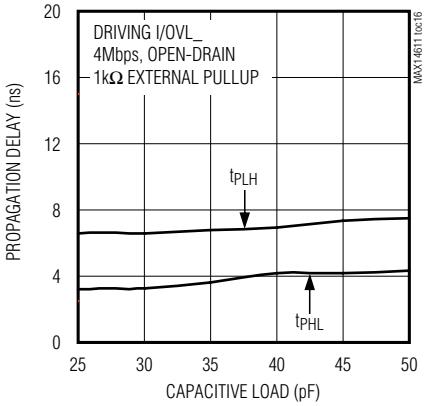
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = 1.8V, R_L = 1MΩ, C_L = 15pF, T_A = +25°C, data rate = 500kbps in open-drain operation and 8Mbps in push-pull operation, unless otherwise noted.)

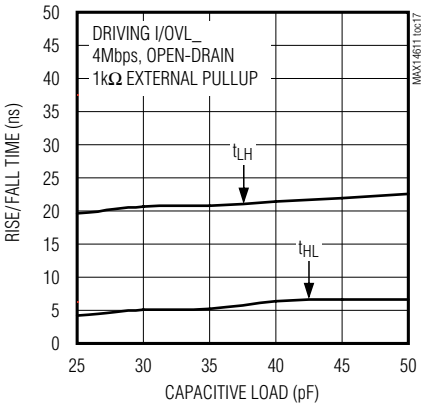
RISE/FALL TIME vs. CAPACITIVE LOAD



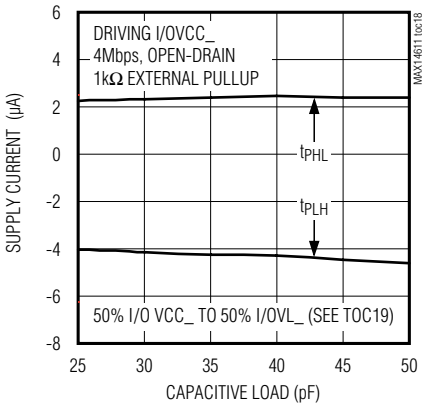
PROPAGATION DELAY vs. CAPACITIVE LOAD



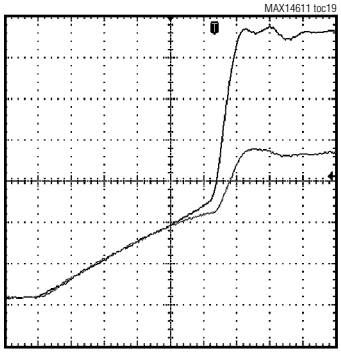
RISE/FALL TIME vs. CAPACITIVE LOAD



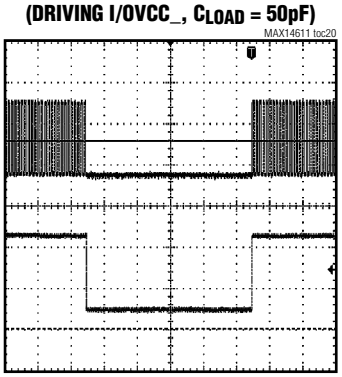
PROPAGATION DELAY vs. CAPACITIVE LOAD



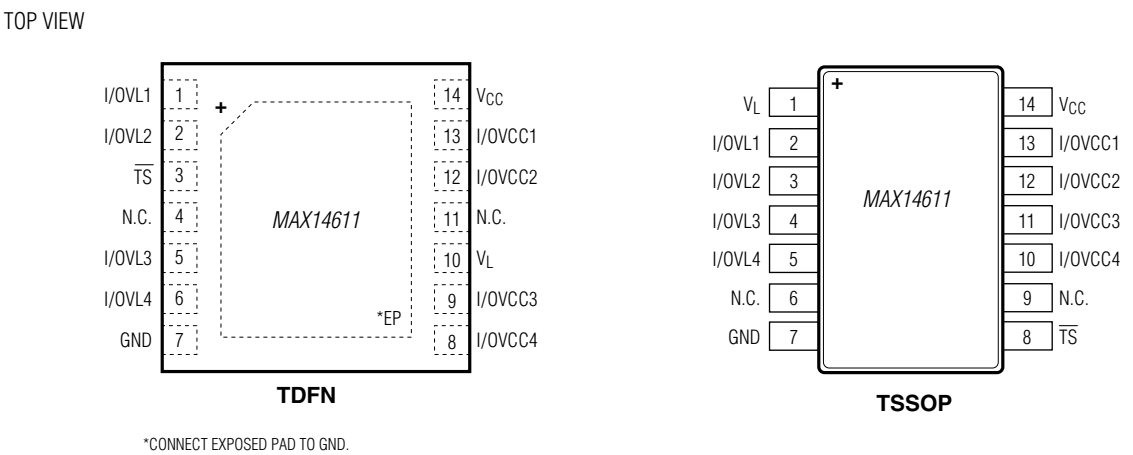
LOW-TO-HIGH TRANSITION, OPEN-DRAIN ZOOM



ENTERING AND EXITING THREE-STATE MODE (DRIVING I/OVCC_, C_{LOAD} = 50pF)



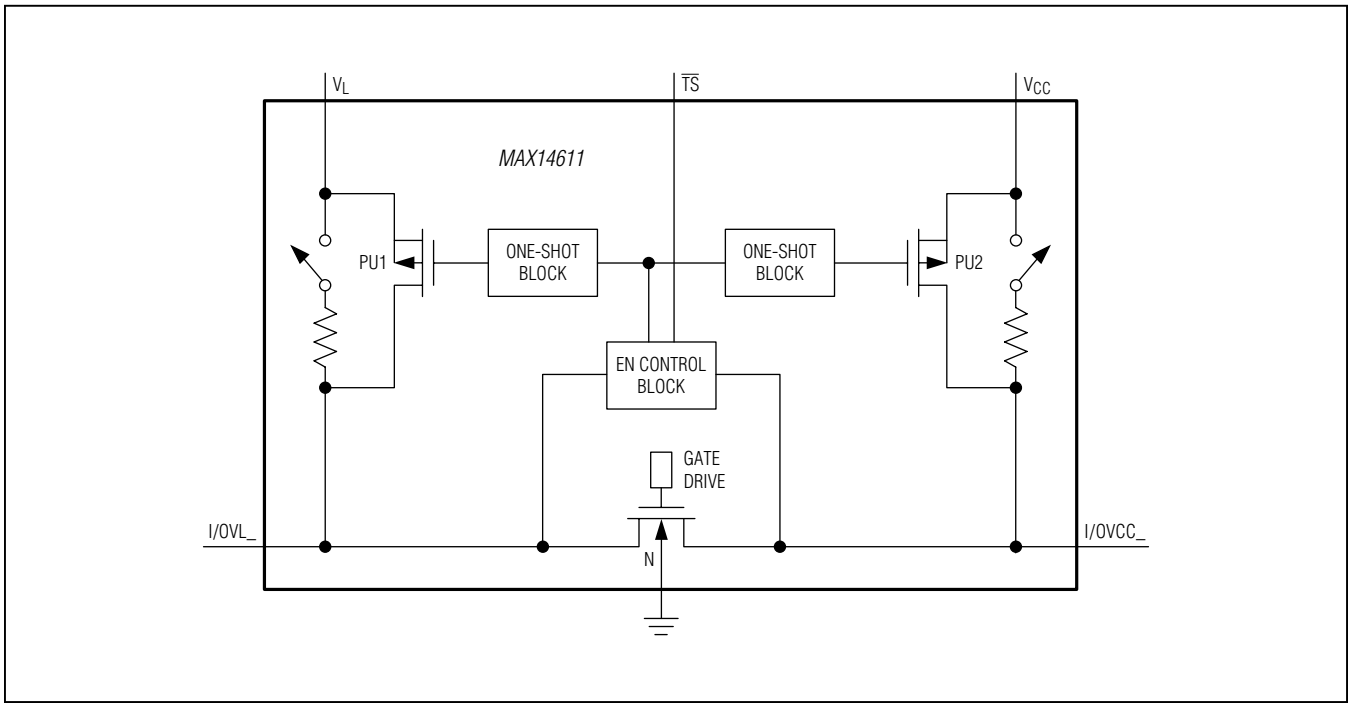
Pin Configurations



Pin Description

PIN		NAME	FUNCTION
TDFN-EP	TSSOP		
1	2	I/OVL1	Input/Output 1. Reference to V_L.
2	3	I/OVL2	Input/Output 2. Reference to V_L.
3	8	$\overline{TS}$	Three-State Select Input. Drive $\overline{TS}$ low to place the device in three-state output mode. I/OVCC_ and I/OVL_ are high impedance in three-state output mode. **Note:** Logic referenced to V_L (for logic thresholds, see the *Electrical Characteristics* table).
4, 11	6,9	N.C.	No Connection. Not internally connected.
5	4	I/OVL3	Input/Output 3. Reference to V_L.
6	5	I/OVL4	Input/Output 4. Reference to V_L.
7	7	GND	Ground
8	10	I/OVCC4	Input/Output 4. Reference to V_{CC}.
9	11	I/OVCC3	Input/Output 3. Reference to V_{CC}.
10	1	V_L	Logic Supply Voltage Input, $0.9V \le V_L \le \min(5.0V, (V_{CC} + 0.3V))$. Connect a 0.1µF ceramic capacitor as close as possible to the pin.
12	12	I/OVCC2	Input/Output 2. Reference to V_{CC}.
13	13	I/OVCC1	Input/Output 1. Reference to V_{CC}.
14	14	V_{CC}	Power Supply Input. The supply range is $1.65V \le V_{CC} \le 5.5V$. Bypass V_{CC} with a 1µF ceramic capacitor as close as possible to the pin to achieve higher ESD protection (±6kV HBM).
—	—	EP	Exposed Pad (TDFN Only). EP is internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Functional Diagram



Detailed Description

The MAX14611 ESD-protected level translator provides the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. A low-voltage logic signal present on the V_L side of the device appears as a high-voltage logic signal on the V_{CC} side of the device, and vice-versa.

The MAX14611 bidirectional level translator utilizes a transmission-gate based design (see the *Functional Diagram*) to allow data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The device accepts V_L from +0.9V to +5.0V and V_{CC} from +1.65V to +5.5V, making it ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The device features a three-state output mode, thermal short-circuit protection, and ±6kV ESD protection on the V_{CC} side for greater protection in applications that route signals externally.

Level Translation

For proper operation, ensure that $+1.65V \le V_{CC} \le +5.5V$, $0.9V \le V_L \le 5.0V$, and $V_L \le (V_{CC} + 0.3V)$. It is permissible for V_L to exceed (V_{CC} + 0.3V) during power-up sequencing. During power-supply sequencing, when V_{CC} is disconnected and V_L is powered up, a current can be sourced without a latchup or any damage to the device. The maximum data rate of the MAX14611 depends heavily on load capacitance (see the *Typical Operating Characteristics*), output impedance of the driver, and the operational voltage (see the *Timing Characteristics* table).

Speed-Up Circuitry

The device features a one-shot generator that decreases the rise time of the output. When triggered following a rising edge, MOSFETs PU1 and PU2 turn on for a short time to pull up I/OVL_ and I/OVCC_ to their respective supplies (see the *Functional Diagram*). This greatly reduces the rise time and propagation delay for the low-to-high transition.

Rise-Time Accelerators (Figure 5)

The device has internal rise-time accelerators, allowing operation up to 20Mbps. The rise-time accelerators are present on both sides of the device and act to speed up the rise time of the input and output of the device, regardless of the direction of the data. The triggering mechanism for these accelerators is both level and edge sensitive. To prevent false triggering of the rise-time accelerators, and to take full advantage of them, signal rise/fall times of less than 2ns/V are recommended for both sides of the device. In open-drain driving, the recommendation only applies for fall time. Under less noisy conditions, longer signal fall times can be acceptable.

Three-State Output Mode ($\overline{TS}$)

Drive $\overline{TS}$ low to place the device in three-state output mode. Connect $\overline{TS}$ to V_L (logic-high) for normal operation. Activating the three-state output mode disconnects the internal 10kΩ pullup resistors on the I/OVCC_ and I/OVL_ lines. This forces the I/O lines to a high-impedance state and decreases the supply current to less than 1µA. The high-impedance I/O lines in three-state output mode allow for use in a multidrop network. When in three-state output mode, keep the I/OVL_ voltage below (V_L + 0.3V), and keep the I/OVCC_ voltage below (V_{CC} + 0.3V).

Thermal Short-Circuit Protection

Thermal-overload detection protects the device from short-circuit fault conditions. In the event of a short-circuit fault and when the junction temperature (T_J) reaches +150°C (typ), a thermal sensor signals the three-state output mode logic to force the device into three-state output mode. When T_J has cooled to +130°C (typ), normal operation resumes.

High ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/OVCC_ lines have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±6kV without damage.

The ESD structures withstand high ESD in all states: normal operation, three-state output mode, and powered down. After an ESD event, the device keeps working without latchup, whereas competing products can latch and must be powered down to remove latchup. ESD protection can be tested in various ways. The I/OVCC_ lines of this product family are characterized for protection.to ±6kV using the Human Body Model.

ESD Test Conditions

Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Applications Information

Power-Supply Decoupling

Bypass V_L to ground with a 0.1µF capacitor to reduce ripple and ensure correct data transmission. See the *Typical Operating Circuit*. To ensure full ±6kV ESD protection, bypass V_{CC} to ground with a 1µF capacitor. Place all capacitors as close as possible to the power-supply pins (V_{CC} and V_L).

Push-Pull vs. Open-Drain Driving

The device can be driven in a push-pull configuration. The device includes internal 10kΩ resistors that pull up I/OVL_ and I/OVCC_ to their respective power supplies, allowing operation of the I/O lines with open-drain devices. See the *Timing Characteristics* table for maximum data rates when using open-drain drivers (Figure 1, Figure 2, Figure 3, Figure 4).

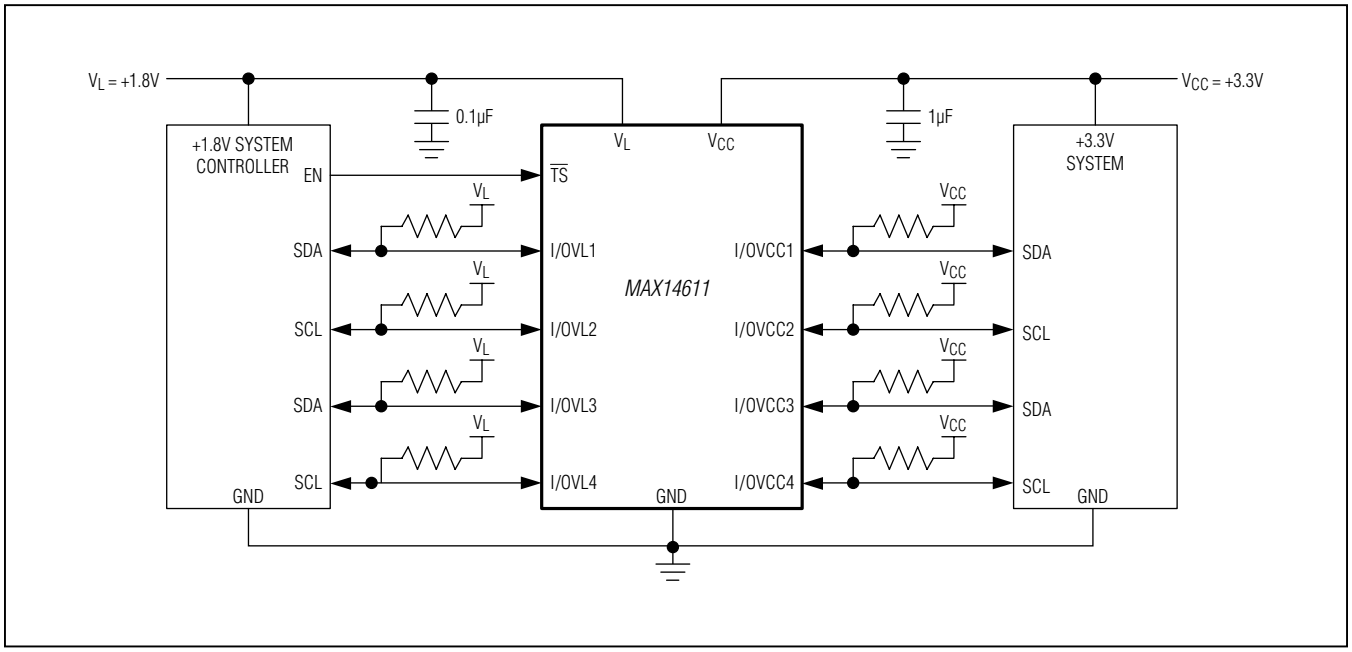
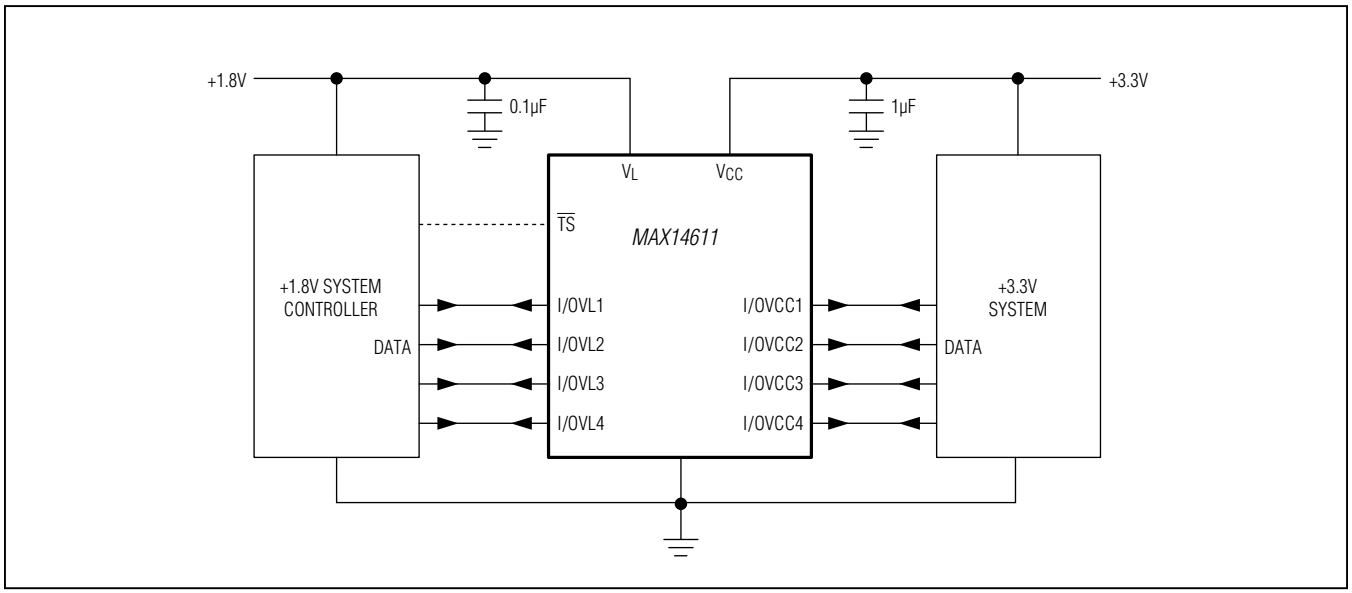


Figure 5. Open-Drain Operation

Applications Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14611ETD+	-40°C to +85°C	14 TDFN-EP*
MAX14611EUD+**	-40°C to +85°C	14 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TDFN-EP	T1433+2	21-0137	90-0063
14 TSSOP	U14+1	21-0066	90-0113

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/12	Initial release	—

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