THE DATASHEET OF

MAX14920ECB+T

www.win-source.net 0086-755-83957316

EVALUATION KIT AVAILABLE

MAX14920/MAX14921

High-Accuracy 12-/16-Cell Measurement AFEs

General Description

The MAX14920/MAX14921 battery measurement analog front-end devices accurately sample cell voltages and provide level shifting for primary/secondary battery packs up to 16 cells/+65V (max). The MAX14920 monitors up to 12 cells, while the MAX14921 monitors up to 16 cells. Both devices simultaneously sample all cell voltages, allowing accurate state-of-charge and source-resistance determination. All cell voltages are level shifted to ground reference with unity gain, simplifying external ADC data conversion.

The devices have a low-noise, low-offset amplifier that buffers differential voltages of up to +5V, allowing monitoring of all common lithium-ion (Li+) cell technologies. The resulting cell voltage error is ±0.5mV.

The devices' high accuracy make them ideal for monitoring cell chemistries with very flat discharge curves, such as lithium-metal phosphate.

Passive-cell balancing is supported by external FET drivers. Integrated diagnostics in the devices allow open-wire detection and undervoltage/overvoltage alarms. The devices are controlled by a daisy-chainable SPI interface.

The MAX14920 is available in a 64-pin (10mm x 10mm) TQFP package with an exposed pad. The MAX14921 is available in an 80-pin (12mm x 12mm) TQFP package. Both devices are specified over the -40°C to +85°C extended temperature range.

Applications

Industrial Battery Backup Systems

Telecom Battery Backup Systems

Energy Storage Packs

e-Transportation Energy Packs

Benefits and Features

- **High Accuracy**
  - **±0.5mV (max) Cell Voltage Error**
  - **Simultaneous Cell Voltage Sampling**
  - **Self-Calibration**
- **Integrated Diagnostics**
  - **Open-Wire and Short Fault Detection**
  - **Undervoltage/Overvoltage Warning**
  - **Thermal Shutdown**
- **High Flexibility**
  - **SPI Interface**
  - **12-Cell and 16-Cell Versions**
  - **+6V Minimum (3 Cells) Operation**
  - **+0.5V to +4.5V Cell Voltage Range**
  - **Integrated Cell-Balancing FET Drivers**
  - **Integrated 5V LDO**
- **Low Power**
  - **1µA Shutdown Mode**
  - **1µA/10µA Cell Current Draw**

Ordering Information appears at end of data sheet.

Functional Diagram appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6496; Rev 3; 3/15

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to AGND.)

V_P .....-0.3V to +70V
LDOIN ..... (V_A - 0.3V) to (V_P + 0.3V)
V_A .....-0.3V to +6V
V_L .....-0.3V to +5.5V
CV0, DGND.....-0.3V to +0.3V
SCLK, SDI, $\overline{CS}$, EN.....-0.3V to +6V
SDO, SAMPL..... -0.3V to (V_L + 0.3V)
CV1.....-0.3V to +6V
CV2–CV12 .....($V_{CV(n^* - 1)}$ - 0.3V) to (V_P + 0.3V)
CT1–CT12..... -0.3V to (V_{CV1}–V_{CV12} + 0.3V)
CB2–CB12.....-0.3V to ($V_{CV(n^* - 1)}$ + 0.3V)
CV2–CV16
(MAX14921 only).....($V_{CV(m^{**} - 1)}$ - 0.3V) to (V_P + 0.3V)
CT1–CT16
(MAX14921 only).....-0.3V to (V_{CV1}–V_{CV16} + 0.3V)
CB2–CB16
(MAX14921 only).....-0.3V to ($V_{CV(m^{**} - 1)}$ + 0.3V)
BA1..... -0.3V to (V_{CV1} + 0.3V)
BA2–BA12 .....($V_{CV(n^* - 1)}$ - 0.3V) to min((V_{CVn^*} + 0.3V) or +6V)
BA2–BA16 (MAX14921 only) .....($V_{CV(m^{**} - 1)}$ - 0.3V) to min (($V_{CVm^{**}}$ + 0.3V) or +6V)
AOUT, T1, T2, T3 .....-0.3V to (V_A + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
64-Pin TQFP-EP (derate 31.3mW/°C above +70°C)...2508mW
80-Pin TQFP (derate 23.3mW/°C above +70°C) 1860mW
Operating Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C
n = 2–12
***m = 2–16*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA})
64-Pin TQFP-EP.....31.9°C/W
80-Pin TQFP .....43°C/W

Junction-to-Case Thermal Resistance (θ_{JC})
64-Pin TQFP-EP.....1°C/W
80-Pin TQFP .....8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

(V_P = +65V, DGND = AGND, V_L = V_{EN} = +3.3V, V_A = +5V, C_{SAMPLE} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_P Supply Voltage	V_P		+6		+65	V
V_P Supply Current	I_{P_OFF}	EN = low or LOPW = 1			1	µA
	I_{P_ON}	EN = high		65	150	
LDOIN Supply Voltage	V_{LDOIN}		+6		+65	V
LDOIN Supply Current	I_{LDOIN_OFF}	EN = low, I_A = 0A		75	125	µA
	I_{LDOIN_ON}	EN = high, I_A = 0A		350	500	
V_A Analog Supply Voltage	V_A	V_A supply externally, V_A = V_{LDOIN}	+4.75	+5	+5.25	V
V_A Analog Supply Current	I_{A_OFF}	EN = low, V_A = V_{LDOIN}		50	75	µA
	I_{A_ON}	EN = high, V_A = V_{LDOIN}		350	450	
V_L Supply Voltage	V_L		+1.62		+5.5	V
V_L Supply Current	I_L	All logic inputs static, held at logic-low or logic-high		2.5	5	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_P = +65V, DGND = AGND, V_L = V_{EN} = +3.3V, V_A = +5V, C_{SAMPLE} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_P UVLO	UV_V_{PVTH}	V_P rising			+6	V
UVLO Hysteresis	UV_V_{PHYST}			200		mV
LDOIN UVLO	UV_LDOIN_{VT}	V_{LDOIN} rising	+5.25		+6	V
V_A UVLO	UV_V_{AVTH}	V_A rising			+4.7	V
V_L UVLO	UV_V_{LVTH}	V_L rising			+1.6	V
LDO Output Voltage	$V_{A_LDO_OUT}$	$0 < I_{LOAD} < 10mA$	+4.75	+5	+5.25	V
ANALOG INPUTS (T1, T2, T3)						
Input Signal Range	V_T	Reference to AGND	0		V_A	V
On-Resistance	R_{ONA}				200	Ω
Input Leakage Current	I_{T_LEAK}	T_ route to buffer amplifier	-1		+1	µA
		T_ route to AOUT	-1		+1	
CAPACITOR INPUTS (CT_)						
Capacitor Discharge Current	$I_{LT_}$	Hold phase, SAMPL = low	-1		+1	µA
ANALOG INPUTS (CV_)						
Differential Input Signal Range for Guaranteed Accuracy	V_{Dn}	$V_{CVn} - V_{CVn-1}$ (Note 3)	+0.5		+4.5	V
CV1 Input Voltage Range	V_{CV1}		0		+5	V
CV2–CV12 Input Voltage Range (MAX14920)	V_{CVn}	$n \geq 2$, $V_{CVn} \geq V_{CVn-1}$ (Note 3)	+1.5		+65	V
CV2–CV16 Input Voltage Range (MAX14921)	V_{CVm}	$m \geq 2$, $V_{CVm} \geq V_{CVm-1}$ (Note 3)	+1.5		+65	V
Input Leakage Current	$I_{LS_}$	During sampling phase	-1		+1	µA
	$I_{LH_}$	During holding phase	-1		+10	
	$I_{LC_}$	During calibration	-1		+10	
	$I_{LD_}$	During diagnostics, DIAG = 1		10		
Balancing Input Current	$I_{LB_}$	BA_ active, $V_{CVn} - V_{CVn-1}$ = +4.5V (Note 3)		6.5	12	mA
Sample Switch On-Resistance	R_{SAMPLE}	V_{CVn} > +2V, I_{SINK} = 2mA (Note 3)		80	150	Ω
		V_{CVn} > +1.5V, I_{SINK} = 1mA (Note 3)		90		
	R_{SWCAL}	V_{CVn} > +2V, I_{SINK} = 2mA (Note 3) during charge injection error calibration		800	16,000	
Cell Undervoltage Threshold	UV_V_{CVTH}	An undervoltage sets the associated SPI Cn bit	+1.4	+1.5	+1.6	V
Cell Overvoltage Threshold	OV_V_{CVTH}	An overvoltage sets the associated SPI Cn bit		V_A		V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_P = +65V, DGND = AGND, V_L = V_{EN} = +3.3V, V_A = +5V, C_{SAMPLE} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG OUTPUT (AOUT)							
Output Signal Range	V_{AOUT}	Reference to AGND		+0.3		V_A - 0.3	V
Amplifier Offset Voltage	V_{OFFSET}	V_{AOUT} = +3.3V, after self-calibration (Note 5)			±50	±100	µV
Temperature Offset Drift		If not recalibrated			±1.5		µV/°C
Gain	A_V	Gain = V_{AOUT}/V_D			1		V/V
Output Error	V_{O_ERR}	(Note 4)		-0.5		+0.5	mV
Amplifier Gain Error	V_{GAIN_ERR}	R_{OUT} = 100kΩ, V_D = 2V to 4.5V (Note 6)		-0.2		+0.2	mV
V_P Monitor Voltage	V_{PMON}	[SC0, SC1, SC2, SC3] = [0, 0, 1, 1]	MAX14920		V_P/12		V
			MAX14921		V_P/16		
V_P Monitor Accuracy	V_{PMONA}	[SC0, SC1, SC2, SC3] = [0, 0, 1, 1]		-0.25	0	+2.5	%
CHARGE-BALANCE DRIVERS (BA_)							
Output Low	V_{BAL}	$I_{BA_}$ = 30µA, $V_{CV(n)}$ - $V_{CV(n-1)}$ = +3.3V (Note 3)		$V_{CV(n-1)}$		$V_{CV(n-1)}$ + 0.9	V
Output High	V_{BAH}	$I_{BA_}$ = -30µA, $V_{CV(n)}$ - $V_{CV(n-1)}$ = +3.3V (Note 3)		$V_{CV(n)}$ - 1.5		$V_{CV(n)}$	V
Pulldown Resistance	R_{PDWN}			10.5	14.8	21.5	kΩ
LOGIC OUTPUT (SDO)							
Output Low Voltage	V_{OL}	I_{SINK} = 10mA				+0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA		V_L - 0.25			V
Output Leakage Current	I_L	$V_{\overline{CS}}$ = V_L		-1		+1	µA
LOGIC INPUTS (SDI, SCLK, EN, SAMPL)							
Input Low Voltage	V_{IL}	V_L < +2.3V				0.2 x V_L	V
		+2.3V < V_L < +5.5V				0.3 x V_L	
Input High Voltage	V_{HL}	V_L < +2.3V		0.8 x V_L			V
		+2.3V < V_L < +5.5V		0.7 x V_L			
Input Leakage Current	I_L			-1		+1	µA
DYNAMIC CHARACTERISTICS							
AOUT Settling Time	t_{SET}	Measured between channels with +4V signal change. Settling to ±1mV accuracy, C_{LOAD} = 100pF (Figure 1)			5		µs
Sampling Time	t_{SAMPL}	C_{SAMPLE} = 1µF, during charge injection error calibration		40			ms
Holding Delay Time	t_{HD}	Delay from $\overline{SMPLB}$ set to 1 or SAMPL falling edge to holding of all cell voltages			0.5		µs

DC ELECTRICAL CHARACTERISTICS (continued)

(V_P = +65V, DGND = AGND, V_L = V_{EN} = +3.3V, V_A = +5V, C_{SAMPLE} = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Level-Shifting Delay Time	t_{LS_DELAY}	Delay from $\overline{SMPLB}$ set to 1 or SAMPL falling edge to shifting of all cell voltages to ground and available for reading		25	50	µs
AOUT Voltage-Droop Time	t_{DROOP}	Droop to -1mV (Figure 2)	1			ms
T_ Settling Time	t_{TS}	Measured between T_ input selection and AOUT settling to +1mV accuracy, C_{LOAD} = 100pF, SC2 = 1		5		µs
T_ Turn-On Delay Time	t_{TD}				0.2	µs
V_P Settling Time	t_{VPS}	Measured between V_P/12 (MAX14920), V_P/16 (MAX14921) input selection and AOUT, settling to 2.5%, C_{LOAD} = 100pF, SC3 = 1		25	60	µs
Self-Calibration Time					8	ms
THERMAL DETECTION						
Thermal Shutdown				+140		°C
Thermal-Shutdown Hysteresis				15		°C
SPI TIMINGS (Figure 3)						
SDI to SCLK Setup	t_{DS}		50			ns
SDI to SCLK Hold	t_{DH}				12	ns
SCLK to SDO Valid	t_{DO}				100	ns
$\overline{CS}$ Fall to SDO Enable	t_{DV}				100	ns
$\overline{CS}$ Rise to SDO Disable	t_{TR}				80	ns
$\overline{CS}$ Pulse Width	t_{CSW}		50			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CSH}				0	ns
SCLK High Pulse Width	t_{CH}		65			ns
SCLK Low Pulse Width	t_{CL}		65			ns
SCLK Period	t_{CP}		208			ns

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 3: Where n = 1–12 (MAX14920) and n = 1–16 (MAX14921).

Note 4: Output error V_{O_ERR} is the difference between the input cell difference voltage (V_D = $V_{CV(n)}$ - $V_{CV(n - 1)}$) and the output voltage V_{AOUT}. Where n = 1–12 (MAX14920) and n = 1–16 (MAX14921). Output error depends on buffer amplifier errors and parasitic capacitance charge injection error. Since parasitic capacitance error is PCB dependent, output error is guaranteed by design for a sampling capacitor of 1µF and parasitic capacitance less than 2.5pF on CTn (see the *Measurement Accuracy* section for a detailed explanation).

Note 5: Buffer amplifier self-calibrates its offset at power-up and every time it is requested. Due to possible thermal drift after power-up phase, it is suggested to run self-calibration on a regular basis to get best performance (see the *Buffer Amplifier Offset Calibration* section for a detailed explanation).

Note 6: Amplifier error is the sum of all errors including amplifier offset and gain error.

Timing Diagrams

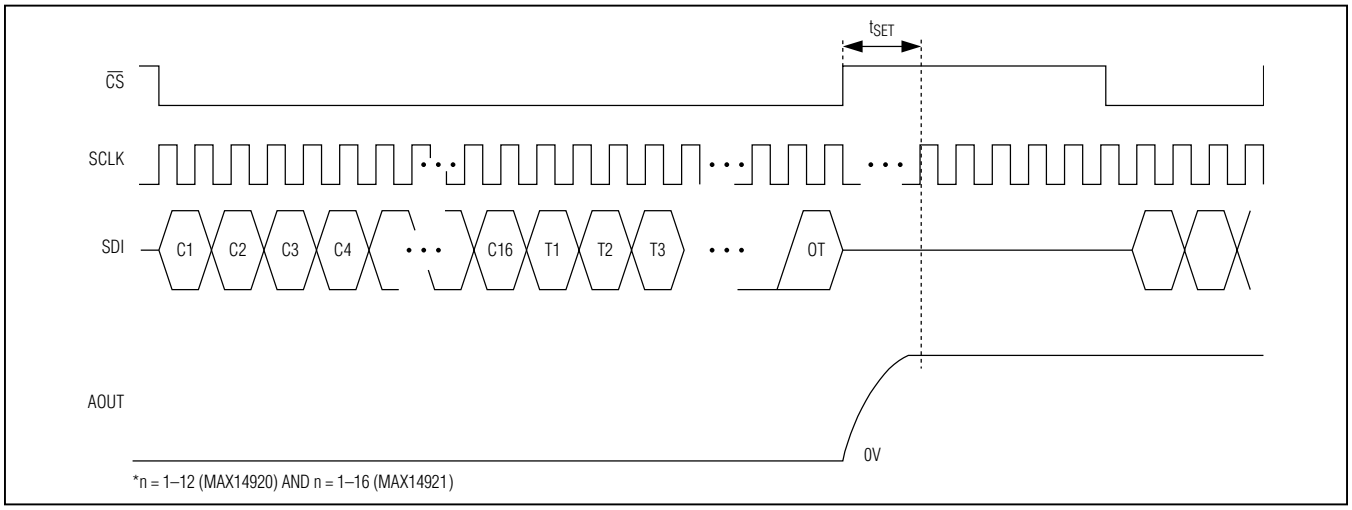


Figure 1. AOUT Delay from SPI Select

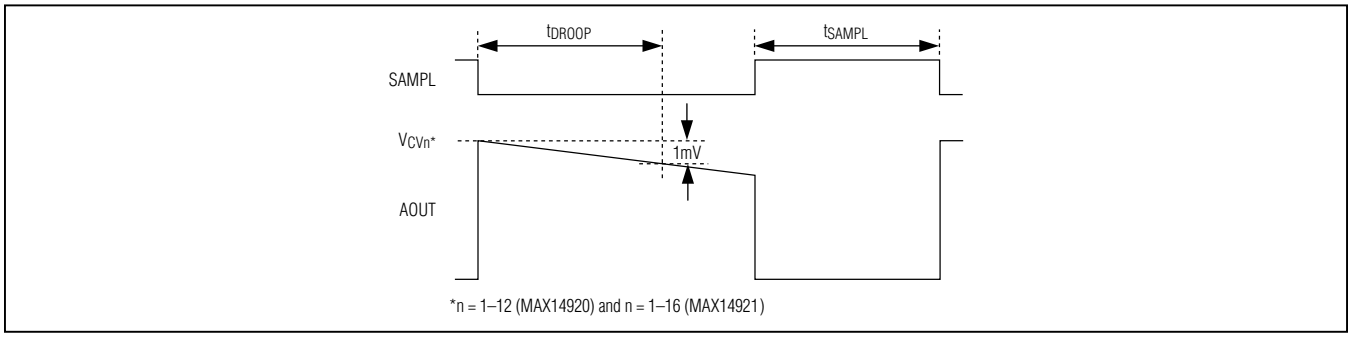


Figure 2. AOUT Voltage-Droop Time

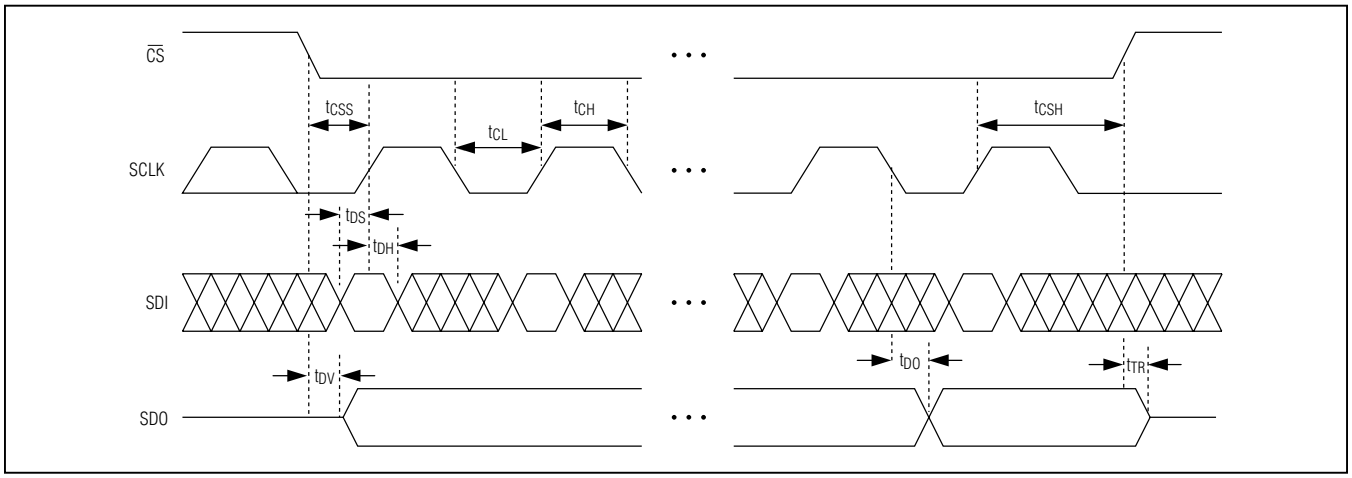
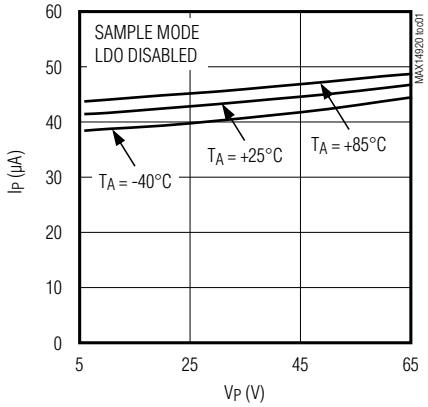


Figure 3. SPI Timing

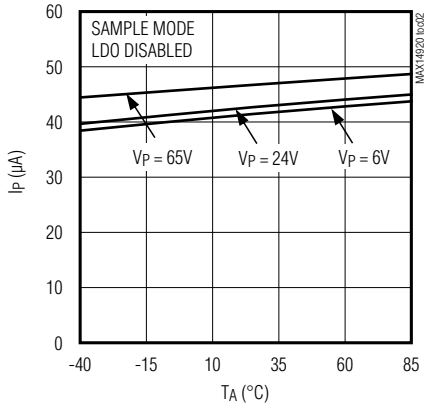
Typical Operating Characteristics

(V_{CVn} - $V_{CV(n-1)}$ = +3.3V (where n = 1–12 (MAX14920) and n = 1–16 (MAX14921)), T_A = +25°C, unless otherwise noted.)

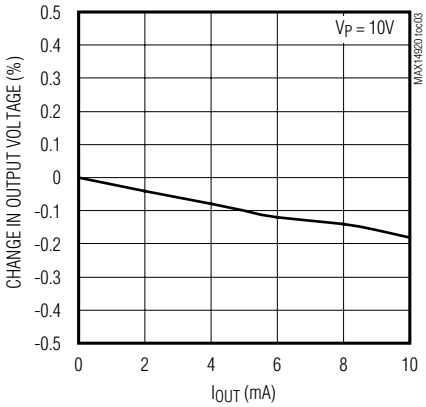
I_P vs. V_P



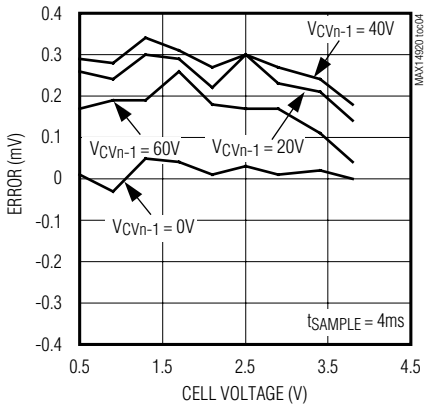
I_P vs. TEMPERATURE



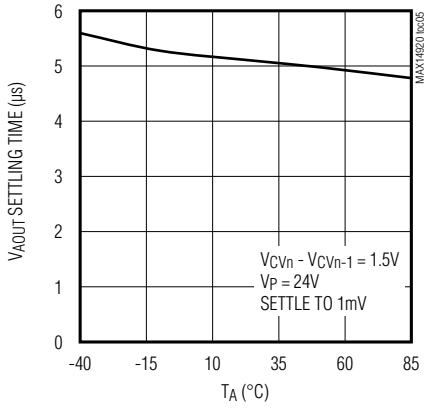
LDO OUTPUT VOLTAGE CHANGE vs. LOAD CURRENT



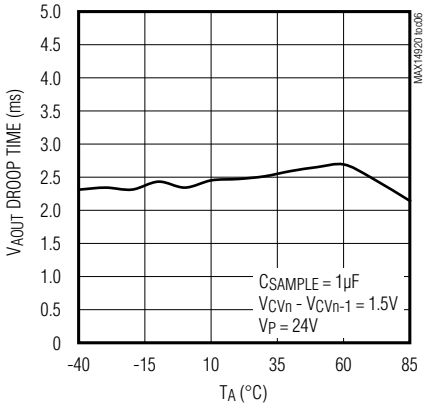
VOLTAGE ERROR vs. CELL VOLTAGE



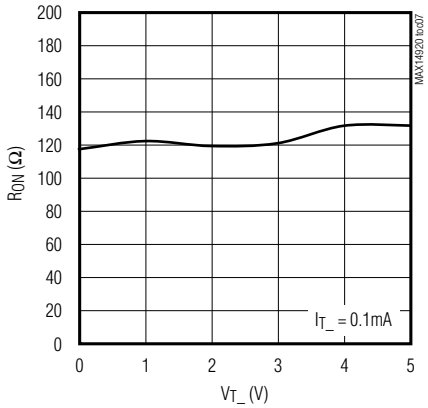
V_{AOUT} SETTLING TIME vs. TEMPERATURE



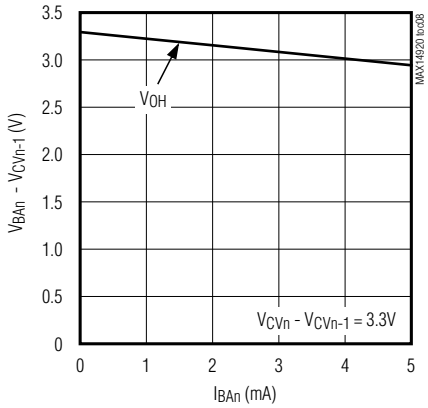
V_{AOUT} DROOP TIME vs. TEMPERATURE



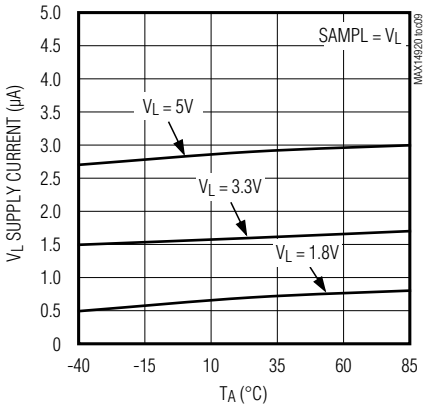
T_ ON-RESISTANCE vs. $V_{T_}$



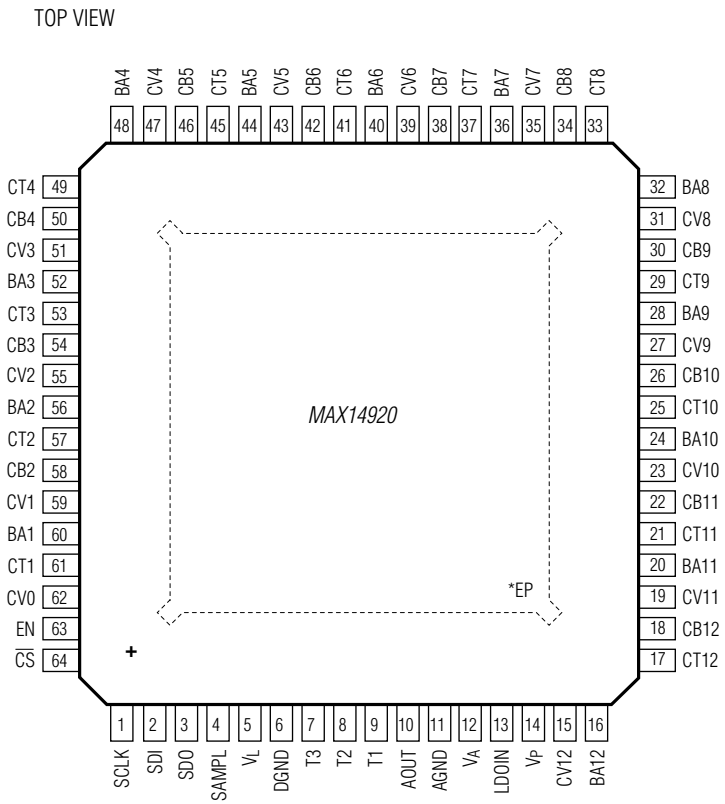
V_{BAn} - V_{CVn-1} vs. I_{BAn}



V_L SUPPLY CURRENT vs. TEMPERATURE



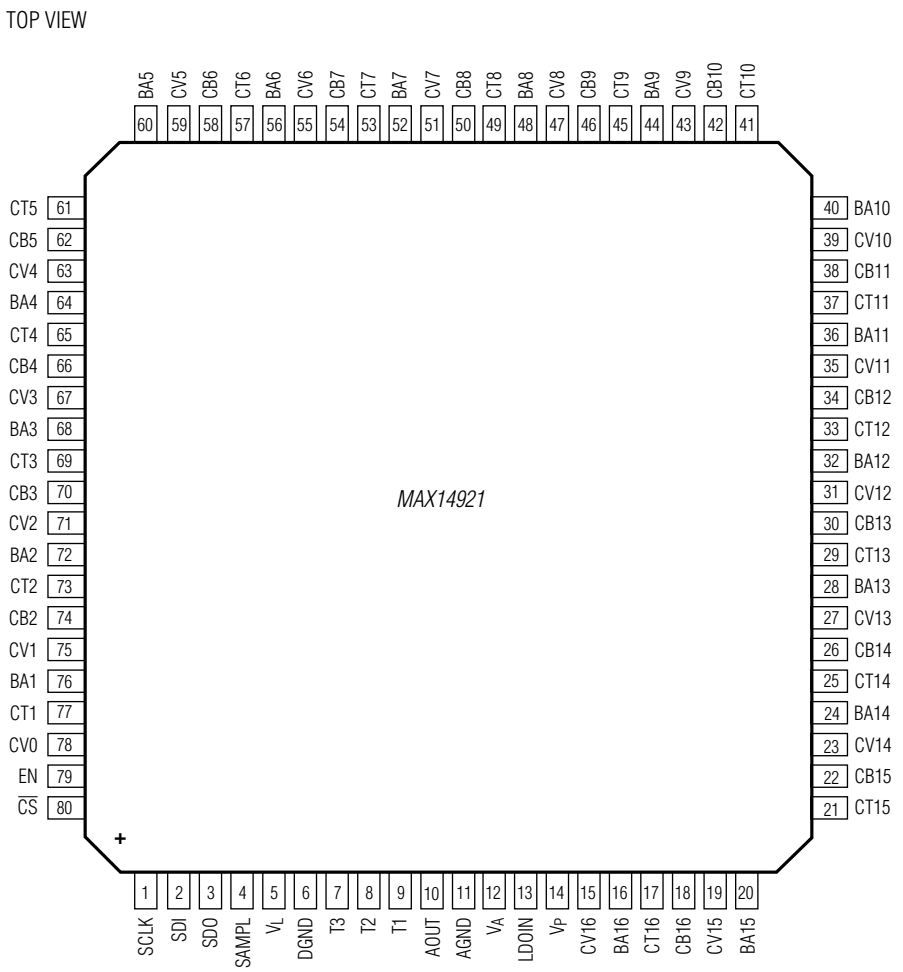
Pin Configurations



64 TQFP-EP
(10mm x 10mm)

*CONNECT EP TO GND

Pin Configurations (continued)



80 TQFP
(12mm x 12mm)

Pin Description

PIN		NAME	FUNCTION
MAX14920 (64 TQFP-EP)	MAX14921 (80 TQFP)		
1	1	SCLK	SPI Clock Input
2	2	SDI	SPI Data Line Input
3	3	SDO	SPI Data Line Output
4	4	SAMPL	Sample Control Input. Voltages at CV_ inputs are tracked when SAMPL is logic-high. When SAMPL transitions from high to low, the differential voltages on CV_ are held internally and made ready for readout at the AOUT output.
5	5	V_L	Logic Supply Input. Bypass V_L to DGND with a 0.1µF capacitor as close as possible to the device.
6	6	DGND	Digital Ground
7	7	T3	Single-Ended Voltage Input. T3 can be connected to a temperature sensor or other analog voltage.
8	8	T2	Single-Ended Voltage Input. T2 can be connected to a temperature sensor or other analog voltage.
9	9	T1	Single-Ended Voltage Input. T1 can be connected to a temperature sensor or other analog voltage.
10	10	AOUT	Buffered Amplifier Output. The AOUT output voltage is relative to CV0.
11	11	AGND	Analog Ground. AGND is a low-noise ground. Connect CV0 to AGND. Connect DGND to AGND.
12	12	V_A	+5V LDO Output. Bypass V_A to AGND with a 1µF capacitor as close as possible to the device.
13	13	LDOIN	+5V LDO Power Supply. Connect LDOIN to V_P to enable the LDO. Connect LDOIN to V_A to disable the LDO and use an external +5V supply.
14	14	V_P	Power Supply. Connect to the highest voltage of the battery cell stack. Bypass V_P to AGND with a 0.1µF capacitor as close as possible to the device.
15	31	CV12	Cell Voltage Input 12. Connect CV12 to cell anode/cathode. Connect CV12 to the highest voltage of the battery cell stack if not used.
16	32	BA12	Cell-Balancing Gate Driver Output 12. Connect BA12 to the gate of the external n-channel FET. Leave BA12 unconnected if not used.
17	33	CT12	Sampling Capacitor 12 High Terminal. CT12 internally connects to CV12 when SAMPL is logic-high. Connect a 1µF capacitor between CT12 and CB12. Leave CT12 unconnected if not used.
18	34	CB12	Sampling Capacitor 12 Low Terminal. CB12 internally connects to CV11 when SAMPL is logic-high. Connect a 1µF capacitor between CT12 and CB12. Leave CB12 unconnected if not used.
19	35	CV11	Cell Voltage Input 11. Connect CV11 to cell anode/cathode. Connect CV12 to the highest voltage of the battery cell stack if not used.
20	36	BA11	Cell-Balancing Gate Driver Output 11. Connect BA11 to the gate of the external n-channel FET. Leave BA11 unconnected if not used.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX14920 (64 TQFP-EP)	MAX14921 (80 TQFP)		
21	37	CT11	Sampling Capacitor 11 High Terminal. CT11 internally connects to CV11 when SAMPL is logic-high. Connect a 1µF capacitor between CT11 and CB11. Leave CT11 unconnected if not used.
22	38	CB11	Sampling Capacitor 11 Low Terminal. CB11 internally connects to CV10 when SAMPL is logic-high. Connect a 1µF capacitor between CT11 and CB11. Leave CB11 unconnected if not used.
23	39	CV10	Cell Voltage Input 10. Connect CV10 to cell anode/cathode. Connect CV10 to the highest voltage of the battery cell stack if not used.
24	40	BA10	Cell-Balancing Gate Driver Output 10. Connect BA10 to the gate of the external n-channel FET. Leave BA10 unconnected if not used.
25	41	CT10	Sampling Capacitor 10 High Terminal. CT10 internally connects to CV10 when SAMPL is logic-high. Connect a 1µF capacitor between CT10 and CB10. Leave CT10 unconnected if not used.
26	42	CB10	Sampling Capacitor 10 Low Terminal. CB10 internally connects to CV9 when SAMPL is logic-high. Connect a 1µF capacitor between CT10 and CB10. Leave CB10 unconnected if not used.
27	43	CV9	Cell Voltage Input 9. Connect CV9 to cell anode/cathode. Connect CV9 to the highest voltage of the battery cell stack if not used.
28	44	BA9	Cell-Balancing Gate Driver Output 9. Connect BA9 to the gate of the external n-channel FET. Leave BA9 unconnected if not used.
29	45	CT9	Sampling Capacitor 9 High Terminal. CT9 internally connects to CV9 when SAMPL is logic-high. Connect a 1µF capacitor between CT9 and CB9. Leave CT9 unconnected if not used.
30	46	CB9	Sampling Capacitor 9 Low Terminal. CB9 internally connects to CV8 when SAMPL is logic-high. Connect a 1µF capacitor between CT9 and CB9. Leave CB9 unconnected if not used.
31	47	CV8	Cell Voltage Input 8. Connect CV8 to cell anode/cathode. Connect CV8 to the highest voltage of the battery cell stack if not used.
32	48	BA8	Cell-Balancing Gate Driver Output 8. Connect BA8 to the gate of the external n-channel FET. Leave BA8 unconnected if not used.
33	49	CT8	Sampling Capacitor 8 High Terminal. CT8 internally connects to CV8 when SAMPL is logic-high. Connect a 1µF capacitor between CT8 and CB8. Leave CT8 unconnected if not used.
34	50	CB8	Sampling Capacitor 8 Low Terminal. CB8 internally connects to CV7 when SAMPL is logic-high. Connect a 1µF capacitor between CT8 and CB8. Leave CB8 unconnected if not used.
35	51	CV7	Cell Voltage Input 7. Connect CV7 to cell anode/cathode. Connect CV7 to the highest voltage of the battery cell stack if not used.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX14920 (64 TQFP-EP)	MAX14921 (80 TQFP)		
36	52	BA7	Cell-Balancing Gate Driver Output 7. Connect BA7 to the gate of the external n-channel FET. Leave BA7 unconnected if not used.
37	53	CT7	Sampling Capacitor 7 High Terminal. CT7 internally connects to CV7 when SAMPL is logic-high. Connect a 1µF capacitor between CT7 and CB7. Leave CT7 unconnected if not used.
38	54	CB7	Sampling Capacitor 7 Low Terminal. CB7 internally connects to CV6 when SAMPL is logic-high. Connect a 1µF capacitor between CT7 and CB7. Leave CB7 unconnected if not used.
39	55	CV6	Cell Voltage Input 6. Connect CV6 to cell anode/cathode. Connect CV6 to the highest voltage of the battery cell stack if not used.
40	56	BA6	Cell-Balancing Gate Driver Output 6. Connect BA6 to the gate of the external n-channel FET. Leave BA6 unconnected if not used.
41	57	CT6	Sampling Capacitor 6 High Terminal. CT6 internally connects to CV6 when SAMPL is logic-high. Connect a 1µF capacitor between CT6 and CB6. Leave CT6 unconnected if not used.
42	58	CB6	Sampling Capacitor 6 Low Terminal. CB6 internally connects to CV7 when SAMPL is logic-high. Connect a 1µF capacitor between CT6 and CB6. Leave CB6 unconnected if not used.
43	59	CV5	Cell Voltage Input 5. Connect CV5 to cell anode/cathode. Connect CV5 to the highest voltage of the battery cell stack if not used.
44	60	BA5	Cell-Balancing Gate Driver Output 5. Connect BA5 to the gate of the external n-channel FET. Leave BA5 unconnected if not used.
45	61	CT5	Sampling Capacitor 5 High Terminal. CT5 internally connects to CV5 when SAMPL is logic-high. Connect a 1µF capacitor between CT5 and CB5. Leave CT5 unconnected if not used.
46	62	CB5	Sampling Capacitor 5 Low Terminal. CB5 internally connects to CV4 when SAMPL is logic-high. Connect a 1µF capacitor between CT5 and CB5. Leave CB5 unconnected if not used.
47	63	CV4	Cell Voltage Input 4. Connect CV4 to cell anode/cathode. Connect CV4 to the highest voltage of the battery cell stack if not used.
48	64	BA4	Cell-Balancing Gate Driver Output 4. Connect BA4 to the gate of the external n-channel FET. Leave BA4 unconnected if not used.
49	65	CT4	Sampling Capacitor 4 High Terminal. CT4 internally connects to CV4 when SAMPL is logic-high. Connect a 1µF capacitor between CT4 and CB4. Leave CT4 unconnected if not used.
50	66	CB4	Sampling Capacitor 4 Low Terminal. CB4 internally connects to CV3 when SAMPL is logic-high. Connect a 1µF capacitor between CT4 and CB4. Leave CB4 unconnected if not used.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX14920 (64 TQFP-EP)	MAX14921 (80 TQFP)		
51	67	CV3	Cell Voltage Input 3. Connect CV3 to cell anode/cathode. Connect CV3 to the highest voltage of the battery cell stack if not used.
52	68	BA3	Cell-Balancing Gate Driver Output 3. Connect BA3 to the gate of the external n-channel FET. Leave BA3 unconnected if not used.
53	69	CT3	Sampling Capacitor 3 High Terminal. CT3 internally connects to CV3 when SAMPL is logic-high. Connect a 1µF capacitor between CT3 and CB3. Leave CT3 unconnected if not used.
54	70	CB3	Sampling Capacitor 3 Low Terminal. CB3 internally connects to CV2 when SAMPL is logic-high. Connect a 1µF capacitor between CT3 and CB3. Leave CB3 unconnected if not used.
55	71	CV2	Cell Voltage Input 2. Connect CV2 to cell anode/cathode. Connect CV2 to the highest voltage of the battery cell stack if not used.
56	72	BA2	Cell-Balancing Gate Driver Output 2. Connect BA2 to the gate of the external n-channel FET. Leave BA2 unconnected if not used.
57	73	CT2	Sampling Capacitor 2 High Terminal. CT2 internally connects to CV2 when SAMPL is logic-high. Connect a 1µF capacitor between CT2 and CB2. Leave CT2 unconnected if not used.
58	74	CB2	Sampling Capacitor 2 Low Terminal. CB2 internally connects to CV1 when SAMPL is logic-high. Connect a 1µF capacitor between CT2 and CB2. Leave CB2 unconnected if not used.
59	75	CV1	Cell Voltage Input 1. Connect CV1 to cell anode/cathode.
60	76	BA1	Cell-Balancing Gate Driver Output 1. Connect BA1 to the gate of the external n-channel FET. Leave BA1 unconnected if not used.
61	77	CT1	Sampling Capacitor Connection 1 High Terminal. CT1 internally connects to CV1 when SAMPL is logic-high. Connect a 1µF capacitor between CT1 and CV0. Leave CT1 unconnected if not used.
62	78	CV0	Cell Voltage Input 0. Connect CV0 to AGND.
63	79	EN	Enable Input. Drive EN low to put the device into shutdown mode and reset the SPI registers. The +5V LDO remains active in the shutdown mode. Drive EN high for normal operation.
64	80	$\overline{CS}$	SPI Chip-Select Input. Active low.
—	15	CV16	Cell Voltage Input 16. Connect CV16 to cell anode/cathode. Connect CV16 to the highest voltage of the battery cell stack if not used.
—	16	BA16	Cell-Balancing Gate Driver Output 16. Connect BA16 to the gate of the external n-channel FET. Leave BA16 unconnected if not used.
—	17	CT16	Sampling Capacitor Connection 16 High Terminal. CT16 internally connects to CV16 when SAMPL is logic-high. Connect a1µF capacitor between CT16 and CB16. Leave CT16 unconnected if not used.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX14920 (64 TQFP-EP)	MAX14921 (80 TQFP)		
—	18	CB16	Sampling Capacitor Connection 16 Low Terminal. CB16 internally connects to CV15 when SAMPL is logic-high. Connect a 1µF capacitor between CT16 and CB16. Leave CB16 unconnected if not used.
—	19	CV15	Cell Voltage Input 15. Connect CV15 to cell anode/cathode. Connect CV15 to the highest voltage of the battery cell stack if not used.
—	20	BA15	Cell-Balancing Gate Driver Output 15. Connect BA15 to the gate of the external n-channel FET. Leave BA15 unconnected if not used.
—	21	CT15	Sampling Capacitor Connection 15 High Terminal. CT15 internally connects to CV15 when SAMPL is logic-high. Connect a 1µF capacitor between CT15 and CB15. Leave CT15 unconnected if not used.
—	22	CB15	Sampling Capacitor Connection 15 Low Terminal. CB15 internally connects to CV14 when SAMPL is logic-high. Connect a 1µF capacitor between CT15 and CB15. Leave CB15 unconnected if not used.
—	23	CV14	Cell Voltage Input 14. Connect CV14 to cell anode/cathode. Connect CV14 to the highest voltage of the battery cell stack if not used.
—	24	BA14	Cell-Balancing Gate Driver Output 14. Connect BA14 to the gate of the external n-channel FET. Leave BA14 unconnected if not used.
—	25	CT14	Sampling Capacitor Connection 14 High Terminal. CT14 internally connects to CV14 when SAMPL is logic-high. Connect a 1µF capacitor between CT14 and CB14. Leave CT14 unconnected if not used.
—	26	CB14	Sampling Capacitor Connection 14 Low Terminal. CB14 internally connects to CV13 when SAMPL is logic-high. Connect a 1µF capacitor between CT14 and CB14. Leave CB14 unconnected if not used.
—	27	CV13	Cell Voltage Input 13. Connect CV13 to cell anode/cathode. Connect CV13 to the highest voltage of the battery cell stack if not used.
—	28	BA13	Cell-Balancing Gate Driver Output 13. Connect BA13 to the gate of the external n-channel FET. Leave BA13 unconnected if not used.
—	29	CT13	Sampling Capacitor Connection 13 High Terminal. CT13 internally connects to CV13 when SAMPL is logic-high. Connect a 1µF capacitor between CT13 and CB13. Leave CT13 unconnected if not used.
—	30	CB13	Sampling Capacitor Connection 13 Low Terminal. CB13 internally connects to CV12 when SAMPL is logic-high. Connect a 1µF capacitor between CT13 and CB13. Leave CB13 unconnected if not used.
—	—	EP	Exposed Pad (MAX14920 Only). Connect EP to AGND.

Detailed Description

The MAX14920/MAX14921 analog front-end devices are used in multicell battery measurement systems to monitor primary/secondary battery packs up to 16 cells/+65V (max). The devices perform the signal conditioning required for enabling accurate cell voltage measurement. Both devices simultaneously sample all cell voltages, allowing accurate state-of-charge and source-resistance determination, even under transient load current conditions. The cell voltage measurements are shifted down to ground reference with unity gain, simplifying external ADC data conversion. The devices enable passive cell balancing through drivers that control external discharge FETs.

A high-accuracy, low-offset amplifier buffers differential voltages up to +5V for monitoring of the common rechargeable cell technologies such as lithium-ion (Li+). The resulting cell measurement errors from the devices are below ±0.5mV (max). The devices' high accuracy make them ideal for monitoring cell chemistries with very flat discharge curves, such as a lithium-metal phosphate cell. Diagnostics detect open-wire and short conditions, and warn about overvoltage/undervoltage.

The SPI interface is used for control and monitoring through a host controller. The SPI interface is daisy-chainable. Both devices can operate with a minimum of +6V total stack voltage (typically equating to 3 cells).

Voltage Sampling

The voltages of all cells are tracked by the sampling capacitors connected between the CTn and CBn pins (where n = 1–12 (MAX14920) and n = 1–16 (MAX14921)), while the $\overline{SMPLB}$ bit is set to 0 and the SAMPL input is driven high (Figure 4). When the $\overline{SMPLB}$ bit is set to 1, and the SAMPL input transitions low, all cell voltages are simultaneously sampled on their associated capacitors. The voltages are held by the capacitors while the $\overline{SMPLB}$ bit is 1, or the SAMPL pin is held low. When sample and holding is controlled by the SAMPL input, set the $\overline{SMPLB}$ bit to 0. When sample and hold is controlled by the $\overline{SMPLB}$ bit, keep the SAMPL input high.

In sample phase selecting any cell voltage (ECS = 1), AOUT equals $V_P/12$ (MAX14920) or $V_P/16$ (MAX14921).

In order to allow random connection of the battery cells to the BMS electronics, 3kΩ resistors must be placed in series with the CV_ inputs for protection, as shown in Figure 11. These protection resistors are not needed on CV0 and CVT, where CVT refers to CVn pins connected to the battery's top (B+) terminal. Only if the following connection sequence can be guaranteed, all of the protection resistors can be left away or their value reduced: First connect the battery pack's bottom (B-) and top (B+) terminals to the BMS electronics' AGND/CV0 and VP/CVT pins - then connect all of the remaining intermediary cell connections to the CV_ pins.

Consider the sampling switches' on-resistance of 150Ω (max) when calculating the filter and settling times. Using 3kΩ protection resistors in series with the CV_ pin together with 1µF sampling capacitors, the RC settling time from 0V to within 200µV of a possible 4.5V cell voltage is about 60ms. If shorter sampling times are required, smaller sampling capacitors can be used, but note the effect of increased charge injection errors. The sampling capacitors only discharge minimally during the hold phase, and if the battery's load is nearly static, the cell voltages will only change minimally between successive samples, resulting in much reduced settling times. In the holding phase, each capacitor's voltage can be independently routed to the analog AOUT output under SPI control.

Voltage Readout

When the $\overline{SMPLB}$ bit is set high, or when the SAMPL input is driven low, the sampling switches are opened after 0.5µs (typ) and the cell voltages are held on the external sampling capacitors. Within the time of t_{LS_DELAY} < 50µs (max), the capacitors' voltages are all shifted to ground reference. Then the undervoltage/overvoltage monitoring of all cells is valid and the cell voltage is available for sequential readout under SPI control. The SPI control can select the readout of any cell voltages, in any order (Figure 5).

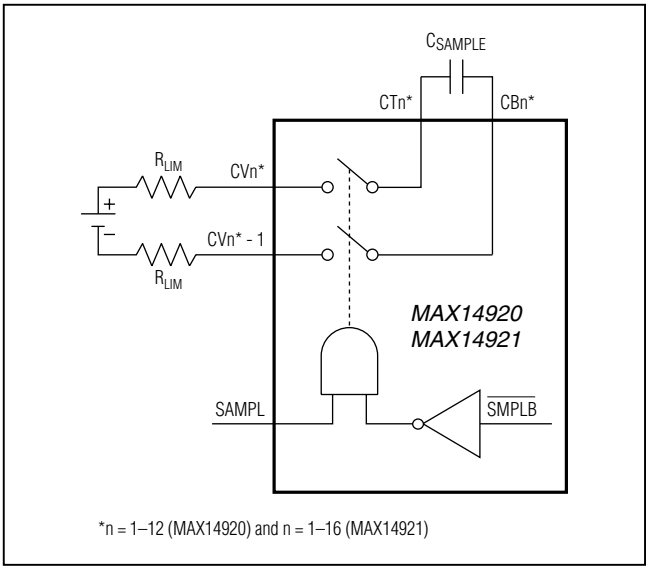


Figure 4. Voltage Sampling

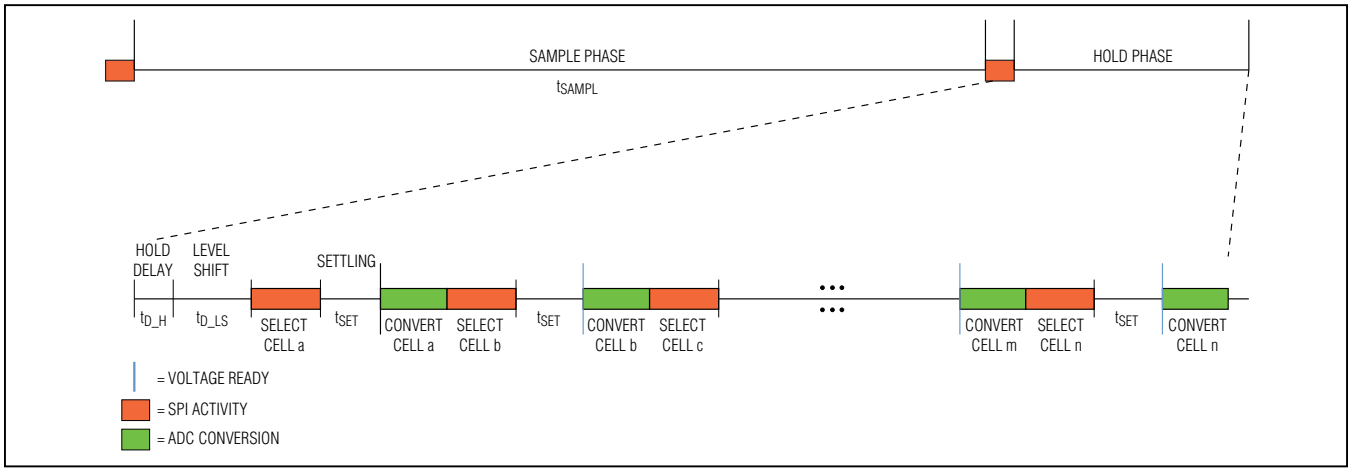


Figure 5. SPI Control Cells Voltage Readout

With the ECS bit set to 1, a selected cell's voltage appears at the AOUT output according to the cell selection (as defined by the SC_ cell select bits). A low-leakage, low-noise, low-offset amplifier buffers the capacitor charge and provides the high-accuracy AOUT analog output. After a settling time of t_{SET}, from the rising edge of the $\overline{CS}$ signal, the voltage is available at AOUT with specified accuracy. An ADC can then sample and convert the AOUT voltage. The AOUT output voltage droops over time due to capacitor discharge. The droop time for 1mV of change is larger than t_{DROOP} (> C_{SAMPLE}/I_{CT_LEAK}).

Measurement Accuracy

The accuracy of cell-voltage measurement (i.e., the difference of the AOUT voltage relative to the cell voltages) is determined by four factors:

1) Sampling Time relative to the RC setting time
2) Held voltage droop due to leakage on the CT_ pins
3) Internal buffer amplifier's voltage errors
4) Capacitive level-shifting circuit error

The CT_ leakage (1µA, max) is a current that mainly comes from the CV_ pin and increases with temperature.

Neglecting the PCB leakage across the sampling capacitance, the voltage drift error is given by:

$$V_{ERR_LEAK} = \frac{I_{CT_LEAK}}{C_{SAMPLE}} \times t_{READOUT}$$

where:

C_{SAMPLE} is the sampling capacitance

I_{CT_LEAK} is the leakage current on the CT_ pin

$t_{READOUT}$ is the delay between hold starts and readout of the cell voltage

For example, with 1µF sampling capacitors and an ADC conversion rate > 20kHz, V_{ERR_LEAK} is less than 1mV. Cells with a higher common-mode voltage have a higher leakage. To reduce the voltage drift over time, start sequential voltage readout from the highest cell in the stack first.

The buffer amplifier errors are nondeterministic in nature, and vary from chip to chip. They are also affected by temperature. The buffer amplifier offset error can be calibrated out through an internal offset-calibration function. This calibration is automatically performed at power-up. The calibration can also be initiated under SPI control. Due to temperature drifts over time, it is best done on a regular basis. Once the buffer amplifier offset is calibrated out, the total error of the buffer is below 0.3mV. After power-up, if the devices do not calibrate regularly, a temperature offset drift of ±1.5µV/°C can occur.

The level shifting is subject to deterministic errors due to charge injection by parasitic PCB-related capacitance on the CT_ pins. The charge-injected sampling error can be calculated as follows:

$$V_{ERR_CHARGE_INJECTION} = \frac{C_{PAR}}{C_{SAMPLE}} \times V_{CVn}$$

where:

C_{PAR} is the parasitic capacitance of the CTn pin, where n = 1–12 (MAX14920) and n = 1–16 (MAX14921)

C_{SAMPLE} is the sampling capacitor

V_{CVn} is the voltage of the CTn pin with respect to AGND, where n = 1–12 (MAX14920) and n = 1–16 (MAX14921)

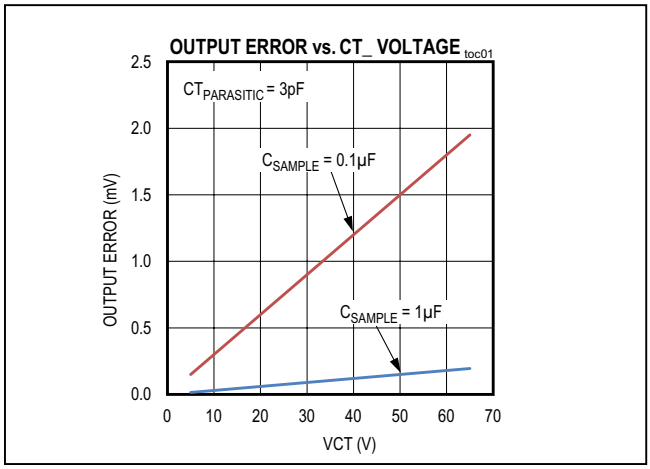


Figure 6. Charge Injection Error Voltage for 3pF Parasitic Capacitance

Figure 6 shows the charge-injected sampling error for 1pF of parasitic capacitance in worst-case conditions for a 100nF and 1µF sampling capacitor if charge injection error correction is not employed.

Minimizing the parasitic capacitance on the CT_ pins to a few picofarads, with a sampling capacitor of 1µF, is enough to achieve output error below 1mV target.

Alternatively, if a sampling capacitor lower than 1µF or a parasitic capacitance of more than 15pF are present, these errors can be calibrated out to achieve a < 1mV accuracy level through a calibration procedure for each cell. These per-cell errors are simply subtracted from every cell voltage measurement (see the *Parasitic Capacitance Charge Injection Error Calibration* section).

Parasitic Capacitance Charge Injection Error Calibration

This calibration is performed with all cells connected to the CV_ terminals. Setting the [ECS, SC0, SC1, SC2, SC3] bits to [0, 0, 0, 0, 0] configures the devices for parasitic capacitance charge-injection error calibration.

During the sampling phase, every sampling capacitor's CTn and CBn terminals are shorted together by internal calibration switches (R_{SWCAL} = 800Ω typ), so that only the parasitic capacitance is charged to the cell's common-mode voltage V_{CVn}, where n = 1–12 (MAX14920) and n = 1–16 (MAX14921).

The subsequent cell voltage readout sequence then shows the value of $V_{ERR_CHARGE_INJECTION}$ for each cell at AOUT, multiplied by 128. If $V_{ERR_CHARGE_INJECTION}$ is large enough to affect the required 1mV accuracy, this calibration method provides a measurement of the parasitic capacitance on each CT_ pin so the microcontroller can use this to correct $V_{ERR_INJECTION}$ in its readings.

A simple way to correct cell voltages is to store the ADC data of each cell obtained during calibration (i.e., error values), divided by 128, and subtract these from the subsequently measured cell voltages.

Note that the charge injection errors only depend on the parasitic capacitance of the CTn pin and the common mode voltage. The parasitic capacitance is PCB layout dependent and does not change from board to board.

Buffer Amplifier Offset Calibration

On power-up, the devices automatically go through a self-calibration phase to minimize the internal buffer's offset voltage. In addition, the offset voltage can be calibrated out at any time under host control. Offset calibration is configurable by setting the [ECS, SC0, SC1, SC2, SC3] bits to [0, 1, 0, 0] and is initiated on the low to high $\overline{CS}$ transition in sampling phase. This offset-calibration procedure takes 8ms to complete. The AOUT output is high impedance during this period. No regular cell voltage measurement can be taken during this time period. However, the SPI operates normally when communicating with other devices (e.g., in daisy-chain mode). So as not to affect calibration, do not take measurement and keep the devices in sample mode (ECS = 0, SC2 = 0, $\overline{SMPLB}$ = 0). After power-up, if the devices do not calibrate regularly, a temperature offset drift of ±1.5µV/°C can occur.

Monitoring Less Than 12/16 Cells

The devices can monitor from 3 (V_P > +6V) to 12/16 cells (V_P < +65V). When monitoring less than the maximum number of possible cells per device, connect the most negative cell stack voltage to the bottom of the voltage input string (CV0). The unused CV_ inputs at the top of the string should be shorted together and connected to V_P. Leave the unused BA_, CT_ , and CB_ pins unconnected.

Reading Total Cell Stack Voltage

Besides monitoring the individual cell voltages, the devices can monitor the total voltage of the cell stack. An internal resistive voltage-divider between V_P and AGND divides the stack voltage by 12 (MAX14920) or 16 (MAX14921). This provides a way to quickly determine the state of the total battery pack, as well as the average

voltage of all cells. The settling time of AOUT is 60µs. To read out the total cell stack voltage, set the [ECS, SC0, SC1, SC2, SC3] bits to [0, 0, 0, 1, 1]. The total cell stack voltage can be read during the sample or hold phase.

SPI Serial Interface

Control of the devices is done through a 24-bit SPI interface. The controller sends the serial data to the devices through the SDI input. The devices simultaneously send out monitoring data at the SDO output. This scheme allows daisy-chained operation with other daisy-chainable devices, such as ADC converters. Figure 7 shows the serial bit sequence.

CB1 is the first bit expected from the controller and C1 is the first bit that the devices sent to the controller. The SDO data changes on the falling edge of the SCLK signals. The devices sample the SDI data on the rising edge of SCLK.

SPI Configuration/Control Bits

The configuration/control bits allow enabling of the charge-balance switches, sampling and holding of all the cell voltages, selecting the cell for voltage output, selecting the T_ input channels, and enabling diagnostics mode. Table 1 describes the bits that the devices receive from the host controller for configuration and control through SDI.

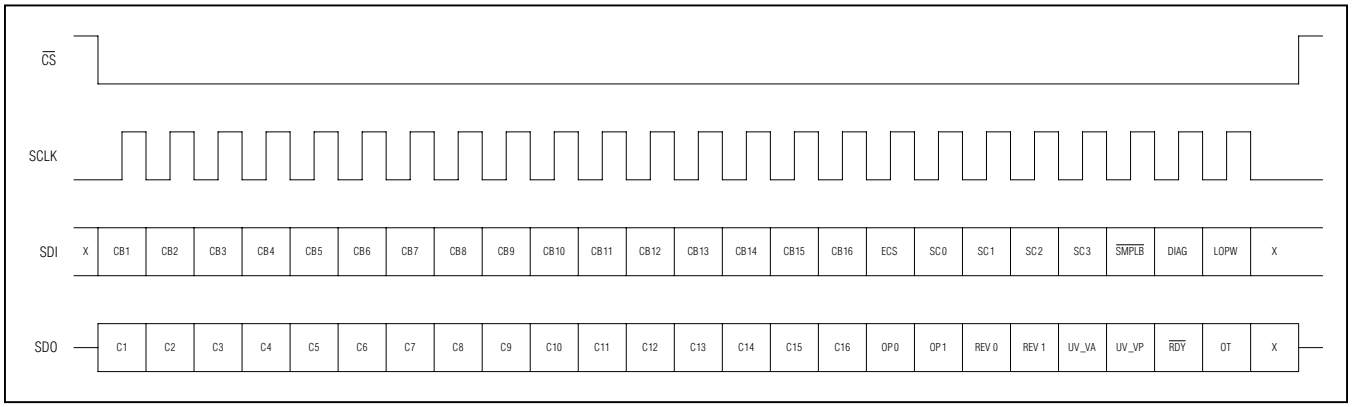


Figure 7. SPI Serial Interface Bits

Table 1. SPI Configuration/Control Bits

NAME	BITS	ACCESS	RESET	DESCRIPTION
CB1	0	W	0	0: Set BA1 output low
				1: Set BA1 output high
CB2	1	W	0	0: Set BA2 output low
				1: Set BA2 output high
CB3	2	W	0	0: Set BA3 output low
				1: Set BA3 output high
CB4	3	W	0	0: Set BA4 output low
				1: Set BA4 output high
CB5	4	W	0	0: Set BA5 output low
				1: Set BA5 output high
CB6	5	W	0	0: Set BA6 output low
				1: Set BA6 output high
CB7	6	W	0	0: Set BA7 output low
				1: Set BA7 output high
CB8	7	W	0	0: Set BA8 output low
				1: Set BA8 output high

Table 1. SPI Configuration/Control Bits (continued)

NAME	BITS	ACCESS	RESET	DESCRIPTION
CB9	8	R/W	0	0: Set BA9 output low
				1: Set BA9 output high
CB10	9	R/W	0	0: Set BA10 output low
				1: Set BA10 output high
CB11	10	R/W	0	0: Set BA11 output low
				1: Set BA11 output high
CB12*	11	R/W	0	0: Set BA12 output low
				1: Set BA12 output high
CB13*	12	R/W	0	0: Set BA13 output low
				1: Set BA13 output high
CB14*	13	R/W	0	0: Set BA14 output low
				1: Set BA14 output high
CB15*	14	R/W	0	0: Set BA15 output low
				1: Set BA15 output high
CB16*	15	R/W	0	0: Set BA16 output low
				1: Set BA16 output high
ECS	16	R/W	0	0: Cell selection is disabled
				1: Cell selection is enabled
SC0	17	R/W	0	[ECS, SC0, SC1, SC2, SC3] 1 – SC0, SC1, SC2, SC3: Selects the cell for voltage readout during hold phase.** The selected cell voltage is routed to AOUT after the rising $\overline{CS}$ edge. See Table 2. 0 – 0, 0, 0, 0: AOUT is three-stated and sampling switches are configured for parasitic capacitance error calibration. 0 – 1, 0, 0, 0: AOUT is three-stated and self-calibration of buffer amplifier offset voltage is initiated after the following rising $\overline{CS}$. 0 – SC0, SC1, 0, 1: Switches the T1, T2. T2 analog inputs directly to AOUT. See Table 3. 0 – 0, 0, 1, 1: V_P/12 (MAX14920) or V_P/16 (MAX14921) voltage is routed to AOUT on the next rising $\overline{CS}$ 0 – SC0, SC1, 1, 1: Routes and buffers the T1, T2. T3 to AOUT. See Table 3.
SC1	18	R/W	0	
SC2	19	R/W	0	
SC3	20	R/W	0	
$\overline{SMPLB}$	21	R/W	0	0: Device in sample phase if SAMPL input is logic-high
				1: Device in hold phase
DIAG	22	R/W	0	0: Normal operation
				1: Diagnostic enable, 10µA leakage is sunk on all CV_ inputs (CV0–CV16).
LOPW	23	R/W	0	0: Normal operation
				1: Low-power mode enabled. Current into LDOIN is reduced to 125µA. Current into V_P is reduced to 1µA.

**Not available on the MAX14920. Setting the bit to 0 or 1 does not affect the operating of the MAX14920.*

***For the MAX14920, if n > 12, V_{AOUT} = 0V.*

Table 2. Cell Selection

CELL	SC0	SC1	SC2	SC3
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13*	0	0	1	1
14*	1	0	1	1
15*	0	1	1	1
16*	1	1	1	1

**For MAX14921 only.*

Table 3. Analog Input Selection

T_	SC0	SC1
T1	1	0
T2	0	1
T3	1	1

SPI Monitoring Bits

The monitoring bits provide feedback of undervoltage conditions and thermal shutdown, as well as indication when the devices are ready for operation after power-up. Table 4 describes the diagnostics/monitoring bits that the devices send back to the host controller through the SDO output.

Flexible Logic Interface

The serial/parallel logic control interface logic levels can be defined to be in a range between +1.62V (min) and +5.5V (max). The voltage applied to the V_L pin defines the logic levels. Choose the V_L voltage to match the controller and ADC's I/O logic levels.

Table 4. SPI Monitoring Bits

NAME	BITS	ACCESS	DESCRIPTION
C1	0	R	1: During hold phase if cell 1 voltage is below UV_VCVTH or above VA
C2	1	R	1: During hold phase if cell 2 voltage is below UV_VCVTH or above VA
C3	2	R	1: During hold phase if cell 3 voltage is below UV_VCVTH or above VA
C4	3	R	1: During hold phase if cell 4 voltage is below UV_VCVTH or above VA
C5	4	R	1: During hold phase if cell 5 voltage is below UV_VCVTH or above VA
C6	5	R	1: During hold phase if cell 6 voltage is below UV_VCVTH or above VA
C7	6	R	1: During hold phase if cell 7 voltage is below UV_VCVTH or above VA
C8	7	R	1: During hold phase if cell 8 voltage is below UV_VCVTH or above VA
C9	8	R	1: During hold phase if cell 9 voltage is below UV_VCVTH or above VA
C10	9	R	1: During hold phase if cell 10 voltage is below UV_VCVTH or above VA
C11	10	R	1: During hold phase if cell 11 voltage is below UV_VCVTH or above VA
C12*	11	R	1: During hold phase if cell 12 voltage is below UV_VCVTH or above VA
C13*	12	R	1: During hold phase if cell 13 voltage is below UV_VCVTH or above VA
C14*	13	R	1: During hold phase if cell 14 voltage is below UV_VCVTH or above VA
C15*	14	R	1: During hold phase if cell 15 voltage is below UV_VCVTH or above VA
C16*	15	R	1: During hold phase if cell 16 voltage is below UV_VCVTH or above VA
OP0	16	R	Product identifying bits MAX14921 (OP0 = 0, OP1 = 0) MAX14920 (OP0 = 1, OP1 = 0)
OP1	17	R	
REV0	18	R	Die version MAX14920/MAX14921 version bits
REV1	19	R	
UV_VA	20	R	1: VA is below UV_VAVTH
UV_VP	21	R	1: VP is below UV_VPVTH. If LOPW = 1, VP UVLO circuit is disabled and this bit is always set to 1
$\overline{RDY}$	22	R	1: Device is not ready to operate (power-up phase or buffer amplifier is in self-calibration procedure)
OT	23	R	1: Device is in thermal shutdown

**Not available on the MAX14920. Setting the bit to 0 or 1 does not affect the operating of the MAX14920.*

Linear Regulator

The internal linear regulator has LDOIN as its input voltage and regulates this down to +5V ±5% at the V_A output with a load current of 10mA (max). The LDO is automatically enabled when LDOIN is above +5.5V. The internal LDO is short-circuit protected with a current limit higher than 14mA (22mA, typ). An external +5V regulator can be used instead of the internal one. When using an external +5V regular, LDOIN must be connected to V_A.

Thermal Protection

The devices have thermal shutdown to protect them against thermal overheating. In thermal shutdown, the LDO, amplifier, and charge-balance circuitry stop operation. The SPI interface is functional in thermal shutdown.

Shutdown Mode

The devices can be placed into low standby-power shutdown mode through the LOPW bit. The internal LDO remains on and the amplifier disabled, bringing the VP supply current down to 1µA (max).

Analog/Temperature Inputs

The T1, T2, and T3 inputs are single-ended, CV0-referenced, general-purpose analog inputs that are multiplexed to AOUT or to AOUT through a buffer (Figure 8). These inputs can be used for connection of temperature sensors or for a current monitor.

The total mux and switch series resistance is less than 200Ω. In applications where the load current flowing to the AOUT output is so high that significant errors are introduced due to series resistance in the voltage source and/or the signal path, use the buffer amplifier to improve accuracy.

Route the T_ inputs through the buffer to AOUT by setting the SPI bits [ECS, SC0, SC1, SC2, SC3] = [0, b, a, 1, 1]. Route the T_ inputs directly to the AOUT output by setting the bits [ECS, SC0, SC1, SC2, SC3 = [0, b, a, 0, 1]. Bits a and b select one of the three T_ inputs or three-state the AOUT output.

Three-Stating the AOUT Output

The AOUT output can be three-stated to share this pin with other external signal sources, such as additional temperature sensors. Use the ECS and SC_ bits to three-state the AOUT output.

Charge Balancing

Enhancement-mode n-channel FETs can be connected for passive balancing of cells. Select low on-resistance FETs with a V_T between 0.9V and half of the minimal cell voltage seen during cell balancing. Connect the FETs between each cell's anode and cathode with a current-limiting resistor in the drain (Figure 9).

The charge-balancing FETs can be enabled through SPI control. An internal 14.8kΩ (typ)/21.5kΩ (max) pulldown resistor assures that the FET is normally switched off. When balancing is active, a leakage current of 5µA is sunk from CV_. In addition, an internal balancing current flowing from CVn to CVn - 1 of 10mA (max) is present, where n = 1–12 (MAX14920) and n = 1–16 (MAX14921). The power dissipation created by the internal current during balancing should be considered for total package power management. Resistors between the cells and the CVn inputs cause IR voltage drop due to the internal 12mA(max) balance current. This results in measurement errors during balancing. Therefore, measuring cell voltages during charge balancing is not meaningful.

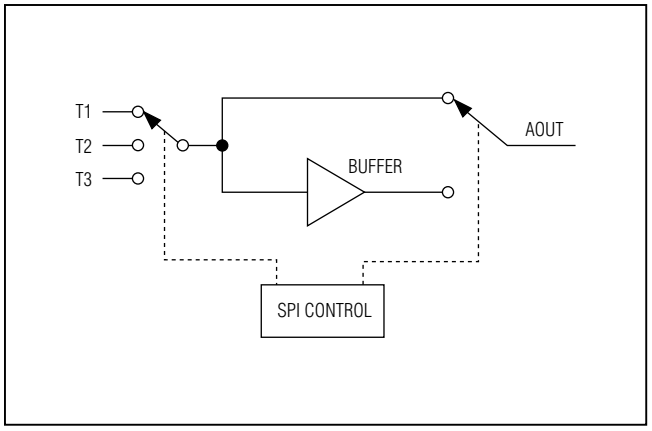


Figure 8. Analog/Temperature Measurement

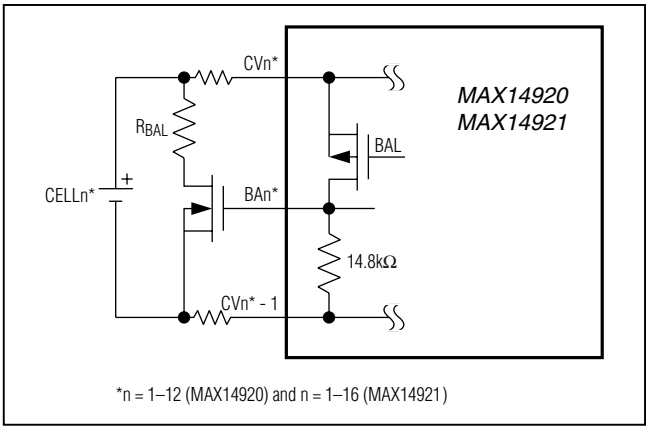


Figure 9. Charge Balancing

Diagnostics

The devices' integrated diagnostics allow detection of shorts between wires, as well as open-wire conditions of the CV_ pins.

Shorts between cell connections can be detected during normal operation. The cell readout voltage results in ~0V or ~V_A depending on where the short happens. In the case of shorts, the maximum currents flowing in/out of the pins must be limited and overvoltages avoided, including the external components (balancing FETs and sampling capacitors).

Open-wire conditions between the CV_ inputs and the cells can be detected in two different ways:

The first method of open-wire detection:

Set the DIAG bit to 1 while in the sampling phase. This applies a leakage current of 10µA to the CVn inputs. If CVn is unconnected, the leakage current starts discharging the sampling capacitor with a slew rate of I_{LEAK}/C_{SAMPLE} (~10µA/1µF = 100mV/10ms) down to CVn - 1. Two successive readouts show considerable cell voltage change in case of an open wire. Alternatively, waiting for a sampling time of ~300ms to 500ms reduces the cell voltage to below the UV_VC_{VTH} threshold voltage.

First open-wire detection procedure:

- Set DIAG bit to 1
- Wait > 0.5s before hold phase
- Read out the Cn bit or the CVn voltage under SPI control, where n = 1–12 (MAX14920) and n = 1–16 (MAX14921)

The second method of open-wire detection:

To check for a single open-wire connection, it is faster to enable the balancing FET only on the selected cell during the sampling phase and then reading out the selected cell voltage. If CVn is unconnected, the balancing FET rapidly (time depends on the balancing resistance used) shorts CVn to CVn - 1 and the readout phase shows ~0V or CVn and a voltage higher than V_A on CVn + 1.

Second open-wire detection procedure:

- Set the BAn bit to 1
- Wait for a time of R_{BAL} x C_{SAMPLE} before switching to the hold phase
- Route the CVn voltage to AOUT
- Repeat this procedure for all cells

During this procedure, the capacitors and external FETs need to withstand a voltage equal to V_{CVn} - V_{CVn-1}, where n = 1–12 (MAX14920) and n = 1–16 (MAX14921).

Input-Voltage Clamping

The devices have internal ESD-protection diodes that clamp input voltage lower than AGND or higher than V_P than VP (for CVn where n > 1) or 6V (for CV1) during a fault condition. Connect 3kΩ series resistors (R_{LIM}) to the inputs to limit the currents flowing through the forward-biased diodes during fault conditions or hot plugging (Figure 10). Sampling capacitors and balancing FETs must be chosen appropriately or protected with external voltage clamps to survive such events.

Power Sequencing

The V_A and V_L supplies can be applied at any sequence with respect to each other and also independently of the V_P and supplies CV_ inputs. The V_P voltage has to connect to the highest voltage of the cell stack.

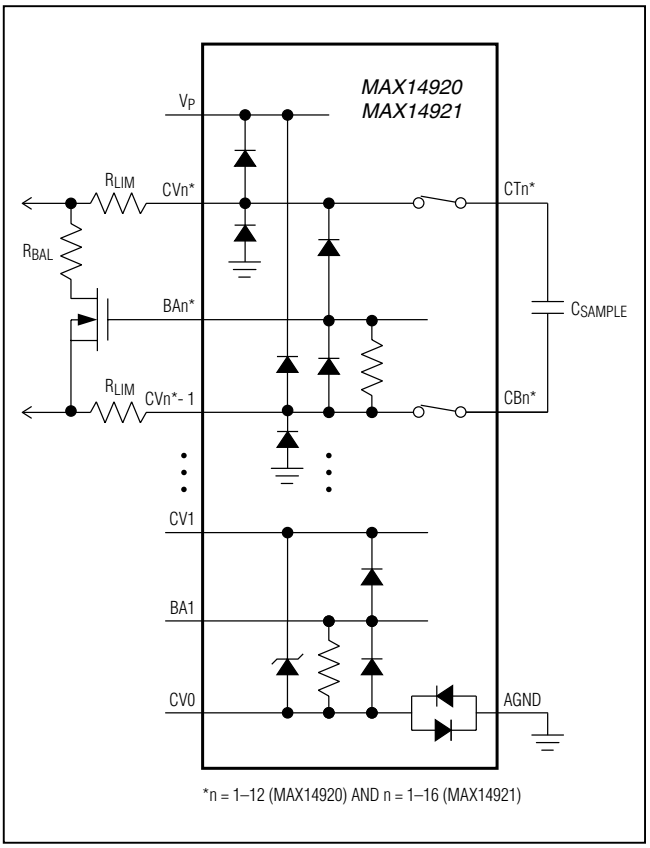


Figure 10. Input-Voltage Clamp

Applications Information

Connecting the Battery Pack to the BMS

When connecting the battery cells to the BMS electronics, large inrush currents can flow through the CVn pins that charges capacitance present on the VP pin. These inrush currents must be limited to avoid damage. Connect 3kΩ resistors in series with each CVn input pin, except the CV0 and CVT/VP pins, as shown in Figure 11. CVT refers to the top CVn terminal, which would for example be CV16 in the case of a 16S cell pack or CV10 in case of a 10S cell pack.

Only if the following connection sequence of the BMS electronics to the battery pack can be guaranteed, are the 3kΩ protection resistors not required or their value can be reduced: FIrst connect the battery's bottom (B-) and top (B+) terminals to the BMS' AGND/CV0 and VP/CVT terminals, then connect the remaining CVn cells connections.

Sampling Speed and Capacitor-Selection Considerations

Capacitor values of 1µF are recommended for achieving low charge injection errrors. In combination with 3kΩ current-limiting resistors, this results in sample and hold times in the order of 60ms. With 1µF capacitors and good PCB layout, charge injection-error correction is normally not required.

If higher/lower sampling speeds are required, the sampling capacitors can be reduced and/or increased.

The cell sampling capacitors connected to the CT_ and CB_ terminals affect:

- Speed of operation
- Cell readout accuracy

The smaller the sampling capacitor values, the lower their RC time constant and hence the faster their charging time. Therefore, for higher-speed operation, smaller capacitor values can be selected.

One application case can be when the cell voltages are known to only vary by small amounts from one sample to the next. In this case, the sampling capacitors can be made smaller, as the sampling phases only need to charge the capacitors by the charge lost during the previous level shift and hold phase, including the small change in cell voltage. See the *Measurement Accuracy* section for details on how to calculate the voltage drop due to these two factors. For example, sampling capacitors of approximately 100nF can be adequate, thereby reducing the sampling phase by a factor of 10. If this technique is used, the initial sampling times, after initial power-up, either have to be made longer to allow the initially discharged sampling capacitors to charge up to the cell voltages, or the initial samples are disregarded until the monitored voltages stabilize to their final cell value.

The accuracy dependence on the capacitor values is determined by the discharge during the hold phase and by the errors introduced during level shifting (both were previously described). By speeding up the readout of the cell voltages during the hold phase, discharging is reduced. Note that the last cell voltage being read out is most affected by discharging, due to its longer hold delay until being read out. Smaller capacitor values are prone to higher charge injection errors caused by level-shifting. Both low-capacitance layout and charge injection error calibration compensation reduce these errors.

Typical Application Circuit

Figure 11 shows a high-accuracy measurement application based on an accurate 16-bit ADC, together with a high-quality voltage reference. The internal linear regulator is used for supplying V_A (+5V), and uses the SAMPL input for controlling the cell voltage sample and hold times. Thermistors are connected to the T1, T2, and T3 inputs to monitor three temperatures.

If less absolute measurement accuracy is acceptable, an ADC with internal reference, such as the MAX11163, can be used. In applications where accuracy is not a critical factor, a microcontroller's internal ADC may be adequate.

Multipack Applications

In applications that require more than 12/16 cells to achieve higher voltages, multiple cell packs can be stacked. Each pack in the stack does not have to have the same number of cells. A minimum of +6V or 3 cells can be monitored by the devices.

In stacked packs, the sample signal can either be centrally controlled by a common signal for simultaneous sampling, or the sample/hold can be initiated through SPI. Two cell packs stacked on one another can be interconnected through an SPI or other communication interface. The packs can either have internal controllers or multiple packs can be controlled by one common controller. Internal controllers perform autonomous calibration and measurements, and allow an external controller to collect the data on demand. This scheme is shown in Figure 12. To translate the inter-pack communication signals between the differing common-mode pack voltages, use opto-isolators, digital isolators, or digital ground level shifters (Figure 12).

Layout Considerations

Keep the PCB traces to the sampling capacitors as short as possible and minimize parasitic capacitance between the capacitor pins and the ground plane.

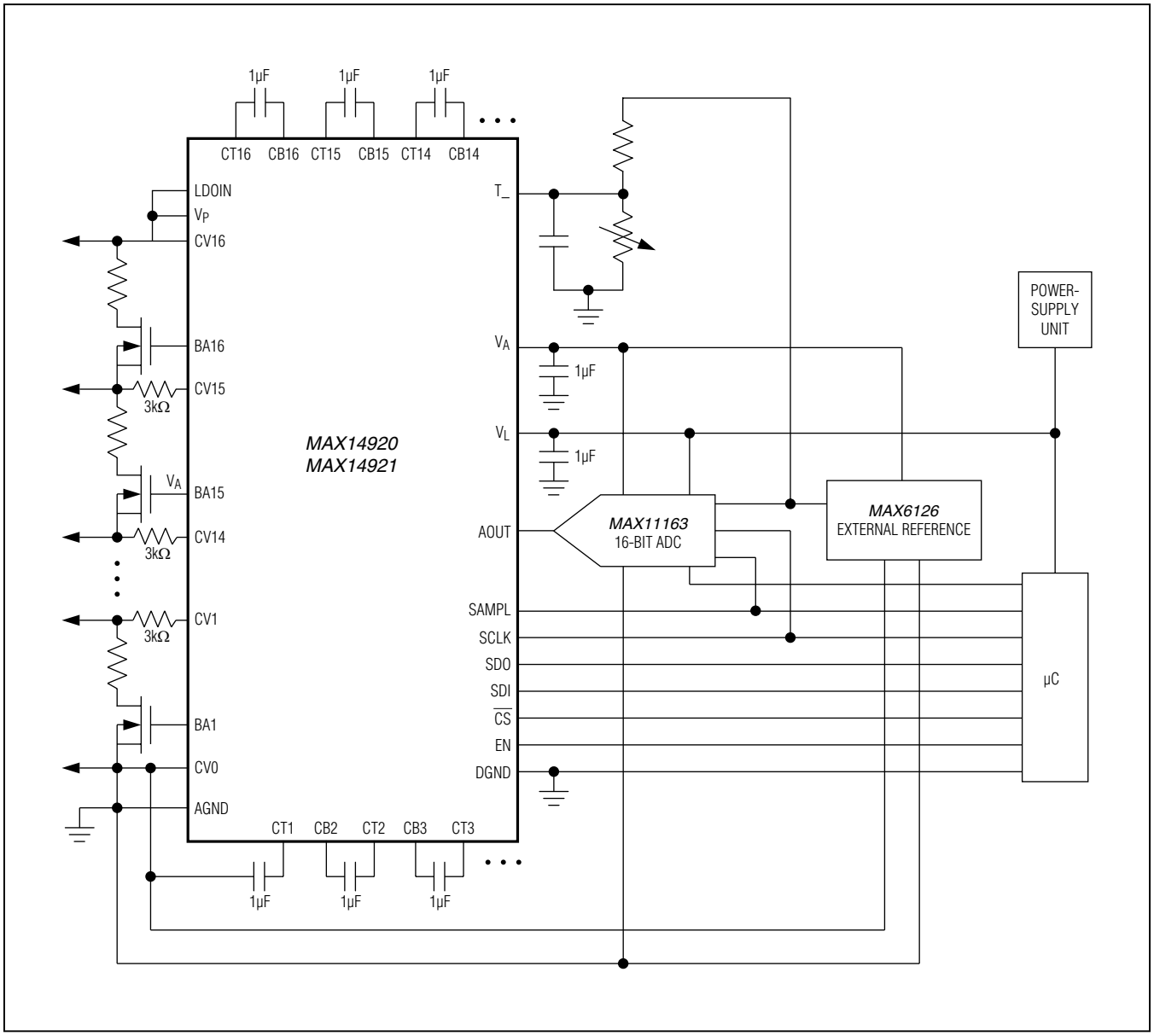


Figure 11. Typical Application Circuit

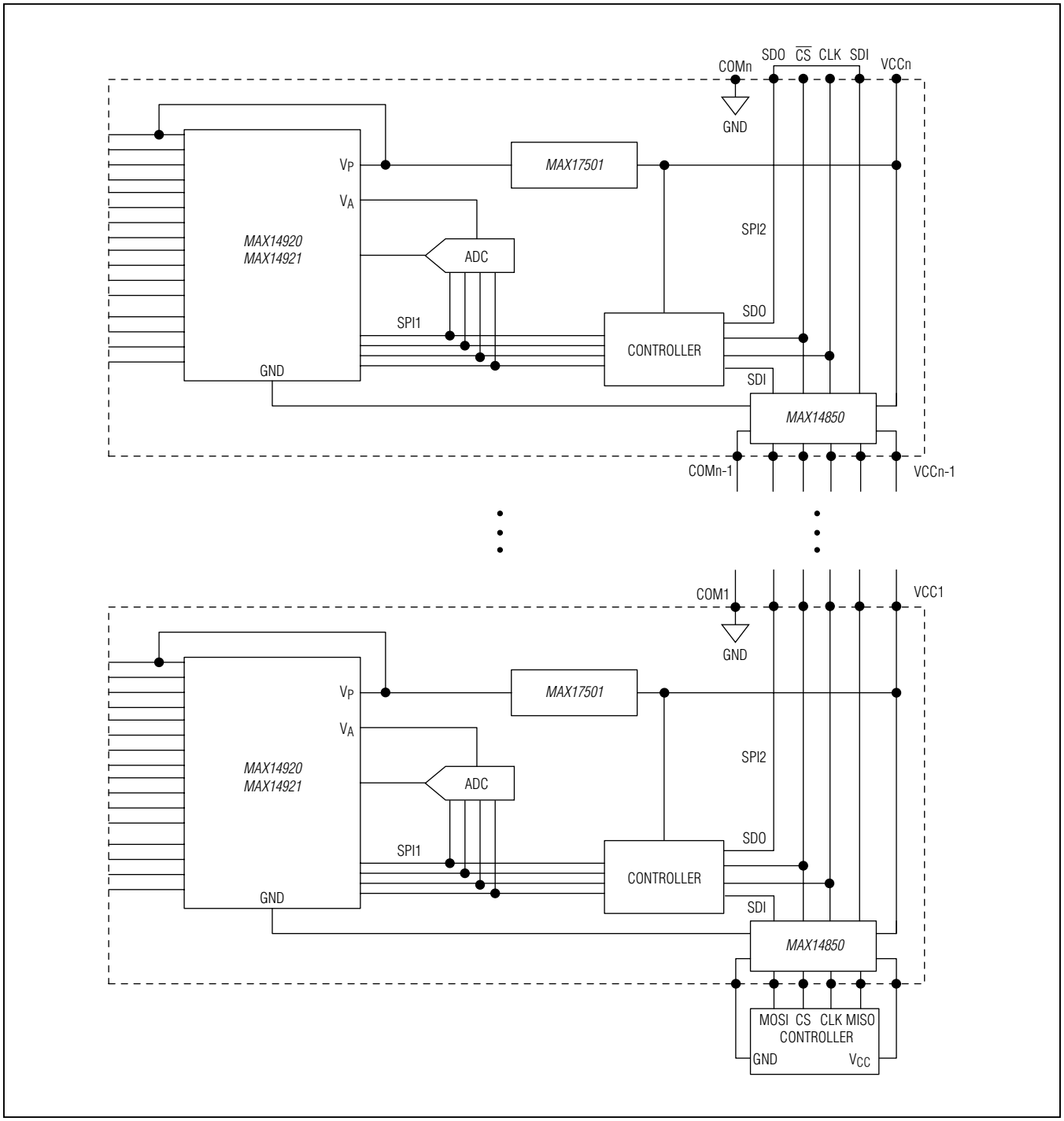
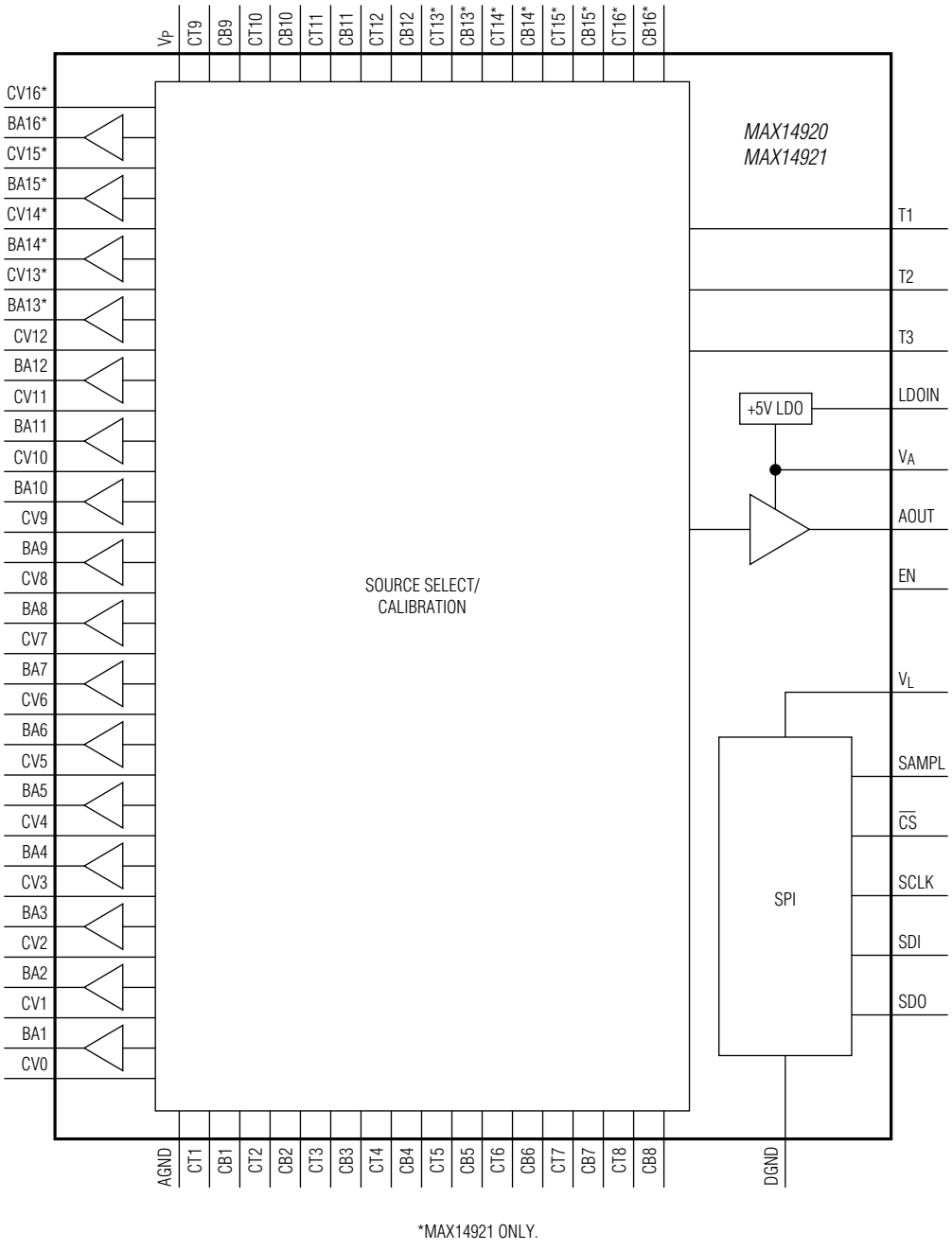


Figure 12. Stacked Battery Pack Application Diagram Based on Daisy-Chained SPI

Functional Diagram



*MAX14921 ONLY.

Ordering Information

PART	CELLS	TEMP RANGE	PIN-PACKAGE
MAX14920ECB+	12	-40°C to +85°C	64 TQFP-EP*
MAX14921ECS+	16	-40°C to +85°C	80 TQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 TQFP-EP	C64E+10	21-0084	90-0329
80 TQFP	C80+1	21-0072	—

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/12	Initial release	—
1	2/13	Removed future products asterisks from the MAX14920	28
2	6/14	Recommend the use of 3kW resistors in series with VCn for hot plug protection The SDO logic VOL(max) spec has been changed from 0.9V to 0.4V.	16
3	3/15	Added 3kΩ resistors to ***Typical Application Circuit*** and updated TOCs, ***Electrical Characteristics*** table and applications information.	1-4, 7, 10, 15-17, 22-25,

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