WINSOURCE ELECTRONICS

THE DATASHEET OF

MAX17823BGCB/V+T

MAX17823B 12-Channel High-Voltage Data Acquisition System

General Description

The MAX17823B is a data acquisition system for the management of high-voltage battery modules. The system features a 12-bit SAR ADC that can measure 12 cell voltages and two temperatures in 161 µs. There are 12 internal switches for cell-balancing and extensive built-in diagnostics. Up to 32 devices can be daisy-chained together to manage 384 cells and monitor 64 temperatures.

Cell voltages (0V to 5V) are measured differentially over a 65V common-mode range. Cell measurements have a typical accuracy of 2mV (3.6V cell, 25°C). If oversampling is enabled, up to 128 measurements per channel can be averaged internally with 14-bit resolution. The system can shut itself down in the event of a thermal overload by measuring its own die temperature.

The system uses Maxim's battery-management UART protocol for robust communications and when used in conjunction with the MAX17880 12-channel battery monitor, it is ideal for automotive battery-management systems that require a high safety integrity level.

Applications

- High-Voltage Battery Stacks
- Electric Vehicles (EVs)
- Hybrid Electric Vehicles (HEVs)
- Electric Bikes
- Battery-Backup Systems (UPS)
- Super-Cap Systems
- Battery-Powered Tools

Benefits and Features

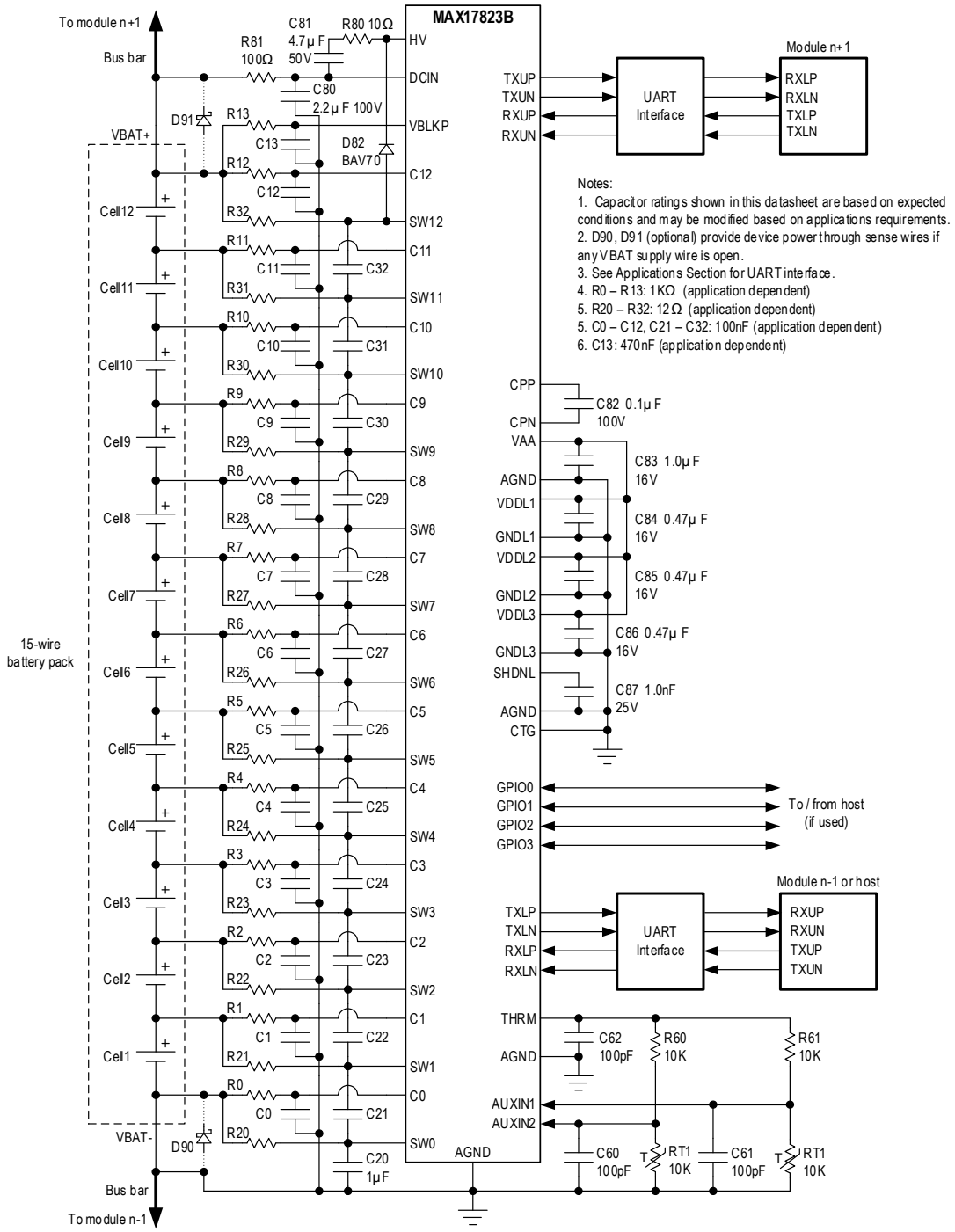
- AEC-Q100 Grade 2 Temperature Range
  - -40°C to 105°C
- Operating Voltage from 9V to 65V
- Ultra-Low Power Operation
  - Standby Mode: 2mA
  - Shutdown Mode: 2µA
- 12 Cell-Voltage Measurement Channels
  - 2mV Accuracy (3.6V, +25°C)
  - 5mV Accuracy (0°C to +45°C)
  - 10mV Accuracy (-40°C to +105°C)
- 12 Cell-Balancing Switches
  - Up to 150mA per switch
  - Emergency Discharge Mode
- Two Temperature Measurement Channels
- Die Temperature Measurement
- Automatic Thermal Protection
- 29 Voltage Threshold Alerts
  - 12 Over-Voltage Faults
  - 12 Under-Voltage Faults
  - Two Over-Temperature Faults
  - Two Under-Temperature Faults
  - One Cell Mismatch Alert (highest cell versus lowest cell)
- Four GPIOs
- Built-in Diagnostics to Support ASIL D and FMEA Requirements
- Battery-Management UART Protocol
  - Daisy-Chain up to 32 Devices
  - Communication Port Isolation
  - Up to 2Mbps Baud Rate (auto-detect)
  - 1.5µs Propagation Delay per Device
  - Packet-Error Checking (PEC)
- Factory-Trimmed Oscillators
  - No External Crystals Required
- 10mm x 10mm Package (64-pin LQFP)

Ordering Information appears at end of data sheet.

maxim integrated™

19-6912; Rev 5; 9/19

Simplified Operating Circuit



Absolute Maximum Ratings

HV to AGND ..... -0.3 to +80V
DCIN, SWn, VBLKP, Cn to AGND ..... -0.3V to min (V_{HV} + 0.3V, 72V)
Cn to Cn-1 ..... -72V to +72V
SWn to SWn-1 ..... -0.3V to +16V
VAA to AGND ..... -0.3v to +4V
VDDL1 to GNDL1 ..... -0.3V to +4V
VDDL2 to GNDL2 ..... -0.3V to +6V
VDDL3 to GNDL3 ..... -0.3V to +6V
VAA to VDDL1, VDDL2, VDDL3 ..... -0.3V to + 0.3V
AGND to GNDL1, GNDL2, GNDL3 ..... -0.3V to + 0.3V
AUXIN1, AUXIN2, THRM to AGND ..... -0.3V to V_{AA} + 0.3V
SHDNL to AGND ..... -0.3 to V_{DCIN} + 0.3V
CTG to AGND ..... -0.3V to +6V
RXLP, RXLN, RXUP, RXUN to AGND ..... -30V to +30V
TXLP, TXLN to GNDL2 ..... -0.3V to +6V
TXUP, TXUN to GNDL3 ..... -0.3V to +6V
CPP to AGND ..... V_{DCIN} - 1V to V_{HV} + 1V
CPN to AGND ..... -0.3V to V_{DCIN} + 0.3V
GPIO0, GPIO1, GPIO2, GPIO3 to GNDL1 ..... -0.3V to V_{DDL1} + 0.3V

Maximum Continuous Current into Any Pin (see Note 1) ..... ±20mA
Maximum Continuous Current into SWn Pin (see Note 2) ..... ±400mA
Maximum Average Power for ESD Diodes (see Note 3) ..... 14.4W/√τ
Package Continuous Power (see Note 4) 2000mW
Operating Temperature Range ..... -40° to +105°C
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 42.93°C
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 8.63°C
Storage Temperature Range ..... -55° to +150°C
Junction Temperature (continuous) ..... 150°C
Soldering Lead Temperature (10s maximum) ..... 300°C

Note 1: Balancing switches disabled.
Note 2: One balancing switch enabled, 60s maximum.
Note 3: Average power for time period τ where τ is the time constant (in µs) of the transient diode current during hot-plug event. For, example, if τ is 330µs, the maximum average power is 0.793W. Peak current must never exceed 2A. Actual average power during hot-plug must be calculated from the diode current waveform for the application circuit and compared to the maximum rating.
Note 4: Multi-layer board. For T_A > 70ºC derate 25mW/ºC.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DCIN} = +48V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, where T_{MIN} = -40°C and T_{MAX} = +105°C. Typical values are at T_A = +25°C. Operation is with the recommended application circuit. See Note 5.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage	V_{DCIN}		9		65	V
DCIN Current, Shutdown Mode	I_{DCSHDN}	V_{SHDNL}= 0V		0.1	2	µA
DCIN Current, Standby Mode (Note 16)	I_{DCSTBY}	V_{SHDNL} > 1.8V, UART in idle mode, not in acquisition mode, BALSWEN, CTSTEN = 0000h	1.4	2.0	2.6	mA
DCIN Current, Acquisition Mode (Note 16)	I_{DCMEAS}	MEASUREEN = 0FFFh, acquisition mode	3.5	5.4	8.5	mA
Incremental DCIN Current, Communication Mode (Note 16)	I_{DCCOMM}	Baud rate = 2Mb/s (0% idle time preambles mode), 200pF load on TXUP, 200pF on TXUN, TXL not active, not in acquisition mode, BALSWEN, CTSTEN = 0000h		1.5	3	mA
HV Current, Acquisition Mode	I_{HVMEAS}	Acquisition mode, MEASUREEN = 0FFFh, V_{HV} = V_{DCIN} + 5.5V	0.9	1.1	1.3	mA
Incremental HV Current, Cell-Balancing Mode	I_{HVBAL}	V_{HV} = V_{DCIN} + 5.5V, n balancing switches enabled	(n+1)x5	(n+1)x13.5	(n+1)x26	µA
CELL VOLTAGE INPUTS (Cn, VBLKP)						
Differential Input Range (Note 11)	V_{CELLn}	Unipolar mode	0.2		4.8	V
		Bipolar mode	-2.3		+2.3	V
Common-Mode Input Range	V_{CnCM}	Not connected to SWn inputs	0		65	V
Input Leakage Current	I_{LKG_Cn}	Not in acquisition mode, V_{Cn} = 65V	-200	±10	+200	nA
VBLKP Input Resistance	R_{VBLKP}	V_{BLKP} = V_{DCIN} = 57.6V	4.5	10	20	MΩ
HVMUX Switch Resistance	R_{HVMUX}	CTSTDAC[3:0] = Fh	1.7	3.3	5	kΩ
CELL-BALANCING INPUTS (SWn)						
Leakage Current	I_{LKG_SW}	V_{SW0} = 0V, V_{SWn} = 5V, V_{SWn-1} = 0V	-1		+1	µA
Resistance, SWn to SWn-1	R_{SW}	BALSWEN[n-1] = 1, I_{SWn} = 100mA	0.5	2	5	Ω
Maximum Allowed Balancing Current (Note 15)	I_{BAL_MAX}	T_j = 105°C, 25% average duty-cycle per switch		256		mA
AUXILIARY INPUTS (AUXIN1, AUXIN2)						
Input Voltage Range	V_{AUXIN}		0		V_{THRM}	V
Input Leakage Current	I_{LKG_AUX}	Not in acquisition mode, V_{AUXINn} = 1.65V	-400	10	+400	nA
THRM OUTPUT						
Switch Resistance, VAA to THRM	R_{THRM}			25	70	Ω
Leakage Current	I_{LKG_THRM}	V_{THRM} = 3.3V	-1		1	µA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MEASUREMENT ACCURACY						
Total Measurement Error, HVMUX Inputs (Note 12)	$V_{CELLnERR}$	Unipolar mode, V_{CELLn} = 3.6V		±2		mV
		Bipolar mode, V_{CELLn} = 1.1V				
		Unipolar mode 0.2V ≤ V_{CELLn} ≤ 4.3V, 0ºC ≤ T_A ≤ 45ºC	-5	±3.6	+5	
		Unipolar mode, 0.2V ≤ V_{CELLn} ≤ 4.8V	-10		+10	
		Bipolar mode, -2.3V ≤ V_{CELLn} ≤ 2.3V, SWn inputs not connected				
Total Measurement Error, ALTMUX Inputs (Note 12)	V_{SWnERR}	Unipolar mode, V_{CELL} = 3.6V		±2		mV
		Bipolar mode, V_{CELLn} = 1.1V				
		Unipolar mode, 0.2V ≤ V_{CELLn} ≤ 4.8V	-10		+10	
		Bipolar mode, 0V ≤ V_{CELLn} ≤ 2.3V				
Channel Noise (Note 7)	$V_{CELLNOISE}$	No oversampling		1.1		mVRMS
Total Measurement Error, V_{BLKP} Input	$V_{BLKPERR}$	9V ≤ V_{BLKP} ≤ 57.6V, V_{DCIN} = 57.6V, Average of 64 acquisitions	-180		+180	mV
Offset Error, AUXIN Inputs	V_{OS_AUX}		-3		+3	mV
Gain Error, AUXIN Inputs	A_{V_AUX}		-0.3		+0.3	%
Total Measurement Error, Die Temperature (Note 7)	T_{DIE_ERR}	T_j = -40ºC to 105ºC, no oversampling	-5	±3	+5	ºC
Differential Non-Linearity (any conversion)	DNL			±1.0		LSbs
ADC Resolution			12			bits
Level-shifting Amplifier Offset (Note 14)	V_{OS_LSAMP}	DIAGSEL[2:0] = 011b	-200	-10	+200	mV

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SHDNL INPUT AND CHARGE PUMP						
Input Low Voltage	V_{IL_SHDNL}				0.6	V
Input High Voltage	V_{IH_SHDNL}		1.8			V
Regulated Voltage	$V_{SHDNLIMIT}$	$V_{DCIN} \geq 12V$	8	9.5	12	V
		$V_{DCIN} = 9V$		6.7		V
Pull-down Resistance	$R_{FORCEPOR}$	FORCEPOR = 1	2.5	4.7	8	kΩ
Input Leakage Current	I_{LKG_SHDNL}	$V_{SHDNL} = 3.3V$			1	µA
		$V_{SHDNL} = 65V$		40	75	µA
Charge Pump Current (Note 10)	I_{SHDNL}	$V_{SHDNL} < V_{SHDNLIMIT}$, baud rate = 2Mbps	15	117	350	µA
GENERAL-PURPOSE I/O (GPIOn)						
Input Low Voltage	V_{IL_GPIO}				0.8	V
Input High Voltage	V_{IH_GPIO}		2.4			V
Pull-down Resistance	R_{GPIO}	GPIO[15:12] = 0h (input)	0.5	2	7.5	MΩ
Output Low Voltage	V_{OL_GPIO}	$I_{SINK} = 3mA$			0.4	V
Output High Voltage	V_{OH_GPIO}	$I_{SOURCE} = 3mA$	V_{DDL1} - 0.4			V
REGULATOR						
Output Voltage	V_{AA}	$0 \leq I_{AA} < 10mA$	3.2	3.3	3.4	V
Short-Circuit Current	I_{AASC}	VAA shorted to AGND	10	20	70	mA
POR Threshold	$V_{PORFALL}$	V_{AA} falling	2.85	2.95	3.02	V
	$V_{PORRISE}$	V_{AA} rising		3.0	3.1	V
POR Hysteresis	V_{PORHYS}			40		mV
Thermal Shutdown Temperature (Note 7)	T_{SHDN}	Temperature rising		145		ºC
Thermal Shutdown Hysteresis (Note 7)	T_{HYS}			15		ºC
HV CHARGE PUMP						
Output Voltage (V_{HV}-V_{DCIN})	$V_{HV-DCIN}$	$9V \leq V_{DCIN} \leq 12V$, I_{LOAD} = 1.5mA	5	5.5	6	V
		$12V \leq V_{DCIN} \leq 65V$, $I_{LOAD} = 3mA$	5	5.5	6	
Charge Pump Efficiency (Note 18)		$V_{DCIN} = 57.6V$		38		%
HV Headroom (V_{HV}-V_{C12})	V_{HVHDRM}	ALRTHVHDRM = 0	4.7			V
OSCILLATORS						
32kHz Oscillator Frequency	f_{OSC_32K}		32.11	32.768	33.42	kHz
16MHz Oscillator Frequency	f_{OSC_16M}		15.68	16	16.32	MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIAGNOSTIC TEST SOURCES						
Cell Test Source Current	I_{TSTCn}	CTSTDAC[3:0] = Fh, $V_{Cn} < V_{AA}$ - 1.4V, V_{AA} = 3.3V	80	100	120	µA
		CTSTDAC[3:0] = 6h, $V_{Cn} < V_{AA}$ - 1.4V, V_{AA} = 3.3V	36	45	54	
		CTSTDAC[3:0] = 6h, $V_{Cn} > V_{AGND}$ + 1.4V	-54	-45	-36	
		CTSTDAC[3:0] = Fh, $V_{Cn} > V_{AGND}$ + 1.4V	-120	-100	-80	
HVMUX Test Source Current	I_{TSTMUX}	CTSTDAC[3:0] = Fh, $V_{Cn} < V_{HV}$ - 1.4V, V_{HV} = 53.5V	40	50	60	µA
		CTSTDAC[3:0] = 6h, $V_{Cn} < V_{HV}$ - 1.4V, V_{HV} = 53.5V	18	22.5	27	
AUXIN Test Source Current	$I_{TSTAUXIN}$	CTSTDAC[3:0] = Fh, $V_{AUXINn} < V_{AA}$ - 1.4V, V_{AA} = 3.3V	80	100	120	µA
		CTSTDAC[3:0] = 6h, $V_{AUXINn} < V_{AA}$ - 1.4V, V_{AA} = 3.3V	36	45	54	
		CTSTDAC[3:0] = 6h $V_{AUXINn} > V_{AGND}$ + 1.4V	-54	-45	-36	
		CTSTDAC[3:0] = Fh, $V_{AUXINn} > V_{AGND}$ + 1.4V	-120	-100	-80	
DIAGNOSTIC REFERENCES						
ALTREF Voltage (Note 14)	V_{ALTREF}	DIAGSEL[2:0] = 001b	1.23	1.242	1.254	V
ALTREF Temperature Coefficient ($\Delta V_{ALTREF}/\Delta T$) (Note 7)	A_{ALTREF}			±25		ppm/°C
PTAT Output Voltage (Note 7)	V_{PTAT}	T_J = 120ºC		1.2		V
PTAT Temperature Coefficient ($\Delta V_{PTAT}/\Delta T$) (Note 7)	A_{V_PTAT}			3.07		mV/°C
PTAT Temperature Offset (Note 7)	T_{OS_PTAT}			0		ºC
ALERTS						
ALRTVDDLn Threshold	V_{VDDL_OC}	VAA = 3.3V	3	3.15	3.25	V
ALRTGNDLn Threshold	V_{GNDL_OC}	AGND = 0V	0.05	0.15	0.3	V
ALRTHVUV Threshold	V_{HVUV}	V_{HV} - V_{DCIN} falling	3.8	4.1	4.25	V
ALRTHVOV Threshold	V_{HVOV}	V_{HV} - V_{DCIN} rising	7	8.5	10	V
ALRTTEMP Threshold (Note 7)	$T_{ALRTTEMP}$		115	120	125	ºC
ALRTTEMP Hysteresis (Note 7)	$T_{ALRTTEMPHYS}$			2		ºC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UART OUTPUTS (TXLP, TXLN, TXUP, TXUN)						
Output Low Voltage	V_{OL}	I_{SINK} = 20mA			0.4	V
Output High Voltage (TXLP, TXLN)	V_{OH}	I_{SOURCE} = 20mA	V_{DDL2} - 0.4			V
Output High Voltage (TXUP, TXUN)	V_{OH}	I_{SOURCE} = 20mA	V_{DDL3} - 0.4			V
Leakage Current	I_{LKG_TX}	V_{TX} = 1.5V	-1		1	µA
UART INPUTS (RXLP, RXLN, RXUP, RXUN)						
Input Voltage Range	V_{RX}		-25		25	V
Receiver High Comparator Threshold (Notes 9, 13)	V_{CH}		V_{DDL}/2-0.4	V_{DDL}/2	V_{DDL}/2+0.4	V
Receiver Zero-Crossing Comparator Threshold (Note 9)	V_{ZC}		-0.4	0	0.4	V
Receiver Low Comparator Threshold (Notes 9, 13)	V_{CL}		-V_{DDL}/2-0.4	-V_{DDL}/2	-V_{DDL}/2+0.4	V
Receiver Comparator Hysteresis (Note 9)	V_{HYS_RX}			75		mV
Receiver Common-mode Voltage Bias (Notes 9, 13)	V_{CM}			V_{DDL}/3		V
Leakage Current	I_{LKG_RX}	V_{RX} = 1.5V		±1.0		µA
Input Capacitance (RXLP, RXLN)	C_{RXL}			4		pF
Input Capacitance (RXUP, RXUN)	C_{RXU}			2		pF
UART TIMING						
Bit Period (Note 17)	t_{BIT}	Baud rate = 2Mb/s		8		1/f_{OSC_16M}
		Baud rate = 1Mb/s		16		
		Baud rate = 0.5Mb/s		32		
RX Idle to START Setup Time (Notes 6, 7)	t_{RXSTSU}		0		1	t_{BIT}
STOP Hold Time to Idle (Notes 6, 7)	t_{SPHD}				0.5	t_{BIT}
RX Minimum Idle Time (STOP bit to START bit) (Note 6, 7)	$t_{RXIDLESPST}$		1			t_{BIT}
RX Fall Time (Notes 7, 8)	t_{FALL}				0.5	t_{BIT}
RX Rise Time (Notes 7, 8)	t_{RISE}				0.5	t_{BIT}
Propagation Delay (RX Port to TX port)	t_{PROP}			2.5	3	t_{BIT}
Start-Up Time from SHNDL high and V_{AA} = 0V to RXUP/RXUN valid	$t_{STARTUP}$			1		ms

Note 5: Unless otherwise noted, limits are 100% production-tested at T_A = +25ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 6: Maximum limited by application circuit.

Note 7: Guaranteed by design and not production-tested.

Note 8: Fall time measured 90% to 10%, rise time measured 10% to 90%.

Note 9: Differential signal (V_{RXP} - V_{RXN}) where V_{RXP} and V_{RXN} do not exceed a common-mode voltage range of ±25V.

Note 10: I_{SHDNL} measured with V_{SHDNL} = 0.3V, STOP characters, zero idle time, V_{RX_PEAK} = 3.3V

Note 11: V_{CELLn} = V_{Cn} - $V_{Cn-1,}$ Range over which measurement settling time and accuracy is guaranteed.

Note 12: V_{CELLn} = V_{Cn} - V_{Cn-1}, V_{CELLn} = $V_{CELLn-1}$, and V_{DCIN} = 12 x $\left|V_{CELLn}\right|$ (9V minimum). No oversampling enabled (OVSAMPL[2:0] = 0). Average of 64 acquisitions.

Note 13: V_{DDL} = V_{DDL2} for lower port and V_{DDL} = V_{DDL3} for upper port.

Note 14: As measured during specified diagnostic mode.

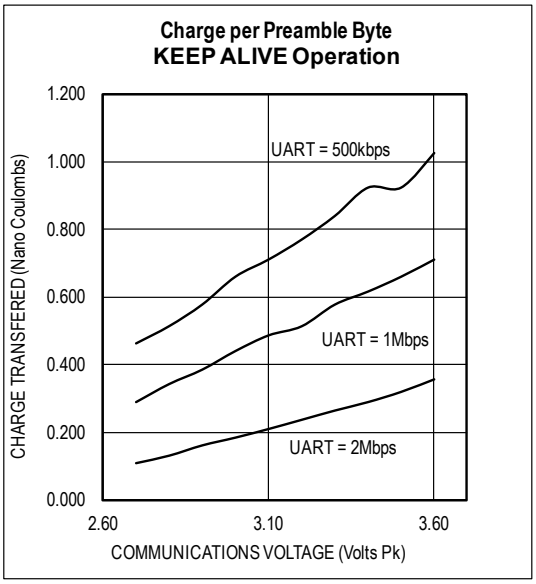
Note 15: Not production tested. See Cell-Balancing section for details on the maximum allowed balancing current. Duty-cycle is calculated for a 10-year device lifetime.

Note 16: Acquisition mode (ADC conversions) is entered when the SCAN bit is set and ends when SCANDONE is set. With the typical acquisition duty-cycle very low, the average current I_{DCIN} is much less than I_{DCMEAS}. Total supply current during communication I_{DCIN} = I_{DCCOMM} + I_{DCSTBY}.

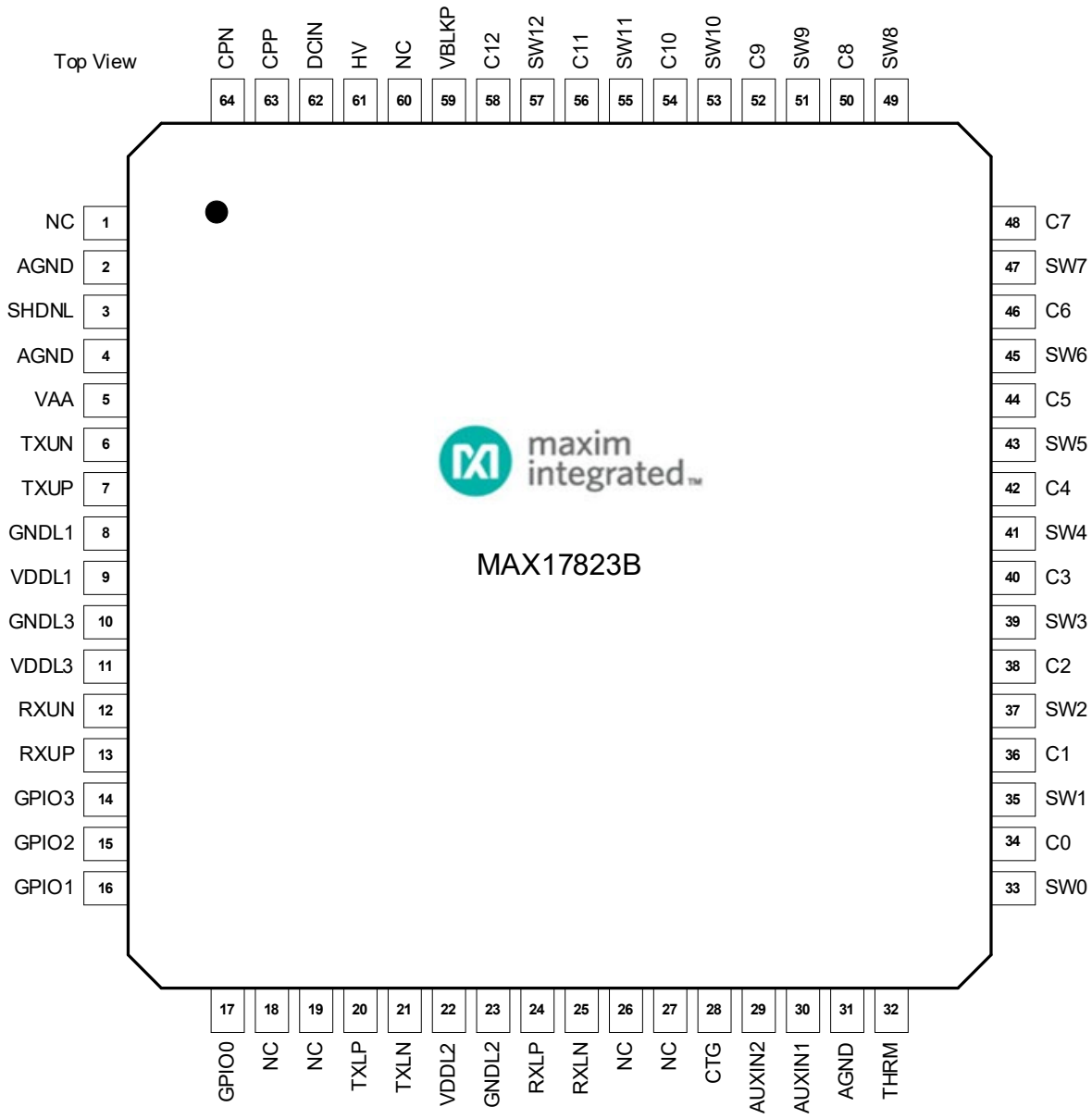
Note 17: In daisy-chain applications, the bit time of the second stop bit may be less than specified to account for clock rate variation and sampling error between devices.

Note 18: Charge pump efficiency = ΔI_{LOAD} / ΔI_{SUPPLY}, where I_{LOAD} is applied from HV to AGND, ΔI_{LOAD} = 5mA, and ΔISUPPLY = I_{DCIN} (for I_{LOAD} = 5mA) - I_{DCIN} (for I_{LOAD} = 0).

Typical Operating Characteristics



Pin Configuration



LQFP

Pin Description

PIN	NAME	FUNCTION	DESCRIPTION
1	NC	NC	Not connected. Connect to ground or leave floating.
2	AGND	Ground	Analog ground. Connect to negative terminal of cell 1 and ground plane.
3	SHDNL	Input	Shutdown active low input. Drive >1.8V to enable operation and drive <0.6V to reset device and place in shutdown mode. +72V tolerant. If not driven externally, this input may be controlled solely via UART communication and software control. Bypass with a 1nF capacitor to AGND. For single–ended UART, SHDNL must be driven externally.
4	AGND	Ground	Analog ground. Connect to negative terminal of cell 1 and ground plane.
5	VAA	Power	3.3V regulator output used to supply VDDL1, VDDL2, and VDDL3. Bypass with a 1µF capacitor to ground.
6	TXUN	Output	Negative output for upper port transmitter. Driven between VDDL3 and GNDL3.
7	TXUP	Output	Positive output for upper port transmitter. Driven between VDDL3 and GNDL3.
8	GNDL1	Ground	Digital ground. Connect to ground plane.
9	VDDL1	Power	3.3V digital supply. Connect externally to VAA and bypass with 0.47µF capacitor to GNDL1.
10	GNDL3	Ground	Ground for upper port transmitter. Connect to ground plane.
11	VDDL3	Power	3.3V supply for upper port transmitter. Connect externally to VAA and bypass with 0.47µF capacitor to GNDL3.
12	RXUN	Input	Negative input for upper port receiver. Tolerates ±30V.
13	RXUP	Input	Positive input for upper port receiver. Tolerates ±30V. Connect to ground for single-ended operation.
14	GPIO3	I/O	General-Purpose I/O 3. Driven between VDDL1 and GNDL1. 2MΩ internal pull-down.
15	GPIO2	I/O	General-Purpose I/O 2. Driven between VDDL1 and GNDL1. 2MΩ internal pull-down.
16	GPIO1	I/O	General-Purpose I/O 1. Driven between VDDL1 and GNDL1. 2MΩ internal pull-down.
17	GPIO0	I/O	General-Purpose I/O 0. Driven between VDDL1 and GNDL1. 2MΩ internal pull-down.
18	NC	NC	Not connected. Connect to ground or leave floating.
19	NC	NC	Not connected. Connect to ground or leave floating.
20	TXLP	Output	Positive output for lower port transmitter. Driven between VDDL2 and GNDL2.
21	TXLN	Output	Negative output for lower port transmitter. Driven between VDDL2 and GNDL2.
22	VDDL2	Power	3.3V supply for lower port transmitter. Connect externally to VAA and bypass with 0.47µF capacitor to GNDL2.
23	GNDL2	Ground	Ground for lower port transmitter. Connect to ground plane.
24	RXLP	Input	Positive input for lower port receiver. Tolerates ±30V. Connect to ground for single-ended operation.
25	RXLN	Input	Negative input for lower port receiver. Tolerates ±30V.
26	NC	NC	Not connected. Connect to ground or leave floating.
27	NC	NC	Not connected. Connect to ground or leave floating.
28	CTG	Input	Reserved for factory use. Connect to ground.
29	AUXIN2	Input	Auxiliary voltage input 2 to measure external temperature. Connect to a voltage divider consisting of a 10KΩ pull-up to THRM and 10KΩ NTC thermistor to ground. If not used, connect to the pull-up only.
30	AUXIN1	Input	Auxiliary voltage input 1 to measure external temperature. Connect to a voltage divider consisting of a 10KΩ pull-up to THRM and a 10KΩ NTC thermistor to ground. If not used, connect to the pull-up only.
31	AGND	Ground	Analog ground. Connect to negative terminal of cell 1 and ground plane.

PIN	NAME	FUNCTION	DESCRIPTION
32	THRM	Power	3.3V switched output used to supply the voltage dividers for the auxiliary inputs. The output is enabled only during measurements or as configured by THRMMODE[1:0]. This output can source up to 2mA.
33	SW0	Input	Balance input for Cell 1 negative.
34	C0	Input	Voltage input for Cell 1 negative. Connect to AGND.
35	SW1	Input	Balance input for Cell 1 positive (Cell 2 negative).
36	C1	Input	Voltage input for Cell 1 positive (Cell 2 negative).
37	SW2	Input	Balance input for Cell 2 positive (Cell 3 negative).
38	C2	Input	Voltage input for Cell 2 positive (Cell 3 negative).
39	SW3	Input	Balance input for Cell 3 positive (Cell 4 negative).
40	C3	Input	Voltage input for Cell 3 positive (Cell 4 negative).
41	SW4	Input	Balance input for Cell 4 positive (Cell 5 negative).
42	C4	Input	Voltage input for Cell 4 positive (Cell 5 negative).
43	SW5	Input	Balance input for Cell 5 positive (Cell 6 negative).
44	C5	Input	Voltage input for Cell 5 positive (Cell 6 negative).
45	SW6	Input	Balance input for Cell 6 positive (Cell 7 negative).
46	C6	Input	Voltage input for Cell 6 positive (Cell 7 negative).
47	SW7	Input	Balance input for Cell 7 positive (Cell 8 negative).
48	C7	Input	Voltage input for Cell 7 positive (Cell 8 negative).
49	SW8	Input	Balance input for Cell 8 positive (Cell 9 negative).
50	C8	Input	Voltage input for Cell 8 positive (Cell 9 negative).
51	SW9	Input	Balance input for Cell 9 positive (Cell 10 negative).
52	C9	Input	Voltage input for Cell 9 positive (Cell 10 negative).
53	SW10	Input	Balance input for Cell 10 positive (Cell 11 negative).
54	C10	Input	Voltage input for Cell 10 positive (Cell 11 negative).
55	SW11	Input	Balance input for Cell 11 positive (Cell 12 negative).
56	C11	Input	Voltage input for Cell 11 positive (Cell 12 negative).
57	SW12	Input	Balance input for Cell 12 positive.
58	C12	Input	Voltage input for Cell 12 positive.
59	VBLKP	Input	Block voltage positive input. Internal 10MΩ pull-down during measurement.
60	NC	NC	Not connected. Connect to ground or leave floating.
61	HV	Power	Decoupling capacitor connection for the HV charge pump. $V_{HV} = V_{DCIN} + 5.5V$ (typical). Bypass with a 50V, 4.7µF capacitor to DCIN.
62	DCIN	Power	DC supply for the low-voltage regulator, HV charge pump, and SHDNL charge pump. Connect to a voltage source between 9V and 65V via a 100Ω series resistor. Bypass with a 100V, 2.2µF capacitor to ground.
63	CPP	Power	Positive capacitor connection for the HV charge pump. Connect a 100V, 0.1µF capacitor from CPP to CPN.
64	CPN	Power	Negative capacitor connection for the HV charge pump.

Detailed Description

The data acquisition system consists of the major blocks shown in Figure 1 and described in Table 1.

Table 1. System Blocks

Block	Description
ADC	Analog-to-Digital Converter. Uses a 12-bit successive-approximation register (SAR) with a reference voltage of 2.307V and supplied by V_{AA}.
HVMUX	12-channel high-voltage (65V) differential multiplexer for Cn inputs.
HV CHARGE PUMP	High-voltage charge-pump supply (V_{DCIN} + 5.5V) for the HVMUX, ALTMUX, BALSW, and LSAMP circuits which must switch high-voltage signals. Supplied by DCIN.
LSAMP	Level-shifting amplifier with a gain of 6/13. The result is that a 5V differential signal is attenuated to 2.307V, which is the reference voltage for the ADC.
LVMUX	Multiplexes various low-voltage signals including the level-shifted signals and temperature signals to the ADC for subsequent A-to-D conversion.
ALTMUX	12-channel, high-voltage differential multiplexer for SWn inputs.
BALSW	Cell-balancing switches.
LINREG	3.3V (V_{AA}) linear regulator used to power the ADC and digital logic. Supplied by DCIN (9V to 65V).
REF	2.307V precision reference voltage for ADC and LINREG. Temperature-compensated.
ALTREF	1.242V precision reference voltage used for diagnostics.
16MHZ OSC	16MHz oscillator with 2% accuracy for clocking state-machines and UART timing.
32KHZ OSC	32,768Hz oscillator for driving charge pumps and timers.
LOWER PORT	Differential UART for communication with host or down-stack devices. Auto-detects baud rates of 0.5Mbps, 1Mbps, or 2Mbps.
UPPER PORT	Differential UART for communication with up-stack devices.
CONTROL AND STATUS	ALUs, control logic, and data registers
DIE TEMP	A Proportional-to-Absolute-Temperature (PTAT) voltage source used to measure the die temperature.

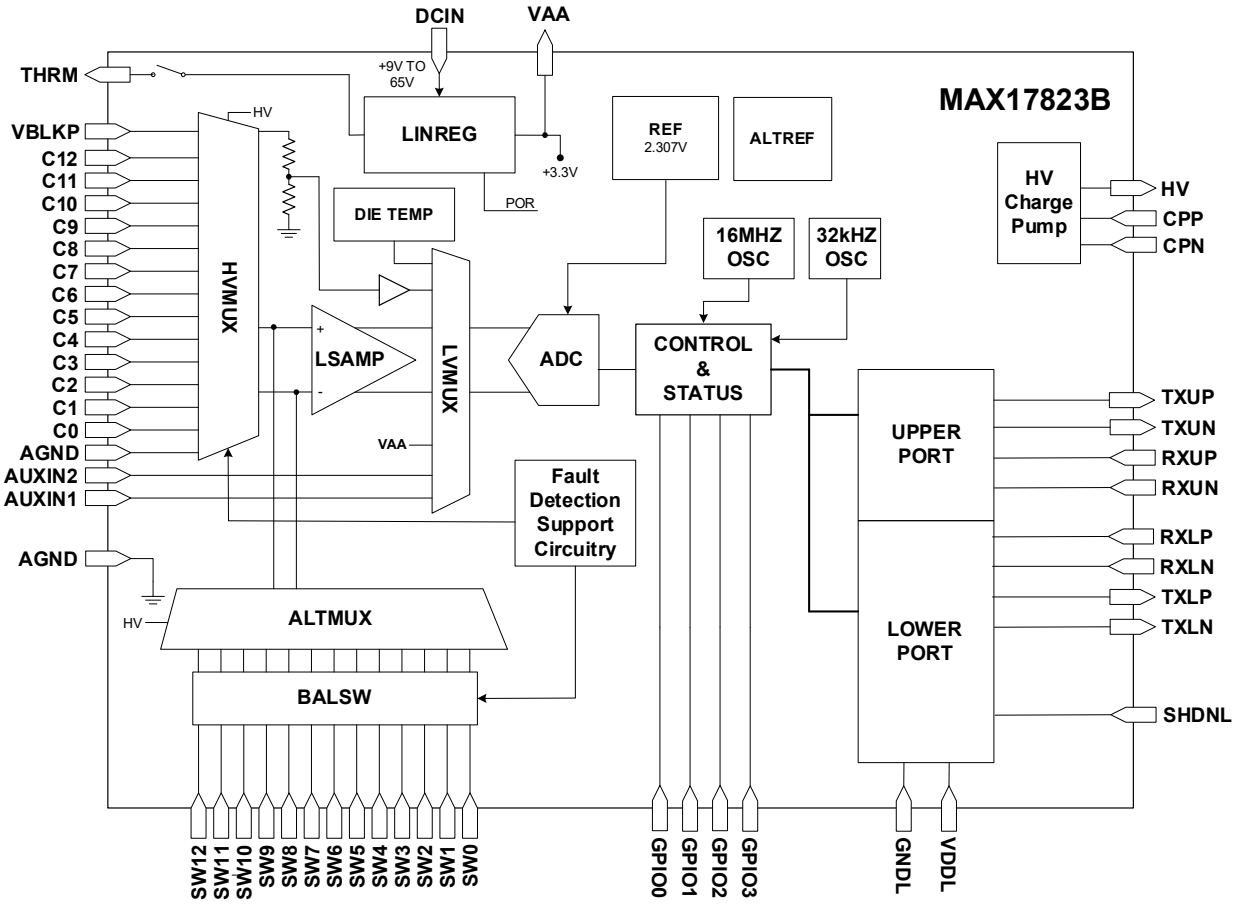
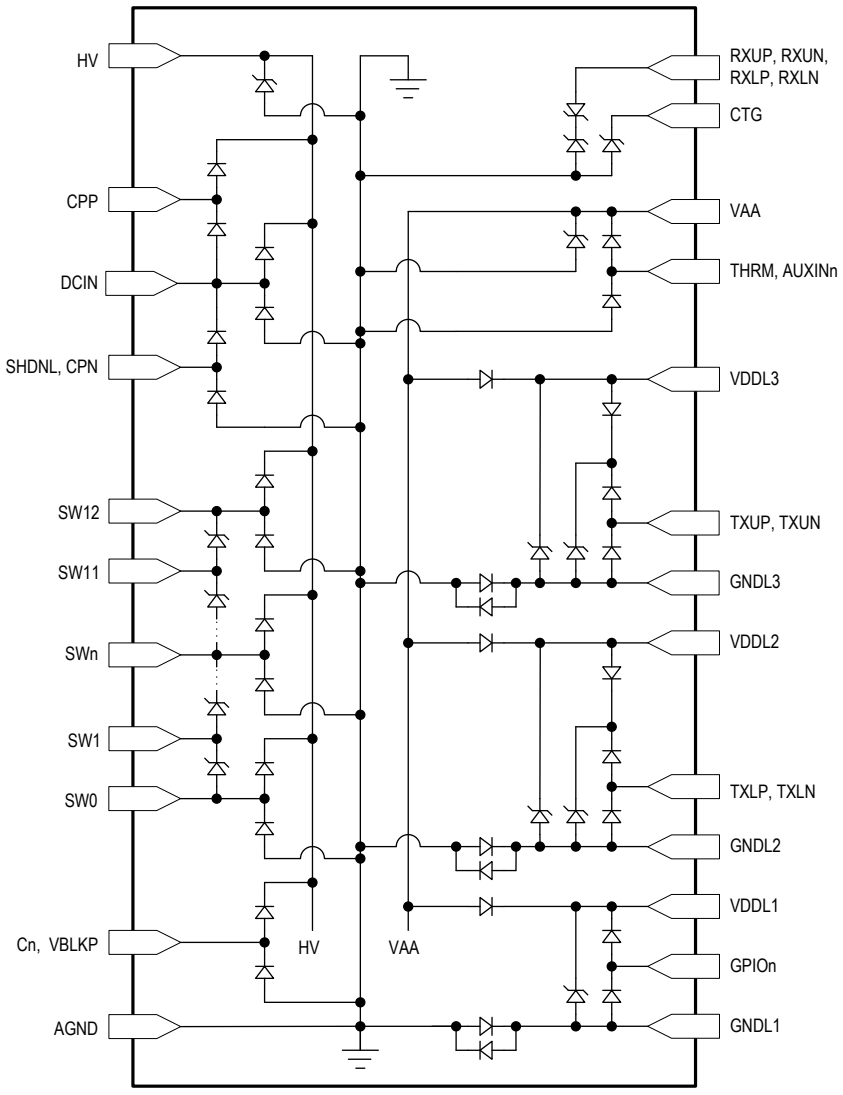


Figure 1. Functional Block Diagram



Notes:
1. All diodes are rated for ESD clamping conditions. They are not intended to accurately clamp DC voltage.
2. All diodes have a parasitic diode from AGND to their cathode that is omitted for clarity. These parasitic diodes have their anode at AGND.

Figure 2. ESD Diodes

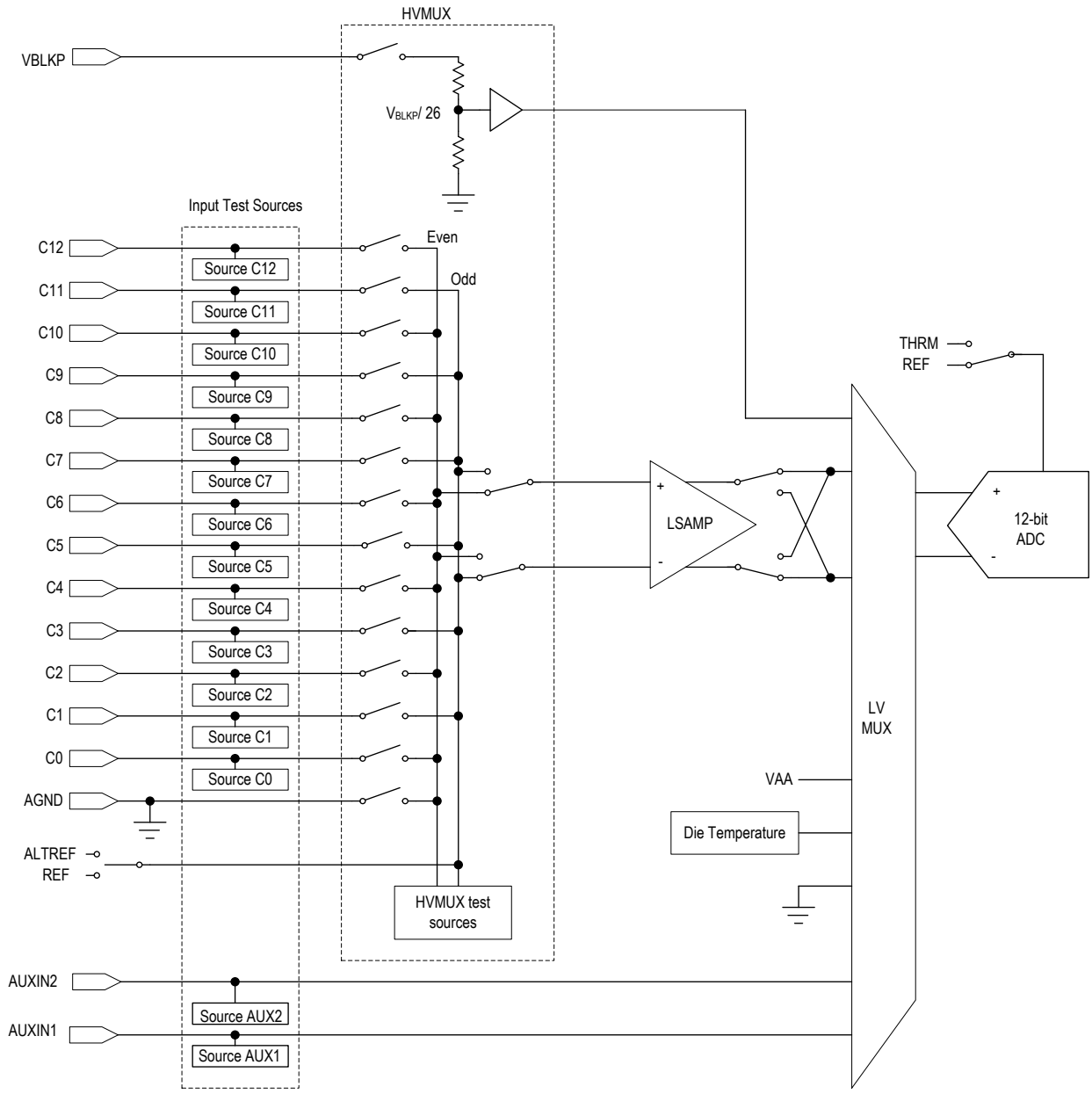


Figure 3. Analog Front-End

Data Conventions

Representation of data follows the conventions shown in Table 2. All registers are 16-bit words.

Table 2. Numeric Conventions

Description	Convention	Example
Binary number	0b prefix	0b01100001 = 61h
Hexadecimal address	0x prefix	0x61
Hexadecimal data	h suffix	61h
Register bit	Register name [x]	STATUS[15] = 1
Register field	Field name [x:y]	DA[4:0] = 0b01100 = 0Ch
Concatenated numbers	{xxxx, yyyy}	{DA[4:0], 0b001} = 61h

Data Acquisition

A data acquisition is composed of the distinct processes defined in Table 3 and controlled by various configuration registers described in this section. Configuration changes should be made prior to the acquisition in which the changes are to be effected.

Table 3. Data Acquisition Processes

Process	Description
Conversion	The ADC samples a single input channel, converts it into a 12-bit binary value, and stores it in an ALU register.
Scan	The ADC sequentially performs conversions on all enabled cell input channels.
Measurement cycle or Sample	The ADC performs two scans for the purpose of minimizing error. The conversions (two for each input channel) are averaged together to form a single 14-bit binary value called a measurement. **Note:** The auxiliary inputs are only scanned once to create the auxiliary measurements.
Acquisition or Acquisition mode	If oversampling is enabled, the ADC takes sequential measurements and averages them together to form one 14-bit binary value for each input channel sampled. If there is no oversampling, the acquisition is essentially a single measurement cycle. **Note:** The auxiliary inputs are never oversampled and are stored as 12-bit values.

Precision Internal Voltage References
The measurement system uses two precision, temperature-compensated voltage references. The references are completely internal to the device and do not require any external components. The primary voltage reference, or REF, is used to derive the linear regulator output voltage and to supply the ADC reference. An alternate, independent reference, ALTREF, may be used to verify the primary reference voltage as described in the Diagnostics section.

Measurement Calibration
The acquisition system is calibrated at the factory and cannot be changed afterwards. The calibration parameters are stored in a ROM consisting of 12 read-only registers, CAL0 – CAL10 and CAL15. ROMCRC[8:0] is an 8-bit CRC value based on the calibration ROM and is stored in ID2[15:8] at the factory. ROMCRC[8:0] may be used to check the integrity of the calibration as described in the Diagnostics section.

Cell Inputs

Up to 12 voltage measurements can be sampled differentially from the 13 cell inputs. The differential signal V_{CELLn} is defined as V_{Cn} - V_{Cn-1} for n = 1 to 12.

The cells to be measured are selected by MEASUREEN[11:0]. During the scan, each selected signal is multiplexed into the level-shifting amplifier (LSAMP) as shown in Figure 3. Since the common-mode range of the input signals is 0V to 65V, the signal must be level-shifted to the common-mode range of the amplifier. The amplifier has a gain of 6/13 so that a 5V differential signal will be attenuated to 2.307V which is the ADC reference voltage.

Once the signal is properly conditioned the ADC can start the conversion. The 12-bit conversion is stored in an ALU register where it can be averaged with subsequent conversions. The ALU output is a 14-bit value and is ultimately stored in a 16-bit register with the two least-significant bits zero. Disabled channels result in a measurement value of 0000h. Unless stated otherwise, measurement values are assumed to be 14-bit values. The 16-bit register values can be converted to 14-bit values by dividing by 4 (and vice-versa). To convert the measurement value in register CELLn to a voltage, convert the 14-bit hexadecimal value to a decimal value and then convert to voltage as follows: V_{CELLn} = CELLn[15:2] x 5V / 16384 = CELLn[15:2] x 305.176µV.

Input Range

The input range in unipolar mode is nominally 0V to 5V. However, the ADC has reduced linearity at its range extents and so accuracy is specified for the input range 0.2V to 4.8V. Some applications may require specified accuracy below 0.2V or even below 0V. To this end, the bipolar mode (POLARITY = 1) has a nominal input range of -2.5V to 2.5V as shown in Table 4 with accuracy specified from -2.3V to 2.3V.

Table 4. Input Range

Cell Input Voltage		CELLn[15:2] (14 Bits)		CELLn[15:0] (16 Bits)
Bipolar Mode	**Unipolar Mode**	**Hexadecimal**	**Decimal**	
-2.5V	0V	0000h	0d	0000h
0V	2.5V	2000h	8192d	8000h
2.5V	5V	3FFFh	16383d	FFFCh

The input range can effectively be extended from -2.5V to 5V by taking one bipolar measurement and one unipolar measurement. Any bipolar measurements over 2.3V should be replaced with the unipolar measurement.

Note: Conversions for some diagnostic modes automatically use either bipolar or unipolar mode regardless of the POLARITY bit value.

Block Voltage Input

The VBLKP input (total module voltage) is selected for measurement by MEASUREEN[14]. The measurement is stored in the VBLOCK register with a full-scale value of 60V (3.662mV / bit). It can be compared to the sum of the cell voltages as a diagnostic. To pre-condition V_{BLKP} for conversion it is voltage-divided by a factor of 26. The divider is disconnected by default to minimize power consumption. The divider is connected by setting MEASUREEN[15] (BLKCONNECT = 1) with sufficient settling time prior to the acquisition. For high acquisition rates, BLKCONNECT can remain enabled to reduce cycle time.

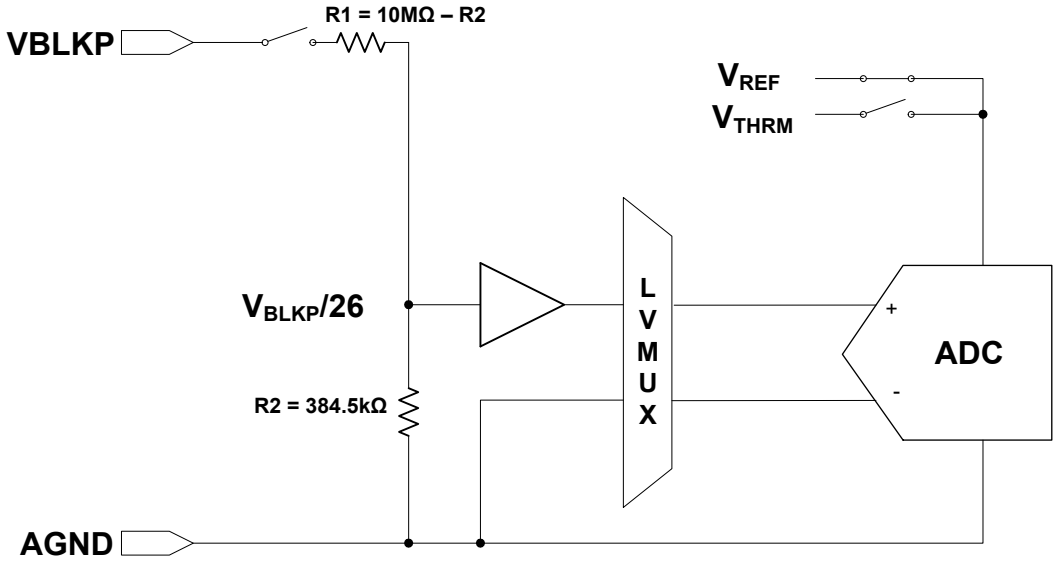


Figure 4. VBLKP Measurement

Auxiliary Inputs

The AUXIN1 and AUXIN2 inputs can be used to measure external temperatures by enabling MEASUREEN[13:12]. These inputs have a common-mode input range of 0V to V_{AA}. For these measurements, the ADC reference voltage is V_{THRM} which is switched from V_{AA} as shown in Figure 5. The auxiliary inputs are not oversampled even if oversampling is enabled; they are measured only once and stored as 12-bit values in the AIN1 and AIN2 registers.

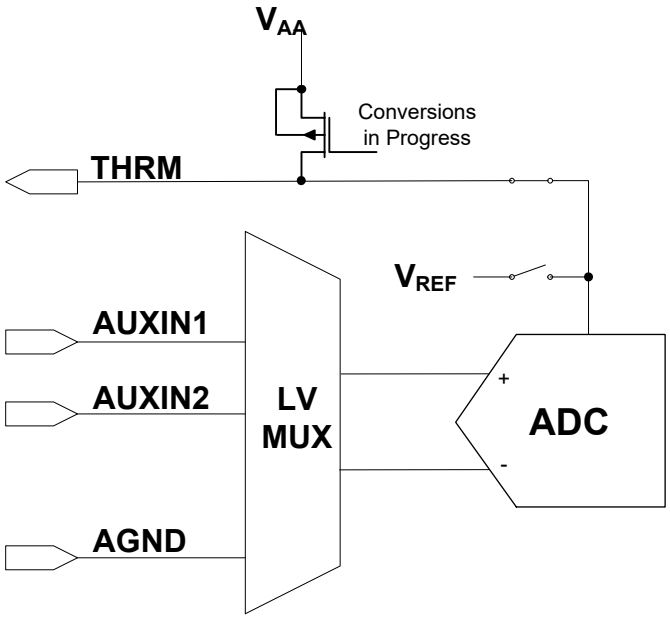


Figure 5. Auxiliary Measurement

To measure external temperature the auxiliary input is connected to a voltage divider consisting of a 10KΩ pull-up to THRM and a 10KΩ NTC thermistor to ground as shown in Figure 6.

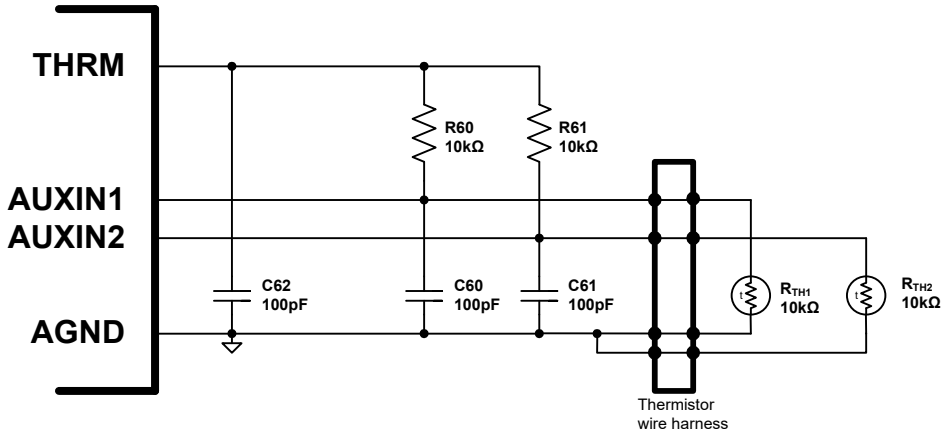


Figure 6. Auxiliary Application Circuit

THRM Output

The THRM output has 2 modes of operation, automatic and manual as shown in Table 5.

Table 5. THRM Output

Mode	ACQCFG[9:8]	Description
Automatic	00b	THRM output enabled at the beginning of the acquisition and disabled at the end of the acquisition.
	01b	
Manual	10b	THRM output is enabled
	11b	THRM output is disabled

The automatic mode minimizes power consumption, but after the THRM output is enabled, the AUXIN voltages must be allowed to settle before the conversion. Since the auxiliary inputs are the last inputs measured, the duration of the measurement cycle itself may provide sufficient settling time depending on what measurements are enabled and the time constants for the auxiliary input circuit. Up to 384µs of additional settling time, if required, can be configured by ACQCFG[5:0] as shown in Table 6 or by utilizing the manual mode. The ability to configure the settling time allows for a range of time constants to be considered in designing the auxiliary application circuit.

Table 6. AINTIME

ACQCFG[5:0] (AINTIME)	Additional Settling Time per Enabled Auxiliary Channel = 6µs + (AINTIME x 6µs)
00h	6µs
01h	12µs
02h	18µs
…	…
1Fh	384 µs

Computing Temperature

In Figure 6, $V_{AUXINn} = V_{THRM} \times R_{TH} / (10K\Omega + R_{TH})$ and this measurement is stored in the AINn register. The thermistor resistance can then be solved for as follows:

$$R_{TH} = (V_{THRM} \times 10K\Omega) / (V_{THRM} - V_{AUXINn}) \text{ where } V_{THRM} = 3.3V \text{ nominally}$$

The resistance of an NTC thermistor increases as the temperature decreases and is typically specified by its resistance R_0 at T_0 = +25°C = 298.15K and a material constant β (3400K typical). To the first order, the resistance R_{TH} is at a temperature T in Kelvin may be computed as follows:

$$R = R_0 e^{(\beta(1/T - 1/T_0))}$$

The temperature T of the thermistor (in °C) can then be calculated as follows:

$$T \text{ (in °C)} = (\beta / \ln((R_{TH} / 10K\Omega) + (\beta / 298.15K)) - 273.15K$$

Temperature Alerts

Auxiliary voltage measurements may be directly compared to pre-calculated voltages in the AINUT and AINOT registers that correspond to specific over- and under-temperature thresholds. When a measurement exceeds the AINUT or AINOT threshold level, the ALRTCOLD or ALRTHOT bits respectively are set in the STATUS register. An alert is cleared only by a new measurement that is within threshold.

Die Temperature Measurement

The die temperature measurement allows the host to compute the device temperature (T_{DIE}) as it relates to the acquisition accuracy and allows the device to automatically shut itself down when T_{DIE} > 145°C. The measurement employs a source whose voltage, V_{PTAT}, is proportional to absolute temperature (PTAT) as shown in Figure 7. The V_{PTAT} measurement is enabled by setting DIAGSEL[2:0] to 0b110 and the 14-bit measurement is stored in DIAG[15:2]. The die temperature measurement requires a settling time of 50us from the start of the measurement cycle until the diagnostic conversion. As long as 2 or more cell measurements are enabled, there will be sufficient settling time for this measurement. Refer to Figure 9 and Table 8 for a detailed view of this timing.

The PTAT voltage is computed as follows:

$$V_{PTAT} = (DIAG[15:2] / 16384d) \times V_{REF}$$

Where V_{REF} = 2.307V. The measured voltage may be converted into °C as follows:

$$T_{DIE} (in °C) = (V_{PTAT} / A_{V_PTAT}) + T_{OS_PTAT} - 273°C$$

Refer to the Electrical Characteristics Table for A_{V_PTAT} and T_{OS_PTAT} values.

Die Temperature Alert

The ALRTTEMP bit is updated at the end of each measurement cycle for which DIAGSEL[2:0] = 0b110. If ALRTTEMP is set, it signifies that $T_{DIE} > T_{ALRTTEMP}$ or that the diagnostic measurement did not have sufficient settling time (< 50µs) and therefore may not be accurate. If ALRTTEMP is set, the host should consider the possibility that the acquisition does not meet the expected accuracy specification, or that the die temperature measurement itself may be inaccurate due to insufficient settling time (< 2 cell measurements enabled).

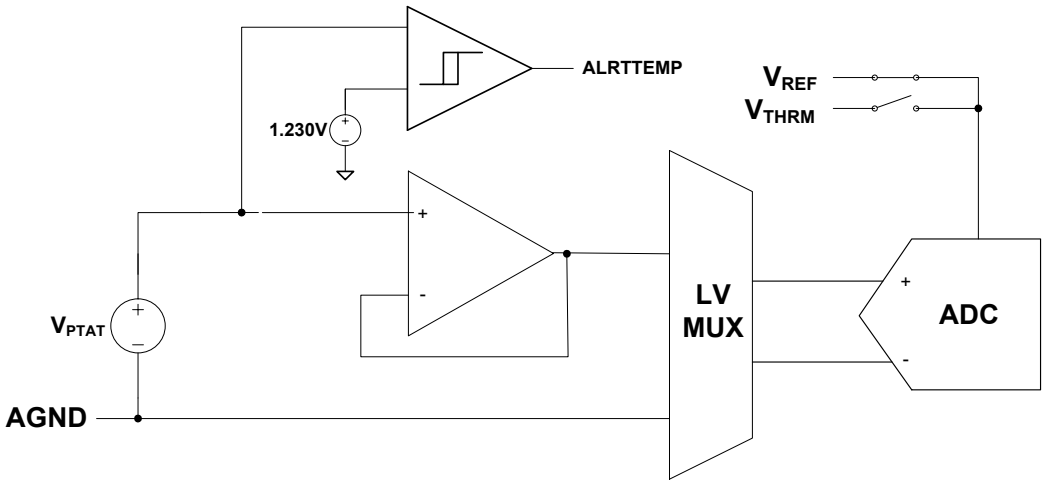


Figure 7. Die Temperature Measurement

Acquisition Mode

The host enters the acquisition mode by writing a logic one to the SCAN bit in the SCANCTRL register. This write is actually an automatic strobe of the bit since SCAN always reads logic zero. In daisy-chained devices, acquisitions in up-stack devices are delayed by the propagation delay, t_{PROP}, of the command packet through each device. The acquisition is complete when the device sets the SCANDONE bit. The basic acquisition process is outlined below with a detailed flowchart in Figure 8.

1. Disable HV charge pump
2. VBLKP conversion, if enabled
3. All enabled cell conversions (first)
    a. ascending order (1 through 12) if pyramid mode or
    b. descending order (12 through 1) if top-down mode
4. All enabled cell conversions (second)
    a. descending order (12 through 1)
5. VBLKP conversion (second), if enabled
6. Diagnostic conversion (first), if enabled
7. Diagnostic conversion (second) if enabled
8. Enable HV charge pump for recovery period unless
    a. OVSAMP[2:0] = 0 (no oversampling) or
    b. all oversample measurements are complete
9. Repeat steps 1 through 8 until all oversamples are done
10. All enabled auxiliary conversions, ascending order (AUXIN1, AUXIN2)
11. Set SCANDONE bit

Oversampling

Oversampling mode performs multiple measurement cycles in a single acquisition and averages the samples in the ALU to reduce the measurement noise and effectively increase the resolution of each measurement result. In oversampling mode, acquisition times are proportional to the number of oversamples as shown in Table 8. The number of oversamples can be configured from 4 to 128 by OVSAMPL[2:0] as shown in Table 7. The AUXIN measurements are never oversampled, even in oversampling mode.

To add n bits of measurement resolution requires at least 2^{2n} oversamples. Since the ADC resolution is 12 bits, 13-bit resolution requires at least 4 oversamples and to achieve the maximum 14-bit resolution requires at least 16 oversamples. Therefore with no oversampling, only the higher 12-bits of the measurement are statistically significant and with 4 or 8 oversamples, only the higher 13 bits are statistically significant. Taking more than 16 oversamples further reduces the measurement variation.

Of course with no oversampling, measurements can be averaged externally to achieve increased resolution but at a higher computational cost for the host.

Acquisition Watchdog Timeout

If the acquisition does not finish within a predetermined time interval, the SCANTIMEOUT bit is set, the ADC logic is reset, the ALU registers are cleared, and the measurement data registers are also cleared. In double-buffer mode (DBLBUF = 1), the data registers are not cleared, however, once data is moved from the ALU registers to the data registers, either automatically or manually (with the DATAMOVE bit), then data registers are cleared as a consequence of the ALU register having been cleared. The acquisition watchdog timeout interval depends on the oversampling configuration as shown in Table 7.

Table 7. Oversampling

OVSAMPL[2:0]	Oversamples	Theoretical Resolution	Acquisition Watchdog Timeout
000b (default)	0	12 bits	1.10ms
001b	4	13 bits	2.08ms
010b	8	13 bits	3.36ms
011b	16	14 bits	5.92ms
100b	32	14 bits	10.99ms
101b	64	14 bits	21.18ms
110b	128	14 bits	41.56ms
111b	128	14 bits	41.56ms

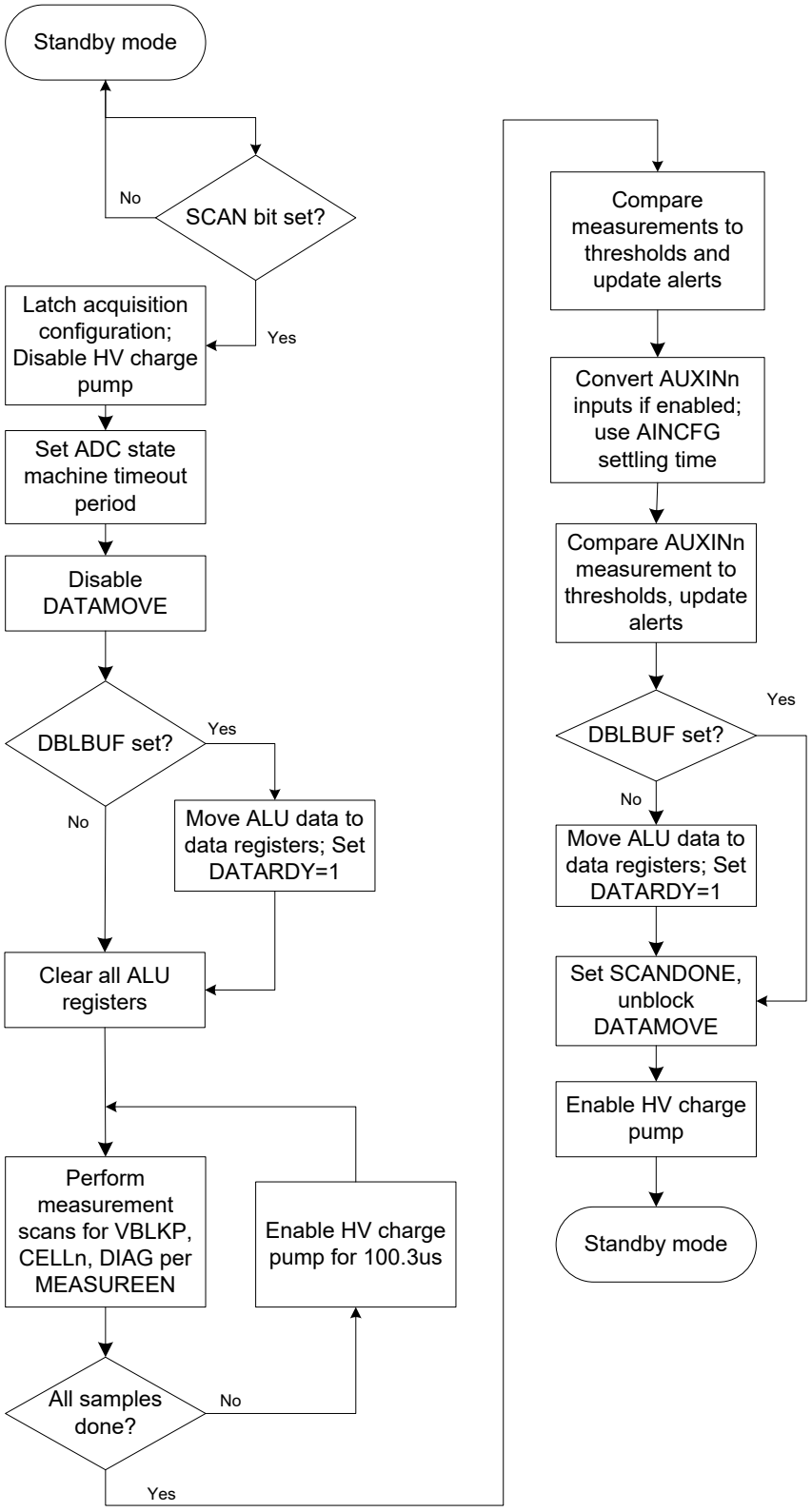


Figure 8. Acquisition Mode Flowchart

Scan Modes

The cell, block, and diagnostic measurement cycle consists of two conversion phases. In each phase, the ADC scans through the enabled input channels. There are two scan modes configured by the SCANMODE bit. If SCANMODE = 0, the mode is pyramid mode as shown in Figure 9. If SCANMODE = 1, the mode is top-down mode. In pyramid mode, the ADC scans first ascending and then descending. In top-down mode, the ADC scans descending in both phases. In the second scan, the amplifier inputs are inverted to effectively chop out any offset and reference-induced errors. The two conversions are then offset corrected and averaged in the ALU.

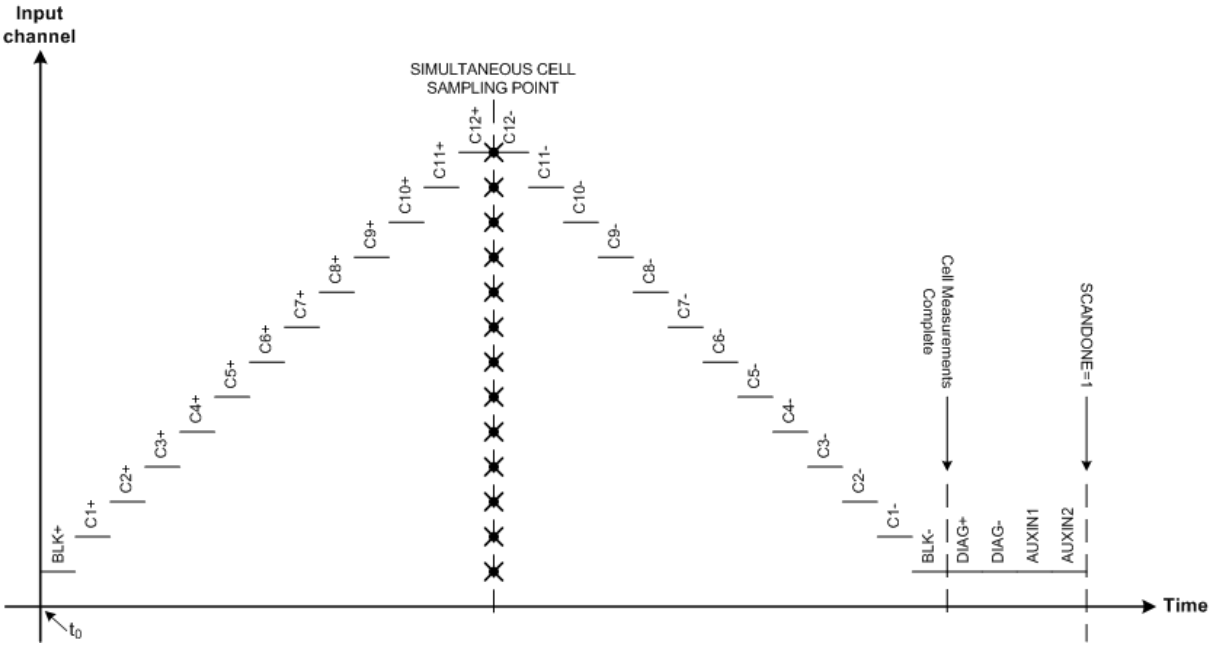


Figure 9. Acquisition, OVSAMP[2:0] = 0h and SCANMODE = 0

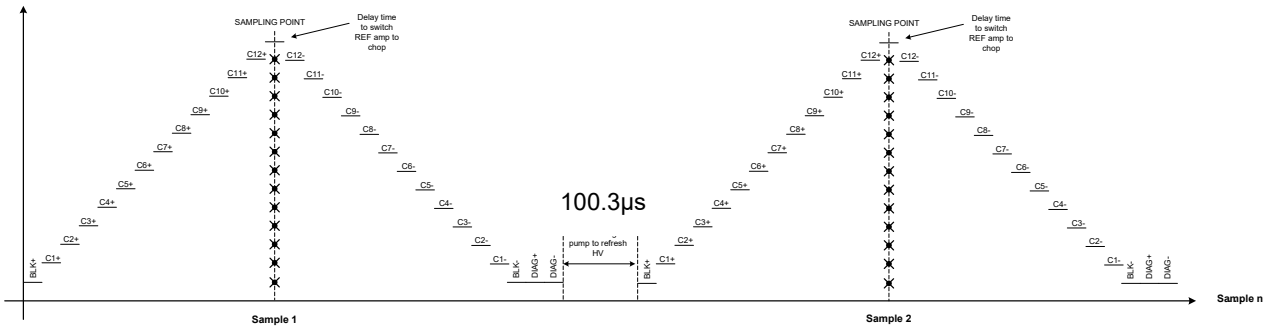


Figure 10. Acquisition, OVSAMP[2:0] > 0 and SCANMODE = 0

After the cell and block scans are complete, the diagnostic conversions are made, if enabled, and finally, the auxiliary inputs, if enabled, are converted. The auxiliary inputs are measured using a single conversion and stored in the AIN1 and AIN2 registers. Any extra settling time, if configured by AINCFG[5:0], is implemented just before the conversion for each AUXIN channel and so if both inputs are enabled, the extra settling time occurs twice.

Acquisition Time

The total acquisition time may calculated by summing all the required processes as shown in Tables 8 and 9. There is one measurement cycle per oversample.

Table 8. Acquisition Time

Process	Time (µs)	Condition	Frequency
Initialization	13	Always	Once per acquisition
VBLKP measurement	27	If VBLKP is enabled	Every measurement cycle
Cell scan setup	12.5	If cell input(s) enabled & VBLKP enabled	
	20	If cell input(s) enabled & VBLKP disabled	
Cell scans	9 x n	For n = # of enabled cell inputs	
Diagnostic measurement (if enabled)	11.4	If zero-scale ADC output diagnostic enabled	
	11.4	If full-scale ADC output diagnostic enabled	
	86.2	If V_{ALTREF} diagnostic enabled	
	22.9	If any other diagnostic mode enabled	
AUXIN measurement (if enabled)	10	If AUXIN1 is enabled	Once per acquisition
	6µs x AINCFG[5:0]		
	10	If AUXIN2 is enabled	
	6µs x AINCFG[5:0]		
HV recovery (if oversampling enabled)	100.3 x m	For m = # of oversamples	After every measurement cycle except last

Table 9. Acquisition Time Examples (with AINCFG[5:0] = 00h)

Enabled Measurements	No oversampling	4 oversamples	8 oversamples
12 cells	141.0µs	825.9µs	1739.1µs
12 cells, VBLKP	160.5µs	903.9µs	1895.1µs
12 cells, AUXIN1&2	161.0µs	845.9µs	1759.1µs
12 cells, VBLKP, AUXIN1&2	180.5µs	923.9µs	1915.1µs
12 cells, VBLKP, die temperature, AUXIN1&2	203.4µs	1015.5µs	2098.3µs

Measurement Data Transfer

By default, all ALU data is automatically transferred to the data registers (CELLn, VBLOCK, AIN1, AIN2, DIAG, MINMAXCELL and TOTAL) at the end of each acquisition. The transfer occurs in parallel, that is, all data registers are loaded at the same time. When this occurs, the DATARDY bit is set and the host can read out the data. In the simplest, sequential approach, the host will initiate the acquisition by setting SCAN, wait for the acquisition to complete (SCANDONE = 1), read the data registers, and then repeat the cycle.

Double-buffer Mode

The double-buffer mode (DBLBUFEN = 1) enables reduced cycle times by allowing the host to read out data registers during the acquisition mode. In this mode, the automatic transfer of measurement results from the ALU to the data registers is delayed until the start of the next acquisition. This delay allows the host to start reading out the first acquisition data while the second acquisition is taking place and to finish reading out the first acquisition even as the second acquisition completes. The host can then start a new acquisition and repeat the cycle. If the first acquisition data is needed before starting the second acquisition, the host can perform a manual data transfer by setting DATAMOVE. The manual transfer cannot occur in acquisition mode so the host may first verify that SCANDONE = 1. Flowcharts for operation of double-buffer mode are shown in Figures 12 and 13.

Note: An alternate double-buffer mode may be enabled (DBLBUFSEL = 1) that offers an even higher degree of pipelining but at the cost of increased complexity in the application code. Contact Maxim Applications for details regarding the alternate double-buffer mode.

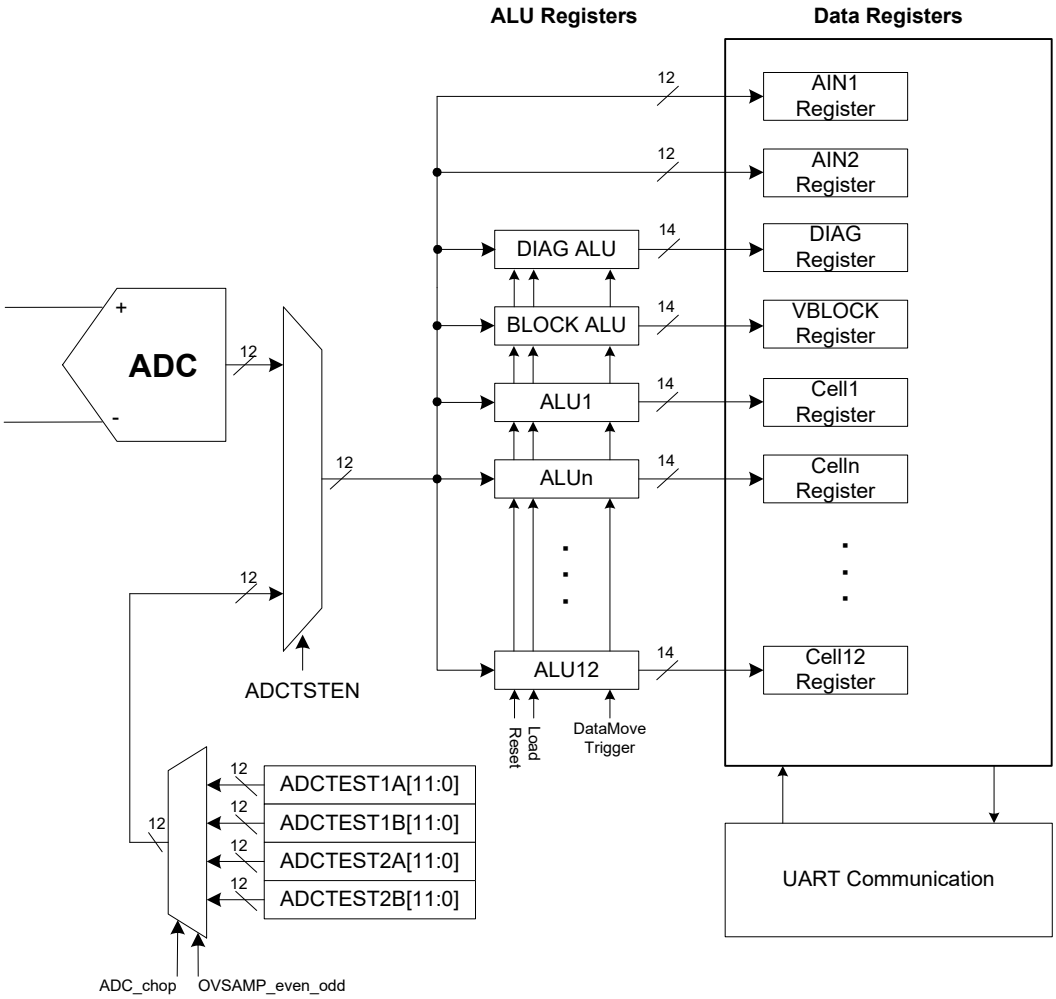


Figure 11. Measurement Data Flow

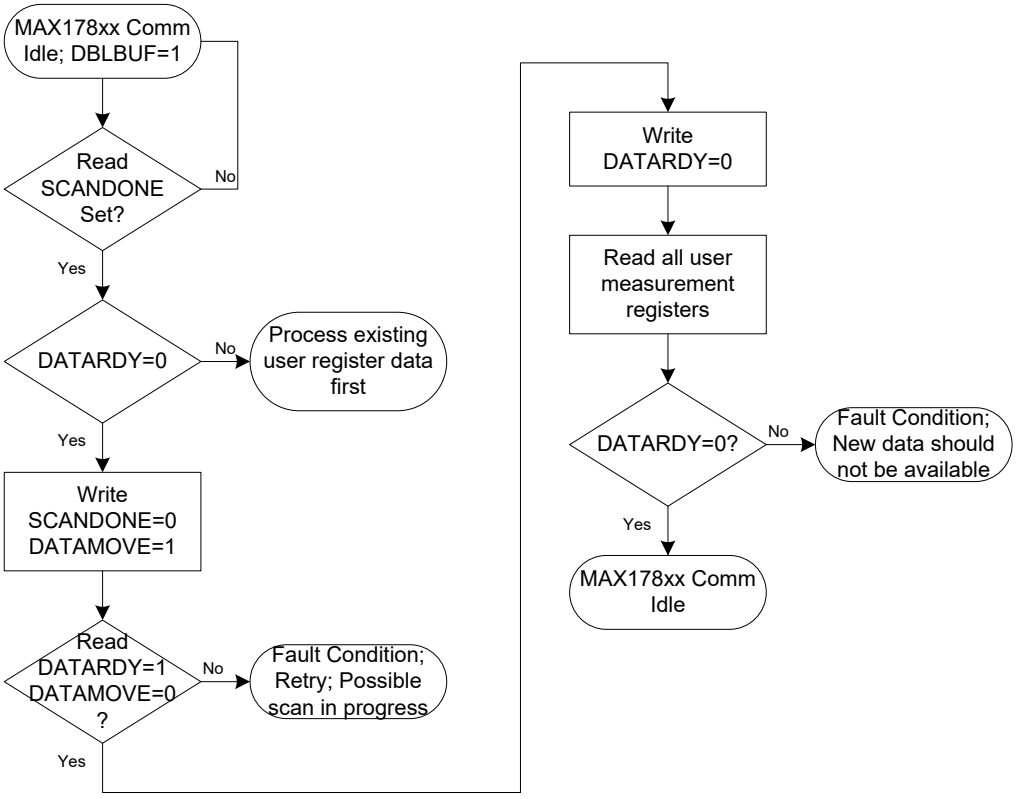


Figure 12. Double-Buffer Mode DATAMOVE

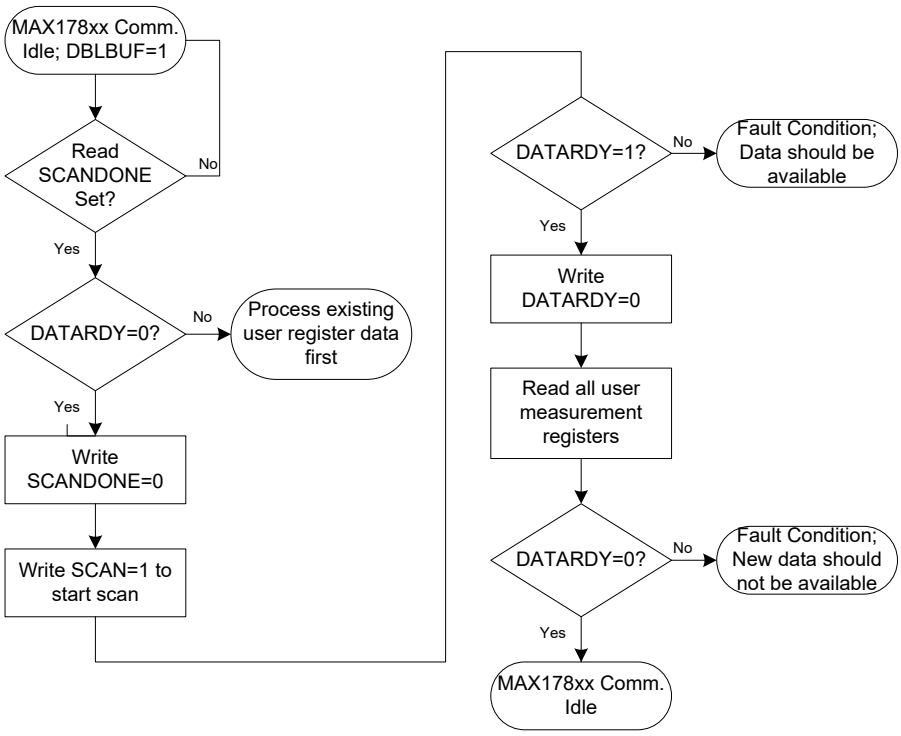


Figure 13. Double-Buffer Mode Register Read

Measurement Alerts

After the measurement cycle, the ALU compares the enabled measurements to the various configured thresholds as shown in Table 10 and sets the alert bits before the ALU data is transferred to the data registers. In oversampling mode, the alert status is updated after the last oversample. The alerts are updated whether or not the data is moved from the ALU registers to the data registers and are only updated for those measurements enabled in the MEASUREEN register.

Table 10. Measurement Alerts

Description	Condition or Result	Alert Bit	Location
Cell over-voltage (OV)	$V_{Cn} - V_{Cn-1} > V_{VOVTHSET}$	ALRTOV, ALRTOVn	STATUS, ALRTOVCELL
Cell under-voltage (UV)	$V_{Cn} - V_{Cn-1} < V_{UVTHSET}$	ALRTUV, ALRTUVn	STATUS, ALRTUVCELL
Cell Mismatch	$V_{MAX} - V_{MIN} > V_{MSMTCH}$	ALRTMSMTCH	STATUS
Cell with minimum voltage	n where $V_{CELLn} = V_{MIN}$	None	MINMAXCELL
Cell with maximum voltage	n where $V_{CELLn} = V_{MAX}$	None	MINMAXCELL
Total of all cell voltages	ΣV_{CELLn} for n = 1 to 12	None	TOTAL
AUXINx over-voltage (under-temperature)	$V_{AUXINx} > V_{AINUT}$	ALTRTCOLD, ALRTOVAINx	STATUS, ALRTOVCELL
AUXINx under-voltage (over-temperature)	$V_{AUXINx} < V_{AINOT}$	ALRTHOT, ALRTUVAINx	STATUS, ALRTUVCELL

Voltage Alerts

Use the ALRTOVEN and ALRTUVEN registers to enable voltage alerts for the cell and auxiliary inputs. If a cell voltage alert is enabled, the cell input voltage is compared against the programmable over-voltage and under-voltage thresholds after every acquisition as shown in Figure 14. Separate thresholds for setting the alert and for clearing the alert provide hysteresis. Configure the set thresholds for cell under-voltage ($V_{UVTHSET}$) and over-voltage ($V_{OVTHSET}$) using the OVTHSET and UVTHSET registers. Configure the clear thresholds for cell under-voltage ($V_{UVTHCLR}$) and cell over-voltage ($V_{OVTHCLR}$) using the OVTHCLR and UVTHCLR registers.

Alert flags in the ALRTOVCELL register are set, if enabled, when the acquired cell voltage is over $V_{OVTHSET}$. Alerts in

the ALRTUVCELL register are set, if enabled, when the acquired cell voltage is under $V_{UVTHSET}$. The alerts are cleared when the cell voltage moves in the opposite direction and crosses the clear threshold. The voltage must cross the threshold; if it is equal to a threshold, the alert flag does not change. Therefore, setting the over-voltage set threshold to full-scale, or setting the under-voltage set threshold to zero-scale, effectively disables voltage alerts.

The ALRTOV and ALRTUV bits in the STATUS register are set when *any* alert flag is set in the ALRTOVCELL or ALRTUVCELL registers respectively. ALRTCELL[n] is the logical OR of ALROVCELL[n] and ALRTUVCELL[n].

Cell Mismatch

Enable the mismatch alert to signal when the minimum and maximum cell voltages differ by more than a specified voltage. The MSMTCH register sets the 14-bit threshold (V_{MSMTCH}) for the mismatch alert, ALRTMSMTCH. Whenever V_{MAX} - V_{MIN} > V_{MSMTCH}, then ALRTMSMTCH = 1. The alert bit will be cleared when a new acquisition does not exceed the threshold condition. To disable the alert, write FFCH to the MSMTCH register (default value).

Cell Statistics

The cell numbers with the lowest and highest voltages are stored in the MINMAXCELL register. When multiple cells have the same minimum or same maximum voltage, only the highest cell position having that voltage is reported. The sum of all enabled cell voltages is stored in the TOTAL register as a 16-bit value. For acquisitions with no enabled cell inputs, the MINMAXCELL and TOTAL registers are not updated.

Temperature Alerts

Temperature alerts, if enabled, occur when the acquired AUXINx input voltages fall outside the thresholds configured by the AINOT and AINUT registers. Unlike the cell-voltage alerts, the temperature thresholds do not have the hysteresis afforded by separate set and clear thresholds.

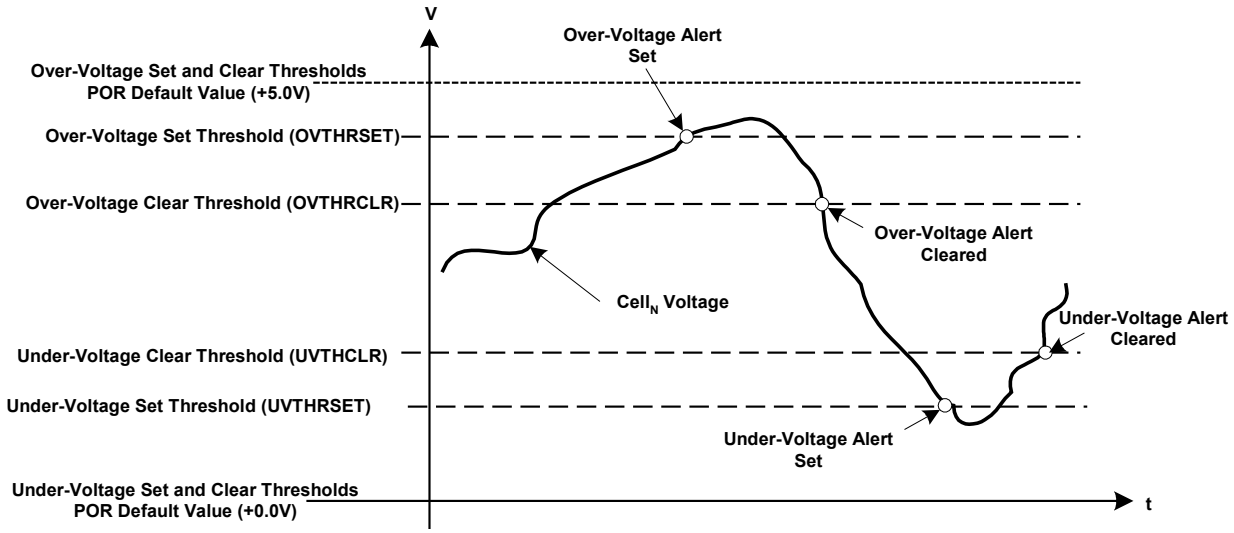


Figure 14. Cell Voltage Alert Thresholds

Cell Balancing

Cell-Balancing Switches

Cell balancing may be performed using any of the twelve internal cell-balancing switches to discharge cells. The cell-balancing current is limited by the external balancing resistors and the internal balancing switch resistance (R_{SW}). Enabling adjacent balancing switches simultaneously may increase the balancing current significantly so care must be taken to not exceed the device's maximum operating conditions. Fault detection is described in the Diagnostics section.

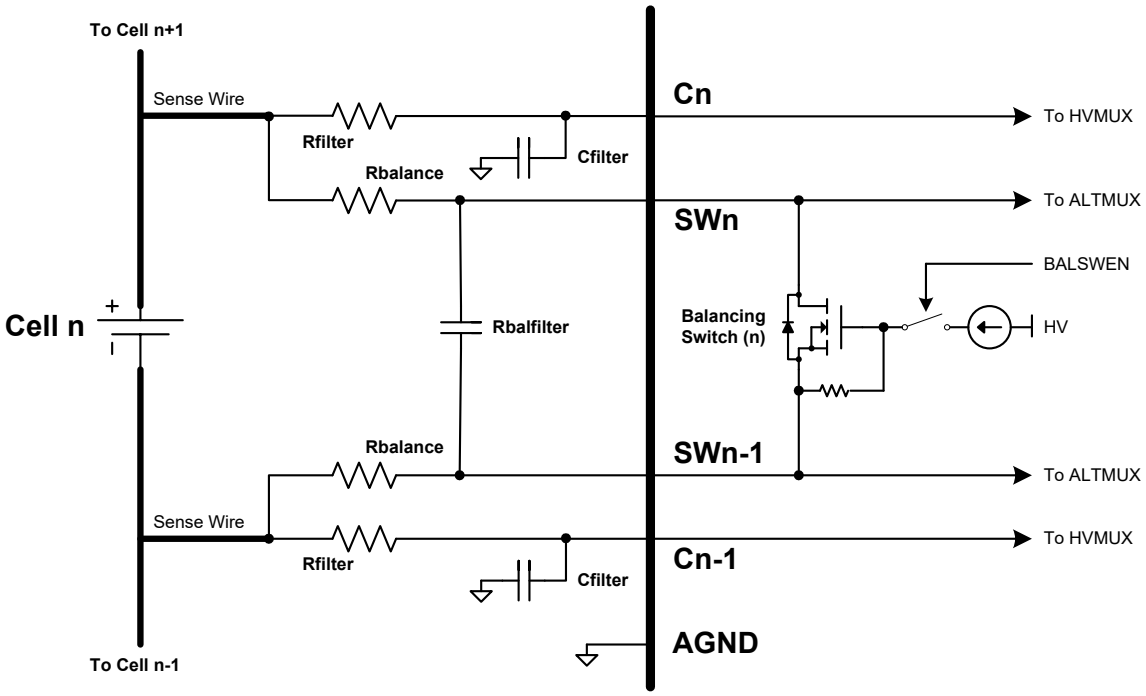


Figure 15. Internal Cell-Balancing

Maximum Cell-Balancing Current

The maximum balancing current is limited by package power dissipation, average die temperature, average duty-cycle of the switch, and the number of switches conducting current at any one time.

The power dissipation must not exceed the absolute maximum rating of the package nor should the die temperature go outside the range specified for the desired level of measurement accuracy. Higher die temperatures and higher average duty-cycles increase the probability of internal electromigration and so the maximum balancing current is lowered accordingly as shown in Table 11 for an assumed 10-year device lifetime.

Table 11. Maximum Allowed Balancing Current per Switch

Average Lifetime Duty-Cycle (10 years)	T_{DIE} = 85°C	T_{DIE} = 105°C	T_{DIE} = 125°C
15%	>320mA	>320mA	215mA
20%	>320mA	320mA	161mA
25%	>320mA	256mA	129mA

Cell-Balancing Watchdog

Even if the host fails to disable the cell-balancing mode, the cell-balancing watchdog can automatically disable the cell-balancing switches regardless of the BALSWEN configuration. The cell-balancing watchdog does not modify the contents of the BALSWEN register. Use the WATCHDOG register to configure the timeout value from 1s to 3840s (64min) as shown in Table 12. The pre-divider configuration CBPDIV[2:0] effectively sets the rate at which the CBTIMER[3:0] counts down as shown in Figure 16.

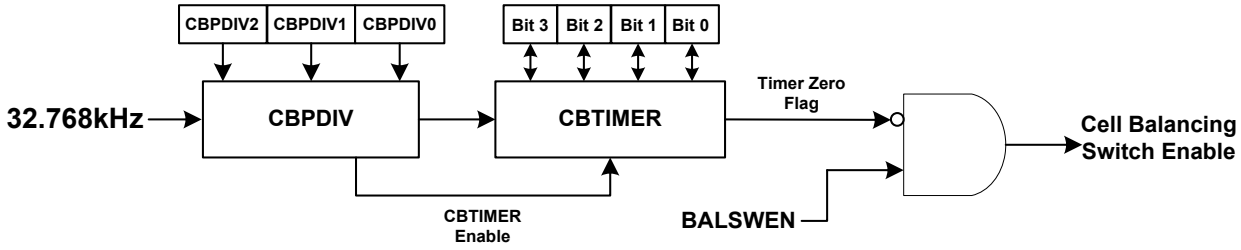


Figure 16. Cell-Balancing Watchdog

Table 12. Cell-Balancing Watchdog Configuration

CBPDIV[2:0]	Timer LSb Period	Range of CBTIMER[3:0]	
		Minimum	Maximum
000b	Timer Disabled	Timer Disabled	
001b	1s	1s	15s
010b	4s	4s	60s
011b	16s	16s	240s
100b	64s	64s	960s
101b	128s	128s	1920s
110b	256s	256s	3840s

The host should periodically update CBTIMER to ensure that it does not count down to zero. If countdown timer is allowed to reach zero, the cell balancing switches are disabled until the timer is either disabled or is refreshed by writing a non-zero value.

To allow timed balancing with no host interaction, the GPIO3 pin is configured to output a logic high level while the timer is counting using the GPIO3TMR configuration bit of the GPIO register. An external diode is connected from GPIO3 to SHDNL to prevent shutdown while the timer is counting. Once the timer expires, the device shuts down. The host may intervene prior to the timer expiring to keep the device active and to reconfigure the device.

Emergency Discharge Mode

The emergency discharge mode performs cell-balancing in a controlled manner so that the cells can be discharged to a safe level in the event of an emergency. The BALSWDCHG and DEVCFG2 registers provide control for this mode. A timeout value for the mode is configured by DISCHGTIME[7:0] as shown in Table 13.

The emergency discharge mode is activated by setting the EMGCYDCHG bit with DCHGTIME[7:0] ≠ 00h. In emergency discharge mode the following occurs:

1) The CBTIMER[3:0] is cleared to prevent the cell-balancing watchdog from disabling the cell-balancing.
2) Cell-balancing switches are controlled by BALSWDCHG, not BALSWEN.
3) The discharge timer starts to countdown.
4) The read-only counter DCHGCNTR[3:0] increments at a 2Hz rate with periodic roll-over at Fh. The host can read this counter periodically to confirm that the mode is active.
5) The GPIO3 pin is driven high while the countdown is active.

The emergency discharge mode alternates between a 1-minute discharge cycle for odd cells and a 1-minute discharge cycle for even cells. There is a 62.5ms minimum off time at the end of each discharge cycle to ensure no overlap between even and odd discharge cycles. The duty-cycle of each discharge cycle may be configured by DCHGWIN[2:0] as shown in the following table:

Table 13. Emergency Discharge Mode

Function	Register Field	Configuration	Behavior
Duty-cycle	DCHGWIN[2:0] 7.5s / bit	0h	Switches on for 7.5s, off for 52.5s
		1h	Switches on for 15s, off for 45s
		…	…
		7h	Switches on for 59.94s, off for 62.5ms
Time-out	DCHGTIME[7:0] 2 hours / bit	00h	Discharge mode disabled
		01h	Discharge mode disabled after 4 hours
		02h	Discharge mode disabled after 6 hours
		…	…
		FFh	Discharge mode disabled after 512 hours

By clearing EMGCYDCHG, the emergency discharge mode terminates and the following occurs:

1) The discharge timer is reset.
2) Control of the cell-balancing switches reverts to the BALSWEN register.
3) Control of GPIO3 reverts to the GPIO register.

The emergency discharge mode also terminates if DCHGTIME[7:0] = 0h or the discharge time has reached the configured timeout.

To prevent the emergency discharge mode from terminating prematurely due to a device shutdown (which could occur due to an extended lapse in host communications), connect an external diode from GPIO3 to SHDNL to keep SHDNL high while the timer is counting.

Low-Voltage Regulator

An internal linear regulator supplies low-voltage power (V_{AA}) for the ADC and digital logic. The regulator is disabled when SHDNL is active-low or when the die temperature (T_{DIE}) exceeds 145°C. Once V_{AA} decays below 2.95V typical, an internal power-on reset (POR) will be generated as shown in Figure 22. This event can be detected with the ALRTRST bit as shown in Table 15. After a thermal shutdown, the regulator will not be enabled until T_{DIE} < 130°C due to hysteresis.

Table 14. Low-Voltage Regulator

Input:	DCIN
Input Voltage:	9V to 65V
Output:	V_{AA}
Output Voltage:	3.3V
Disable:	V_{SHNDL} < 0.6V or T_{DIE} > 145°C

The low-voltage regulator is continuously monitored for under-voltage as described in Table 15.

Table 15. Low-Voltage Regulator Diagnostic

Fault	Condition	Alert	Location
V_{AA} under-voltage	V_{AA} < 2.95V	ALRTRST	STATUS[15]

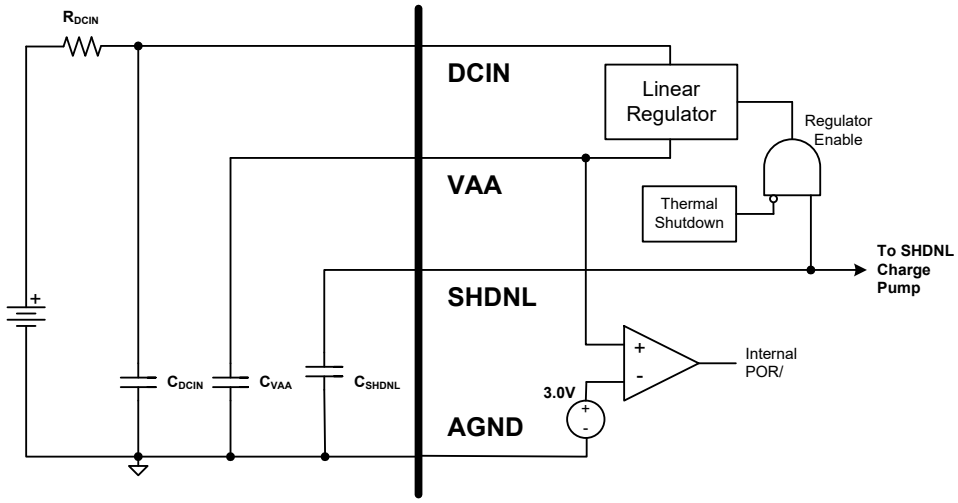


Figure 17. Low-Voltage Regulator

HV Charge Pump

The high-voltage multiplexers must be powered by a supply higher than any monitored voltage. To this end, an internal charge pump draws power from the DCIN input to provide a high-voltage supply V_{HV} which is regulated to V_{DCIN} + 5.5V (nominal). When the charge pump achieves regulation, charge pumping stops until the voltage drops by 20mV. The charge pump is automatically disabled during shutdown and during the measurement cycle to eliminate charge pump noise. The charge pump can also be disabled manually by setting the HVCPDIS bit in the DEVCFG2 register.

If V_{HV} - V_{DCIN} drops below V_{HVUV}, the HV under-voltage flag (ALRTHVUV) is set. If V_{HV} drops too low relative to the C12 input, there is insufficient headroom to guarantee that the HVMUX switch resistance is sufficiently low for an accurate acquisition of the channel. To properly identify this fault condition, if V_{HV} – V_{C12} is too low during the acquisition, the HV headroom alert flag (ALRTHVHDRM) is set in the FMEA2 register. The HV under-voltage and HV headroom alert functions can be verified by disabling the HV charge pump (HVCPDIS = 1) and allowing V_{HV} to decay while in acquisition mode. An overvoltage comparator disables the charge pump in the case where V_{HV} – V_{DCIN} exceeds 8.5V. This condition is indicated by the ALRTHVOV bit in the FMEA2 register. The ALRTHVOV alert does not necessarily indicate a condition that affects measurement accuracy. HV charge pump diagnostics are summarized in Table 16.

Table 16. HV Charge Pump Diagnostics

Fault	Condition	Alert Bit	Location
V_{HV} under-voltage	V_{HV} - V_{DCIN} < V_{HVUV}	ALRTHVUV	FMEA1[3]
V_{HV} over-voltage	V_{HV} - V_{DCIN} > V_{HVOV}	ALRTHVOV	FMEA2[0]
V_{HV} low headroom	V_{HV} - V_{C12} < V_{HVHDRM} (min.)	ALRTHVHDRM	FMEA2[2]

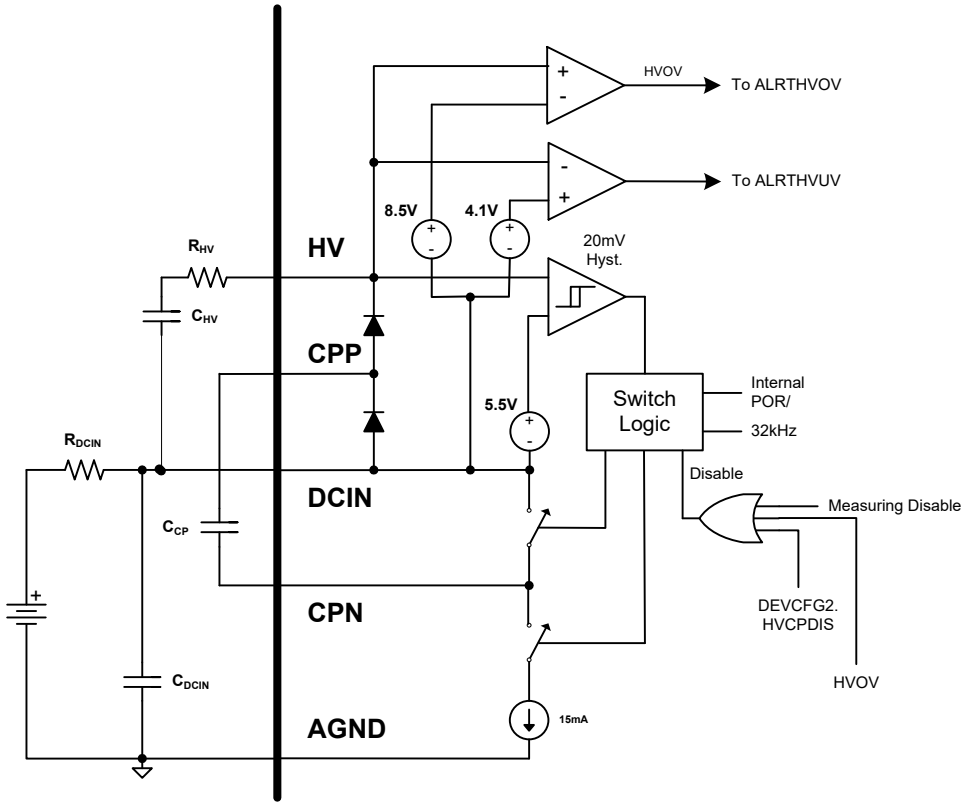


Figure 18. HV Charge Pump

Oscillators

Two factory- trimmed oscillators provide all timing requirements: a 16MHz oscillator for the UART and control logic and a 32.768kHz oscillator for HV charge pump and timers. A special diagnostic counter clocked by the 16MHz signal is employed to check the 32kHz oscillator. Every two periods of the 32kHz clock, the counter is sampled. If the count varies more than 5% from the expected value the ALRTOSC1 bit is set as shown in Table 17. A redundant alert bit, ALRTOSC2, increases the integrity level. If the 16MHz oscillator varies by more than 5%, communication errors will be indicated

Table 17. Oscillator Diagnostics

Fault	Condition	Alert Bit	Location
32.768kHz oscillator	31.129kHz > f_{osc_32k} > 34.406kHz	ALRTOSC1	FMEA1[15]
32.768kHz oscillator	31.129kHz > f_{osc_32k} > 34.406kHz	ALRTOSC2	FMEA1[14]
16MHz oscillator	15MHz > f_{osc_32k} > 17MHz	ALRTMAN or ALRTPAR	STATUS[4], or STATUS[2]

Device ID Number

The ID1[15:0] register together with ID2[7:0] contain a 24-bit manufacturing identification number, DEVID[23:0]. The ID combined with the manufacturing date provides a means of uniquely identifying each device. A device ID of zero is invalid.

POWER-ON AND SHUTDOWN

Applications that remain connected continuously to the power source rely on the SHDNL input to shut down and reset the device. When V_{SHDNL} < 0.6V, the regulator is disabled, the POR signal is asserted, and the device goes into an ultra-low-power shutdown mode. When V_{SHDNL} > 1.8V, POR is deasserted, the regulator is enabled, and the device becomes fully operational in the standby mode.

Power-On Method

The SHNDL input may be driven externally or it may be controlled using UART communication only. In differential mode, the signaling on the lower port receiver drives an internal charge pump that will charge up the external 1nF capacitor connected to the SHDNL input as shown in Figure 19. V_{SHDNL} reaches 1.8V in 200µs typical. The charge pump then self-regulates to $V_{SHDNLIMIT}$ and can maintain V_{SHDNL} at a logic one even with the UART idle 98% of the time.

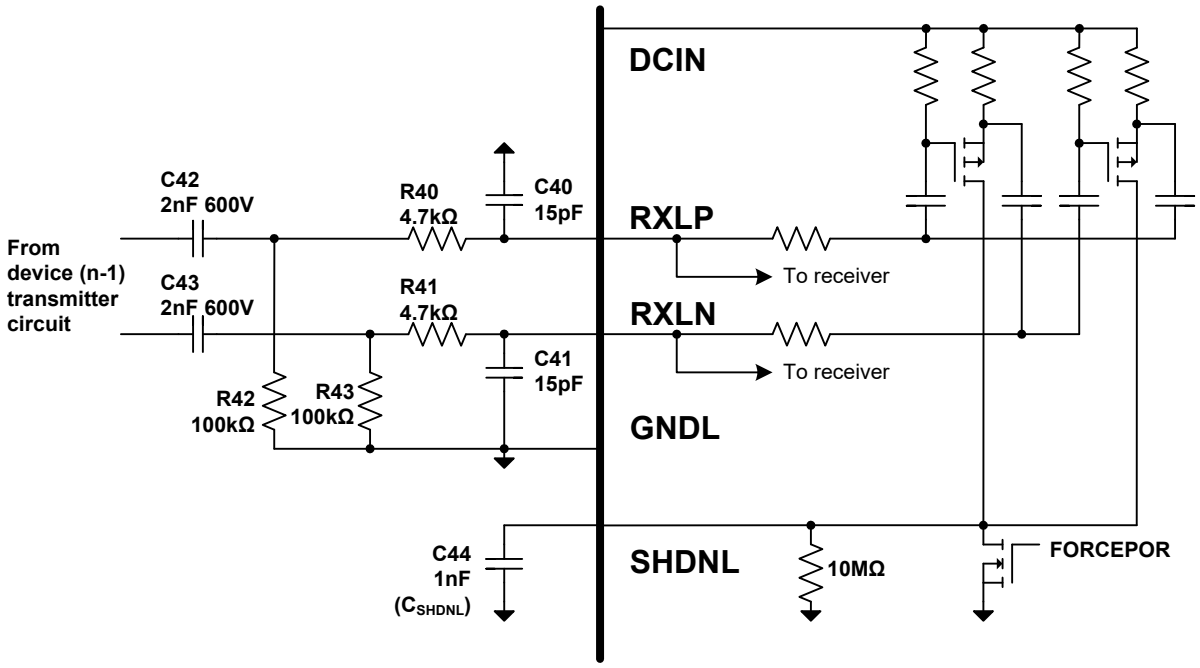


Figure 19. SHDNL Charge Pump

Power-On Sequence

Once V_{SHNDL} > 1.8V, the regulator is enabled. After V_{AA} reaches 3V typical, the POR signal is de-asserted, the oscillators are enabled, and the HV charge pump is enabled. Once the HV charge-pump is stable, the logic is enabled. The device is fully operational (standby mode) within 1ms from the time communication is first received in the shutdown mode. The power-on sequence is shown in Figure 20.

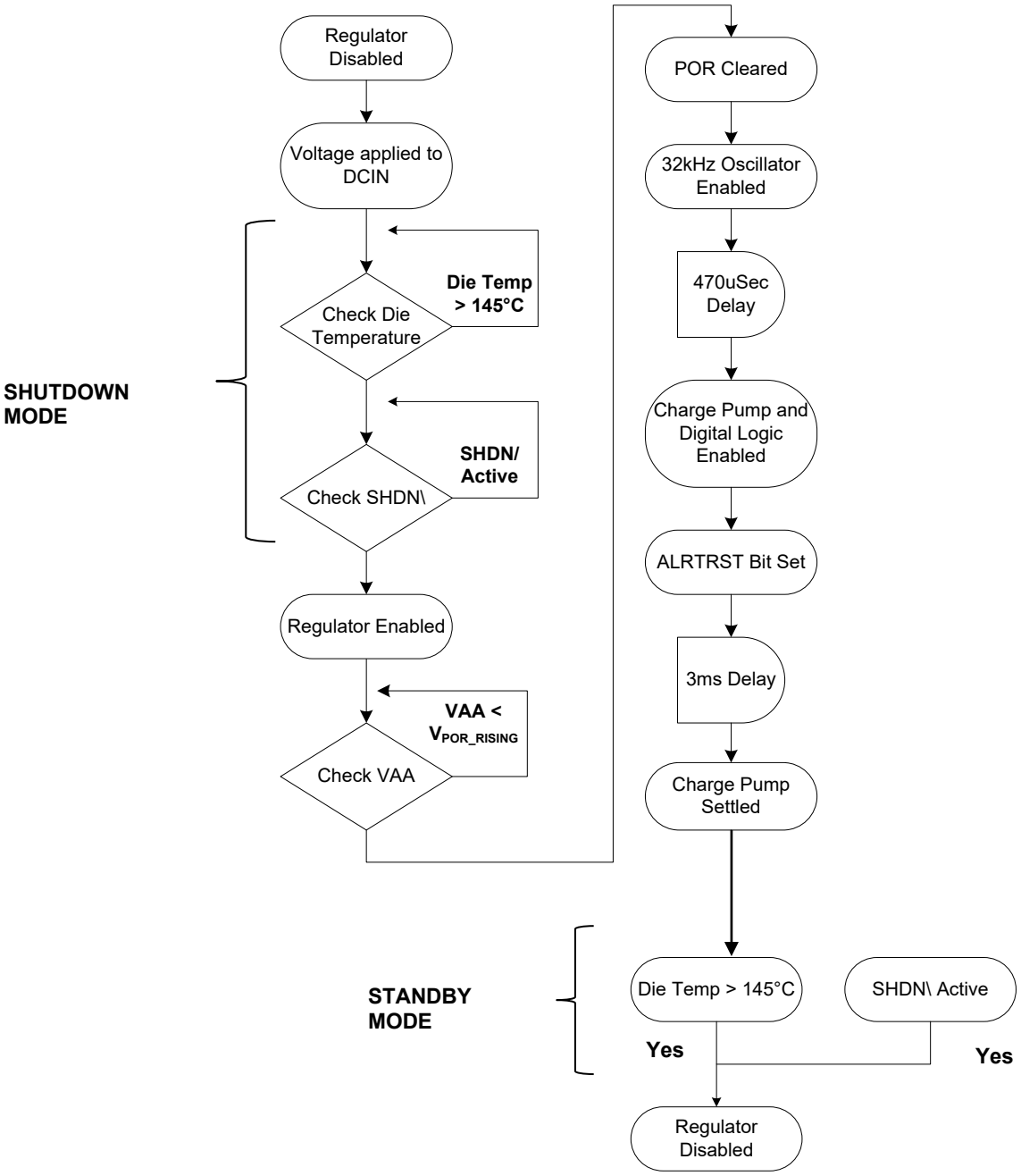


Figure 20. Power-On Sequence

Shutdown Mode
Shutdown is performed by bringing V_{SHDNL} < 0.6V. Table 18 summarizes the methods by which this can be achieved.

Table 18. Shutdown Timing

Shutdown Method	$R_{PULLDOWN}$		C_{SHDNL}	RC
1. Host drives SHDNL pin low	1kΩ	External	1nF	1µs
2. Host sets FORCEPOR bit	5kΩ	Internal		5µs
3. Disconnect DCIN	200kΩ	External		200µs
4. Host places UART in idle mode	10MΩ	Internal		10,000µs

The quickest shutdown can be achieved by driving SHDNL externally with a driver pull-down impedance not exceeding 1kΩ. If SHDNL is not driven externally, the host can discharge C_{SHDNL} under software control by setting the FORCEPOR bit. This will enable a pull-down (4.7kΩ nominal) to discharge the capacitor with a 4.7µs time constant.

The slowest method is for the host to simply cease communication. With the UART idle, there is no charge pumping and the capacitor discharges through an internal 10MΩ resistor with a 10ms time constant. If shutdown faster than 10ms is desired when power is disconnected from the device, a 200kΩ resistor may be connected externally from SHDNL to AGND to create a 200µs time constant.

If only a reset is required, the host can issue a soft reset by setting the SPOR bit. This will reset the device registers and disable high-voltage operation but low-voltage operation remains enabled (the regulator is not disabled).

Note: For single-ended communication, SHDNL must be driven externally since the charge pump operation requires a differential signal.

Shutdown Sequence
The shutdown sequence and timing is shown in Figures 21–23. The ALRTSHDNL status bit will be set and the low-voltage regulator is disabled as soon as V_{SHNDL} < 0.6V. When the V_{AA} and V_{DDL} decoupling capacitors discharge below the POR threshold (2.95V typical) then the device registers are reset and the HV charge pump is disabled. The device is then in an ultra-low-power state until V_{SHDNL} > 1.8V.

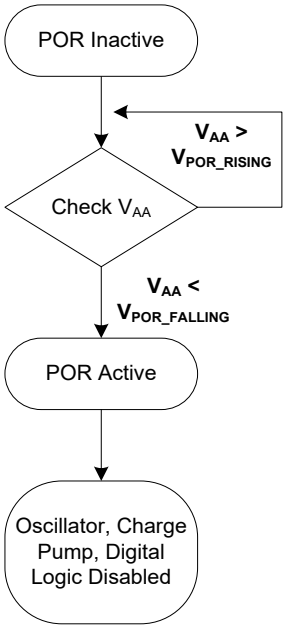


Figure 21. Shutdown Sequence

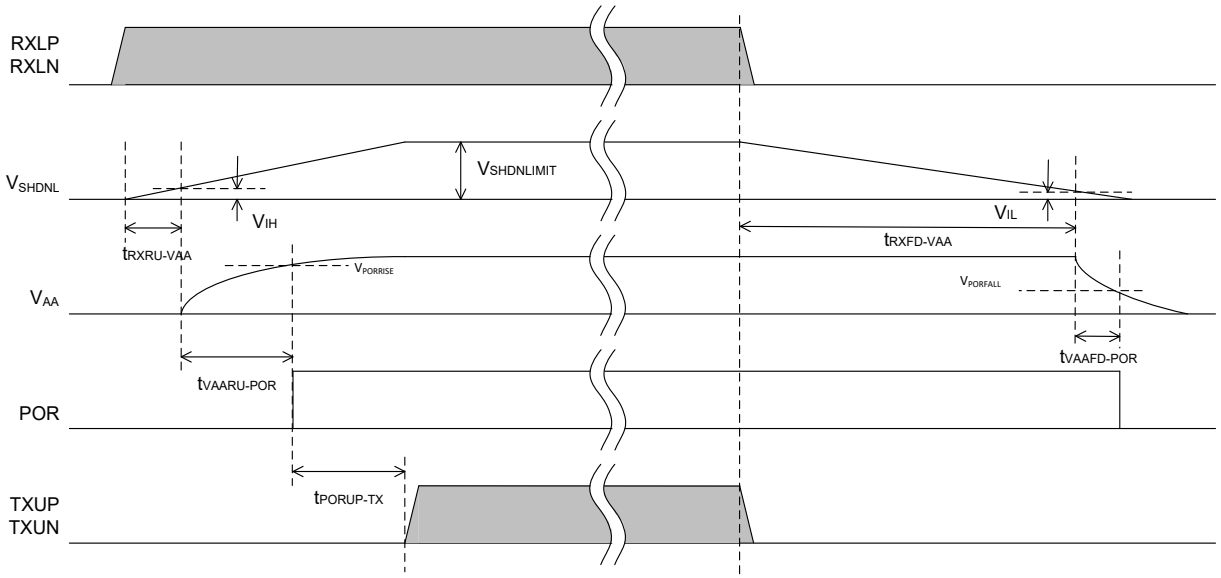


Figure 22. Power-On and Shutdown Timing – UART Control

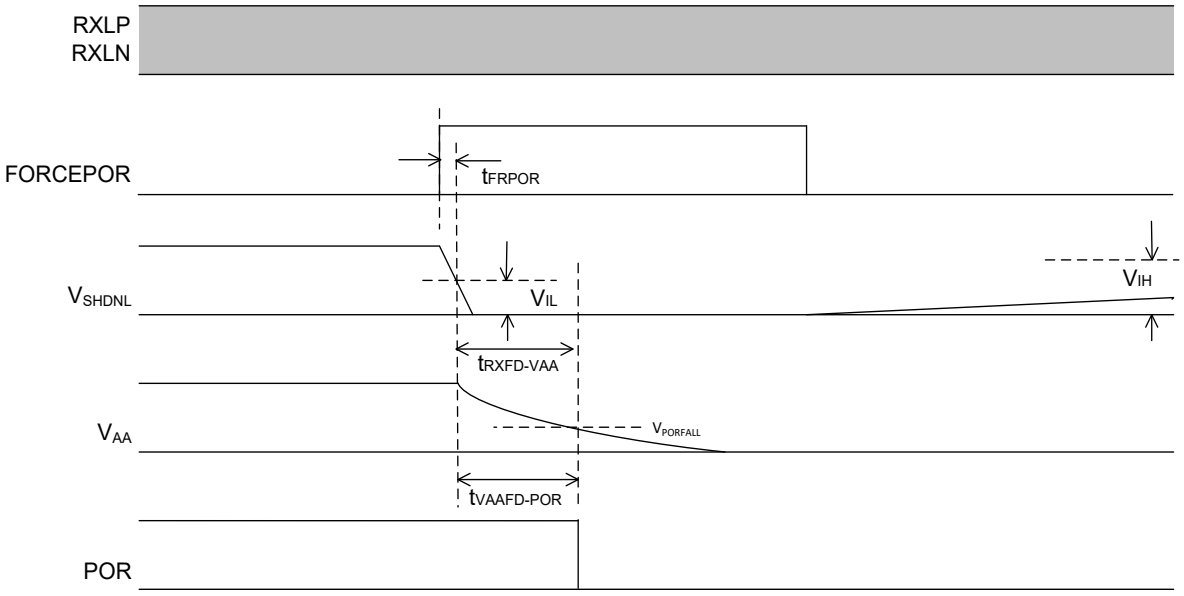


Figure 23. Shutdown Timing - Software Control

UART INTERFACE

The battery-management UART protocol allows up to 32 devices to be connected in daisy-chain fashion as shown in Figure 24. The host initiates all communication with the daisy-chain devices via a UART interface such as the MAX17841B. The data flow is always unidirectional from the host, up the daisy-chain (up-stack) and then loops back down the daisy-chain (down-stack) to the host as shown in Figure 24.

Each device first receives data at its lower RX port and immediately re-transmits data from its upper TX port to the lower RX port of the next up-stack device. The last device transmits data from its upper TX port directly into its upper RX port and then immediately re-transmits the data from its lower TX port to the upper RX port of the next down-stack device. The protocol supports fixed baud rates of 2Mb/s, 1Mb/s, or 0.5Mb/s. The baud rate is set by the host and is automatically detected by the device.

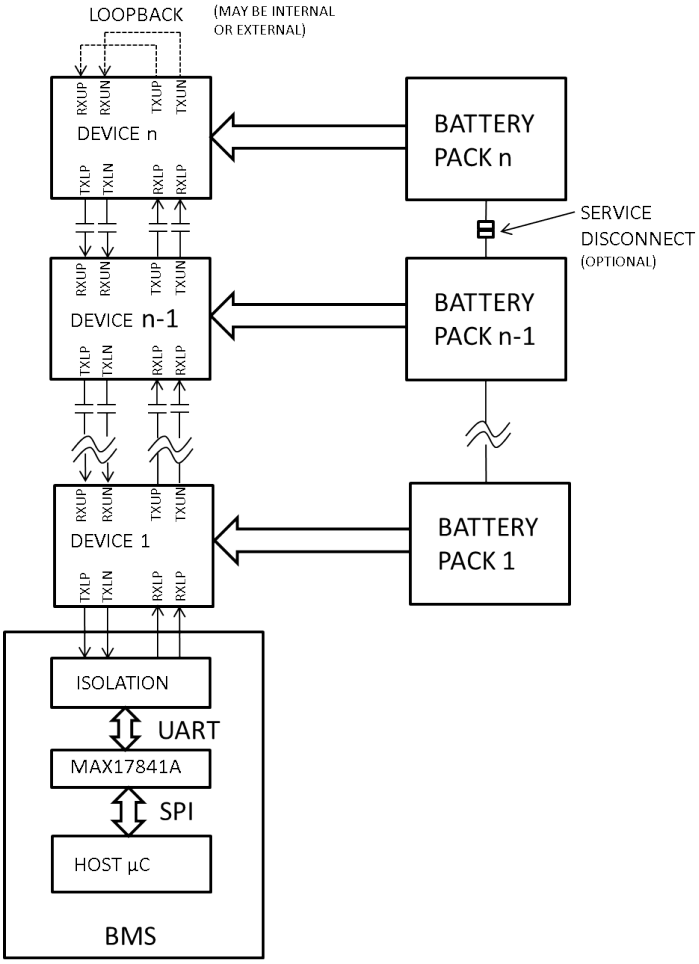


Figure 24. UART Interface

UART Ports

Two UART ports are utilized, a lower port (RXL/TXL) and an upper port (RXU/TXU). Each port consists of a differential line driver and differential line receiver. DC-blocking capacitors or transformers may be used to isolate daisy-chain devices that are operating at different common-mode voltages. During communication, the character encoding provides a balanced signal (50% duty-cycle) that ensures charge neutrality on the isolation capacitors.

UART Transmitter

When no data is being transmitted by the UART, the differential outputs must be driven to a common level to maintain a neutral charge difference between the AC-coupling capacitors or to avoid saturation of the isolation transformers. In the default idle mode (low-Z), the transmitter drives both outputs to a logic-low level to balance the charge on the capacitors and this also works well with transformer coupling. The high-Z idle mode (TXLHIZIDLE, TXUHIZIDLE = 1) places the TX pins in a high-Z state in idle mode which may be desirable to minimize the effects of charging and discharging the isolation capacitors. The idle mode for the upper and lower ports may be controlled independently via the TXLHIZIDLE and TXUHIZIDLE configuration bits.

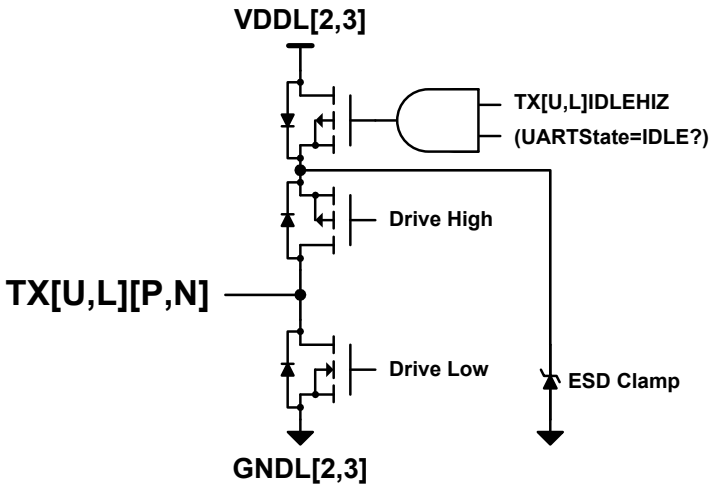


Figure 25. UART Transmitter

UART Receiver

The UART receiver has a wide common-mode input range to tolerate harsh EMC conditions. It can be operated in differential mode or single-ended mode per Table 19. By default, the UART receivers are configured for differential mode. In single-ended mode, the RXP input is grounded and the RXN input receives inverse data as described in the Applications section (Figure 64). In single-ended mode, the receiver input threshold is negative so that a zero differential voltage (V_{RXP}, V_{RXN} = 0V) is considered to be a logic one and a negative differential voltage (V_{RXN} high) is a logic zero.

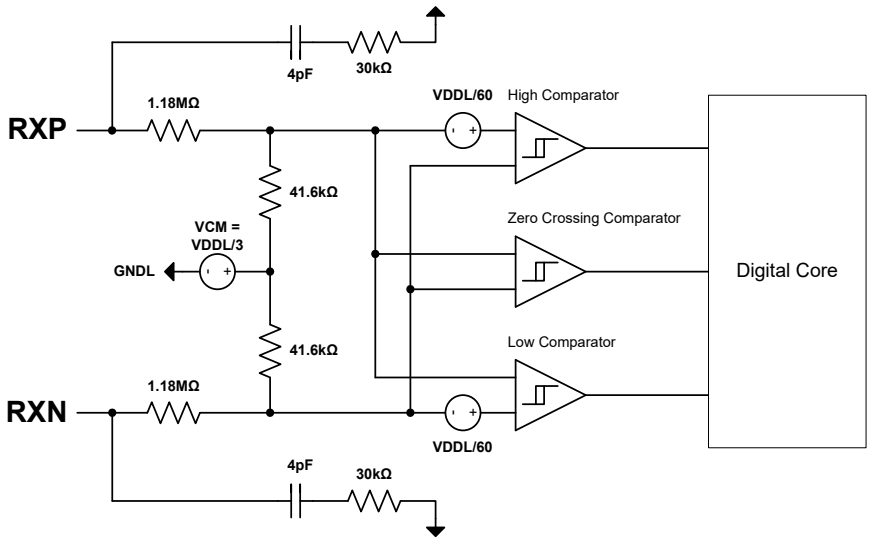


Figure 26. UART Receiver

UART RX Modes

During the first preamble received after a reset, the receiver automatically detects if the received signal is single-ended and if so, places the receiver in single-ended mode. Therefore the device must be reset for any change in the RX-mode hardware configuration to be detected.

The receiver mode is indicated by the ALRTCOMMSEL bit (for lower port) and ALRTCOMMSEU bit (for upper port) of the FMEA1 register as shown in Table 19. If the RXP input is open-circuit, the RX-mode detection will place the UART in single-ended mode so that the port can still operate albeit with reduced noise immunity. The host can diagnose this condition by checking ALRTCOMMSEL and ALRTCOMMSEU after any POR event. Any other faults result in communication errors.

Table 19. UART RX Modes

RXP	RXN	ALRTCOMMSEn	RX Mode
connected to data	connected to inverse data	0	Differential Mode (normal)
grounded	connected to inverse data	1	Single-Ended Mode (normal)
open-circuit (fault)	connected to inverse data	1	Single-Ended Mode (low noise immunity)
connected to data	open-circuit (fault)	0	Differential Mode (communication errors)

UART Loopback
For the last device in the stack, the data must be looped back from the upper transmitter to the upper receiver. This is known as loopback and can be configured externally (default) or internally.

External Loopback Mode
External loopback mode (default) uses a two-wire cable to connect the upper transmitter (TXU) to the upper receiver (RXU). The external loopback has two advantages: 1) it is quicker to determine device count for applications where the host does not assume what the device count is and 2) it helps to match the supply current of the last device to that of the other daisy-chain devices (because the hardware configuration is identical).

Internal Loopback Mode
Internal loopback mode (LASTLOOP = 1) routes the upper port transmit data internally to the upper port receiver. Any signal present on the upper port receiver input pins is ignored in the internal loopback mode, therefore when LASTLOOP is set, the write command that was forwarded to any up-stack devices will be interrupted in the down-stack direction. The host should expect this and read the LASTLOOP bit to verify that the write was successful. If the MAX17841B interface is used, its receive buffer should be cleared before changing LASTLOOP, and cleared again after changing the loopback configuration because the communication was interrupted.

Internal loopback mode is useful to diagnose the location of a daisy-chain signal break by enabling the internal loopback mode on the first device, checking communication, then moving the loopback mode to the next device, and continuing up the stack until communication is lost.

Baud Rate Detection
The UART may operate at a baud rate of 2Mb/s (default), 1Mb/s, or 0.5Mb/s. The baud rate is controlled by the host and is automatically detected by the device when the first preamble character is received after reset. If the host changes the baud rate after reset, it must issue another reset (which may be done by setting the SPOR bit) and resend a minimum of 2 x *n* preambles (where *n* is number of devices). The 2 x *n* preambles are necessary since the transmitter for the upper port will not transmit data until the lower port receiver has detected the baud rate and likewise, the transmitter on the lower port will not transmit data until the upper port receiver has detected the baud rate. A simple way to do this is for the host to start transmitting preambles and stop when a preamble has been received back at the host RX port.

Battery Management UART Protocol

The Battery-Management UART Protocol uses the following features to maximize the integrity of the communications:

- All transmitted data bytes are Manchester-encoded where each data bit is transmitted twice with the second bit inverted (G.E. Thomas convention).
- Every transmitted character contains 12 bits which include a start bit, a parity bit, and two stop bits.
- Read/write packets contain a CRC-8 Packet Error Checking (PEC) byte
- Each packet is framed by a preamble character and stop character.
- Read packets contains a data-check byte for verifying the integrity of the transmission.

The protocol is also designed to minimize power-consumption by allowing slave devices to shut down if the UART is idle for a specified period of time. The host must periodically transmit data to prevent shutdown unless the SHDNL input is driven externally.

Command Packet

A command packet is defined as a sequence of UART characters originating at the host. Each packet starts with a preamble character, followed by data characters, and ending with a stop character as shown in Figure 27. After sending a packet, the host either goes into idle mode or sends another packet.

Figure 27. Command Packet

Preamble Character

The preamble is a framing character that signals the beginning of a command packet. It is transmitted as an un-encoded 15h with a logic one parity bit and a balanced duty-cycle. If any bit(s) other than the stop bits deviate from the unique preamble sequence, then the character is not interpreted as a valid preamble, but rather as a data character.

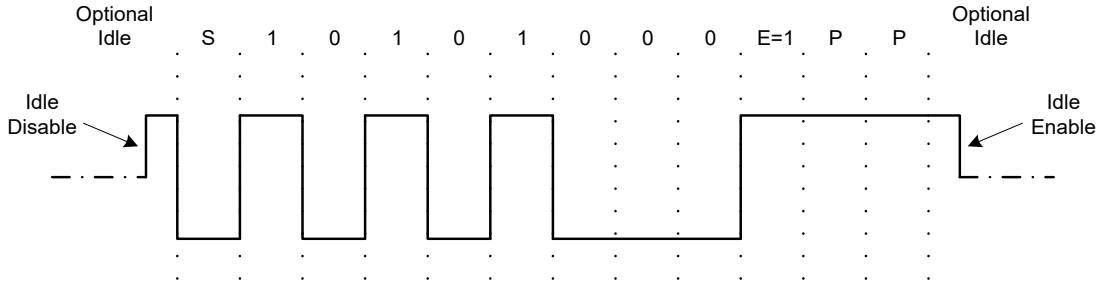


Figure 28. Preamble Character

Data Characters

Each data character contains a single-nibble (four-bit) payload and so two characters must be transmitted for each byte of data. All data is transmitted least-significant bit, least-significant nibble, and least significant byte first. The data itself is Manchester-encoded meaning that each data bit is followed by its complement. If the UART detects a Manchester-encoding error in any received data character, it will set the ALRTMAN bit in the STATUS register.

The parity is even meaning that the parity bit's value should always result in an even number of logic one bits in the character. Given that the data is Manchester-encoded and that there are two stop bits, the parity bit for data characters is always transmitted as a logic zero. If the UART detects a parity error in any received data character it will set the ALRTPAR bit in the STATUS register.

Table 20. Data Character

Bit	Name	Symbol	Description
1	Start	S	First bit in character, always logic zero
2	Data0		Least significant bit of data nibble (true)
3	Data0/		Least significant bit of data nibble (inverted)
4	Data1		Data bit 1 (true)
5	Data1/		Data bit 1 (inverted)
6	Data2		Data bit 2 (true)
7	Data2/		Data bit 2 (inverted)
8	Data3		Most significant bit of data nibble (true)
9	Data3/		Most significant bit of data nibble (inverted)
10	Parity	E	Always logic zero (even parity)
11	Stop	P	Always logic one
12	Stop	P	Last bit in character, always logic one

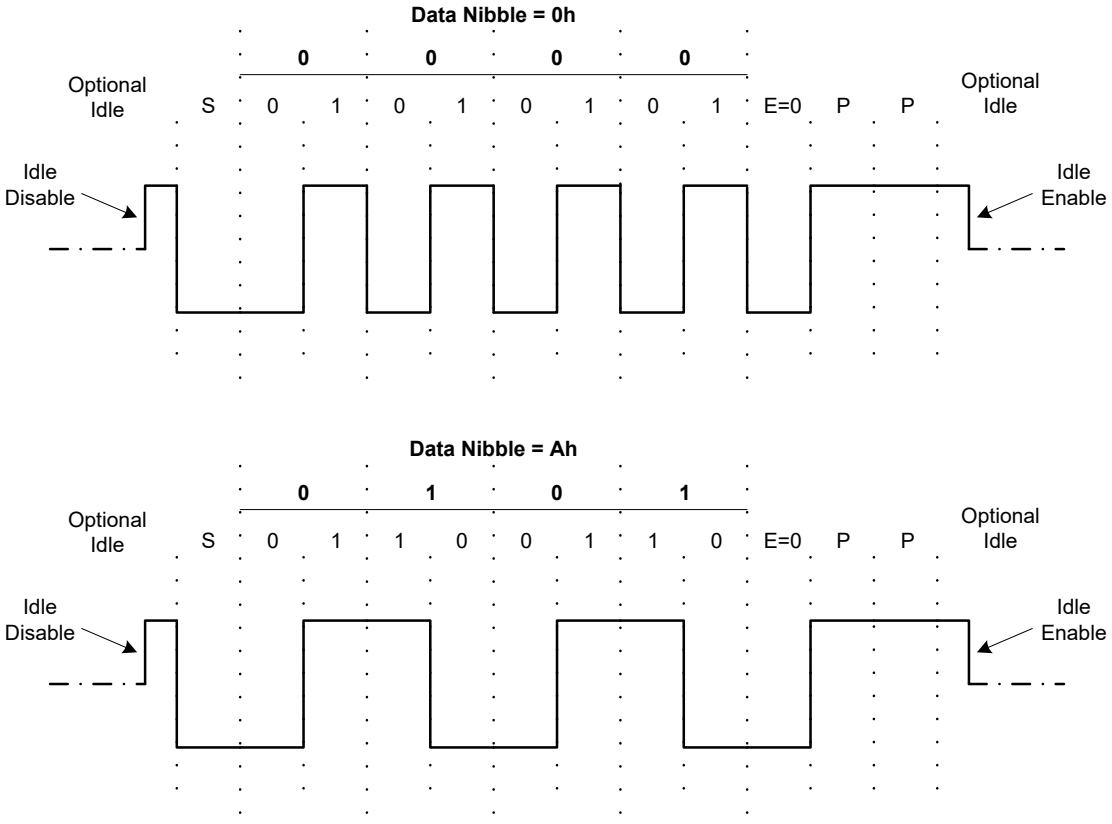


Figure 29. Data Characters

Stop Character

The stop character is a framing character that signals the end of a command packet. It is transmitted as an un-encoded 54h with a logic one parity bit and a balanced duty-cycle.

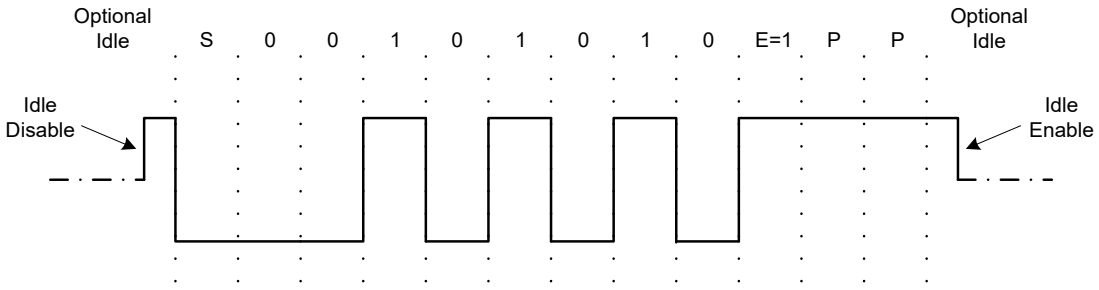


Figure 30. Stop Character

UART Idle Mode

In the low-Z (default) idle mode, the transmitter outputs are both driven to 0V as shown in Figure 31. In the high-Z idle mode, the transmitter outputs are not driven by the UART. The MAX17841B interface automatically places its transmitter in idle mode immediately after each command packet and remains in idle mode until either the next command packet is sent or it goes into keep-alive mode sending periodic stop characters to prevent the daisy-chain device(s) from going into shutdown.

UART Communication Mode

When transitioning from idle mode to communication mode, the TXP pin must be pulled high (logic one) prior to signaling the start bit (logic zero) as shown in Figure 31. The duration of the logic one is minimized to maintain a balanced duty-cycle while still meeting the timing specification. When transitioning from the stop bit back to idle mode, the delay, if any, is also minimized.

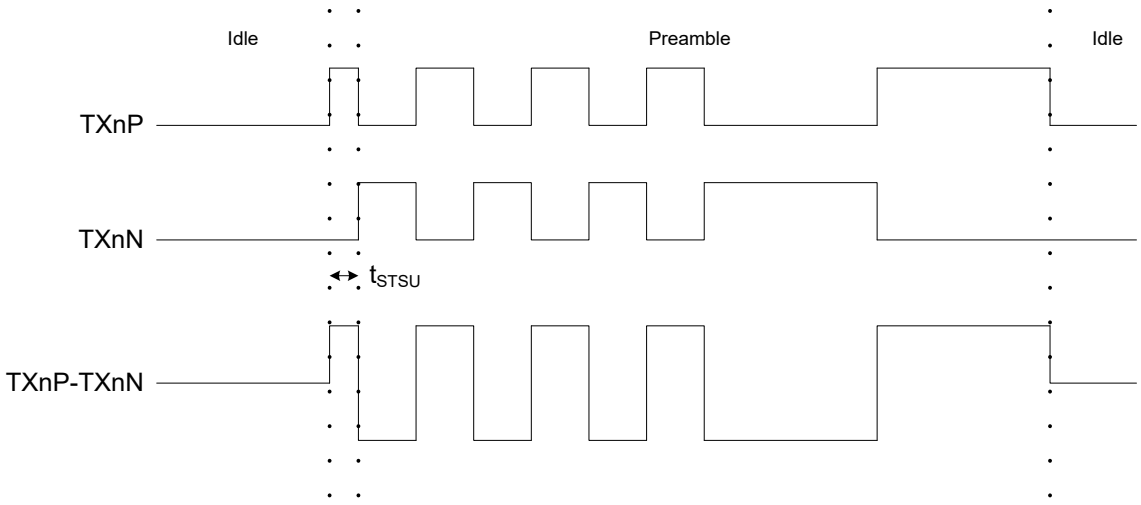


Figure 31. Communication Mode

Data Types

The Battery-Management UART Protocol employs several different data types as described in Table 21.

Table 21. Data Types

Data Type	Description
Command byte	A byte defining the command packet type, generally either a read or a write.
Register address	A byte defining the register address to be read or written.
Register data	Register data bytes being read or written.
Data-check byte	An error and alert status byte sent and returned with all reads.
PEC byte	A Packet Error Checking byte sent and returned with every packet except HELLOALL.
Alive-counter	A byte functioning as a device counter on all reads and writes, if ALIVECNTEN = 1.
Fill byte	Bytes transmitted in READALL command packets for clocking purposes only.

Command Bytes

The Battery-Management UART Protocol supports six command types summarized in Table 22.

Table 22. Command Packet Types

Command	Description	Data-Check	PEC	Alive-Counter	Packet Size (Characters)
HELLOALL	Writes a unique device address to each device in the daisy-chain. Required for system initialization.	No	No	No	8
WRITEALL	Writes a specified register in all devices.	No	Yes	Yes	14
WRITEDEVICE	Writes a specified register in a single device.	No	Yes	Yes	14
READALL	Reads a specific register from all devices.	Yes	Yes	Yes	12 + (4z)
READDEVICE	Reads a specified register from a single device.	Yes	Yes	Yes	16
ROLLCALL	Reads the ADDRESS register for 32 devices.	Yes	Yes	Yes	138

Note: z = total number of devices, ALIVECNTEN = 1, packet size includes framing characters.

Command Byte Encoding

Command bytes encoding is described in Table 23. For READDEVICE and WRITEDEVICE commands, the device address is encoded in the command byte. The device ignores those commands containing a device address other than its own.

Table 23. Command Byte Encoding

Command	Byte*	7	6	5	4	3	2	1	0
HELLOALL	57h	0	1	0	1	0	1	1	1
ROLLCALL	01h	0	0	0	0	0	0	0	1
WRITEDEVICE	04h	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	1	0	0
WRITEALL	02h	0	0	0	0	0	0	1	0
READDEVICE	05h	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	1	0	1
READALL	03h	0	0	0	0	0	0	1	1

*Assumes DA[4:0] = 0x00 where DA[4:0] is the device address in the ADDRESS register.

Register Addresses

All register addresses are single-byte quantities and are defined in the Register Map. In general, if the register or device address in a received command is not a valid address for the device, the device will ignore the read or write and simply pass-through the packet to the next device.

Register Data

All registers are 16-bit words (two data bytes) and are defined in the Register Map.

Data-Check Byte

The host uses the returned data-check byte to promptly determine if any communication errors occurred during the packet transmission and to check if alert flags are set in any devices as shown in Table 24. The data-check byte is returned by the READALL and READDEVICE commands. For READDEVICE, the data-check byte is updated only by the addressed device.

The data-check byte sent by the host is a seed value normally set to 00h although non-zero values may be used as a diagnostic. Each device logically ORs the received data-check byte with its own status and transmits it to the next device. A PEC error detected by any device will set the ALRTPEC bit in the STATUS register and, by extension, the ALRTPEC and ALRTSTATUS bits in the data-check byte.

Table 24. Data-Check Byte

Bit	Name	Description
7	ALRTPEC	ALRTPEC is set
6	ALRTFMEA	ALRTFMEA1 or ALRTFMEA2 is set
5	ALRTSTATUS	STATUS bit other than ALRTFMEA1, ALRTFMEA2, ALRTOV, and ALRTUV is set
4	CHECK	Check bit. Value that is received is forwarded
3	CHECK	Check bit. Value that is received is forwarded
2	ALRTOV	ALRTOV is set
1	ALRTUV	ALRTUV is set
0	CHECK	Check bit. Value that is received is forwarded

PEC Byte

The PEC byte is a CRC-8 Packet Error Check sent by the host with all read and write commands. If any device receives an invalid PEC byte, it sets the ALRTPEC bit in the STATUS register. During any write transaction, a device does not execute the write command internally unless the received PEC matches the expected calculated value. For read commands, the device must return its own calculated PEC byte based on the returned data. The host should verify that the received PEC byte matches the calculated value and if an error is indicated, the data should be discarded. See Applications section for details on the PEC calculation.

Alive-Counter Byte

The alive-counter byte is the last data byte of the command packets (except HELLOALL) if the ALIVECNTEN bit is set in the DEVCFG1 register. The host transmits typically transmits the alive-counter seed value as 00h but any value is permitted. For WRITEALL or READALL commands, each device will re-transmit the alive-counter incremented by one. For WRITEDEVICE or READDEVICE commands, only the addressed device will increment it. The alive-counter is not used in the HELLOALL command. If the alive-counter reaches FFh, the next device increments it to 00h.

Since the alive-counter comes after the PEC byte, an incorrect PEC value will not affect the incrementing of the alive-counter byte. Also, the PEC calculation does not include the alive-counter byte. The host should verify that the alive-counter equals the original seed value + the number of devices and considering that if the alive-counter reaches FFh, the next device increments it to 00h.

Fill Bytes

In the READALL command, the host sends two fill bytes for each device in the daisy-chain. The fill bytes are the locations within the packet and used by the device to place the read data. The fill byte values transmitted by the MAX17841B interface alternate between C2h and D3h. As the command packet propagates through the device, the device overwrites the appropriate fill bytes with the register data. The device uses the ADDRESS register to determine which specific fill bytes in the packet are to be overwritten.

For a READDEVICE command, only two fill bytes are required since only one device responds (returning two data bytes). Also, fill bytes are not required for write commands because the data received is exactly the same as the data re-transmitted.

Battery-Management UART Protocol Commands

HELLOALL Command

The purpose of the HELLOALL command is to initialize the device addresses of all daisy-chain devices. The device address is stored in the DA[4:0] bits of the ADDRESS register. The highest address possible is 0x1F and so a maximum of 32 devices may be addressed. The command must be issued after POR to reinitialize all device addresses.

When the HELLOALL command is first sent by the host, the address specified in the HELLOALL command is stored to the DA[4:0] bits of the ADDRESS register in the first daisy-chain device. The command is then forwarded to the next device in the chain with the DA[4:0] bits of the address byte incremented by 1 as shown in Table 25. This continues in the up-stack direction for each device. The down-stack communication path does not increment the address. The advantage of the host choosing a first address of 0x00 is that it is not necessary to write the first address FA[4:0] to all the devices since the default value of FA[4:0] is 0x00. **Note:** The host should set the first address so that no assigned device address increments from 0x1F to 0x00 during the HELLOALL.

The DA[4:0] value returned to the host is one greater than address assigned to the last device. Once this last address is known, the host can determine how many devices are in the daisy-chain which is required for subsequent READALL commands. A READALL command should be used to verify the ADDRESS registers.

Special considerations exist if the host desires to use internal loopback instead of external loopback. The first HELLOALL command is not returned to the host because the internal loopback bit for the top device has not yet been written. If the number of devices is known to the host, the host can use a WRITEDEVICE to set the internal loopback bit on the last device and then verify with a READALL. If the number of devices is unknown, the internal loopback bit must be set on the first device, verified and then cleared. It can then be set on the second device and verified, and so on incrementally until there is no response (end of stack). With the number of devices known, the loopback bit can be re-set on the last device and all ADDRESS registers verified.

When a device receives a valid HELLOALL command, it clears the ADDRUNLOCK bit of the DEVCFG1 register. When this bit is 0, HELLOALL commands are ignored to prevent inadvertently changing any device address. In order to reconfigure the device address, the ADDRUNLOCK bit must first be set to 1, or a POR event must occur. After configuring the device addresses, they should be verified using the READALL or ROLLCALL commands.

Table 25. HELLOALL Sequencing (z = total number of devices)

Host TX	Device (n) RXL	Device (n) TXU	Host RX
Preamble	Preamble	Preamble	Preamble
57h	57h	57h	57h
00h	00h	00h	00h
{0b000,ADDR[4:0]}	{0b000,ADDR[4:0]+n-1}	{0b000,ADDR[4:0]+n}	{0b000,ADDR[4:0]+z}
Stop	Stop	Stop	Stop

WRITEALL Command

The WRITEALL command writes a 16-bit value to a specified register in all daisy-chain devices. Since most configuration information is common to all the devices, this command allows faster setup than writing to each device individually. If the register address is not valid for the device, the command is ignored. The command sequence is shown in Table 26.

The register value is written immediately after the valid PEC byte is received or, if NOPEC is set, after the last byte is received. If the received PEC byte does not match the internal calculation, the command is not executed, but is still forwarded to the next device. The PEC is calculated from the first four bytes of the command starting after the preamble. A PEC error will generate a PEC alert in the device STATUS register.

Table 26. WRITEALL Sequencing (unchanged by daisy-chain)

Host TX	Device (n) RXL	Device (n) TXU	Host RX
Preamble	Preamble	Preamble	Preamble
02h	02h	02h	02h
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DATA LSB]	[DATA LSB]	[DATA LSB]	[DATA LSB]
[DATA MSB]	[DATA MSB]	[DATA MSB]	[DATA MSB]
[PEC]	[PEC]	[PEC]	[PEC]
[ALIVE]*	[ALIVE]*	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop

*If alive-counter mode is enabled.

WRITEDEVICE Command

The WRITEDEVICE command writes a 16-bit value to the specified register in the addressed device only. If the register address is not valid for the device, the command is ignored. The command sequence is shown in Table 27.

The register value is written immediately after the valid PEC byte is received or, if NOPEC is set, after the last byte is received. If the received PEC byte does not match the internal calculation, the command is not executed, but is still forwarded to the next device. The PEC is calculated from the first four bytes of the command starting after the preamble. A PEC error sets the ALRTPEC bit in the STATUS register. A PEC error can only occur in the addressed device.

Table 27. WRITEDEVICE Sequencing (unchanged by daisy-chain)

Host TX	Device(n) RXL	Device(n) TXU	Host RX
Preamble	Preamble	Preamble	Preamble
{(DA[4:0]),0b100}	{(DA[4:0]),0b100}	{(DA[4:0]),0b100}	{(DA[4:0]),0b100}
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DATA LSB]	[DATA LSB]	[DATA LSB]	[DATA LSB]
[DATA MSB]	[DATA MSB]	[DATA MSB]	[DATA MSB]
[PEC]	[PEC]	[PEC]	[PEC]
[ALIVE]*	[ALIVE]*	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop

*If alive-counter mode is enabled.

READALL Command

The READALL command returns register data from the specified register for all daisy-chain devices. The data for the first device (connected to host) is returned last. The command sequence is shown in Table 28. If the received PEC byte does not match the calculated value, the ALRTPEC bit of the data-check byte and ALRTPEC bit of the STATUS register are set, but the command proceeds. A Manchester error immediately switches the data propagation from read mode to write (pass-through) mode insuring that the Manchester error is propagated through the daisy-chain and back to the host.

Table 28. READALL Command Sequencing (z = no. of devices)

Host TX	Device(n) RXL	Device(n) TXU	Host RX
Preamble	Preamble	Preamble	Preamble
03h	03h	03h	03h
[REG ADDR]	[REG ADDR]	[DATA ADDR]	[REG ADDR]
[DC] = 0x00	[DATA LSB(n-1)]	[DATA LSB(n)]	[DATA LSB(z)]
[PEC]	[DATA MSB(n-1)]	[DATA MSB(n)]	[DATA MSB(z)]
[ALIVE]*	…	…	[DATA LSB(z-1)]
[FD(1) C2h]	…	…	[DATA MSB(z-1)]
[FD(1) D3h]	[DATA LSB(1)]	[DATA LSB(1)]	…
[FD(2) C2h]	[DATA MSB(1)]	[DATA MSB(1)]	…
[FD(2) D3h]	[DC]	[DC]	…
…	[PEC]	[PEC]	…
…	[ALIVE]*	[ALIVE]*	…
…	[FD(1) C2h]	[FD(1) C2h]	…
…	[FD(1) D3h]	[FD(1) D3h]	[DATA LSB(1)]
…	…	…	[DATA MSB(1)]
…	…	…	[DC]
[FD(z) C2h]	[FD(z-n) C2h]	[FD(z-n-1) C2h]	[PEC]
[FD(z) D3h]	[FD(z-n) D3h]	[FD(z-n-1) D3h]	[ALIVE]*
Stop	Stop	Stop	Stop
12 + (4 x z) characters	12 + (4 x z) characters	12 + (4 x z) characters	12 + (4 x z) characters

*If alive-counter mode is enabled.

The fill byte values transmitted by the MAX17841B interface alternate between C2h and D3h as shown. As the packet propagates through the device, the device retransmits it in the order shown in the sequencing table (device TXU column). The device knows which bytes to overwrite since its ADDRESS register contains the first device address and its own device address and therefore it knows where in the data stream it belongs.

READDEVICE Command

The READDEVICE command returns a 16-bit word read from the specified register in the addressed device only. If the register address is not valid for the device, the command is ignored. The command sequence is shown in Table 29.

The command packet is forwarded up the daisy-chain until it reaches the addressed device. The addressed device overwrites the received fill bytes with the two bytes of register data and forwards the packet to the next device. The alive-counter byte is only incremented by the addressed device. A Manchester error immediately switches the data propagation from read mode to write (pass-through) mode insuring that the Manchester error is propagated through the daisy-chain and back to the host.

Table 29. READDEVICE Sequencing

Host TX	Device RXL	Device TXU	Host RX
Preamble	Preamble	Preamble	Preamble
{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}	{DA[4:0], 0b101}
[REG ADDR]	[REG ADDR]	[REG ADDR]	[REG ADDR]
[DC]	[DC]	[DATA LSB]	[DATA LSB]
[PEC]	[PEC]	[DATA MSB]	[DATA MSB]
[ALIVE]*	[ALIVE]*	[DC]	[DC]
[FD(1) C2h]	[FD(1) C2h]	[PEC]	[PEC]
[FD(1) D3h]	[FD(1) D3h]	[ALIVE]*	[ALIVE]*
Stop	Stop	Stop	Stop
16 characters	16 characters	16 characters	16 characters

*If alive-counter mode is enabled.

ROLLCALL Command

While not required for system initialization, the ROLLCALL command (01h) may be used to verify that all devices are responding regardless of the value of FA[4:0]. The response of each device is identical to that of a READALL command of the ADDRESS register where the first device address (FA[4:0]) is 00h and there are 32 devices. Therefore the ROLLCALL command is sent with 64 fill bytes and each device places the data-check and PEC bytes after the 32nd register data word. This ensures that each device can return its ADDRESS register data.

DIAGNOSTICS

Built-in diagnostics support ISO26262 (ASIL) requirements by detecting specific fault conditions as shown in Table 30. The device automatically performs some of the diagnostics while the host can perform others during initialization (e.g., at key-on) or periodically during operation as required by the application. Diagnostics performed automatically by the device are previously described in the relevant functional sections. A description of the diagnostics requiring specific configurations are provided in this section.

Table 30. Summary of Built-In Diagnostics

Diagnostics performed automatically by device with no host intervention			
Fault	**Diagnostic Procedure**		**Output**
V_{AA} under-voltage	Continuous voltage comparison		ALRTRST
V_{HV} under-voltage	Continuous voltage comparison		ALRTHVUV
V_{HV} over-voltage	Continuous voltage comparison		ALRTHVOV
V_{HV} low headroom	voltage comparison – updated during measurement		ALRTHVHDRM
32kHz oscillator fault	Continuous frequency comparison		ALRTOSC1, ALRTOSC2
16MHz oscillator fault	Communication error checking		ALRTMAN, ALRTPAR
Communication fault	Communication error checking		ALRTPEC, ALRTMAN, ALRTPAR
RX pin open/short	Verify RX mode after POR		ALRTCOMMSEUn/ALRTCOMMSELn
VDDLx pin open/short	Continuous voltage comparison		ALRTVDDLx
GNDLx pin open/short	Continuous voltage comparison		ALRTGNDLx
Die over-temperature	Temperature comparison – updated after measurement.		ALRTTEMP
Diagnostics performed during acquisition mode as selected by DIAGSEL or BALSWDIAG			
Fault	**Diagnostic Procedure**	**DIAGSEL[2:0]**	**Output**
Reference voltage fault	ALTREF diagnostic	DIAGSEL = 1h	DIAG[15:0] (ALTREF voltage)
V_{AA} voltage fault	V_{AA} diagnostic	DIAGSEL = 2h	DIAG[15:0] (V_{AA} voltage)
LSAMP Offset too high	LSAMP offset diagnostic	DIAGSEL = 3h	DIAG[15:0] (LSAMP offset voltage)
ADC bit stuck high	Zero-Scale ADC diagnostic	DIAGSEL = 4h	DIAG[15:0] (Zero-scale)
ADC bit stuck low	Full-Scale ADC diagnostic	DIAGSEL = 5h	DIAG[15:0] (Full-scale)
V_{PTAT} or ALRTTEMP fault	Die Temperature diagnostic	DIAGSEL = 6h	DIAG[15:0] (V_{PTAT} voltage), ALRTTEMP
Balancing switch short	BALSW diagnostic mode	BALSWDIAG = 1h	ALRTBALSW
Balancing switch open	BALSW diagnostic mode	BALSWDIAG = 2h	ALRTBALSW
Odd sense-wire open	BALSW diagnostic mode	BALSWDIAG = 5h	ALRTBALSW
Even sense-wire open	BALSW diagnostic mode	BALSWDIAG = 6h	ALRTBALSW
Procedural diagnostics			
Fault	**Diagnostic Procedure**		**Output**
SHDNL stuck high	Idle mode		ALRTSHDNL
HVMUX switch open	Acquisition with HVMUX test sources		ALRTOV, ALRTUV
HVMUX switch short	ALTREF diagnostic		DIAG[15:0]
HVMUX test sources	Acquisition with HVMUX test sources		CELLn
Cn pin open	Acquisition with cell test sources		ALRTOV, ALRTUV
Cn short to SWn	Acquisition with balancing switches		CELLn
Cn pin leakage	ALTMUX vs. HVMUX acquisition		CELLn
Voltage comparator fault	ALTMUX acquisition with balancing switches		CELLn
Voltage comparator fault	ALTMUX acquisition with balancing switches		CELLn
ALRTHVUV comparator	Acquisition with HV charge pump disabled		ALRTHVUV
HVMUX sequencer	Acquisition with cell test sources		CELLn
ALU Data Path	Acquisition with ADCTEST = 1		CELLn, VBLKP, DIAG, and AUXINn
AUXINn Pin Open	Acquisition with AUXIN test sources		AUXINn
Calibration corruption	Read CALx, IDx, perform CRC		ID2

Note: Pin faults such as an open pin or adjacent pins shorted to each other must be detectable. Pin faults do not result in device damage but have a specific device response such as a communication error, or will be detectable through a built-in diagnostic. Analyzing the effect of pin faults is referred to as a pin FMEA. Contact Maxim

Applications to obtain pin FMEA results.

ALTREF Diagnostic Measurement

The ALTREF diagnostic measurement (DIAGSEL[2:0] = 0b001) checks the primary voltage reference of the ADC by measuring the alternate reference voltage, V_{ALTREF}. The result is available in the DIAG register after a normal acquisition.

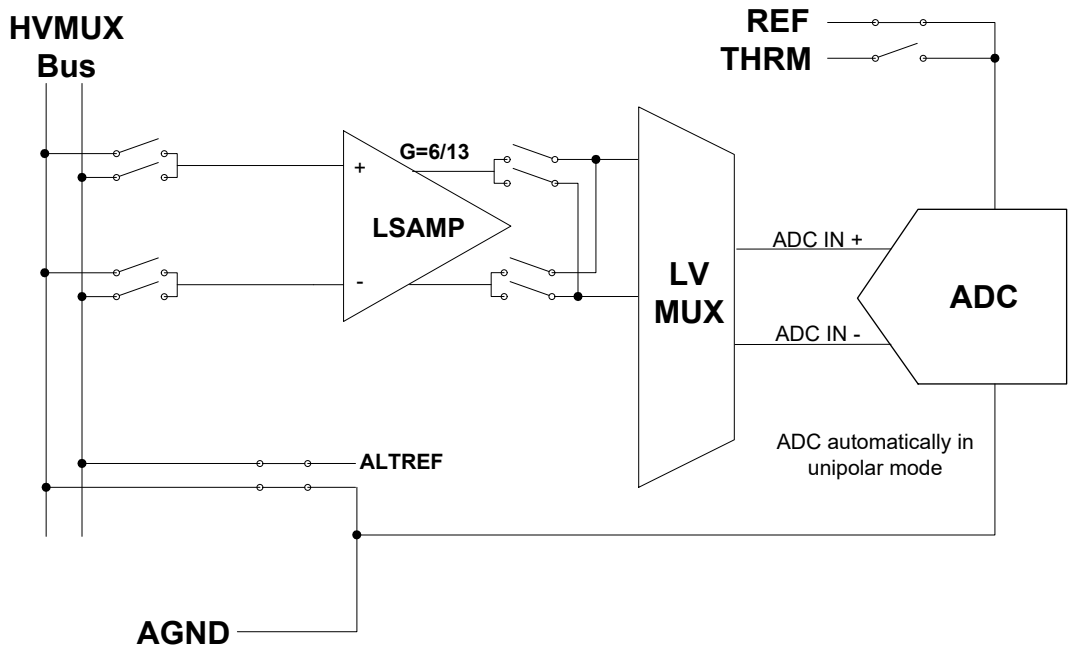


Figure 32. ALTREF Diagnostic

The ALTREF voltage is computed from the result in the DIAG register as follows:

$$V_{ALTREF} = (DIAG[15:2] / 16384d) \times 5V$$

Since 1.23V < V_{ALTREF} < 1.254V and V_{ALTREF} = 1.242V nominally, the expected range for DIAG[15:2] is (1.23V / 5V) x 16384d = 4030d to (1.254V / 5V) x 16384 = 4109d. Therefore, 0FBEh ≤ DIAG[15:2] ≤ 100Dh. To use the 16-bit register value, the 14-bit values must be shifted or multiplied by 4 so that 3EF8h ≤ DIAG[15:0] ≤ 4034h.

V_{AA} Diagnostic Measurement

The V_{AA} diagnostic measurement (DIAGSEL[2:0] = 0b010) verifies that V_{AA} is within specification. This diagnostic measures V_{REF} but using V_{THRM} as the ADC reference.

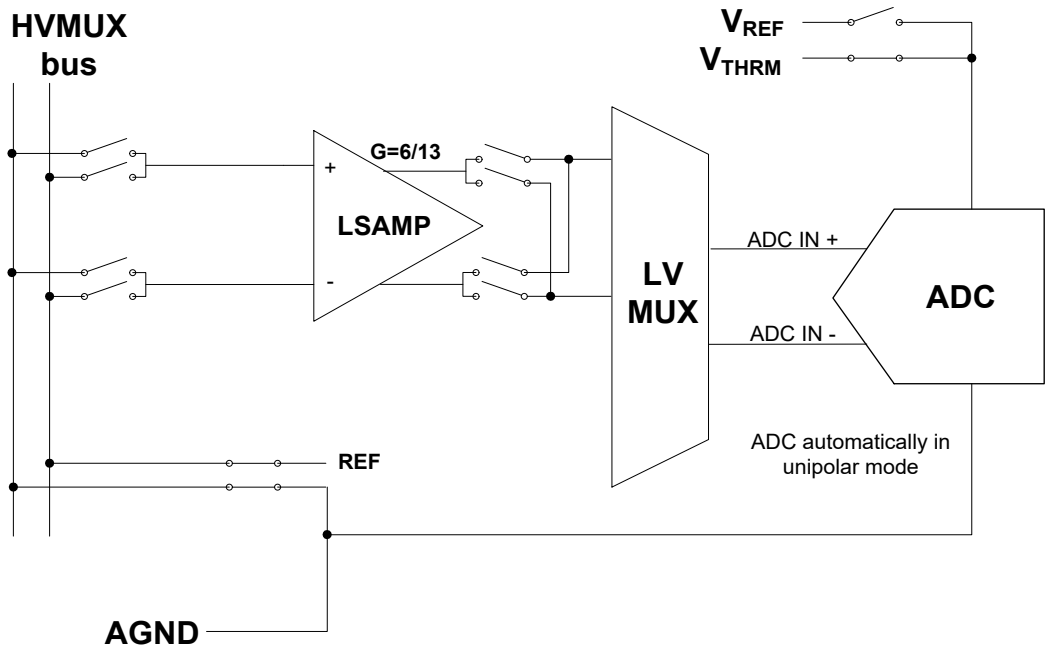


Figure 33. V_{AA} Diagnostic

The voltage into the ADC is computed from the result in the DIAG register as follows:

$$(6/13) \times V_{REF} = (DIAG[15:2] / 16384d) \times V_{THRM}$$

Assuming $V_{THRM} = V_{AA}$, then V_{AA} is given by:

$$V_{AA} = (6/13) \times V_{REF} \times 16384d / DIAG[15:2] \text{ where } V_{REF} = 2.307V$$

The result for V_{AA} should fall within the range provided in the Electrical Characteristics table for V_{AA}.

LSAMP Offset Diagnostic Measurement

The LSAMP diagnostic measurement (DIAGSEL[2:0] = 0b011) measures the level-shift amplifier offset by shorting the LSAMP inputs during the diagnostic portion of the acquisition. The result is available in the DIAG register after a normal acquisition. For this measurement, the ADC polarity is automatically set to bipolar mode to allow accurate measurement of voltages near zero. This measurement eliminates the chopping phase to preserve the offset error. If the diagnostic measurement exceeds the valid range for V_{OS_LSAMP} as specified in the *Electrical Characteristics* table, the chopping function may not be able to cancel out all of the offset error and acquisition accuracy could be degraded accordingly.

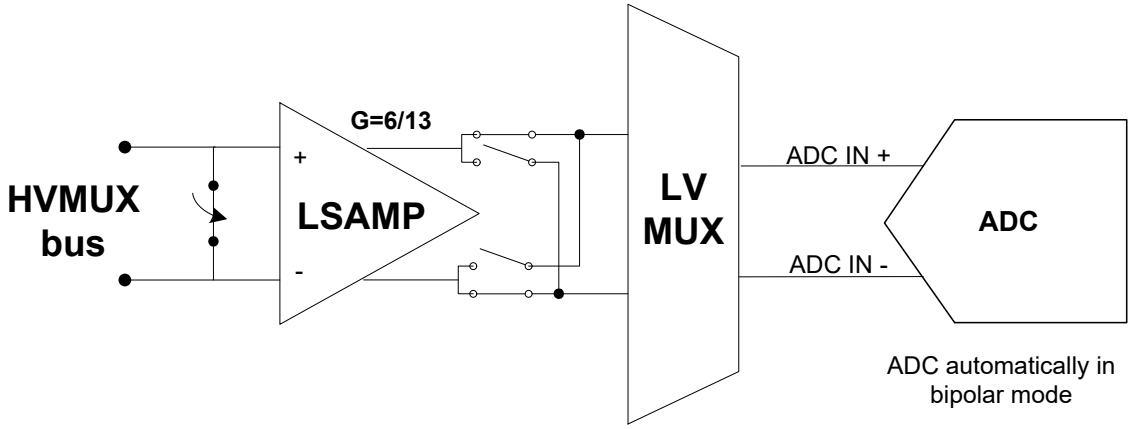


Figure 34. LSAMP Offset Diagnostic

The LSAMP offset is computed from the result in the DIAG register as follows:

LSAMP Offset = (| DIAG[15:2] - 2000h | / 16384d) x 5V

The validity of measurements through LSAMP is further confirmed by the ALTREF and V_{AA} diagnostics, and comparison of the VBLKP measurement to the sum of the cell measurements.

Zero-Scale ADC Diagnostic Measurement

Stuck ADC output bits may be verified with a combination of the zero-scale and full-scale diagnostics. The zero-scale ADC diagnostic measurement (DIAGSEL[2:0] = 0b100) verifies that the ADC conversion results in 000h when its input is at $-V_{AA}$ in bipolar mode (since for an input ≤ -2.5V, DIAG[15:0] = 0000h). For this measurement, the ADC is automatically set to bipolar mode.

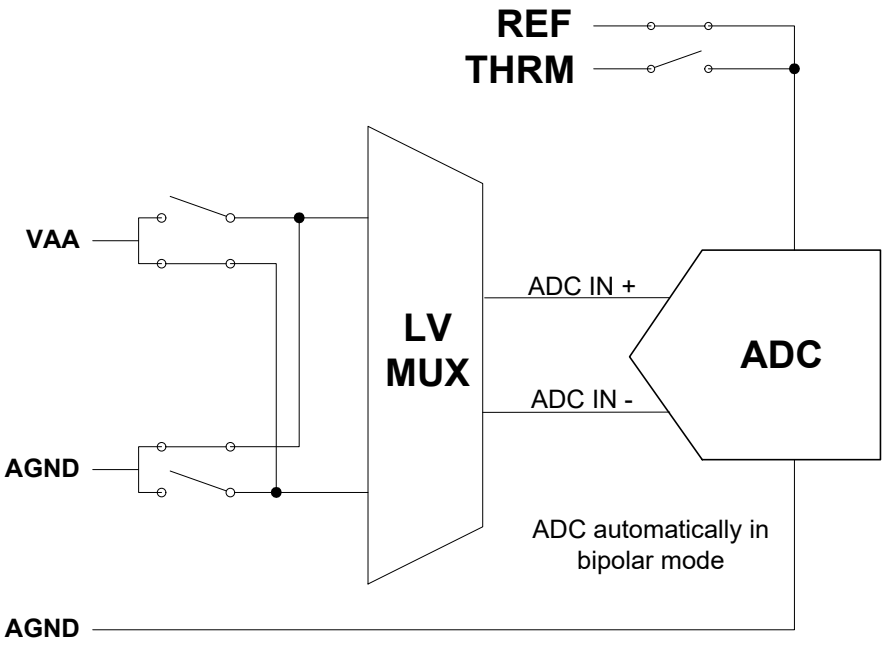


Figure 35. ADC Zero-Scale Diagnostic

Full-Scale ADC Diagnostic Measurement

Stuck ADC output bits may be verified with a combination of the zero-scale and full-scale diagnostics. The full-scale ADC diagnostic measurement (DIAGSEL[2:0] = 0b101) verifies that the ADC conversion results in FFFh when its input is at V_{AA} in bipolar mode (since for an input ≥ 2.5V, DIAG[15:0] = FFF0h). For this measurement, the ADC is automatically set to bipolar mode.

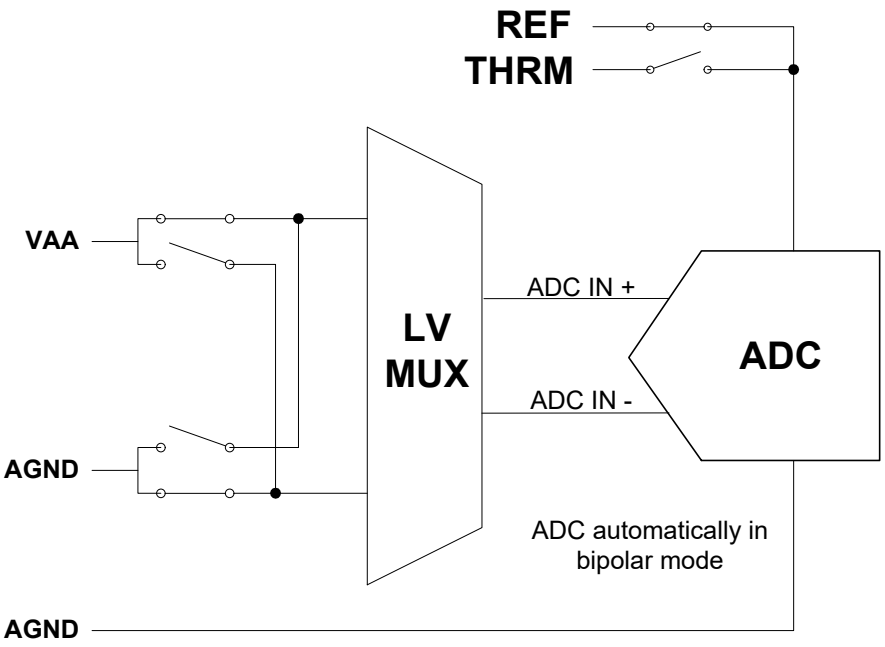


Figure 36. ADC Full-Scale Diagnostic

BALSW Diagnostics

Four balancing switch diagnostic modes are available to facilitate the following diagnostics:

- Balancing switch shorted (BALSWDIAG[2:0] = 0b001)
- Balancing switch open (BALSWDIAG[2:0] = 0b010)
- Odd sense wire open (BALSWDIAG[2:0] = 0b101)
- Even sense wire open (BALSWDIAG[2:0] = 0b110)

Enabling any of these modes automatically preconfigures the acquisition (e.g., enables the ALTMUX measurement path). The host must initiate the acquisition but the diagnostic mode automatically compares the measurements to the specific thresholds, and sets any corresponding alerts. The host presets the thresholds as determined by the minimum and maximum resistance of the switch (R_{SW}) specified in the *Electrical Characteristics* Table and the intended cell-balancing current.

During any balancing switch diagnostic mode, ALRTOV, ALRTUV and ALRTMSMTCH comparisons are disabled. After BALSWDIAG[2:0] is cleared, the modified configurations automatically return to their prior setting. The same configurations and comparisons could be implemented manually but at the expense of more host operations.

BALSW Short Diagnostic

A short-circuit fault in the balancing path could be a short between SWn and SWn-1 as shown in Figure 37 or that the balancing FET is stuck in the conducting state. In the short circuit state, the voltage between SWn and SWn-1 (switch voltage) is less than the voltage between Cn and Cn-1 (cell voltage).

When enabled, the balancing switch short diagnostic mode (BALSWDIAG[2:0] = 0b001) functions as follows:

- Disables the balancing switches automatically
- Configures the acquisition using ALTMUX path automatically
- Host initiates the acquisition
- Compares the measurement to the threshold value BALSHRTTHR automatically (Table 32)
- If outside the threshold, sets the corresponding flag in ALRTBALSW automatically

For the best sensitivity to leakage current, set the threshold value based on the minimum cell voltage minus a small noise margin (100mV) then update the threshold value periodically or every time a measurement is taken depending on how fast the cell voltages are expected to change.

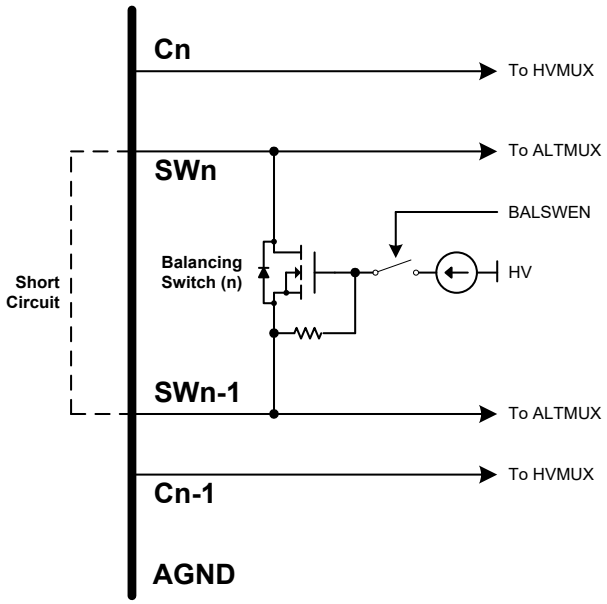


Figure 37. Balancing Switch Short

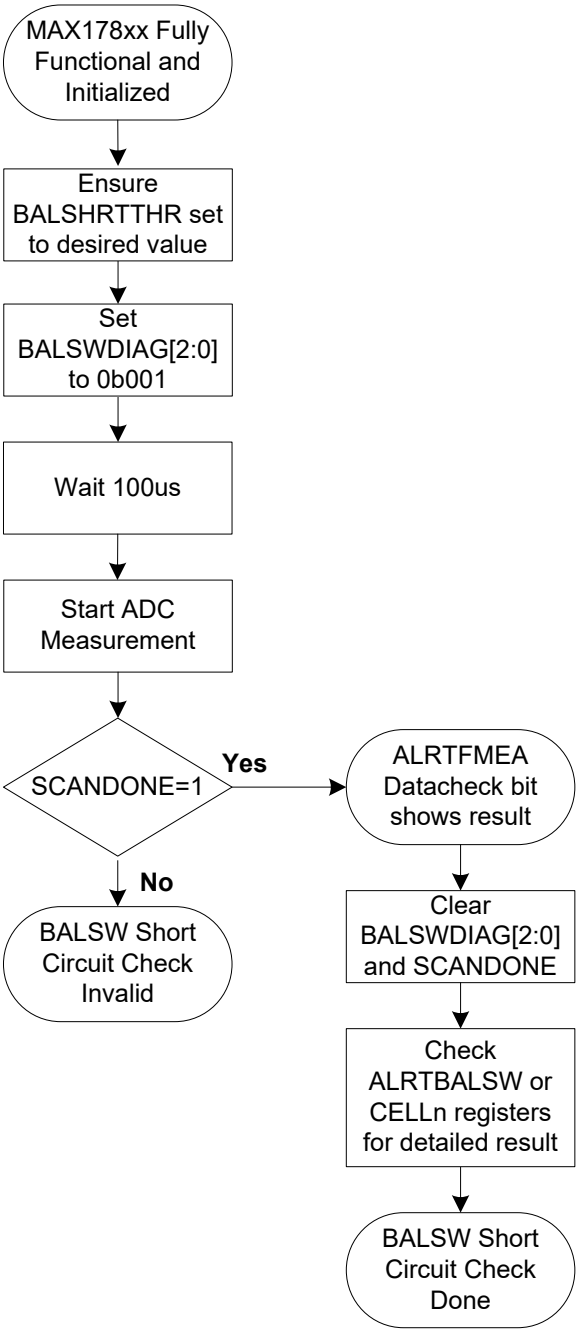


Figure 38. BALSW Short Diagnostic

Table 31. BALSW Short Diagnostic Auto-Configuration

Configuration Bits	Automatic Setting	Purpose
MEASUREEN[14:12]	0b000	Disable AUXIN and VBLKP measurements
BALSWEN[11:0]	000h	Disable all balancing switches
DIAGCFG.ALTMUXSEL	1	Enable ALTMUX measurement path

BALSW Open Diagnostic

The BALSW open diagnostic (BALSWDIAG[2:0] = 0b010) verifies that each enabled balancing switch is conducting (not open) as follows:

- Configures acquisition for bipolar mode (for measuring voltages near zero) automatically
- Configures acquisition for ALTMUX path automatically
- Configures acquisition to measure switch voltages for those switches enabled by BALSWEN automatically
- Host initiates acquisition
- Compares measurement to the threshold value BALLOWTHR and BALHIGHTHR (Table 32) automatically
- If outside the threshold, set the corresponding flag in ALRTBALSW automatically

Set the thresholds by taking into account the minimum and maximum R_{SW} of the switch itself as specified in the Electrical Characteristics table and the balancing current for the application.

Table 32. BALSW Diagnostics

BALSW	V_{SWn}	Fault Indicated?	Possible Fault Condition
On	> V(BALHIGHTHR)	Yes	Switch Open Circuit, or Overcurrent
	> V(BALLOWTHR)	No	None
	< V(BALHIGHTHR)		
	< V(BALLOWTHR)	Yes	Path Open Circuit or Short Circuit
Off	> V(BALSHRTTHR)	No	None
	< V(BALSHRTTHR)	Yes	Short Circuit or Leakage Current

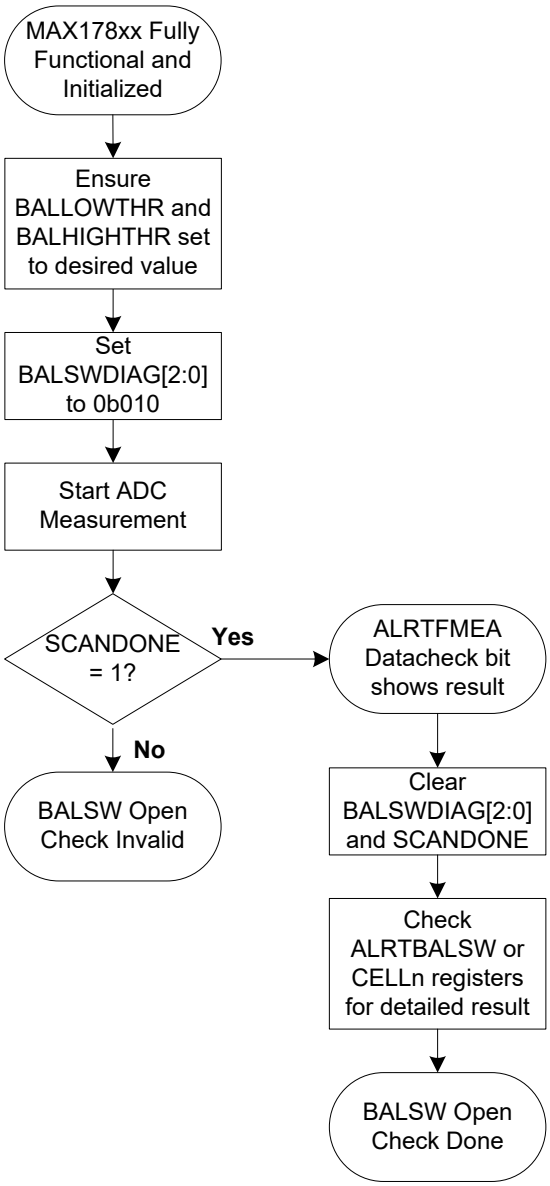


Figure 39. BALSW Open Diagnostic

Table 33. BALSW Open Diagnostic Auto-Configuration

Configuration Bits	Automatic Setting	Purpose
MEASUREEN[14:12]	0b000	Disable AUXINn and VBLKP measurements
MEASUREEN[11:0]	BALSWEN[11:0]	Measure only active switch positions
DIAGCFG.ALTMUXSEL	1	Enable ALTMUX measurement path
SCANCTRL.POLARITY	1	Enable bipolar mode

Even/Odd Sense Wire Open Diagnostics

If enabled, the sense-wire open diagnostic modes detect if a cell-sense wire is disconnected as follows:

- Closes nonadjacent switches (even or odd automatically)
- Configures acquisition to use ALTMUX path automatically
- Host waits 100us for settling and then initiates the acquisition
- Compares the result to the BALHIGHTHR and BALLOWTHR registers automatically
- If outside thresholds, sets flags in ALRTBALSW automatically

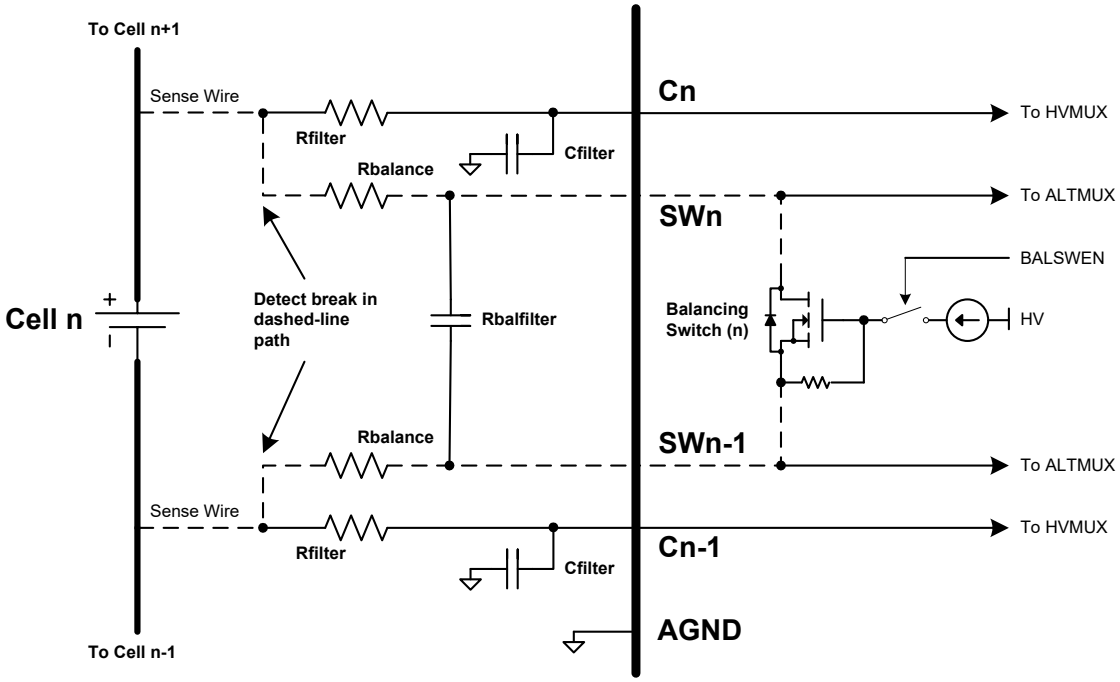


Figure 40. Cell-Sense Wire Open Diagnostic

Table 34. Odd Sense-Wire Open Measurement Result

		Sense Wire Open Fault Location												
		C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
Cell Measurement Change	Cell1	**0V**	**0V**	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell2	NC	**cell1 + cell2**	**cell2 + cell3**	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell3	NC	NC	**0V**	**0V**	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell4	NC	NC	NC	**cell3 + cell4**	**cell4 + cell5**	NC	NC	NC	NC	NC	NC	NC	NC
	Cell5	NC	NC	NC	NC	**0V**	**0V**	NC	NC	NC	NC	NC	NC	NC
	Cell6	NC	NC	NC	NC	NC	**cell5 + cell6**	**cell6 + cell7**	NC	NC	NC	NC	NC	NC
	Cell7	NC	NC	NC	NC	NC	NC	**0V**	**0V**	NC	NC	NC	NC	NC
	Cell8	NC	NC	NC	NC	NC	NC	NC	**cell7 + cell8**	**cell8 + cell9**	NC	NC	NC	NC
	Cell9	NC	NC	NC	NC	NC	NC	NC	NC	**0V**	**0V**	NC	NC	NC
	Cell10	NC	NC	NC	NC	NC	NC	NC	NC	NC	**cell9 + cell10**	**cell10 + cell11**	NC	NC
	Cell11	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	**0V**	**0V**	NC
	Cell12	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	**cell11 + cell12**	**UD**

Note: NC = No Change; UD = Undefined; Maximum result is 5V.

Table 35. Even Sense-Wire Open Measurement Result

		Sense Wire Open Fault Location												
		C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
Cell Measurement Change	Cell1	**UD**	**cell1+ cell2**	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell2	NC	**0V**	**0V**	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell3	NC	NC	**cell2+ cell3**	**cell3+ cell4**	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell4	NC	NC	NC	**0V**	**0V**	NC	NC	NC	NC	NC	NC	NC	NC
	Cell5	NC	NC	NC	NC	**cell4+ cell5**	**cell5+ cell6**	NC	NC	NC	NC	NC	NC	NC
	Cell6	NC	NC	NC	NC	NC	**0V**	**0V**	NC	NC	NC	NC	NC	NC
	Cell7	NC	NC	NC	NC	NC	NC	**cell6+ cell7**	**cell7+ cell8**	NC	NC	NC	NC	NC
	Cell8	NC	NC	NC	NC	NC	NC	NC	**0V**	**0V**	NC	NC	NC	NC
	Cell9	NC	NC	NC	NC	NC	NC	NC	NC	**cell8+ cell9**	**cell9+ cell10**	NC	NC	NC
	Cell10	NC	NC	NC	NC	NC	NC	NC	NC	NC	**0V**	**0V**	NC	NC
	Cell11	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	**cell10+ cell11**	**cell11+ cell12**	NC
	Cell12	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	**0V**	**0V**

Note: NC = No Change; UD = Undefined; Maximum result is 5V.

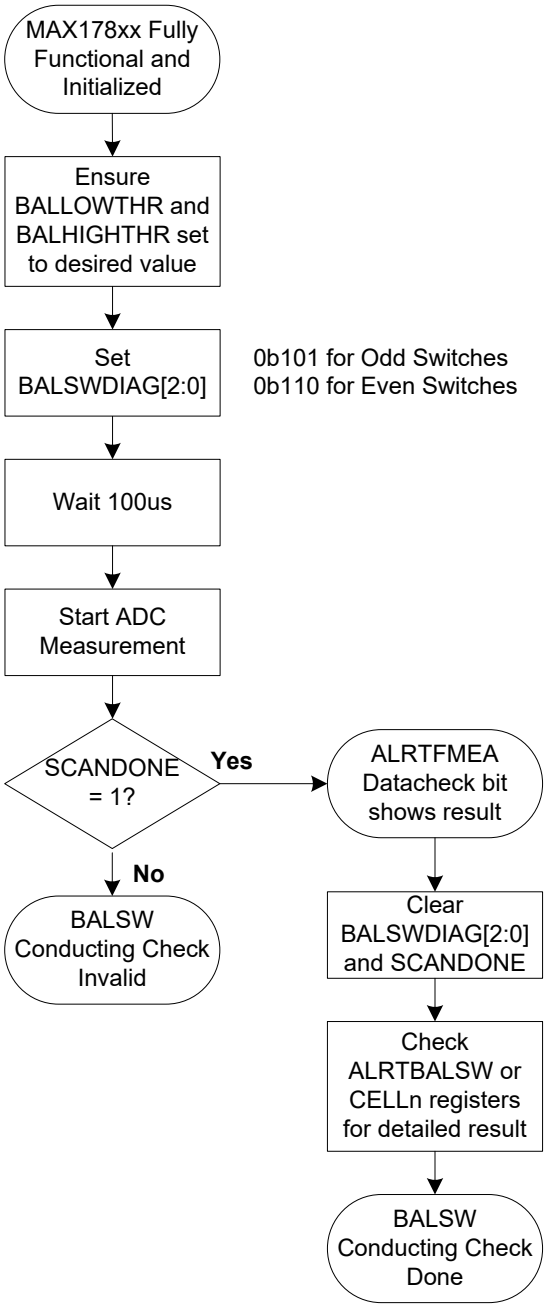


Figure 41. Sense Wire Open Diagnostic

Table 36. Sense-Wire Open Diagnostic Configurations

Configuration Bit(s)	Configuration State	Task
BALSWEN[11:0]	555h (BALSWDIAG = 0b101) or	Enable odd switches
	AAAh (BALSWDIAG = 0b110)	Enable even switches
MEASUREEN[14:12]	0b000	Disable AUXINn and VBLKP measurements
MEASUREEN[11:0]	BALSWEN[11:0]	Measure only active switch positions
DIAGCFG.ALTMUXSEL	1	Enable ALTMUX measurement path
SCANCTRL.POLARITY	1	Enable bipolar mode

Diagnostic Test Sources

Diagnostic test current sources as shown in Figure 42 can be enabled prior to the acquisition mode for the purpose of detecting both internal and external hardware faults in the measurement path. One set of test sources are connected to the HVMUX input side and another set are connected to the HVMUX output side. The basic premise in these diagnostics is that for a symmetrical measurement channel with no faults, the test currents can be applied symmetrically to the differential channel and that there should only be almost no change in the channel measurement. On the other hand, if an asymmetric fault exists on the channel, the resulting change will indicate the nature of the fault (e.g., an open or shorted pin).

For the 15 test current sources on the input channels (13 Cn and 2 AUXINn):

- The test currents are individually enabled per CTSTEN[12:0] and AUXINTSTEN[2:1]
- The test current ranges from 6.25µA up to 100µA per CTSTDAC[3:0] (applies to all enabled sources)
- The test current sources from VAA or sinks to AGND per the CTSTSRC bit (applies to all enabled sources)

For the two test current sources on the HVMUX output side:

- The test currents are enabled by the MUXDIAGEN bit
- The test current always sources from the HV supply
- The test current ranges from 3.125µA up to 50µA per CTSTDAC[3:0] (applies to all enabled sources)
- The test current, by default is applied to both HVMUX outputs (even and odd outputs). However, if MUXDIAGPAIR is set, the test current is applied to only one of the output lines per MUXDIAGBUS. This mode is used to test the test sources themselves.

Table 37. HVMUX Output Assignment

Input Signal	HVMUX Output
C12	Even bus
C11	Odd bus
C10	Even bus
C9	Odd bus
C8	Even bus
C7	Odd bus
C6	Even bus
C5	Odd bus
C4	Even bus
C3	Odd bus
C2	Even bus
C1	Odd bus
C0	Even bus
REF	Odd bus
ALTREF	Odd bus
AGND	Even bus

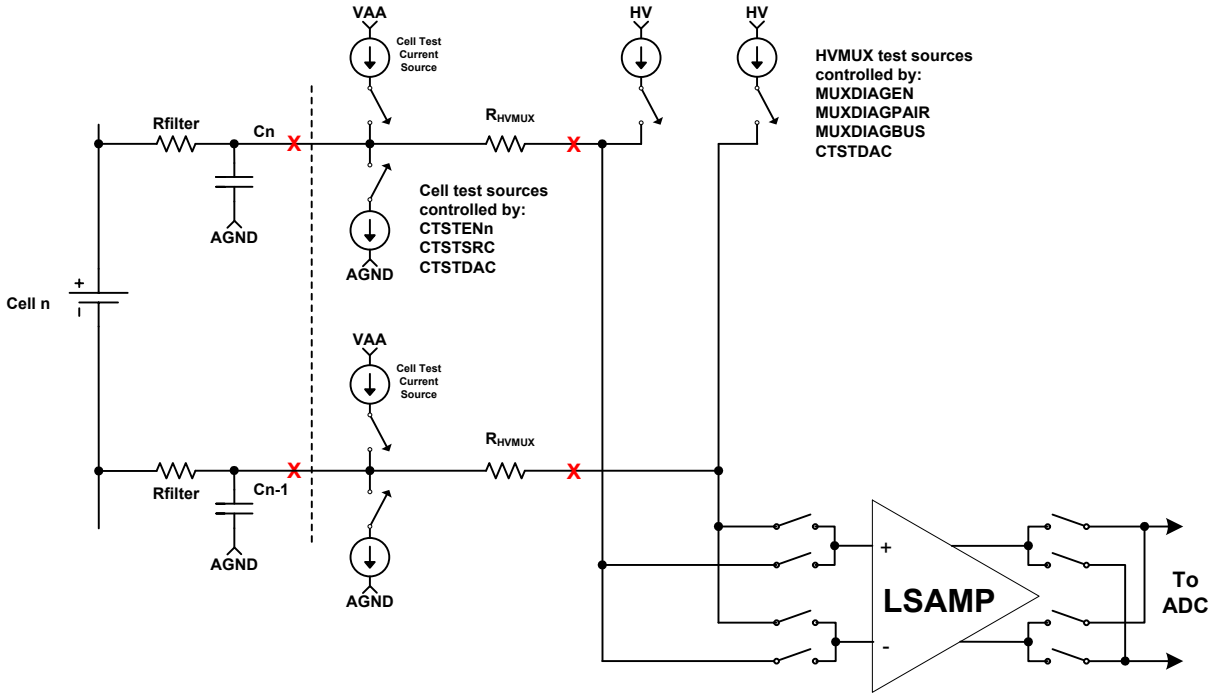


Figure 42. Test Current Sources

Shutdown Diagnostic

The shutdown diagnostic verifies that no hardware fault is preventing the device from shutting down, such as the SHDNL input being stuck at logic one. To perform the diagnostic, the host attempts a shutdown. The timing shown in Figure 43 is for a UART idle mode shutdown. Once V_{SHNDL} < 0.6V, the ALRTSHDNL bit is set in the STATUS register and the regulator is disabled. However, the STATUS register may still be read as long as V_{AA} has not decayed below 2.95V typical, which takes about 1ms. The host should verify that ALRTSHDNL is set. By reading the bit, the charge pump will drive V_{SHDNL} > 1.8V in about 200µs and enable the regulator. The host must clear the ALRTSHDNL bit to complete the diagnostic. The ALRTSHDNLRT bit is a real-time version of ALRTSHDNL that automatically clears when V_{SHDNL} > 1.8V.

Table 38. Shutdown Diagnostic

Fault	Comparison	Alert Bit	Location
SHDNL input stuck	V_{SHDNL} < 0.6V?	ALRTSHDNL	STATUS[12]
SHDNL input stuck	V_{SHDNL} < 0.6V?	ALRTSHNDRT	STATUS[11]

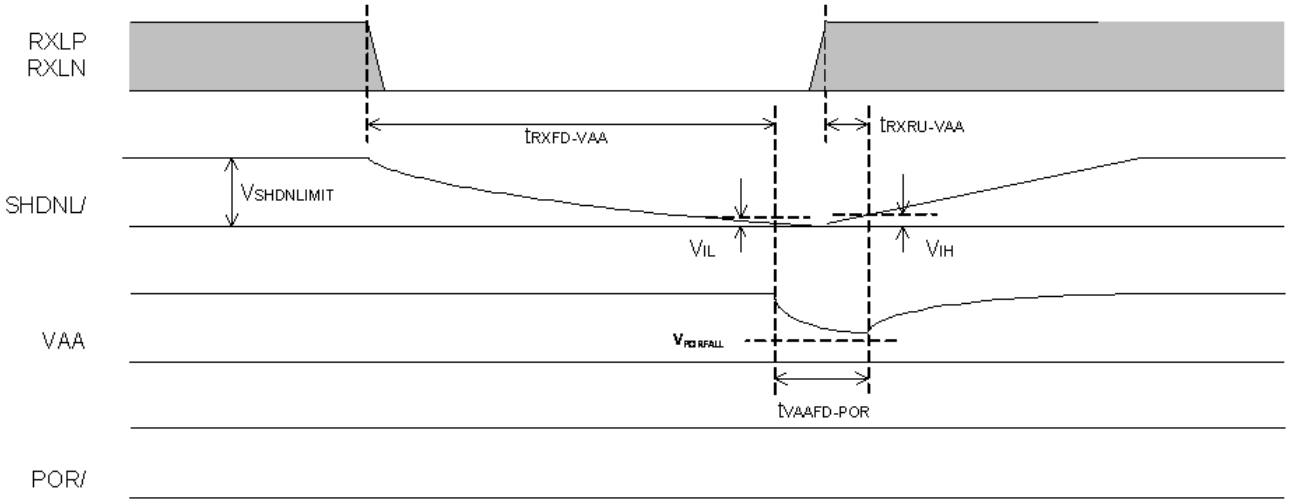


Figure 43. Shutdown Diagnostic Timing

HVMUX Switch Open Diagnostic

Since an open HVMUX switch causes the measured voltage to go to either zero or full-scale, it is possible to execute the test by looking for an over-voltage or under-voltage alert following the diagnostic measurement without analyzing the measurement data. It is possible to read all voltage measurements and let the host compare the results by splitting the test into several segments.

The procedure in Figure 44 is quick and efficient. For higher sensitivity to faults, each cell voltage measurement in the diagnostic mode can be compared to a threshold of 100mV by the host to determine if the HVMUX path is working correctly. The threshold is derived from the worst case HVMUX resistance mismatch and the worst-case diagnostic current source value variation.

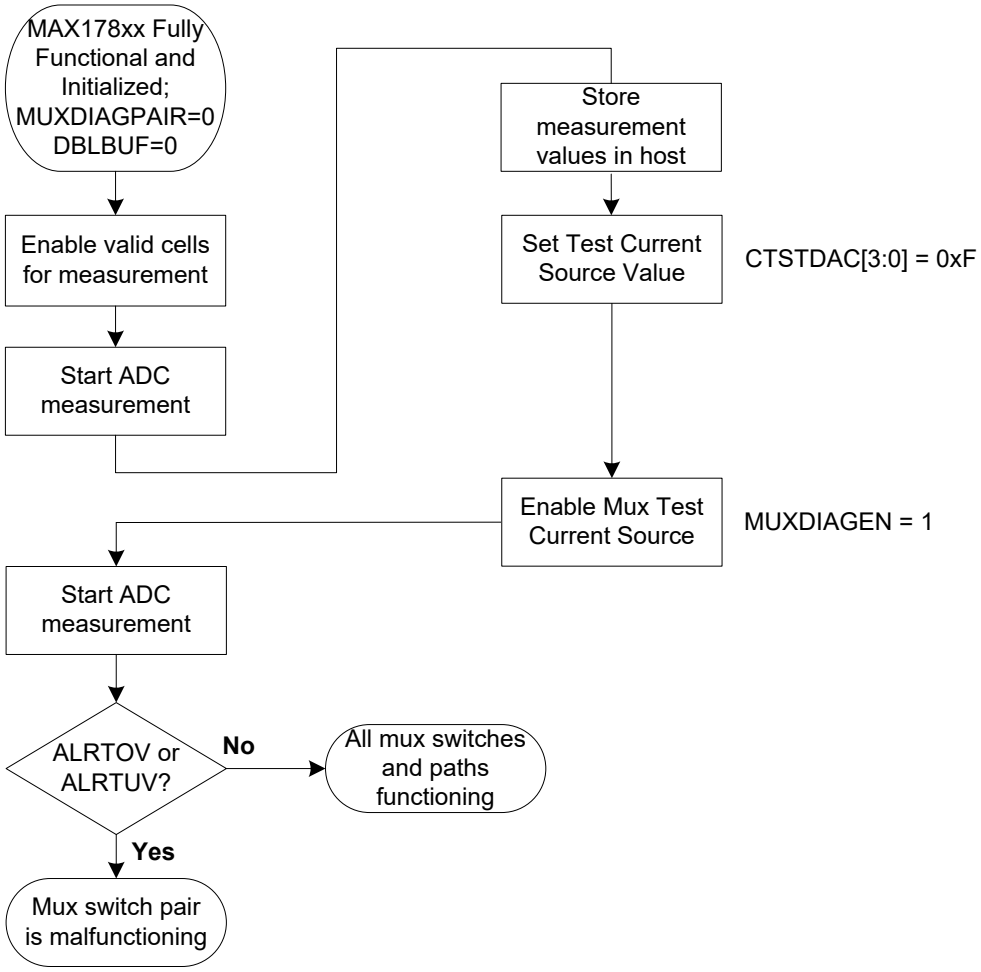


Figure 44. HVMUX Switch Open Diagnostic

Table 39. HVMUX Switch Pin Open Diagnostic

		HVMUX Switch Open Fault Location												
		C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
Cell Measurement	Cell1	**0V**	**5V**	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell2	NC	**0V**	**5V**	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell3	NC	NC	**0V**	**5V**	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell4	NC	NC	NC	**0V**	**5V**	NC	NC	NC	NC	NC	NC	NC	NC
	Cell5	NC	NC	NC	NC	**0V**	**5V**	NC	NC	NC	NC	NC	NC	NC
	Cell6	NC	NC	NC	NC	NC	**0V**	**5V**	NC	NC	NC	NC	NC	NC
	Cell7	NC	NC	NC	NC	NC	NC	**0V**	**5V**	NC	NC	NC	NC	NC
	Cell8	NC	NC	NC	NC	NC	NC	NC	**0V**	**5V**	NC	NC	NC	NC
	Cell9	NC	NC	NC	NC	NC	NC	NC	NC	**0V**	**5V**	NC	NC	NC
	Cell10	NC	NC	NC	NC	NC	NC	NC	NC	NC	**0V**	**5V**	NC	NC
	Cell11	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	**0V**	**5V**	NC
	Cell12	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	**0V**	**5V**

Note: NC = no change.

HVMUX Switch Shorted Diagnostic

A shorted mux switch is detectable in two ways based on corrupted measurement values. First, the ALTREF diagnostic will report a large error. Also, during normal cell measurements, a shorted HVMUX switch will cause the LSAMP to saturate, which is also easily detectable.

HVMUX Test Source Diagnostic

The two current sources attached to the HVMUX even bus and the HVMUX odd bus may be enabled independently instead of as a pair setting the MUXDIAGPAIR bit. MUXDIAGBUS controls which source is enabled (MUXDIAGBUS = 1 for odd bus source). This will cause every measurement to have a definable change as the sources are enabled and disabled. By taking measurements while alternating which current source is enabled, it is possible to verify that each current source is working.

Table 40. HVMUX Test Source Diagnostic

HVMUX Test Source Fault:		Even test source Shorted to HV	Even test source Open Circuit	Odd test source Shorted to HV	Odd test source Open Circuit
Cell Measurement Change	Cell1:	0V	-I x R	5V	I x R
	Cell2:	5V	I x R	0V	-I x R
	Cell3:	0V	-I x R	5V	I x R
	Cell4:	5V	I x R	0V	-I x R
	Cell5:	0V	-I x R	5V	I x R
	Cell6:	5V	I x R	0V	-I x R
	Cell7:	0V	-I x R	5V	I x R
	Cell8:	5V	I x R	0V	-I x R
	Cell9:	0V	-I x R	5V	I x R
	Cell10:	5V	I x R	0V	-I x R
	Cell11:	0V	-I x R	5V	I x R
	Cell12:	5V	I x R	0V	-I x R

Note: I = test source current, R = HVMUX resistance.

Cn Open Diagnostic

If the cell is disconnected from the input, the corresponding cell test source (sinking to AGND) will pull the cell input voltage toward 0V (except for C0, where source to VAA current source will pull the cell input voltage to VAA) A new measurement is taken with the current sources enabled, and a change in measurement value is detected. If no open circuit exists, then the measurement value will change by only the value of the test current across the application circuit series resistor to the Cn pin.

Table 41. Cn Pin Open Diagnostic

		Cn Pin Open Fault Location												
		C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
Cell Measurement	Cell1	**Cell1-3.3V**	**0V**	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell2	NC	**Cell2+Cell1**	**0V**	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell3	NC	NC	**Cell3+Cell2**	**0V**	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Cell4	NC	NC	NC	**Cell4+Cell3**	**0V**	NC	NC	NC	NC	NC	NC	NC	NC
	Cell5	NC	NC	NC	NC	**Cell5+Cell4**	**0V**	NC	NC	NC	NC	NC	NC	NC
	Cell6	NC	NC	NC	NC	NC	**Cell6+Cell5**	**0V**	NC	NC	NC	NC	NC	NC
	Cell7	NC	NC	NC	NC	NC	NC	**Cell7+Cell6**	**0V**	NC	NC	NC	NC	NC
	Cell8	NC	NC	NC	NC	NC	NC	NC	**Cell8+Cell7**	**0V**	NC	NC	NC	NC
	Cell9	NC	NC	NC	NC	NC	NC	NC	NC	**Cell9+Cell8**	**0V**	NC	NC	NC
	Cell10	NC	NC	NC	NC	NC	NC	NC	NC	NC	**Cell10+Cell9**	**0V**	NC	NC
	Cell11	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	**Cell11+Cell10**	**0V**	NC
	Cell12	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	**Cell12+Cell11**	**0V**

Note: NC = no change.

Cn Shorted to SWn Diagnostic

Short circuits between the SWn pins and the cell input pins are detectable. A shorted SWn pin can be detected by an acquisition with the relevant cell balancing switch off and then again with it on. If the SWn pin is not shorted to an adjacent cell input pin, no change in the measured value should be observed for the two cases. If the SWn pin is shorted to the Cn pin, then the measured value will change by approximately 40-50% when the balancing switch is turned on based on the values of $R_{BALANCE}$, and the balancing switch resistance. A short circuit from SWn to Cn-1 produces the same effect. By comparing both the V_{CELLn} measurement value along with the $V_{CELLn+1}$ and $V_{CELLn-1}$ values, it is possible to determine exactly where the short circuit is located.

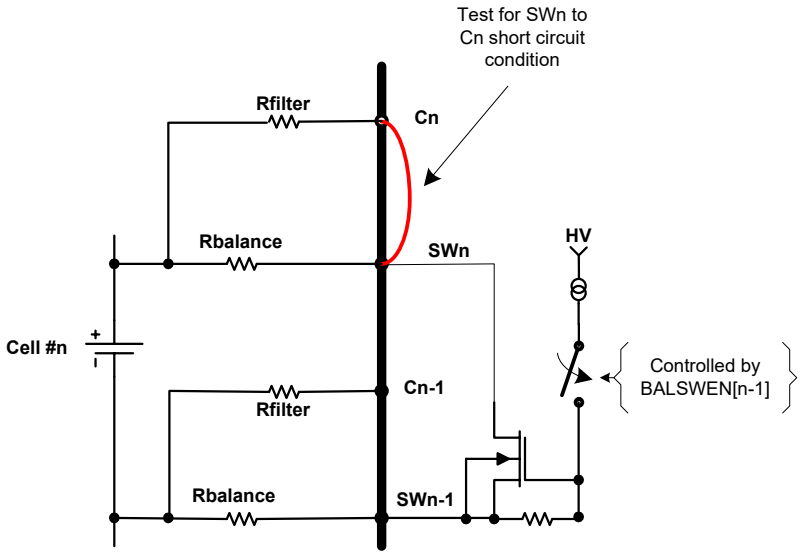


Figure 45. SWn to Cn Short

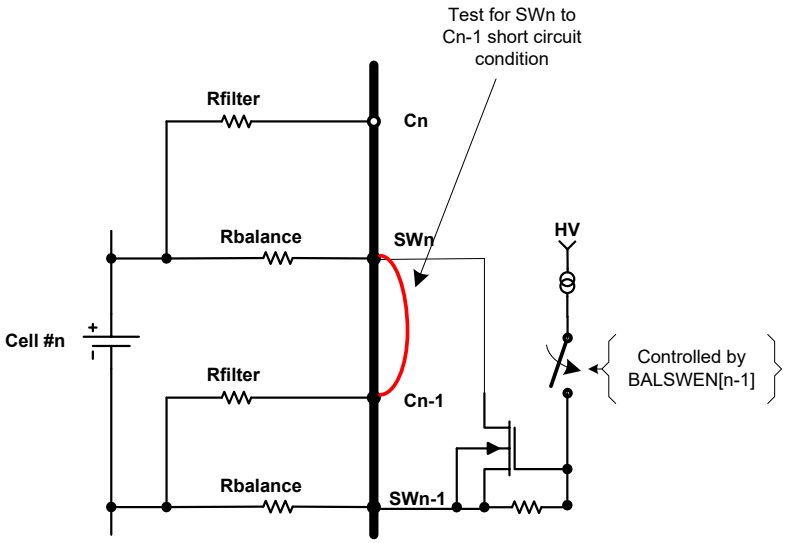


Figure 46. SWn-1 to Cn Short

Cn Leakage Diagnostic

Leakage at the Cn inputs can cause the voltage seen by the ADC to be different than that at the voltage source due to the resistance of the external filter circuit. By utilizing an alternate measurement path, any voltage errors as a result of Cn pin leakage may be detected. The SWn pins are connected to the cell sources through an alternate path. Implementing an HVMUX connection from the SWn pins to the LSAMP completes the redundant measurement path. This alternate measurement path for the cell measurements may be enabled by setting the ALTMUXSEL bit of the DIAGCFG register. When this bit is set and a measurement cycle is started, all cell measurements are taken using the alternate path instead of the Cn pin HVMUX connections. Measurements taken with the normal and alternate paths may be compared and should be nearly identical for a system with no faults. Since the SWn pins typically have a smaller external filter time constant than the Cn pins, increasing the oversampling setting for this diagnostic measurement may be beneficial for reducing measurement noise when the measurement is taken while the cells are exposed to transient loads.

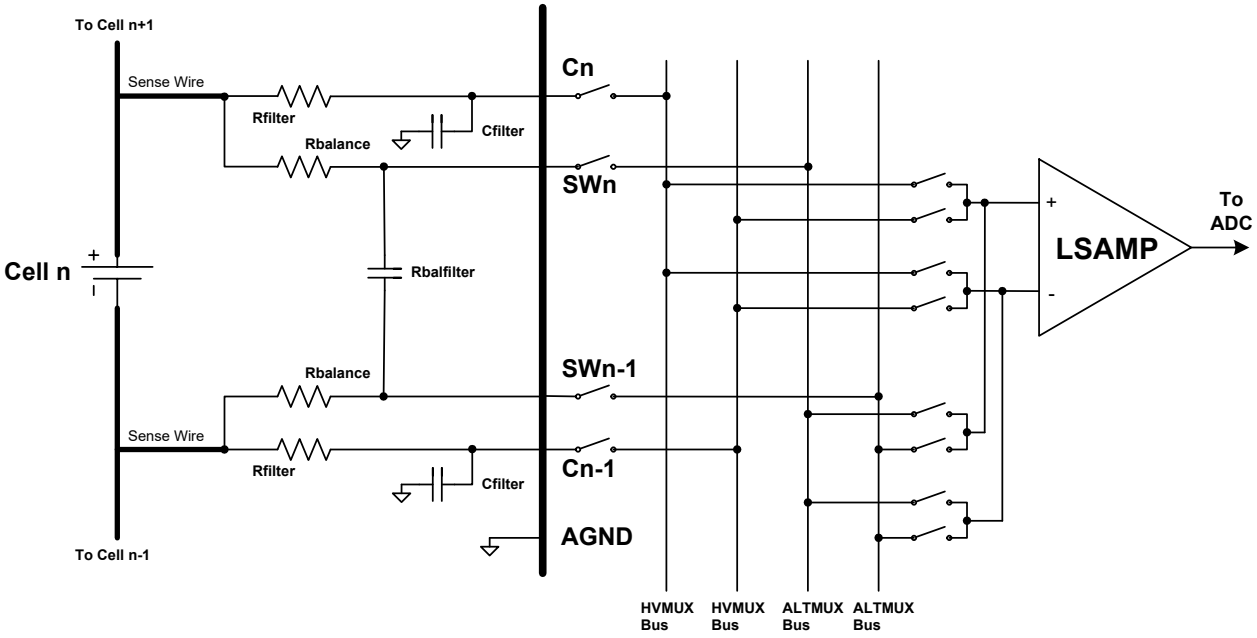


Figure 47. Redundant HVMUX Paths

Cell Over-Voltage Diagnostic
Enabling balancing switches may be used to generate a voltage up to 2 x V_{CELL} at the ALTMUX inputs to test the input range capability assuming the cell is sufficiently charged.

A cell position input voltage is elevated by approximately 1.5 x V_{CELLn} turning on either BALSWn+1 or BALSWn-1. When the adjacent switch is turned on, the SW pin shared with the switch is moved by 0.5 x V_{CELL}, which causes V_{CELLn} to increase by that amount when measured with the ALTMUX path. For the topmost cell position, BALSWn-1 must be used and for the bottom cell position BALSWn+1 must be used. By turning on two adjacent switches instead of one, such as BALSWn+1 and BALSWn+2, the measured voltage is approximately 2 x V_{CELL} assuming all cells are at approximately the same voltage. This technique can create an input voltage that exceeds the overvoltage threshold to verify the higher end of the input range and the overvoltage alert function.

Input range may also be verified by using the cell test sources to induce a higher cell channel voltage. If the change is as expected, it shows that the system can measure voltages above the present nominal input voltage.

Cell Under-Voltage Diagnostic
Turning on the balancing switch may be used to generate a near-zero voltage at any input channel to the ALTMUX path. By successfully measuring this near-zero voltage, the diagnostic verifies the lower-end of the input range and the under-voltage alert function.

Input range may also be verified by using the cell test sources to induce a lower cell channel voltage. If the change is as expected, it shows that the system can measure voltages below the present nominal input voltage.

ALRTHVUV Comparator Diagnostic
The ALRTHVUV comparator functionality may be verified by setting the CPEN bit (to disable the HV charge pump) and then discharging the external HV capacitor by performing an acquisition for 5ms (such as 12 cells, 32 oversamples) or by enabling using one or more of the cell test current sources for an appropriate amount of time. The ALRTHVUV bit should be set after the voltage has decayed.

HVMUX Sequencer Diagnostic

The HVMUX control sequence may be checked using the sources attached to the Cn pins. The sources are controlled by the CTSTEN bits of the CTSTCFG register. The basic test method is as follows:

1. Perform an acquisition
2. Turn on a cell test source
3. Wait for sufficient settling time
4. Perform an acquisition
5. Check that the cell(s) sharing the pin whose current source was turned on had the expected measurement change and other cells had no changes
6. Repeat steps 1–5 for other pins to confirm there are no logic errors in the HVMUX control sequencer

The cell test sources may be turned on for individual pins to create a detectable measurement variation that is determined by the current source value and the series resistance of the cell input filter circuit. The settling time needed for a certain change in measurement value depends on the size of the external filter capacitors and the amplitude of the test current source. A longer settling time will give the full voltage change while a shorter settling time will save test time and should still produce an easily detectable voltage difference. By detecting the expected measurement variation for a given cell input pair and running a sequence of tests to cover all cases, the HVMUX sequencer operation is verified.

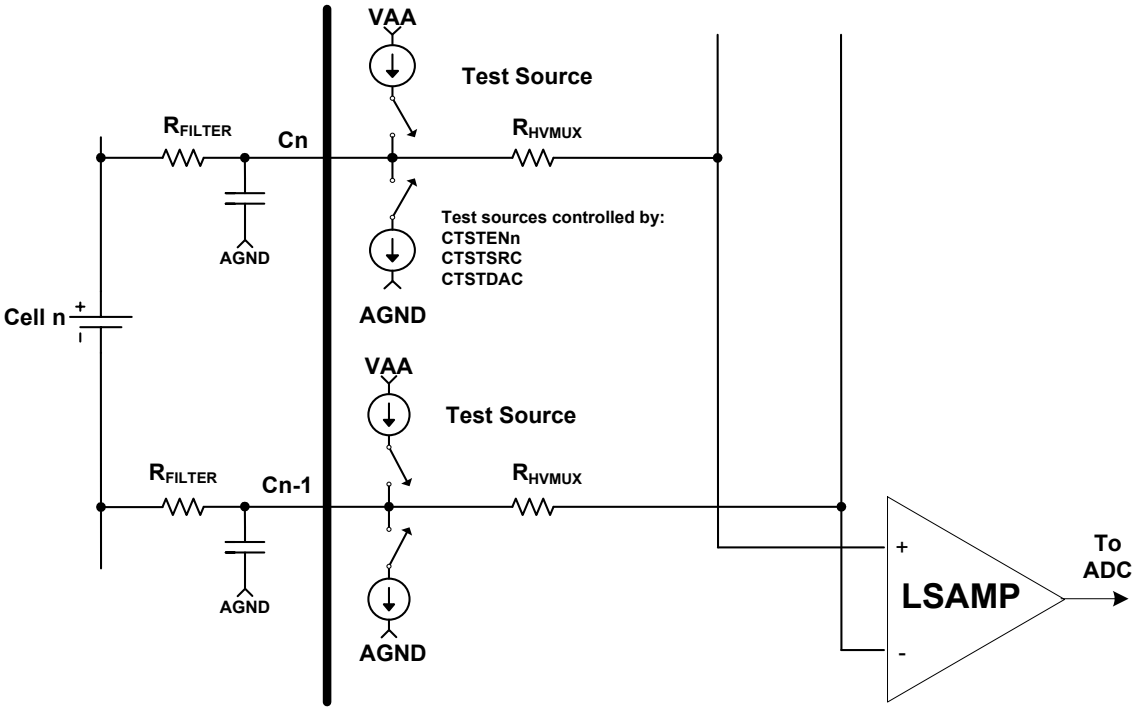


Figure 48. HVMUX Sequencer Diagnostic

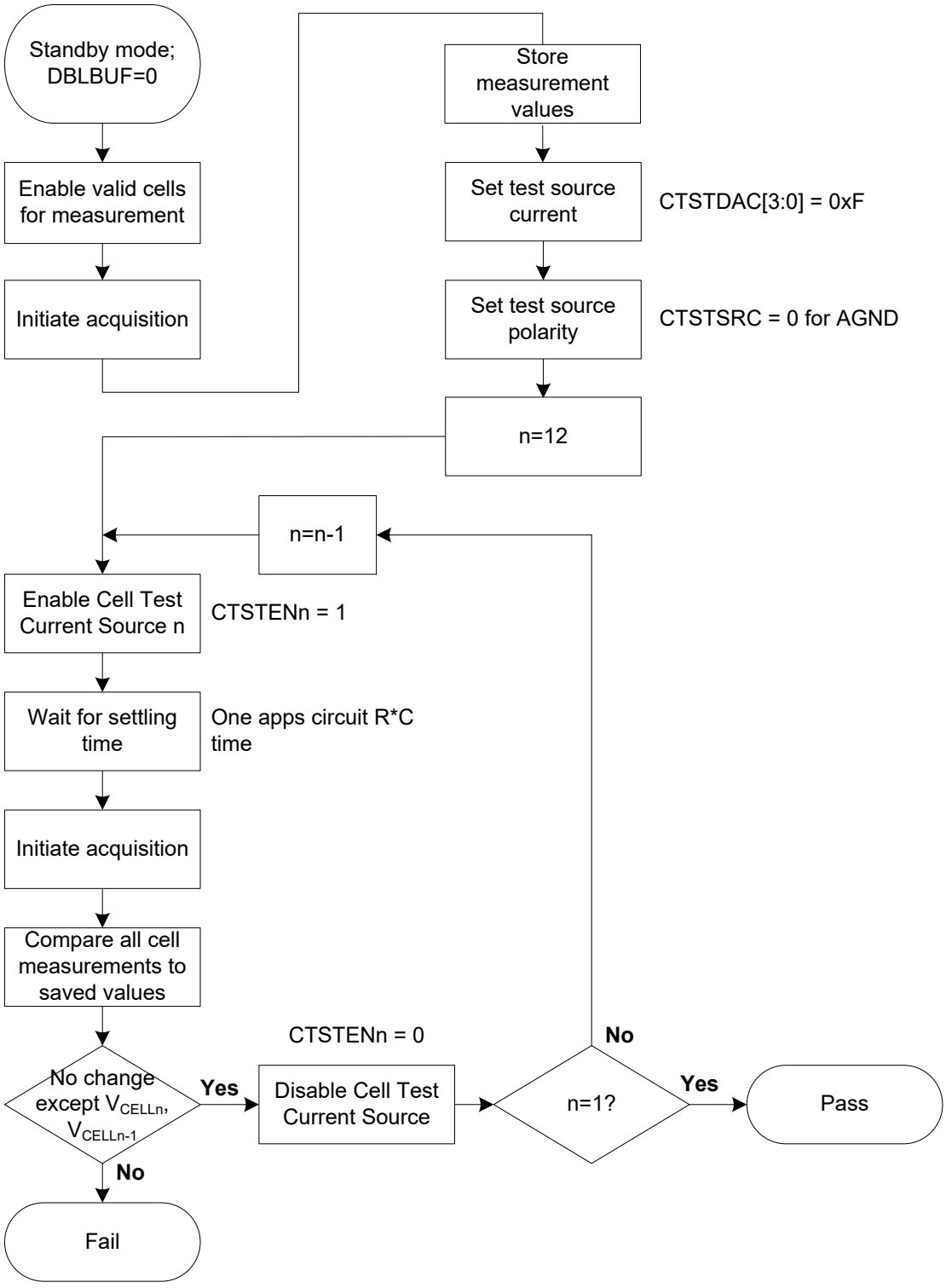


Figure 49. HVMUX Sequencer Diagnostic

ALU Diagnostic

The ALU diagnostic utilizes the ADC test mode (ADCTSTEN = 1) to feed data from specific test registers directly into the ALU instead of from the ADC conversion. The host can write different data combinations to the test registers in this mode to provide test coverage for all ALU and data registers (CELLn, VBLKP, DIAG, and AUXINn) as well as all alerts that are based on the measurement data and the corresponding thresholds (e.g., over-voltage alerts).

The ADCTEST1x registers are used for all odd-numbered samples in oversampling mode as well as in single-sample acquisitions. The ADCTEST2x registers are used for all even-numbered samples (in oversampling mode). The A registers are used in lieu of the first conversion of each measurement and the B registers are used in lieu of the second conversion. After the acquisition, the host may read the measurement data registers and the alert registers and compare the data to expected values to verify the ALU functionality.

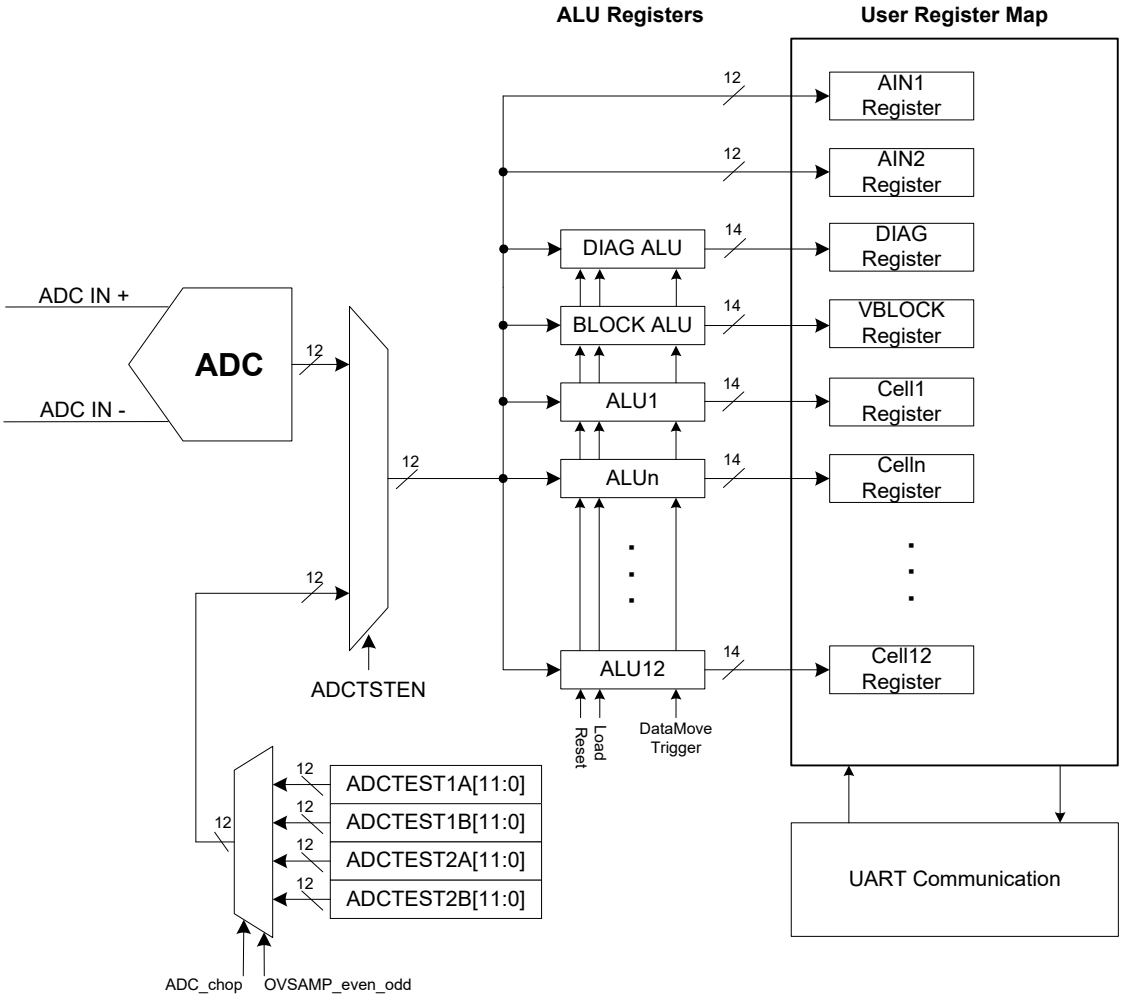


Figure 50. ALU Diagnostic

AUXINn Open Diagnostic

The AUXINn Open diagnostic may be used to detect if the AUXINn pin is open circuit. The diagnostic procedure is shown in Figures 51 and 52.

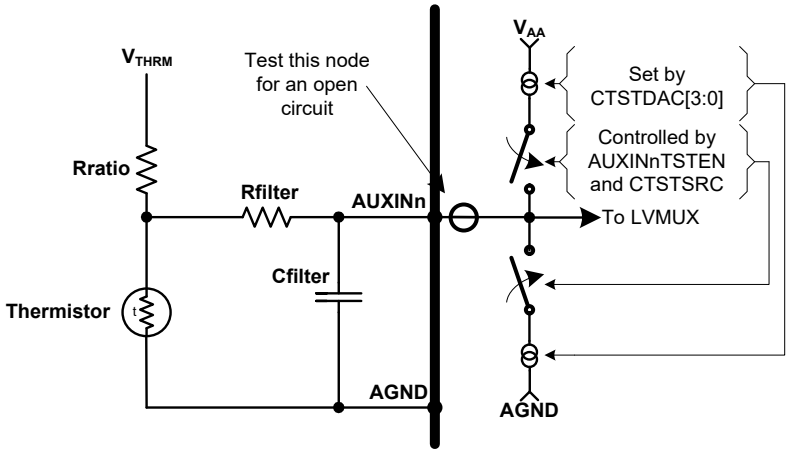


Figure 51. AUXINn Open Diagnostic

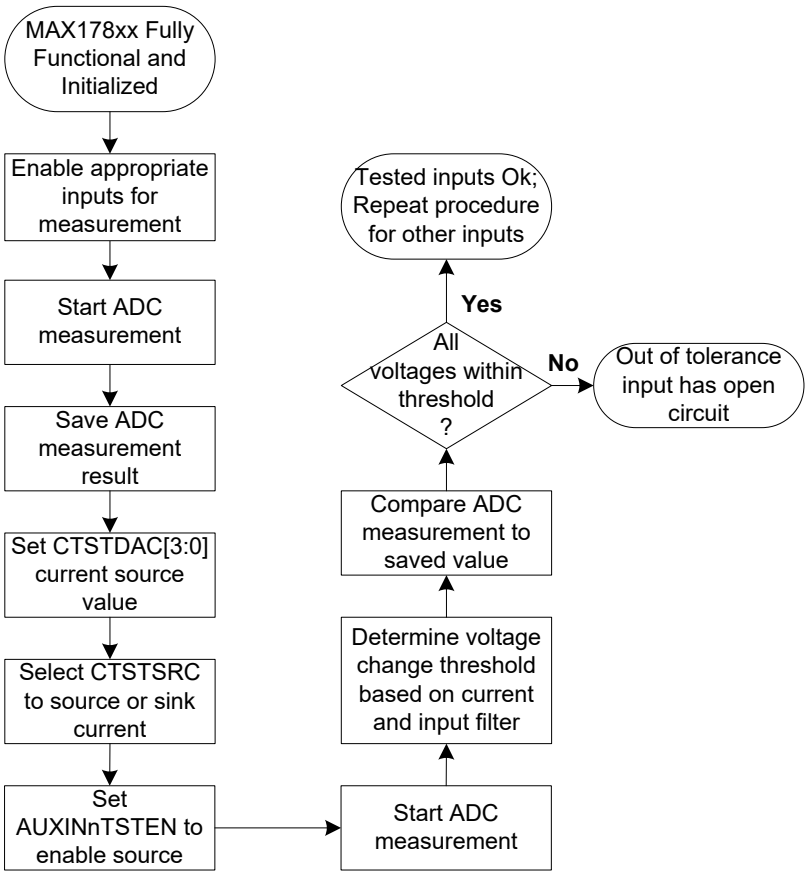


Figure 52. AUXINn Open Diagnostic

Calibration ROM Diagnostic

The CRC for the calibration ROM can be independently computed by the host. Any mismatch between the calculated CRC and the factory CRC indicates that the measurement accuracy may be compromised. The factory CRC, ROMCRC[7:0], is stored in the ID2 register.

The CRC for the calibration ROM uses the same polynomial as the CRC-8 PEC byte and is performed on addresses C0h to CAh, CFh, ID1, and ID2 and processed in the order shown in Table 41, least-significant bit first. Registers CAL11, CAL12, CAL13, and CAL14 are excluded from the calculation. Also, certain ROM bits must be zeroed prior to performing the calculation using the bit-wise AND masks in Table 41.

Table 42. CRC Bit Mask

Order	Address	Name	Bit-Wise AND Mask
1	0xC0	CAL0	0x003F
2	0xC1	CAL1	0x007F
3	0xC2	CAL2	0x3FFF
4	0xC3	CAL3	0xFFFF
5	0xC4	CAL4	0xFFFF
6	0xC5	CAL5	0xFFFF
7	0xC6	CAL6	0xFFFF
8	0xC7	CAL7	0x3F3F
9	0xC8	CAL8	0x003F
10	0xC9	CAL9	0x3FFF
11	0xCA	CAL10	0x0003
12	0xCF	CAL15	0x007F
13	0x0D	ID1	0xFFFF
14	0x0E	ID2	0x00FF

Applications Information

Vehicle Applications

Battery cells can use various chemistries such as NIMH, Li-ion, SuperCap or Lead-Acid. SuperCap cells are used in fast-charge applications such as energy storage for regenerative braking. An electric vehicle system may require a high-voltage battery pack containing up to 200 Li-ion cells or up to 500 NiMH cells.

A battery module is a number of cells connected in series that can be connected with other modules to build a high-voltage battery pack as shown in Figure 53. The modularity allows for economy, configurability, quick assembly, and serviceability. The minimum number of cells connected to any one device is limited by the device's minimum operating voltage. The 9V minimum for V_{DCIN} usually requires at least 2 Li-ion, 6 NiMH or 6 SuperCap cells per module.

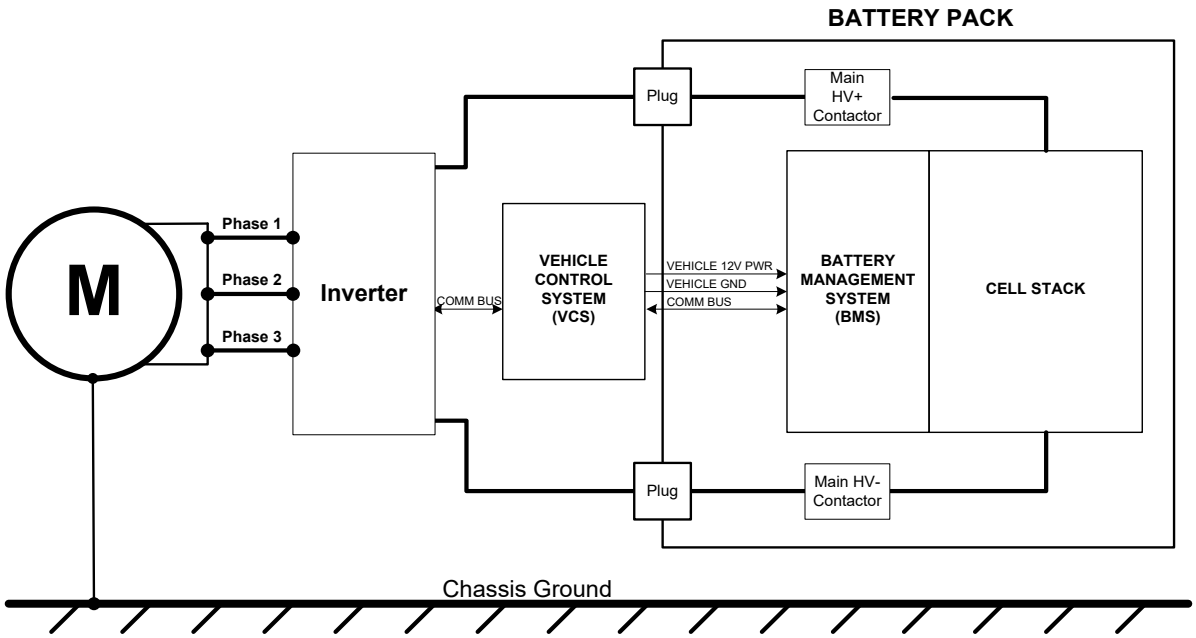


Figure 53. Electric Vehicle System

Battery Management Systems

Daisy-Chain System

A daisy-chain system employs a single data link between the host and all the battery modules. The daisy-chain method reduces cost and requires only a single isolator between the lowest module and the host.

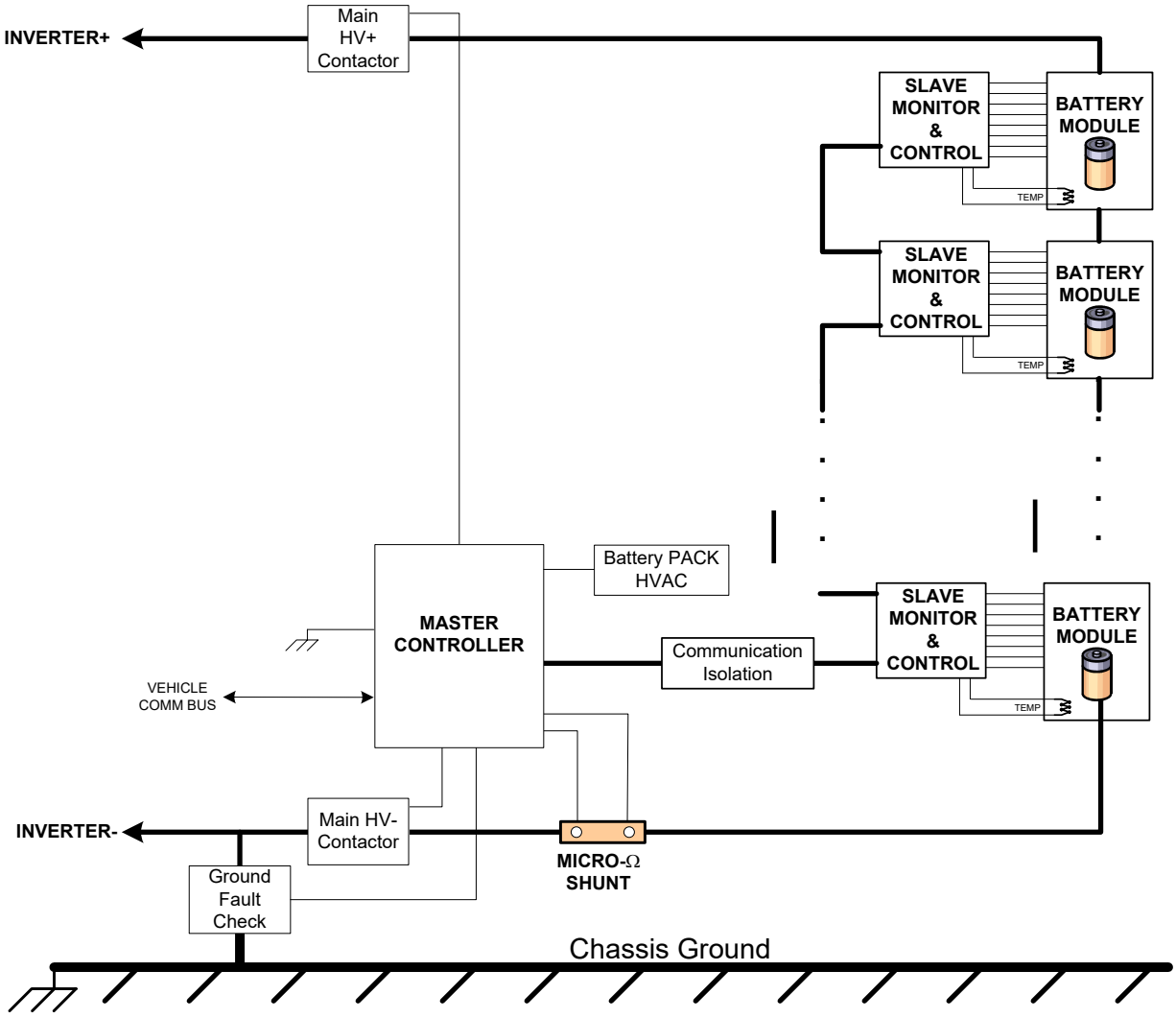


Figure 54. Daisy-Chain System

Distributed-Module Communication

A distributed-module system employs a separate data link and isolator between each battery module and the host with an associated increase in cost.

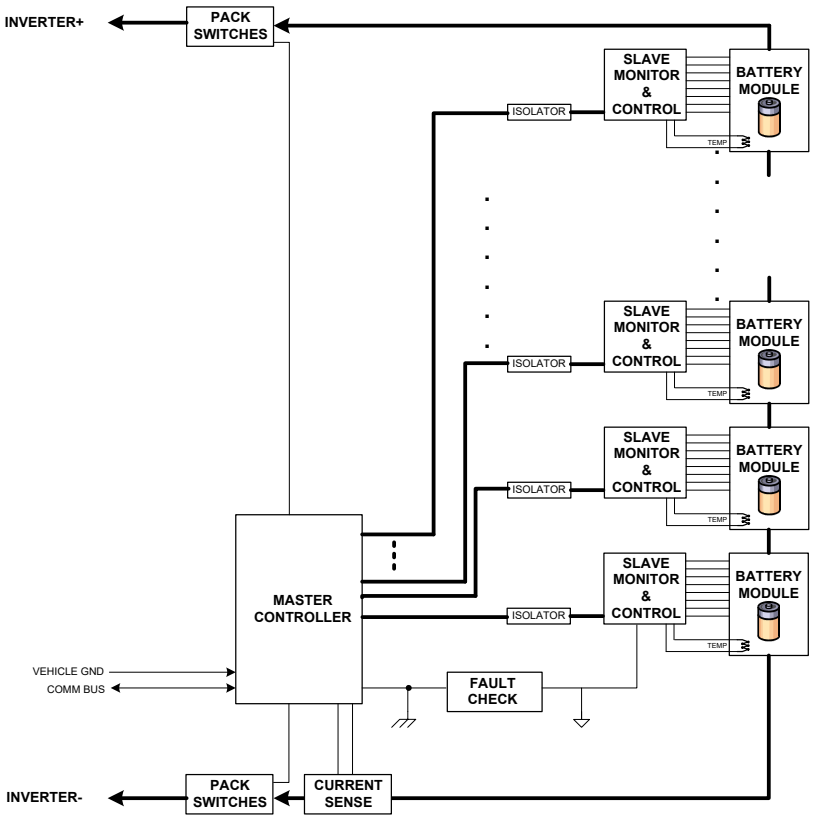


Figure 55. Distributed System

Combining MAX17823B and MAX17880 Devices

The MAX17823B can be used stand-alone or in conjunction with the MAX17880. For systems containing both types of devices, the simplest implementation is to segregate them into two separate daisy chains. The separate daisy-chains increase the reliability and simplify device addressing.

However, if the system employs only a single daisy-chain, the companion devices must coexist in the same daisy-chain. To mitigate any potential addressing conflicts, the battery-management UART protocol allows the host to create a separate address space for each type of device. The host creates the separate address spaces during initialization of the daisy-chain. The host issues separate HELLOALL commands for each type of device using 57h for MAX17823B and A7h for MAX17880. Each type of device will ignore the HELLOALL command intended for the other type. While it does not matter which HELLOALL is issued first, the host must ascertain the address returned from the first HELLOALL command, which is the last device address incremented by one. That value may then be used as the first address sent with the second HELLOALL command. In this manner, separate address spaces are created for each type of device.

Acquisition Latency for Daisy-Chain Systems

A maximum 3-bit delay (1.5µs at 2Mbps) is incurred as any command propagates through each daisy-chain device. For example, for an 8-device stack, a maximum 12µs delay is incurred. This allows all 8 acquisitions to occur within 12µs of each other.

Power Supply Connection

Both internal and external protection circuits permit the device to derive its supply directly from the battery module voltage. The circuits protect against transients such as those that may occur when the battery voltage is first connected to the device, when the vehicle inverter is connected to the battery stack, or during charge/discharge transitions such as regenerative braking. The internal circuits include 72V-tolerant battery inputs and a high noise rejection ratio (PSRR) for the internal low-voltage regulator.

The external protection circuit shown in Figure 56 filters and clamps the DCIN input. During negative voltage transients, the filter capacitor maintains power the device through the transient.

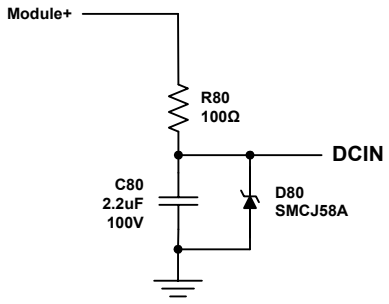


Figure 56. Power Supply Connection

For maximum measurement accuracy, dedicated wires separate from the cell sense wires should be used for the power supply connection (Kelvin sense). This is to eliminate voltage drops in the sense wires induced by supply current. If the application can tolerate the induced error, the supply wires can serve as the sense wires to reduce the wire count.

Connecting Cell Inputs

If the battery stack contains less than 12 cells, the lowest-order inputs (e.g. C1 and C0) should be utilized first and connected to the lowest common-mode signals. Any unused cell inputs should be shorted together and unused switch inputs should be shorted together. The TOPCELL register must also be configured for stacks with less than 12 cells to mask out any false alerts corresponding to the unused channels.

External Cell-Balancing

The cell-balancing current can be switched by external transistors if more power dissipation is required. The internal switches can be used to switch the external transistors and the power is limited by external current-limiting resistors.

External Cell-Balancing using FET Switches

An application circuit for cell-balancing that employs FET switches is shown in Figure 57. $Q_{BALANCE}$ is selected for low V_T that meets the minimum V_{CELLn} requirements of the application during balancing. D_{GATE} protects $Q_{BALANCE}$ from reverse V_{GS} voltage during a hot-plug event. R_{GATE} protects the device by limiting the hot-plug inrush current. C_{GATE} may be added to attenuate transient noise coupled from the drain to the gate to maintain the transistor bias. The cell-balancing current is limited by $R_{BALANCE}$.

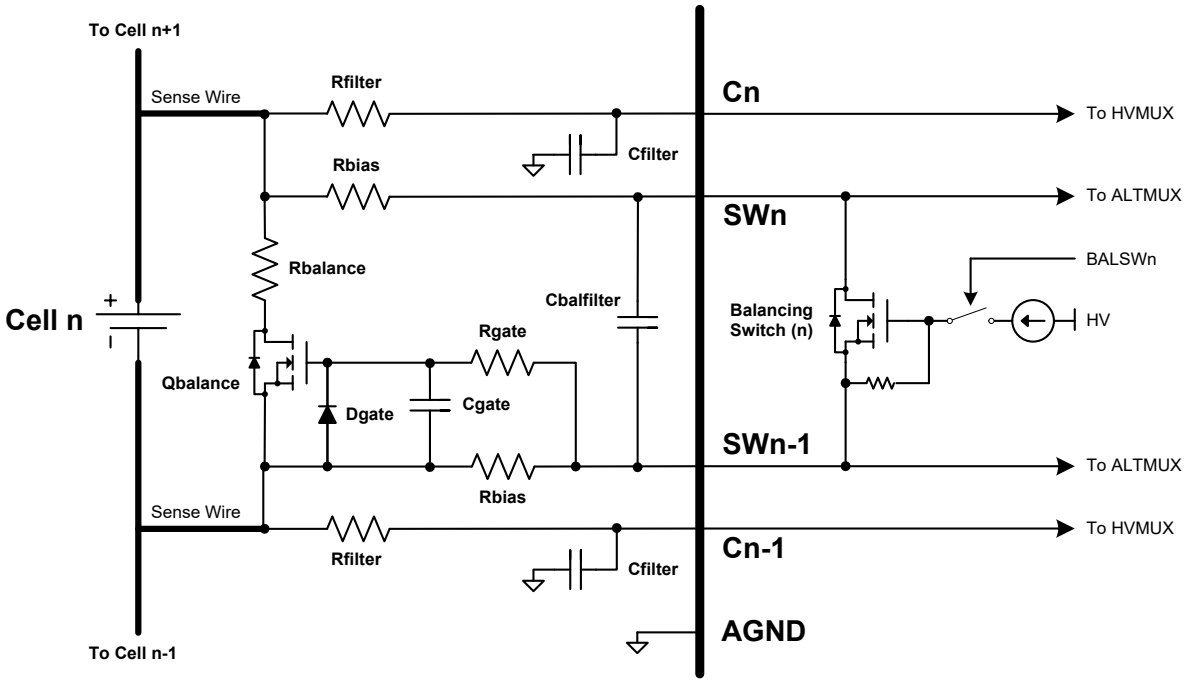


Figure 57. External Balancing (FET)

Table 43. FET Balancing Components

Component Name	Typical Value or Part	Function
R_{BIAS}	1kΩ	Voltage divider for transistor bias
R_{GATE}	100Ω	Hot-plug current-limiting resistor
D_{GATE}	S1B	Reverse-voltage gate protection
C_{GATE}	1nF	Transient V_{GS} suppression
$R_{BALANCE}$	per application	Balancing current-limiting resistor
$Q_{BALANCE}$	SQ2310ES	External switch

External Cell-Balancing using BJT Switches

An application circuit for cell-balancing that employs BJT switches is shown in Figure 58. $Q_{BALANCE}$ is selected for power dissipation based on the I_B drive current available and the cell-balancing current. D_{BASE} protects $Q_{BALANCE}$ from negative V_{GS} during hot-plug events. R_{BASE} protects the device by limiting the hot-plug inrush current. The cell-balancing current is limited by $R_{BALANCE}$.

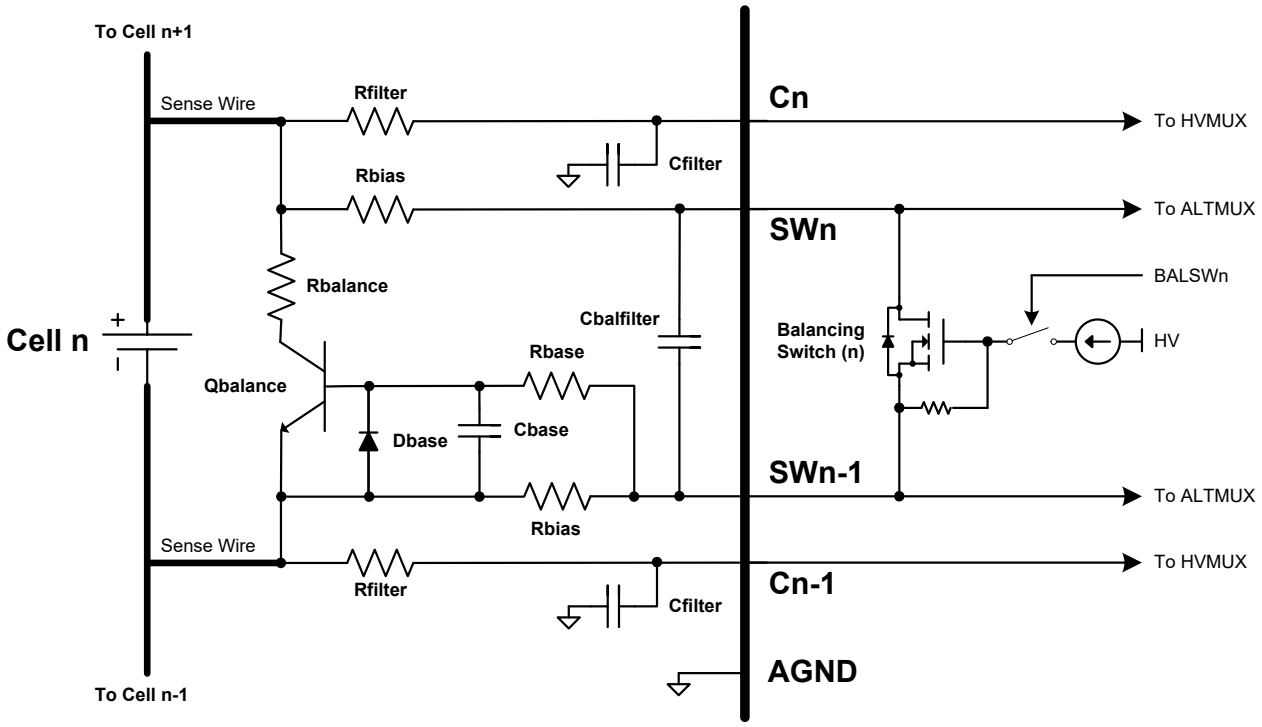


Figure 58. External Cell Balancing (BJT)

Table 44. BJT Balancing Components

Component Name	Typical Value or Part	Function
R_{BIAS}	22Ω	Voltage divider for transistor bias
R_{BASE}	15Ω	Hot-plug current-limiting resistor
D_{BASE}	S1B	Reverse emitter-base voltage protection
C_{BASE}	1nF	Transient V_{BE} suppression
$R_{BALANCE}$	per balancing current requirements	Balancing current-limiting resistor
$Q_{BALANCE}$	NST489AMT1	External switch

External Cell-Balancing Short-Circuit Detection

A short-circuit fault in the external balancing path results in continuous current flow through $R_{BALANCE}$ and $Q_{BALANCE}$. To detect this fault, the voltage drop across the sense-wire parasitic resistance must be measurable. A very small series resistor may added for this purpose.

UART Interface

The UART pins also employ both internal and external circuits to protect against noise. The recommended external filters are shown in Figure 60. ESD protection is shown in Figures 62 and 63.

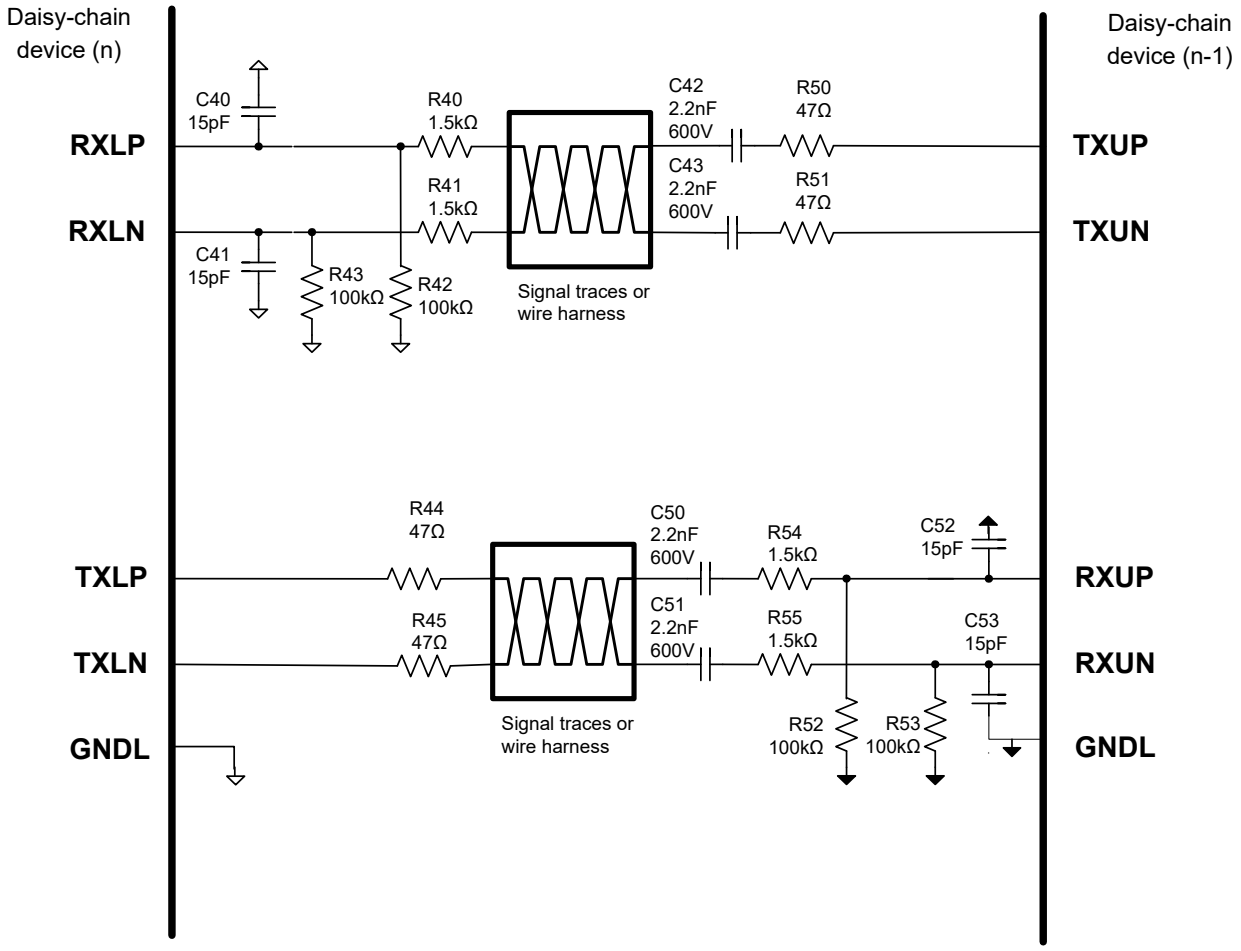


Figure 60. UART Connection

High-Z Idle Mode

The high-Z idle mode lowers radiated emissions from wire harnesses by minimizing the charging and discharging of the AC-coupling capacitors when entering and exiting the idle mode. The application circuit shown in Figure 61 uses a weak resistor divider to bias the TX lines to V_{DDL} during the high-Z idle period and PNP transistor clamps to limit the maximum voltage at the TX pins during high noise injection. The resistor divider and PNP clamps are not needed for applications utilizing only the low-Z mode. The low-Z and high-Z idle modes both exhibit a similar immunity to noise injection. Low-Z mode may be preferred for ports driving inductive loads to minimize ringing.

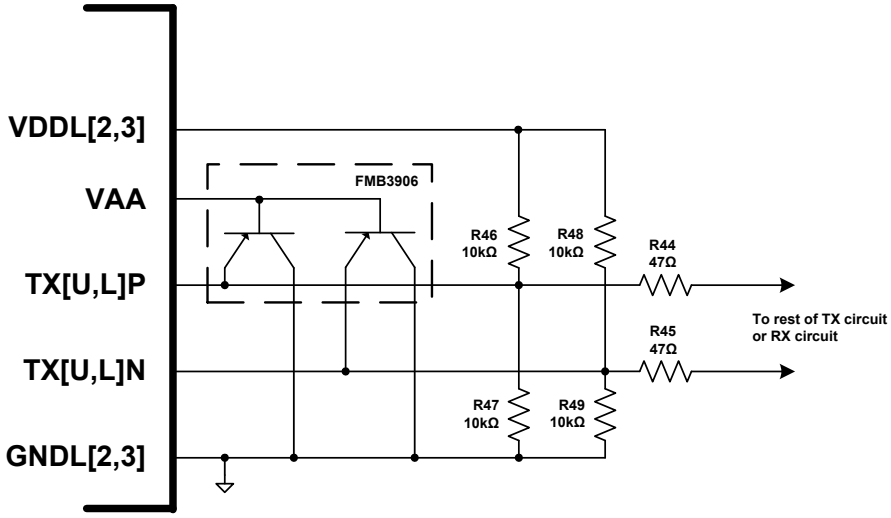


Figure 61. High-Z Idle Mode Application Circuit

UART Supplemental ESD Protection

The UART ports may require supplemental protection to meet IEC61000-4-2 requirements for contact discharge. The recommended circuits to meet ±8kV protection levels are shown in Figures 62 and 63. The protection components should be placed as near as possible to the signal's entry point on the PCB.

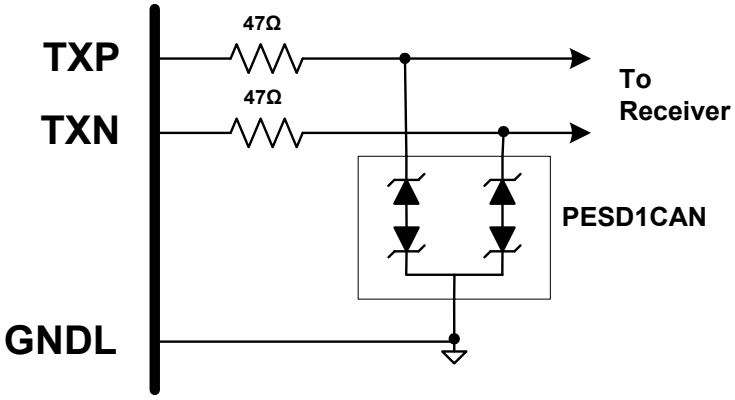


Figure 62. External ESD Protection for UART TX Ports

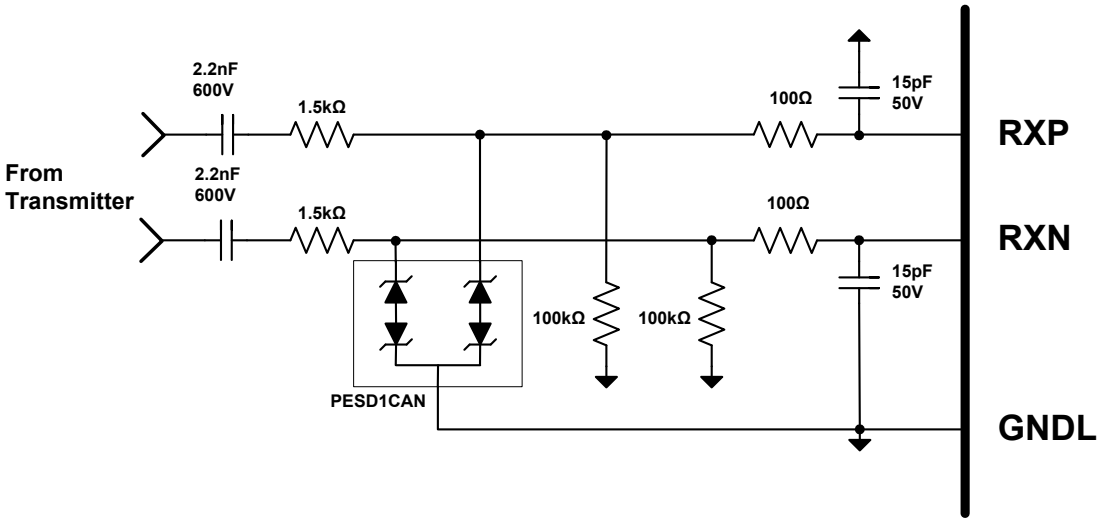


Figure 63. External ESD Protection for UART RX Ports

Single-Ended RX Mode

To configure the lower port for single-ended RX mode, the RXLP input is connected to digital ground and the RXLN input receives the inverted signal, just as it does for differential mode. If the host cannot transmit inverted data then the signal must be inverted as shown in Figure 64. Transmitter operation is not affected. If the up-stack device is single-ended then only the TXUN signal is required. **Note:** In single-ended mode, SHDNL must be driven externally.

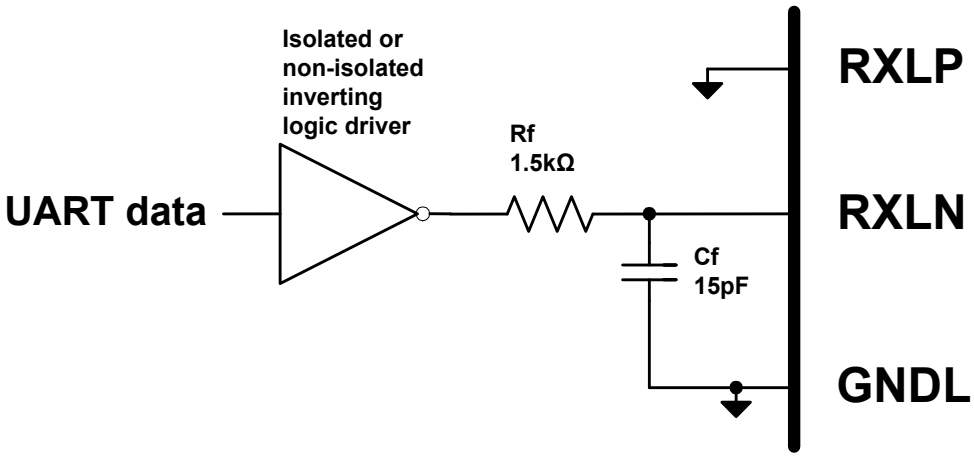


Figure 64. Application Circuit for Single-Ended Mode

UART Isolation

The UART is expected to communicate reliably in noisy high-power battery environments where both high dV/dt supply noise and common-mode current injection induced by electromagnetic fields are prevalent. Common-mode currents may also be induced by parasitic coupling of the system to a reference node such as a battery or vehicle chassis. The daisy-chain physical layer is designed for maximum noise immunity.

The AC-coupled differential communication architecture has a ±30V common-mode range and +6V differential swing. This range is in addition to the static common-mode voltage across the AC-coupling capacitors between modules. Transmitter drivers have low internal impedance and are source-terminated by the application circuit so that impedances are well-matched in the high and low driver states. This architecture minimizes differential noise induced by common-mode current injection. The receiver inputs are filtered above the fundamental communication frequency to prevent high-frequency noise from entering the device. The system is designed for use with isolation transformers or optocouplers to provide an even higher degree of common-mode noise rejection in circuit locations where extremely large common-mode noise is present, such as between vehicle chassis and the high-voltage battery pack terminals.

Since a mid-pack service disconnect safety switch is present in many battery packs, the device is designed to communicate with the entire daisy-chain whether the service-disconnect switch is engaged or open. This is possible with daisy-chains that employ capacitor isolation.

UART Transformer Isolation

The UART ports may be transformer-coupled because of their DC-balanced differential design. Transformer coupling between the MAX17841B interface and the MAX17823B provides excellent isolation and common-mode noise rejection. The center-tap of a signal transformer may be used to enhance common-mode rejection by AC-coupling the node to local ground. Common-mode currents that are able to pass through the parasitic coupling of the primary and secondary are shunted to ground to make a very effective common-mode noise filter.

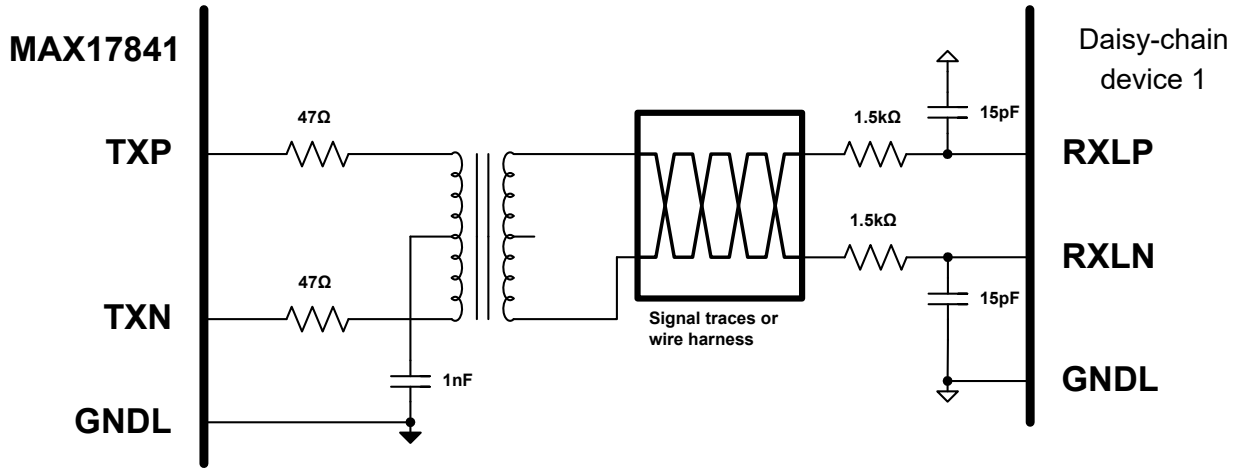


Figure 65. UART Transformer Isolation

UART Optical Isolation

The daisy-chain may use optical isolation instead of transformer or capacitor isolation as shown in Figure 66.

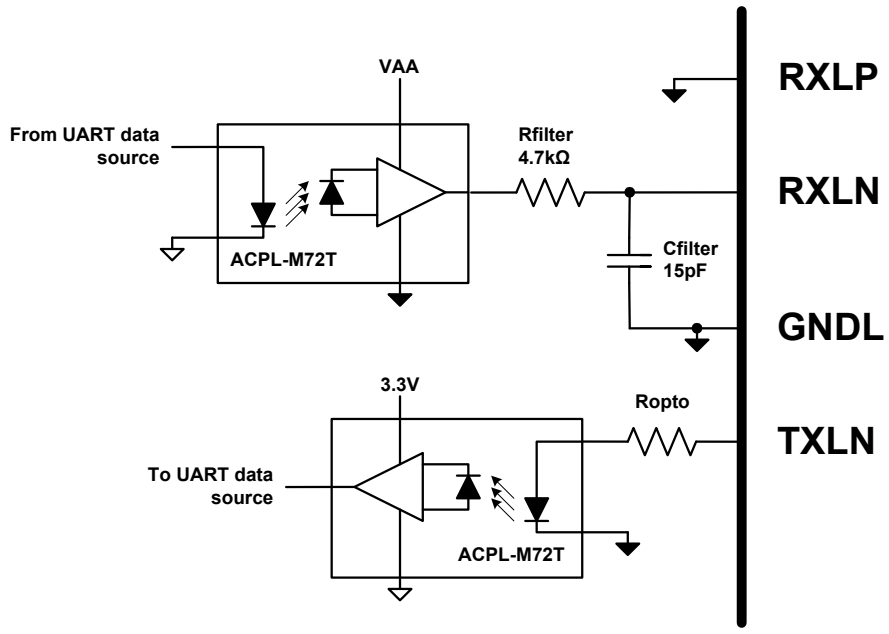


Figure 66. UART Optical Isolation

Device Initialization Sequence

Immediately after reset, all device addresses are set to 0x00 and the UART baud rate and receive modes have not been auto-detected. Therefore the following initialization sequence is recommended after every reset or after any change to the hardware configuration:

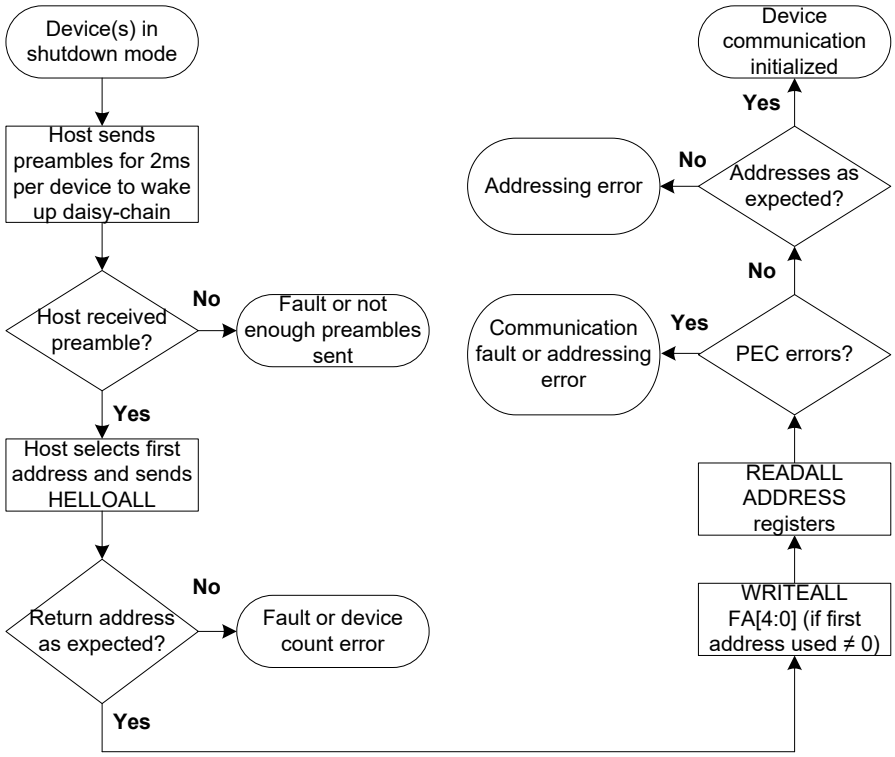


Figure 67. Device Initialization Sequence

After the daisy-chain is initialized, each device should be configured for operation as follows:

1. Perform a READALL of the status registers.
   - The ALRTRST bit should be set in all devices to signify a reset occurred.
   - Check for other unexpected alerts.
2. Clear the ALRTRST bit on each device so that future unintended resets may be detected.
3. Change configuration registers as necessary with WRITEALL commands:
   - Configure the alert enables and alert thresholds as required by the application.
   - Configure the acquisition mode.
4. Perform all necessary key-on diagnostics.
5. Start the acquisition cycle.
6. Continuously monitor diagnostic and alert status bits.
7. Periodically perform additional diagnostics as required by the application.

Error Checking

Data integrity is provided by Manchester-encoding, parity, character framing, and Packet Error Checking (PEC). The combination of these features verify stage-to-stage communication both in the write and read directions with a HD (Hamming Distance) value of 6 for commands with a length up to 247 bits (counted prior to Manchester-encoding and character framing. This is equivalent to the longest possible command packet for a daisy-chain of up to 13 devices. The data-check byte is present in the READALL and READDEVICE commands to verify that the entire command propagated without errors. Using the data-check and PEC bytes, complete transaction integrity for READALL and READDEVICE command packets can be verified.

PEC Errors

If the device receiver receives an invalid PEC byte, the ALRTPEC bit is set in the STATUS register. A device does not execute any write command unless the received PEC matches the calculated PEC so to verify the write command execution, the host should perform a READALL to verify the contents of the written register.

For returned read packets, the host should store the received data, perform the PEC calculation, and compare the results to the received PEC byte before considering the data to be valid. To support PEC, the host must implement a CRC-8 (8-bit cyclic redundancy check) encoding and decoding algorithm based on the following polynomial:

$$P(x) = x^8 + x^6 + x^3 + x^2 + 1$$

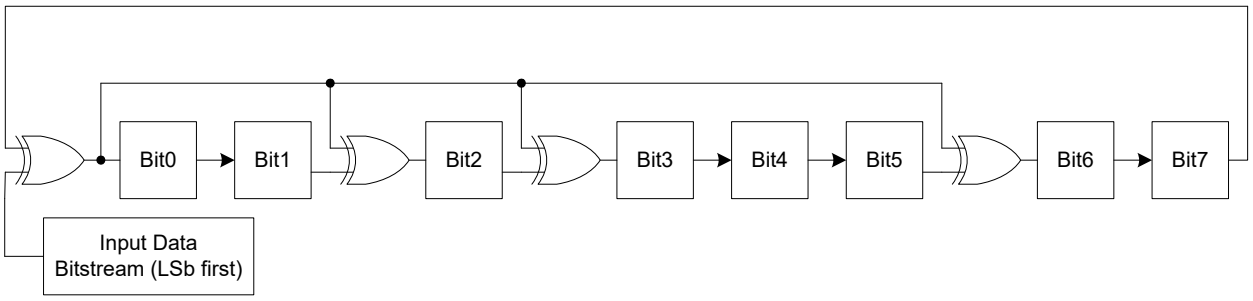


Figure 68. CRC Calculation

The host uses the algorithm to process all bytes received in the command packet prior to the PEC byte itself. Neither the PEC nor the alive-counter bytes are part of the calculation. The bits are processed in the order they are received, LSB first. A byte-wise pseudo-code algorithm is shown in Figure 69, but lookup table solutions are also possible to reduce host calculation time.

For commonly issued command packets, the host can pre-calculate (hard-code) the PEC byte. For commonly-used partial packets, the CRC value of a partial calculation may be used as the initial value for a subsequent run-time calculation.

```
Function PEC_Calculation(ByteList(), NumberOfBytes, CRCByte)
{
   // CRCByte is initialized to 0 for each ByteList in this implementation, where
   // ByteList contains all bytes of a single command.  It is passed into the
   // function in case a partial ByteList calculation is needed.

   // Data is transmitted and calculated in LSb first format
   // Polynomial = x^8+x^6+x^3+x^2+1
   POLY = &HB2   // 10110010b for LSb first

   //Loop once for each byte in the ByteList
   For ByteCounter = 0 to (NumberOfBytes – 1)
   (
      //Bitwise XOR the current CRC value with the ByteList byte
      CRCByte = CRCByte XOR ByteList(Counter1)

      //Process each of the 8 CRCByte remainder bits
      For BitCounter = 1 To 8
      (
         // The LSb should be shifted toward the highest order polynomial
         // coefficient.  This is a right shift for data stored LSb to the right
         // and POLY having high order coefficients stored to the right.

         // Determine if LSb = 1 prior to right shift
         If (CRCByte AND &H01) = 1 Then
            // When LSb = 1, right shift and XOR CRCByte value with 8 LSbs
            // of the polynomial coefficient constant.  “/ 2” must be a true right
            // shift in the target CPU to avoid rounding problems.
            CRCByte = ((CRCByte / 2) XOR POLY)
         Else
            //When LSb = 0, right shift by 1 bit.  “/ 2” must be a true right
            // shift in the target CPU to avoid rounding problems.
            CRCByte = (CRCByte / 2)
         End If

         //Truncate the CRC value to 8 bits if necessary
         CRCByte = CRCByte AND &HFF

         //Proceed to the next bit
         Next BitCounter
      )

      //Operate on the next data byte in the ByteList
      Next ByteCounter
   )

   //  All calculations done; CRCByte value is the CRC byte for ByteList() and
   //  the initial CRCByte value
   Return CRCByte
}
```

Figure 69. PEC Calculation Psuedocode

REGISTER TABLE

ADDRESS	POR	NAME	DESCRIPTION
0x00	8236h	VERSION	Device model and version
0x01	0000h	ADDRESS	Device addresses
0x02	8000h	STATUS	Status flags
0x03	0000h	FMEA1	Failure mode flags 1
0x04	0000h	ALRTCELL	Voltage-fault alert flags
0x05	0000h	ALRTOVCELL	Over-voltage alert flags
0x07	0000h	ALRTUVCELL	Under-voltage alert flags
0x08	0000h	ALRTBALSW	Balancing switch alert flags
0x0A	0F0Fh	MINMAXCELL	Cell number for the highest and lowest voltages measured
0x0B	0000h	FMEA2	Failure mode flags 2
0x0D	XXXXh	ID1	Device ID 1
0x0E	XXXXh	ID2	Device ID 2
0x10	0002h	DEVCFG1	Device configuration 1
0x11	0000h	GPIO	GPIO status and configuration
0x12	0000h	MEASUREEN	Measurement enables
0x13	0000h	SCANCTRL	Acquisition control and status
0x14	0000h	ALRTOVEN	Over-voltage alert enables
0x15	0000h	ALRTUVEN	Under-voltage alert enables
0x18	0000h	TIMERCFG	Timer configuration
0x19	0000h	ACQCFG	Acquisition configuration
0x1A	0000h	BALSWEN	Balancing switch enables
0x1B	0000h	DEVCFG2	Device configuration 2
0x1C	0000h	BALDIAGCFG	Balancing diagnostic configuration
0x1D	0000h	BALSWDCHG	Balancing switch discharge configuration
0x1E	000Ch	TOPCELL	Top cell configuration
0x20	0000h	CELL1	Cell 1 measurement result
0x21	0000h	CELL2	Cell 2 measurement result
0x22	0000h	CELL3	Cell 3 measurement result
0x23	0000h	CELL4	Cell 4 measurement result
0x24	0000h	CELL5	Cell 5 measurement result
0x25	0000h	CELL6	Cell 6 measurement result
0x26	0000h	CELL7	Cell 7 measurement result
0x27	0000h	CELL8	Cell 8 measurement result
0x28	0000h	CELL9	Cell 9 measurement result
0x29	0000h	CELL10	Cell 10 measurement result
0x2A	0000h	CELL11	Cell 11 measurement result
0x2B	0000h	CELL12	Cell 12 measurement result
0x2C	0000h	BLOCK	Block measurement result

0x2D	0000h	AIN1	AUXIN1 measurement result
0x2E	0000h	AIN2	AUXIN2 measurement result
0x2F	0000h	TOTAL	Sum of all cell measurements
0x40	FFFCh	OVTHCLR	Cell over-voltage clear threshold
0x42	FFFCh	OVTHSET	Cell over-voltage set threshold
0x44	0000h	UVTHCLR	Cell under-voltage clear threshold
0x46	0000h	UVTHSET	Cell under-voltage set threshold
0x48	FFFCh	MSMTCH	Cell mismatch threshold
0x49	0000h	AINOT	AUXIN over-temperature threshold
0x4A	FFF0h	AINUT	AUXIN under-temperature threshold
0x4B	0000h	BALSHRTTHR	Balancing switch diagnostic, short-circuit threshold
0x4C	0000h	BALLOWTHR	Balancing switch diagnostic, on-state low threshold
0x4D	0000h	BALHIGHTHR	Balancing switch diagnostic, on-state high threshold
0x50	0000h	DIAG	Diagnostic measurement result
0x51	0000h	DIAGCFG	Diagnostic configuration
0x52	0000h	CTSTCFG	Test source configuration
0x57	0000h	ADCTEST1A	User-specified data for ALU diagnostic
0x58	0000h	ADCTEST1B	User-specified data for ALU diagnostic
0x59	0000h	ADCTEST2A	User-specified data for ALU diagnostic
0x5A	0000h	ADCTEST2B	User-specified data for ALU diagnostic

VERSION Register (address 0x00)

<table>
<tr><th>Bit</th><th>POR</th><th>Name</th><th>Description</th></tr>
<tr><td>D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4</td><td>823h</td><td>MOD[11:0]</td><td>Model number. Always reads 823h.</td></tr>
<tr><td>D3
D2
D1
D0</td><td>xh</td><td>VER[3:0]</td><td>Die version per table below:
<table><tr><th>Version</th><th>VER[3:0]</th></tr><tr><td>MAX17823B</td><td>6h</td></tr><tr><td>Reserved</td><td>5h</td></tr><tr><td>Reserved</td><td>4h</td></tr><tr><td>MAX17823</td><td>3h</td></tr><tr><td>MAX17823</td><td>2h</td></tr><tr><td>MAX17823</td><td>1h</td></tr></table></td></tr>
</table>

ADDRESS Register (address 0x01)

Bit	POR	Name	Description
D15 D14 D13	0	Reserved	Always reads logic zero.
D12 D11 D10 D9 D8	0	FA[4:0]	Address of the device connected to the host (first address). If the host uses a first address other than 0x00 in the HELLOALL command, then the host must write that first address to all devices in the daisy-chain with a WRITEALL command. READALL commands require that FA[4:0] and DA[4:0] be correct in order for the data-check and PEC features to function as intended.
D7 D6 D5	0	Reserved	Always reads logic zero.
D4 D3 D2 D1 D0	0	DA[4:0]	Device address written by the HELLOALL command as it propagates up the daisy-chain and is automatically incremented for each device. The host must choose a first address so that the last device address will not exceed the maximum address of 0x1F during the HELLOALL command. Writing has no effect except with a HELLOALL command while ADDRUNLOCK = 1.

STATUS Register (address 0x02)

Bit	POR	Name	Description
D15	1	ALRTRST	Indicates a power-on reset event occurred. Clear after power-on and after a successful HELLOALL to detect future resets. Writing to a logic one has no effect.
D14	0	ALRTOV	Bit-wise logical OR of ALRTOVCELL[15:0]. Read-only.
D13	0	ALRTUV	Bit-wise logical OR of ALRTUVCELL[15:0]. Read-only.
D12	0	ALRTSHDNL	Indicates $V_{SHDNL} < V_{IL}$. Read during shutdown diagnostic when VAA > $V_{PORFALL}$. Cleared by writing to logic zero or POR. Writing to a logic one has no effect.
D11	0	ALRTSHDNLRT	Indicates $V_{SHDNL} < V_{IL}$. Read during shutdown diagnostic when VAA > $V_{PORFALL}$. Read-only.
D10	0	ALRTMSMTCH	Indicates $V_{MAX} - V_{MIN} > V_{MSMTCH}$. Cleared at next acquisition if the condition is false. Read-only.
D9	0	ALRTTCOLD	Logical OR of ALRTOVAIN0 and ALRTOVAIN1. Read-only.
D8	0	ALRTTHOT	Logical OR of ALRTUVAIN0 and ALRTUVAIN1. Read-only.
D7	0	ALRTPEC	Indicates a received character contained a PEC error. Cleared only by writing to logic zero. Writing to a logic one has no effect.
D6 D5	0	Reserved	Always reads logic zero.
D4	0	ALRTMAN	Indicates that a character received by the lower UART contained a Manchester error. Cleared only by writing to logic zero. Writing to a logic one has no effect.
D3	0	0	Write ignored, Read back '0'
D2	0	ALRTPAR	Indicates that a character received by the lower UART contained a parity error. Cleared only by writing to logic zero. Writing to logic one has no effect.
D1	0	ALRTFMEA2	Bit-wise logical OR of FMEA2[15:0]. Read-only.
D0	0	ALRTFMEA1	Bit-wise logical OR of FMEA1[15:0]. Read-only.

FMEA1 Register (address 0x03)

Bit	POR	Name	Description
D15	0	ALRTOSC1	Indicates that the 32kHz oscillator frequency is not within ±5% of its expected value. The status is updated every two cycles (32kHz). Cleared only by writing to logic zero. Writing to a logic one has no effect.
D14	0	ALRTOSC2	Same as ALRTOSC1 (redundant alert). Cleared only by writing to logic zero. Writing to a logic one has no effect.
D13	0	0	Always reads logic zero.
D12	0	ALRTCOMMSEU1	Indicates that the UART has placed the upper-port receiver in single-ended mode based on the first preamble received after POR. This bit is not set until the ALRTRST bit is cleared. Read-only.
D11	0	ALRTCOMMSEL1	Indicates that the UART has placed the lower-port receiver in single-ended mode based on the first preamble received after POR. This bit is not set until the ALRTRST bit is cleared. Read-only.
D10	0	ALRTCOMMSEU2	Same as ALRTCOMMSEU1 (redundant alert) except that it sets before ALRTRST is cleared. Read-only.
D9	0	ALRTCOMMSEL2	Same as ALRTCOMMSEL2 (redundant alert) except that it sets before ALRTRST is cleared. Read-only.
D8	0	ALRTVDDL3	Indicates $V_{DDL3} < V_{VDDL_OC}$. This bit is not set until the ALRTRST bit is cleared and cleared only by writing to logic zero. Writing to a logic one has no effect.
D7	0	ALRTVDDL2	Indicates $V_{DDL2} < V_{VDDL_OC}$. This bit is not set until the ALRTRST bit is cleared and cleared only by writing to logic zero. Writing to a logic one has no effect.
D6	0	ALRTGNDL2	Indicates an open-circuit on the GNDL2 pin. This bit is not set until the ALRTRST bit is cleared and cleared only by writing to logic zero. Writing to a logic one has no effect.
D5	0	ALRTBALSW	Bit-wise logical OR of ALRTBALSW[15:0]. Read-only.
D4	0	ALRTTEMP	Indicates that T_{DIE} > 115°C (120°C typical) or that the diagnostic measurement did not have sufficient settling time (< 50µs) and therefore may not be accurate. Cleared only by writing to logic zero. Writing to a logic one has no effect.
D3	0	ALRTHVUV	Indicates $V_{HV} < V_{HVUV}$. This bit is not set until the ALRTRST bit is cleared and cleared only by writing to logic zero. Writing to logic one has no effect.
D2	0	ALRTGNDL3	Indicates an open-circuit on the GNDL3 pin. This bit is not set until the ALRTRST bit is cleared and cleared only by writing to logic zero. Writing to a logic one has no effect.
D1	0	ALRTVDDL1	Indicates $V_{DDL1} < V_{VDDL_OC}$. This bit is not set until the ALRTRST bit is cleared and cleared only by writing to logic zero. Writing to a logic one has no effect.
D0	0	ALRTGNDL1	Indicates an open-circuit on the GNDL1 pin. This bit is not set until the ALRTRST bit is cleared and cleared only by writing to logic zero. Writing to a logic one has no effect.

ALRTCELL Register (address 0x04)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13	0	ALRTAIN1	Logical OR of ALRTOVAIN1 and ALRTUVAIN1. Read-only.
D12	0	ALRTAIN0	Logical OR of ALRTOVAIN0 and ALRTUVAIN0. Read-only.
D11	0	ALRTCELL[12:1]	ALRTCELL[n] is the logical OR of ALROVCELL[n] and ALRTUVCELL[n]. Read-Only.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

ALRTOVCELL Register (address 0x05)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13	0	ALRTOVAIN1	Indicates V_{AIN1} > AINUT (cold). Cleared at next acquisition if the condition is false. Read-only.
D12	0	ALRTOVAIN0	Indicates V_{AIN0} > AINUT (cold). Cleared at next acquisition if the condition is false. Read-only.
D11	0	ALRTOV[12:1]	ALRTOV[n] indicates V_{CELLN} > V_{OV} (OVTHRSET threshold) if ALRTOVEN[n] = 1. Cleared at next acquisition if the condition is false. Read-only.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

ALRTUVCELL Register (address 0x07)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13	0	ALRTUVAIN1	Indicates V_{AIN1} < AINOT (hot). Cleared at next acquisition if the condition is false. Read-only.
D12	0	ALRTUVAIN0	Indicates V_{AIN0} < AINOT (hot). Cleared at next acquisition if the condition is false. Read-only.
D11	0	ALRTUV[12:1]	ALRTUV[n] indicates V_{CELLn} < V_{UV} (UVTHRSET threshold) if ALRTUVEN[n] = 1. Cleared at next acquisition if the condition is false. Read-only.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

ALRTBALSW Register (address 0x08)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13			
D12			
D11	0	ALRTBALSW[11:0]	ALRTBALSW[n] indicates the corresponding measurement result exceeds the threshold specified by BALSWDIAG[2:0]. Cleared at next acquisition if the condition is false. Read-only.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

MINMAXCELL Register (address 0x0A)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13			
D12			
D11	Fh	MAXCELL[3:0]	Cell number of the maximum cell voltage currently in the measurement registers. If multiple cells have the same maximum value, this field contains the highest cell number with that measurement. Read-only.
D10			
D9			
D8			
D7	0	Reserved	Always reads logic zero.
D6			
D5			
D4			
D3	Fh	MINCELL[3:0]	Cell number of the minimum cell voltage currently in the measurement registers. If multiple cells have the same minimum value, this field contains the highest cell number with that measurement. Read-only.
D2			
D1			
D0			

FMEA2 Register (address 0x0B)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2	0	ALRTHVHDRM	Indicates that V_{HV} - V_{C12} was too low during the acquisition for an accurate measurement. Cleared only by writing to logic zero. Writing to a logic one has no effect.
D1	0	Reserved	Always reads logic zero.
D0	0	ALRTHVOV	Indicates that V_{HV} - V_{DCIN} > V_{HVOV}. This bit is not set until the ALRTRST bit is cleared and cleared only by writing to logic zero. Writing to a logic one has no effect.

ID1 Register (address 0x0D)

Bit	POR	Name	Description
D15	xxxxh	DEVID[15:0]	The two least-significant bytes of the 24-bit factory-programmed device ID. A valid device ID has two or more bits set to logic one. Read-only.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

ID2 Register (address 0x0E)

Bit	POR	Name	Description
D15	xxh	ROMCRC[7:0]	8-bit CRC value computed from the onboard read-only memory. Read-only.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7	xxh	DEVID[23:16]	Most-significant byte of the 24-bit factory-programmed device ID. A valid device ID has two or more bits set to logic one. Read-only.
D6			
D5			
D4			
D3			
D2			
D1			
D0			

DEVCFG1 Register (address 0x10)

Bit	POR	Name	Description
D15	0	Reserved	Reads back the written value.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7	0	FORCEPOR	Enables hard POR by pulling down SHDNL internally. If cleared before the POR occurs, it will disable the active pull-down on SHDNL.
D6	0	ALIVECNTEN	Enables inclusion of alive-counter byte at end of all write and read packets.
D5	0	ADCTSTEN	Enables the ALU test mode. This mode feeds 12-bit data from the ADCTEST registers directly into the ALU instead of from the ADC conversion.
D4	0	SCANTODIS	Disables the acquisition watchdog but does not clear the SCANTIMEOUT flag in the SCANCTRL register if it is set.
D3	0	DBLBUFEN	Enables the double-buffer mode. This mode automatically transfers data from the ALU to the data registers at the start of the next acquisition instead of at the end of the acquisition. This mode may be used in conjunction with the DATAMOVE bit so the host can start an acquisition and then start reading the previous acquisition (during the current acquisition) even if the read cycle takes longer than the acquisition.
D2	0	NOPEC	Disables packet-error checking (PEC).
D1	1	ADDRUNLOCK	Disables write-protection of device address DA[4:0]. Cleared only by HELLOALL command (write-protected).
D0	0	SPOR	Enables soft POR. Writing to a logic zero has no effect. Always reads logic zero.

GPIO Register (address 0x11)

Bit	POR	Name	Description
D15	0	DIR[3:0]	Setting DIR[n] enables GPIOn as an output. Default state is high-impedance input.
D14			
D13			
D12			
D11	0	RD[3:0]	Indicates the current logic state of each GPIOn pin input buffer. The logic state is sampled at the end of the parity bit of the register address byte during a read of this register. Read-only.
D10			
D9			
D8			
D7	0	GPIO3TMR	Enables the GPIO3 timer mode. This mode overrides DIR[3] and DRV[3] and drives GPIO3 to logic one when the timer is counting, and drives to logic zero when the timer times out. Emergency discharge mode (EMGCYDCHG=1) automatically enables the GPIO3 timer mode.
D6	0	Reserved	Always reads logic zero.
D5			
D4			
D3	0	DRV[3:0]	Setting DRV[n] sets GPIOn to logic one if DIR[n] is set.
D2			
D1			
D0			

MEASUREEN Register (address 0x12)

Bit	POR	Name	Description
D15	0	BLKCONNECT	Connects the voltage divider to the VBLKP pin. Must be enabled prior to the VBLOCK measurement.
D14	0	BLOCKEN	Enables measurement of the VBLKP input in the acquisition mode.
D13	0	AIN2EN	Enables measurement of the AUXIN2 input in the acquisition mode.
D12	0	AIN1EN	Enables measurement of the AUXIN1 input in the acquisition mode.
D11	0	CELLEN[12:1]	Enables measurement of the respective cell in the acquisition mode. Disabled channels result in a measurement value of 0000h.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

SCANCTRL Register (address 0x13)

<table>
<tr><th>Bit</th><th>POR</th><th>Name</th><th>Description</th></tr>
<tr><td>D15</td><td>0</td><td>SCANDONE</td><td>Indicates the acquisition has completed. Cleared only by writing it to logic zero to detect completion of the next acquisition. Writing to logic 1 has no effect. A new acquisition will not commence if this bit is set.</td></tr>
<tr><td>D14</td><td>0</td><td>SCANTIMEOUT</td><td>Indicates the acquisition did not complete in the expected period of time. The timeout depends on the oversampling configuration. Cleared only by writing it to logic zero to allow detection of future timeout events. The acquisition watchdog can be disabled by setting SCANTOEN in the DEVCFG1 register.</td></tr>
<tr><td>D13</td><td>0</td><td>DATARDY</td><td>Indicates the measurement data from the acquisition has been transferred from the ALU to the data registers and may now be read. Data for all measurement registers and MIN/MAX/TOTAL is transferred at the same time. Cleared by writing it to logic zero to allow detection of the next data transfer. Writing to logic one has no effect.</td></tr>
<tr><td>D12
D11</td><td>0</td><td>Reserved</td><td>Always reads logic zero.</td></tr>
<tr><td>D10
D9
D8</td><td>0</td><td>BALSWDIAG[2:0]</td><td>Configures the cell-balancing switch diagnostic modes per table below. When selected, these modes effectively override the BALSWEN, MEASUREEN, ALTMUXSEL, and POLARITY configurations during the acquisition mode and update the ALRTBALSW register per the BALHIGHTHR and BALLOWTHR thresholds. Refer to Diagnostic section for details.

<table>
<tr><th>BALSWDIAG[2:0]</th><th>Diagnostic Test</th></tr>
<tr><td>000</td><td>None</td></tr>
<tr><td>001</td><td>Balancing Switch Short</td></tr>
<tr><td>010</td><td>Balancing Switch Open</td></tr>
<tr><td>011</td><td>None</td></tr>
<tr><td>100</td><td>None</td></tr>
<tr><td>101</td><td>Cell Sense Open Odds</td></tr>
<tr><td>110</td><td>Cell Sense Open Evens</td></tr>
<tr><td>111</td><td>None</td></tr>
</table></td></tr>
<tr><td>D7</td><td>0</td><td>POLARITY</td><td>Enables bipolar mode for ADC (input range is -2.5V to 2.5V). Default is unipolar mode (input range is 0V to 5V)</td></tr>
<tr><td>D6
D5
D4</td><td>0</td><td>OVSAMPL[2:0]</td><td>Configures for the number oversamples in the acquisition per table below:

<table>
<tr><th>OVSAMPL [2:0]</th><th>Oversamples</th></tr>
<tr><td>000</td><td>1</td></tr>
<tr><td>001</td><td>4</td></tr>
<tr><td>010</td><td>8</td></tr>
<tr><td>011</td><td>16</td></tr>
<tr><td>100</td><td>32</td></tr>
<tr><td>101</td><td>64</td></tr>
<tr><td>110</td><td>128</td></tr>
<tr><td>111</td><td>128</td></tr>
</table></td></tr>
<tr><td>D3</td><td>0</td><td>0</td><td>Always reads logic zero.</td></tr>
<tr><td>D2</td><td>0</td><td>SCANMODE</td><td>Enables top-down scan mode. Default is pyramid scan mode.</td></tr>
<tr><td>D1</td><td>0</td><td>DATAMOVE</td><td>Initiates transfer of measurement data from ALU to data registers (manual transfer) and sets DATARDY. ALU data is preserved until a new acquisition is started. Always reads logic zero. Ignored in acquisition mode.</td></tr>
<tr><td>D0</td><td>0</td><td>SCAN</td><td>Enables the acquisition mode and (if in double-buffer mode) transfers previous acquisition data from ALU to data registers. Acts as a strobe bit and therefore does not need to be cleared. Always reads logic zero. Ignored in acquisition mode.</td></tr>
</table>

ALRTOVEN Register (address 0x14)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13	0	AINOVALRTEN1	Enables the AIN1 over-voltage alert
D12	0	AINOVALRTEN0	Enables the AIN0 over-voltage alert
D11	0	OVALRTEN[12:1]	Enables the over-voltage alert for the respective cell. Clearing also clears the associated cell alert.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

ALRTUVEN Register (address 0x15)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13	0	AINUVALRTEN1	Enables the AIN1 under-voltage alert
D12	0	AINUVALRTEN0	Enables the AIN0 under-voltage alert
D11	0	UVALRTEN[12:1]	Enables the under-voltage alert for the respective cell. Clearing also clears the associated cell alert.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

WATCHDOG Register (address 0x18)

<table>
<tr><th>Bit</th><th>POR</th><th>Name</th><th>Description</th></tr>
<tr><td>D15</td><td>0</td><td>Reserved</td><td>Always reads logic zero.</td></tr>
<tr><td>D14
D13
D12</td><td>0</td><td>CBPDIV[2:0]</td><td>Sets the step size of the cell balancing timer LSB per table below:

<table><tr><th>CBPDIV[2:0]</th><th>Step Size</th><th>Timeout Range</th></tr><tr><td>000</td><td>Disabled</td><td>No timeout</td></tr><tr><td>001</td><td>1s</td><td>1–15s</td></tr><tr><td>010</td><td>4s</td><td>4–60s</td></tr><tr><td>011</td><td>16s</td><td>16–240s</td></tr><tr><td>100</td><td>64s</td><td>64–960s</td></tr><tr><td>101</td><td>128s</td><td>128–1920s</td></tr><tr><td>110</td><td>256s</td><td>256–3840s</td></tr><tr><td>111</td><td>256s</td><td>256–3840s</td></tr></table></td></tr>
<tr><td>D11
D10
D9
D8</td><td>0</td><td>CBTIMER[3:0]</td><td>Watchdog timer for the cell-balancing switches. The timer counts down at a rate set by CBPDIV. When the timer reaches 0, all cell-balancing switches are disabled by a signal separate from the BALSWEN bits. The timer should be periodically rewritten with a timeout value to keep the cell balancing switches enabled. When the timer value is read, the value reported is latched during the stop bit time following the ACQCFG UART register address of the READALL command. If the GPIO3TMR configuration is enabled, the GPIO3 pin is driven high while CBTIMER[3:0] is nonzero and is driven low when the timer value is zero. The cell-balancing timer is reset to zero when EMGCYDCHG =1.</td></tr>
<tr><td>D7
D6
D5
D4
D3
D2
D1
D0</td><td>0</td><td>Reserved</td><td>Always reads logic zero.</td></tr>
</table>

ACQCFG Register (address 0x19)

<table>
<tr><th>Bit</th><th>POR</th><th>Name</th><th>Description</th></tr>
<tr><td>D15
D14
D13
D12
D11
D10</td><td>0</td><td>Reserved</td><td>Always reads logic zero.</td></tr>
<tr><td>D9
D8</td><td>0</td><td>THRMMODE[1:0]</td><td>Configures the THRM mode based on the table below:

<table><tr><th>THRMMODE[1:0]</th><th>Operation</th></tr><tr><td>00</td><td>Auto mode (on in acquisition mode)</td></tr><tr><td>01</td><td>Auto mode (on in acquisition mode)</td></tr><tr><td>10</td><td>Manual mode, THRM switch off</td></tr><tr><td>11</td><td>Manual mode, THRM switch on</td></tr></table></td></tr>
<tr><td>D7
D6</td><td>0</td><td>Reserved</td><td>Always reads logic zero.</td></tr>
<tr><td>D5
D4
D3
D2
D1
D0</td><td>0</td><td>AINTIME[5:0]</td><td>Configures the pre-conversion settling time for each enabled AUXIN input from 6µs (default) up to 384µs (6µs / bit). This is to allow extra settling time if the application circuit requires it since the THRM voltage is not driven out until the start of the acquisition (in auto mode).</td></tr>
</table>

BALSWEN Register (address 0x1A)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13			
D12			
D11	0	BALSWEN[11:0]	BALSWEN[n-1] enables the balancing switch (conducting) between SWn and SWn-1.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

DEVCFG2 Register (address 0x1B)

Bit	POR	Name	Description
D15	0	LASTLOOP	Enables UART loopback mode which internally connects upper port transmitter to upper port receiver. The loopback mode allows the host to locate a break in daisy-chain communication whether or not the last daisy-chain device uses an external wire loopback wire or the internal loopback.
D14	0	Reserved	Always reads logic zero.
D13			
D12	0	DBLBUFSEL	Enables alternate double-buffer mode. Contact Maxim Applications for details, otherwise leave in default state.
D11	0	TXLIDLEHIZ	Enables High-Z idle mode which causes the TX drivers of the lower UART to idle in the high-Z state instead of idling in the logic zero state (default mode). Leave in default state for normal operation.
D10	0	TXUIDLEHIZ	Enables High-Z idle mode which causes the TX drivers of the upper UART to idle in the high-Z state instead of idling in the logic zero state (default mode). Leave in default state for normal operation.
D9	0	RESERVED	Reserved for future use. Reads the written value.
D8	0	EMGCYDCHG	Set to enable emergency discharge mode (configured by BALSWDCHG).
D7	0	Reserved	Always reads logic zero.
D6			
D5			
D4			
D3			
D2			
D1			
D0	0	HVCPDIS	Disables the HV charge pump. Used for ALRTHVUV diagnostic. If the HV charge pump is disabled in normal operation, measurement errors will result due to V_{HV} under-voltage.

BALDIAGCFG1 Register (address 0x1C)

Bit	POR	Name	Description
D15 D14	0	Reserved	Always reads logic zero.
D13	0	ALTMUXSEL_M	Mirror for ALTMUXSEL bit.
D12	0	POLARITY_M	Mirror for POLARITY bit.
D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	0	CELLEN_M[12:1]	Mirror for CELLEN[12:1] in the MEASUREEN register. Writing to this field also updates CELLEN[12:1]. Reading this field reflects CELLEN[12:1].

BALSWDCHG Register (address 0x1D)

Bit	POR	Name	Description
D15 D14 D13	0	DCHGWIN[2:0]	Configuration for emergency discharge mode (EMGCYDCHG = 1). Sets the duty-cycle for each discharge cycle (even or odd) per the table below: **DCHGWIN[2:0] (LSb = 7.5s)** / **Behavior** 0h / Switches on for 7.5s, off for 52.5s 1h / Switches on for 15s, off for 45s … / … 7h / Switches on for 59.94s, off for 62.5ms
D12	0	Reserved	Always reads logic zero.
D11 D10 D9 D8	0	DCHGCNTR[3:0]	Discharge counter which can be read to verify operation of the emergency discharge mode (EMGCYDCHG = 1). During the emergency discharge mode, the discharge counter counts at 2Hz rolling over at Fh to 0h and continuing until the emergency discharge mode terminates. Read-only.
D7 D6 D5 D4 D3 D2 D1 D0	0	DCHGTIME[7:0]	Write to set the timeout value of the emergency discharge mode (EMGCYDCHG = 1) per the table below. Writing to 00h disables the timer and terminates the emergency discharge mode. The timer starts when EMGCYDCHG = 1 (and DCHGTIME[7:0] ≠ 00h) and stops when it reaches the timeout. The timer is reset when EMGCYDCHG = 0. **DCHGTIME[7:0] (LSb = 2 hours)** / **Timeout** 00h / Discharge mode disabled 01h / Discharge mode disabled after 4 hours 02h / Discharge mode disabled after 6 hours … / … FFh / Discharge mode disabled after 512 hours

TOPCELL Register (address 0x1E)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3	Ch	TOPCELL[3:0]	Configures the top cell position if less than 12 channels are used. This is to properly mask the ALRTBALSW diagnostic alerts. TOPCELL[3:0] = 0h is not a valid configuration and is identical to the default, Ch (12d).
D2			
D1			
D0			

CELLn Register (addresses 0x20 to 0x2B)

Bit	POR	Name	Description
D15	0	CELLn[15:0]	CELLn[15:2] contains the 14-bit measurement result for CELLn. CELLn[1:0] always reads logic zero. Read-only.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

VBLOCK Register (address 0x2C)

Bit	POR	Name	Description
D15	0	VBLOCK[15:0]	VBLOCK[15:2] contains the 14-bit measurement result for VBLKP. VBLOCK[1:0] always reads logic zero. Read-only.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

AIN1 Register (address 0x2D)

Bit	POR	Name	Description
D15	0	AIN1[15:0]	AIN1[15:4] contains the 12-bit measurement result for AUXIN1. AIN1[3:0] always reads logic zero. Read-only.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

AIN2 Register (address 0x2E)

Bit	POR	Name	Description
D15	0	AIN2[15:0]	AIN2[15:4] contains the 12-bit measurement result for AUXIN2. AIN2[3:0] always reads logic zero. Read-only.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

TOTAL Register (address 0x2F)

Bit	POR	Name	Description
D15	0	SUM[15:0]	16-bit sum of all cell voltages CELLn[15:4] that are enabled by MEASUREEN. Read-only.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

OVTHCLR Register (address 0x40)

Bit	POR	Name	Description
D15	FFFCh	OVTHCLR[15:0]	14-bit over-voltage clear threshold. UVTHCLR[1:0] always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

OVTHSET Register (address 0x42)

Bit	POR	Name	Description
D15	FFFCh	OVTHSET[15:0]	14-bit over-voltage set threshold. UVTHCLR[1:0] always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

UVTHCLR Register (address 0x44)

Bit	POR	Name	Description
D15	0	UVTHCLR[15:0]	14-bit under-voltage clear threshold. UVTHCLR[1:0] always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

UVTHSET Register (address 0x46)

Bit	POR	Name	Description
D15	0	UVTHSET[15:0]	14-bit under-voltage set threshold. UVTHSET[1:0] always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

MSMTCH Register (address 0x48)

Bit	POR	Name	Description
D15	FFFCh	MSMTCH[15:0]	14-bit voltage threshold for ALRTMSMTCH. MSMTCH[1:0] always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

AINOT Register (address 0x49)

Bit	POR	Name	Description
D15	0	AINOT[15:0]	12-bit under-voltage (over-temperature) threshold for AUXIN alerts. AINOT[3:0] always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

AINUT Register (address 0x4A)

Bit	POR	Name	Description
D15	FFF0h	AINUT[15:0]	12-bit over-voltage (under-temperature) threshold for AUXIN alerts. AINUT[3:0] always reads logic zero..
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

BALSHRTTHR Register (address 0x4B)

Bit	POR	Name	Description
D15	0	BALSHRTTHR[15:0]	14-bit voltage threshold for the balancing switch short circuit diagnostic test. The ADC results in this test mode are compared against the threshold. If any result is below the threshold, it is flagged as a balancing switch alert. Results above the threshold are considered normal. The threshold should be set by the system controller prior to making a diagnostic measurement. BALSHRTTHR[1:0] always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

BALLOWTHR Register (address 0x4C)

Bit	POR	Name	Description
D15	0	BALLOWTHR[15:0]	14-bit low-voltage threshold for the balancing switch conducting and cell sense wire diagnostic tests. The ADC results in this test mode are compared against the threshold. If any result is below the threshold, it is flagged as a balancing switch alert. Results above the threshold are considered normal. The threshold should be set by the system controller prior to making a diagnostic measurement. BALLOWTHR[1:0] always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

BALHIGHTHR Register (address 0x4D)

Bit	POR	Name	Description
D15	0	BALHIGHTHR[15:0]	14-bit high-voltage threshold for the balancing switch conducting and cell sense wire diagnostic tests. The ADC results in this test mode are compared against the threshold. If any result is above the threshold, it is flagged as a balancing switch alert. Results below the threshold are considered normal. The threshold should be set by the system controller prior to making a diagnostic measurement. BALHIGHTHR[1:0] always reads logic zero.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

DIAG Register (address 0x50)

Bit	POR	Name	Description
D15	0	DIAG[15:0]	DIAG[15:2] contains the 14-bit measurement result for the diagnostic selected by DIAGCFG[2:0]. DIAG[1:0] always reads logic zero. Read-only.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

DIAGCFG Register (address 0x51)

<table>
<tr><th>Bit</th><th>POR</th><th>Name</th><th>Description</th></tr>
<tr><td>D15
D14
D13
D12</td><td>0</td><td>CTSTDAC[3:0]</td><td>Configures the current level for all enabled test sources per the table below (either 6.25µA or 3.125µA per bit.
<table>
<tr><th rowspan="2">CTSTDAC{3:0]</th><th colspan="2">Test Source Current</th></tr>
<tr><th>Cn, AUXINn</th><th>HVMUX</th></tr>
<tr><td>0h</td><td>6.25 µA</td><td>3.125 µA</td></tr>
<tr><td>1h</td><td>12.5 µA</td><td>6.25 µA</td></tr>
<tr><td>2h</td><td>18.75 µA</td><td>9.375 µA</td></tr>
<tr><td>…</td><td>….</td><td>…</td></tr>
<tr><td>Dh</td><td>87.5 µA</td><td>43.75 µA</td></tr>
<tr><td>Eh</td><td>93.75 µA</td><td>46.875 µA</td></tr>
<tr><td>Fh</td><td>100 µA</td><td>50 µA</td></tr>
</table></td></tr>
<tr><td>D11</td><td>0</td><td>CTSTSRC</td><td>Configures the cell input test current sources to either source current from VAA (logic one), or sink current to AGND (logic zero).</td></tr>
<tr><td>D10</td><td>0</td><td>Reserved</td><td>Always reads logic zero.</td></tr>
<tr><td>D9
D8</td><td>0
0</td><td>AUXINTSTEN[2:1]</td><td>Enables the test current sources connected to the corresponding AUXIN input for diagnostic testing. The current level is configured by the CTSTDAC[3:0] and the current direction is configured by CTSTSRC.</td></tr>
<tr><td>D7</td><td>0</td><td>MUXDIAGBUS</td><td>Selects the HVMUX output to which the HVMUX test current source is connected, if MUXDIAGPAIR is enabled, as shown below:
<table>
<tr><th>MUXDIAGBUS</th><th>HVMUX Output</th></tr>
<tr><td>0</td><td>Output used for even cells, C0, and AGND</td></tr>
<tr><td>1</td><td>Output used for odd cells and REF, and ALTREF</td></tr>
</table></td></tr>
<tr><td>D6</td><td>0</td><td>MUXDIAGPAIR</td><td>Configures a single HVMUX test current source to be connected to only one HVMUX output (as selected by MUXDIAGBUS). In the default configuration (MUXDIAGPAIR = 0), both HVMUX test current sources are connected to both HVMUX outputs.</td></tr>
<tr><td>D5</td><td>0</td><td>Reserved</td><td>Always reads logic zero.</td></tr>
<tr><td>D4</td><td>0</td><td>MUXDIAGEN</td><td>Enables the HVMUX test current source(s). The current level is configured by CSTDAC[3:0] and the connectivity is configured by MUXDIAGPAIR, and MUXDIAGBUS</td></tr>
<tr><td>D3</td><td>0</td><td>ALTMUXSEL</td><td>Enables cell measurements on the SWn inputs (ALTMUX data path) instead of the Cn inputs (HVMUX data path). Refer to Diagnostics section.</td></tr>
<tr><td>D2
D1
D0</td><td>0</td><td>DIAGSEL[2:0]</td><td>Selects the diagnostic measurement for the acquisition per table below:
<table>
<tr><th>DIAGSEL[2:0]</th><th>Diagnostic Measurement</th></tr>
<tr><td>0b000</td><td>No measurement</td></tr>
<tr><td>0b001</td><td>V_{ALTREF}</td></tr>
<tr><td>0b010</td><td>V_{AA} (with ADC reference = V_{THRM})</td></tr>
<tr><td>0b011</td><td>LSAMP Offset</td></tr>
<tr><td>0b100</td><td>Zero-scale ADC output (000h)</td></tr>
<tr><td>0b101</td><td>Full-scale ADC output (FFFh)</td></tr>
<tr><td>0b110</td><td>Die temperature</td></tr>
<tr><td>0b111</td><td>No measurement</td></tr>
</table></td></tr>
</table>

CTSTEN Register (address 0x52)

Bit	POR	Name	Description
D15 D14 D13	0	Reserved	Always reads logic zero.
D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	0	CTSTEN[12:0]	Enables the current sources connected to the corresponding cell input for diagnostic testing. The current level is configured by the CTSTDAC[3:0] and the current direction is configured by CTSTSRC in the DIAGCFG register.

ADCTEST1A Register (address 0x57)

Bit	POR	Name	Description
D15 D14 D13 D12	0	Reserved	Always reads logic zero.
D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0		ADCTEST1A[11:0]	User-specified test data for the ALU diagnostic (ADCTEST = 1). This 12-bit data is fed into the ALU during the first conversion of odd-numbered samples (e.g., first sample).

ADCTEST1B Register (address 0x58)

Bit	POR	Name	Description
D15 D14 D13 D12	0	Reserved	Always reads logic zero.
D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0		ADCTEST1B[11:0]	User-specified test data for the ALU diagnostic (ADCTEST = 1). This 12-bit data is fed into the ALU during the second conversion of odd-numbered samples (e.g., first sample).

ADCTEST2A Register (address 0x59)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13			
D12			
D11	0	ADCTEST2A[11:0]	User-specified test data for the ALU diagnostic (ADCTEST = 1). This 12-bit data is fed into the ALU during the first conversion of even-numbered samples in oversampling mode.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

ADCTEST2B Register (address 0x5A)

Bit	POR	Name	Description
D15	0	Reserved	Always reads logic zero.
D14			
D13			
D12			
D11	0	ADCTEST2B[11:0]	User-specified test data for the ALU diagnostic (ADCTEST = 1). This 12-bit data is fed into the ALU during the second conversion of even-numbered samples in oversampling mode.
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

CALx Registers (addresses 0xC0 – 0xCA, 0xCF)

Bit	POR	Name	Description
D15	xxh	CALx[15:0]	Contains factory calibration data. Read-only.
D14			
D13			
D12			
D11			
D10			
D9			
D8			
D7			
D6			
D5			
D4			
D3			
D2			
D1			
D0			

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17823BGCB+	-40°C to +105°C	64 LQFP
MAX17823BGCB/V+	-40°C to +105°C	64 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive-qualified part.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 LQFP	C64+1	21-0083	90-0141

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/14	Initial release	—
1	3/14	Added MAX17823B to data sheet	1–129
2	9/14	DIAGSEL[2:0] changed to 0b110 from 0b101, changed FFFCh to FFF0h for ADC Full scale diagnostic, separation of Cn pin open and HVMUX switch open, CTST current sources for Cn pin open table addition	22, 59, 72, 73
3	2/16	Deleted “ID1[0] always reads logic one” from ID1 Register (address 0x0D) table	101
4	10/17	Changed SWn to SWn-1 in *Absolute Maximum Ratings* section from “-0.3V to +0.9V” to “-0.3V to +16V”	3
4.1		Correcting 10/17 Rev History: Changed SWn to SWn-1 in *Absolute Maximum Ratings* section from “-0.3V to +9V” to “-0.3V to +16V”	—
5	9/19	Removed MAX17823A from title and *Ordering Information*; added thermal resistance values to *Absolute Maximum Ratings* section	1–129

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