



# THE DATASHEET OF MAX808LESA+T





# 8-Pin $\mu$ P Supervisory Circuits with $\pm 1.5\%$ Reset Accuracy

MAX801L/M/N, MAX808L/M/N

## General Description

The MAX801/MAX808 microprocessor ( $\mu$ P) supervisory circuits monitor and control the activities of +5V  $\mu$ Ps by providing backup-battery switchover, low-line indication, and  $\mu$ P reset. Additional features include a watchdog for the MAX801 and CMOS RAM write protection for the MAX808.

The MAX801/MAX808 offer a choice of reset-threshold voltage (denoted by suffix letter): 4.675V (L), 4.575V (N), and 4.425V (M). These devices are available in 8-pin DIP and SO packages.

## Applications

- Computers
- Controllers
- Intelligent Instruments
- Critical  $\mu$ P Power Monitoring
- Portable/Battery-Powered Equipment
- Embedded Systems

## Features

- ◆ Precision Voltage Monitoring,  $\pm 1.5\%$  Reset Accuracy
- ◆ 200ms Power-OK/Reset Time Delay
- ◆ **RESET** Output (MAX808)  
RESET and **RESET** Outputs (MAX801)
- ◆ Watchdog Timer (MAX801)
- ◆ On-Board Gating of Chip-Enable Signals (MAX808):  
Memory Write-Cycle Completion  
3ns CE Gate Propagation Delay
- ◆ 1 $\mu$ A Standby Current
- ◆ Power Switching:  
250mA in VCC Mode  
20mA in Battery-Backup Mode
- ◆ MaxCap™/SuperCap™ Compatible
- ◆ **RESET** Guaranteed Valid to VCC = 1V
- ◆ Low-Line Threshold 52mV Above Reset Threshold

MaxCap is a trademark of The Carborundum Corp.

SuperCap is a trademark of Baknor Industries.

## Ordering Information

PART*	TEMP RANGE	PIN-PACKAGE
MAX801_CPA	0°C to +70°C	8 Plastic DIP
MAX801_CSA	0°C to +70°C	8 SO
MAX801_EPA	-40°C to +85°C	8 Plastic DIP
MAX801_ESA	-40°C to +85°C	8 SO
MAX801_MJA	-55°C to +125°C	8 CERDIP**
MAX808_CPA	0°C to +70°C	8 Plastic DIP
MAX808_CSA	0°C to +70°C	8 SO
MAX808_EPA	-40°C to +85°C	8 Plastic DIP
MAX808_ESA	-40°C to +85°C	8 SO
MAX808_MJA	-55°C to +125°C	8 CERDIP**

\*These parts offer a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.

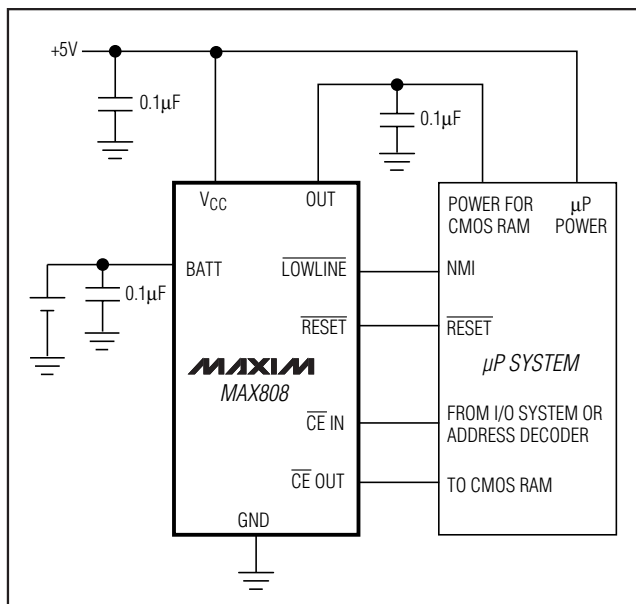
\*\*Contact factory for availability and processing to MIL-STD-883.

Devices in PDIP, SO and  $\mu$ MAX packages are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.

SUFFIX	RESET THRESHOLD (V)		
	MIN	TYP	MAX
L	4.60	4.675	4.75
N	4.50	4.575	4.65
M	4.35	4.425	4.50

Pin Configurations appear at end of data sheet.

## Typical Operating Circuit



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## ABSOLUTE MAXIMUM RATINGS

Input Voltage (with respect to GND)		OUT Continuous.....500mA
VCC.....	-0.3V to +6V	All Other Outputs .....50mA
VBATT.....	-0.3V to +6V	Continuous Power Dissipation (TA = +70°C)
All Other Pins.....	-0.3V to (VOUT + 0.3V)	Plastic DIP (derate 9.09mW/°C above +70°C) .....727mW
Input Current		SO (derate 5.88mW/°C above +70°C).....471mW
VCC Peak.....	1.0A	CERDIP (derate 8.00mW/°C above +70°C).....640mW
VCC Continuous.....	500mA	Operating Temperature Ranges
IBATT Peak.....	250mA	MAX801_C_A/MAX808_C_A.....0°C to +70°C
IBATT Continuous.....	50mA	MAX801_E_A/MAX808_E_A.....-40°C to +85°C
GND.....	50mA	MAX801_MJA/MAX808_MJA.....-55°C to +125°C
All Other Inputs.....	50mA	Storage Temperature Range.....-65°C to +160°C
Output Current		Lead Temperature (soldering, 10sec).....+300°C
OUT Peak.....	1.0A	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(VCC = 4.6V to 5.5V for the MAX80\_L, VCC = 4.5V to 5.5V for the MAX80\_N, VCC = 4.35V to 5.5V for the MAX80\_M; VBATT = 2.8V; TA = TMIN to TMAX. Typical values are at VCC = 5V and TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range VCC, BATT (Note 1)			0	X	5.5	V
VOUT in Normal Operating Mode	VCC = 4.5V	IOUT = 25mA		VCC - 0.02		V
		IOUT = 250mA, MAX80_C/E	VCC - 0.38	VCC - 0.25		
		IOUT = 250mA, MAX80_M	VCC - 0.45			
	VCC = 3V, VBATT = 2.8V, IOUT = 100mA		VCC - 0.25	VCC - 0.12		
VCC to OUT On-Resistance	VCC = 4.5V, IOUT = 250mA	MAX80_C/E		1.0	1.5	$\Omega$
		MAX80_M			1.8	
	VCC = 3V, IOUT = 100mA			1.2	2.5	
VOUT in Battery-Backup Mode	VCC = 0V	VBATT = 4.5V, IOUT = 20mA		VBATT - 0.16		V
		VBATT = 2.8V, IOUT = 10mA	VBATT - 0.25	VBATT - 0.12		
		VBATT = 2.0V, IOUT = 5mA	VBATT - 0.20	VBATT - 0.08		
BATT to OUT On-Resistance	VCC = 0V	VBATT = 4.5V, IOUT = 20mA		8		$\Omega$
		VBATT = 2.8V, IOUT = 10mA		12	25	
		VBATT = 2.0V, IOUT = 5mA		16	40	
Supply Current in Normal Operating Mode (excludes IOUT)		MAX801		68	110	$\mu$ A
		MAX808		48	90	
Supply Current in Battery- Backup Mode (excludes IOUT) (Note 2)	VCC = 0V, VBATT = 2.8V	TA = +25°C		0.4	1	$\mu$ A
		TA = TMIN to TMAX	MAX80_C/E		5	
			MAX80_M		50	
BATT Standby Current (Note 3)	VBATT + 0.2V $\leq$ VCC	TA = +25°C	-0.1		0.1	$\mu$ A
		TA = TMIN to TMAX	-1.0		1.0	
Battery-Switchover Threshold	VBATT = 2.8V	Power-up		VBATT + 0.05		V
		Power-down		VBATT		
Battery-Switchover Hysteresis				50		mV

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = 4.6V$  to  $5.5V$  for the MAX80\_L,  $V_{CC} = 4.5V$  to  $5.5V$  for the MAX80\_N,  $V_{CC} = 4.35V$  to  $5.5V$  for the MAX80\_M;  $V_{BATT} = 2.8V$ ;  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $V_{CC} = 5V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>RESET AND LOW-LINE</b>							
Reset Threshold	VRST	VCC rising and falling	MAX80_L	4.600	4.675	4.750	V
			MAX80_N	4.500	4.575	4.650	
			MAX80_M	4.350	4.425	4.500	
Reset-Threshold Hysteresis				13			mV
$\overline{LOWLINE}$ to $\overline{RESET}$ Threshold Voltage	VLR	VCC falling		30	52	70	mV
$\overline{LOWLINE}$ Threshold, VCC Rising	VLL	MAX80_L			4.73	4.81	V
		MAX80_N			4.63	4.71	
		MAX80_M			4.48	4.56	
VCC to $\overline{RESET}$ Delay	tRD	VCC falling at 1mV/ $\mu$ s			17		$\mu$ s
VCC to $\overline{LOWLINE}$ Delay	tLL	VCC falling at 1mV/ $\mu$ s			17		$\mu$ s
$\overline{RESET}$ Active Timeout Period	tRP	VCC rising		140	200	280	ms
$\overline{RESET}$ Output Voltage		ISINK = 50 $\mu$ A, VBATT = 0V, VCC falling	VCC = 1.0V, MAX80_C			0.3	V
			VCC = 1.2V, MAX80_E/M			0.3	
		ISINK = 3.2mA, VCC = 4.25V			0.1	0.4	
		ISOURCE = 0.1mA	VCC - 1.5	VCC - 0.1			
$\overline{RESET}$ Output Short-Circuit Current	ISC	Output sink current, VCC = 4.25V			40		mA
		Output source current			1.6		
$\overline{RESET}$ Output Voltage (MAX801)		ISINK = 3.2mA				0.4	V
		ISOURCE = 5mA, VCC = 4.25V	VCC - 1.5				
$\overline{RESET}$ Output Short-Circuit Current (MAX801)	ISC	Output sink current			55		mA
		Output source current, VCC = 4.25V			15		
$\overline{LOWLINE}$ Output Voltage		ISINK = 3.2mA, VCC = 4.25V				0.4	V
		ISOURCE = 5mA, VCC = 4.25V	VCC - 1.5				
$\overline{LOWLINE}$ Output Short-Circuit Current	ISC	Output sink current, VCC = 4.25V			40		mA
		Output source current			20		
<b>WATCHDOG TIMER (MAX801)</b>							
Watchdog Timeout Period	tWD			1.12	1.6	2.24	sec
Minimum Watchdog Input Pulse Width		VIL = 0.8V, VIH = 0.75V x VCC		100			ns
WDI Threshold Voltage (Note 4)	VIH			0.75 x VCC			V
	VIL					0.8	
WDI Input Current		RESET deasserted, WDI = 0V		-50	-10		$\mu$ A
		RESET deasserted, WDI = VCC			16	50	

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = 4.6V$  to  $5.5V$  for the MAX80\_L,  $V_{CC} = 4.5V$  to  $5.5V$  for the MAX80\_N,  $V_{CC} = 4.35V$  to  $5.5V$  for the MAX80\_M;  $V_{BATT} = 2.8V$ ;  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $V_{CC} = 5V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CHIP-ENABLE GATING (MAX808)</b>						
$\overline{CE}$ IN Leakage Current		$V_{CC} = 4.25V$		$\pm 0.00002$	$\pm 1$	$\mu A$
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance (Note 5)		Enabled mode, $V_{CC} = V_{RST(max)}$		75	150	$\Omega$
$\overline{CE}$ OUT Short-Circuit Current ( $\overline{RESET}$ Active)		$V_{CC} = 4.25V, \overline{CE} OUT = 0V$		15		mA
$\overline{CE}$ IN to $\overline{CE}$ OUT Propagation Delay (Note 6)		$V_{CC} = 5V, C_{LOAD} = 50pF, 50\Omega$ source-impedance driver		3	8	ns
$\overline{CE}$ OUT Output Voltage High ( $\overline{RESET}$ Active)		$V_{CC} = 4.25V, I_{OUT} = 2mA$	3.5			V
		$V_{CC} = 0V, I_{OUT} = 10\mu A$	$V_{BATT} - 0.1$	$V_{BATT}$		
$\overline{RESET}$ to $\overline{CE}$ OUT Delay (Note 7)		$V_{CC}$ falling, $\overline{CE} IN = 0V$		18		$\mu s$

**Note 1:** Either  $V_{CC}$  or  $V_{BATT}$  can go to  $0V$  if the other is greater than  $2V$ .

**Note 2:** The supply current drawn by the MAX80\_ from the battery (excluding  $I_{OUT}$ ) typically goes to  $15\mu A$  when  $(V_{BATT} - 0.1V) < V_{CC} < V_{BATT}$ . In most applications, this is a brief period as  $V_{CC}$  falls through this region (see *Typical Operating Characteristics*).

**Note 3:** "+" = battery-discharging current, "-" = battery-charging current.

**Note 4:** WDI is internally connected to a voltage divider between  $V_{CC}$  and GND. If unconnected, WDI is typically driven to  $1.8V$ , disabling the watchdog function.

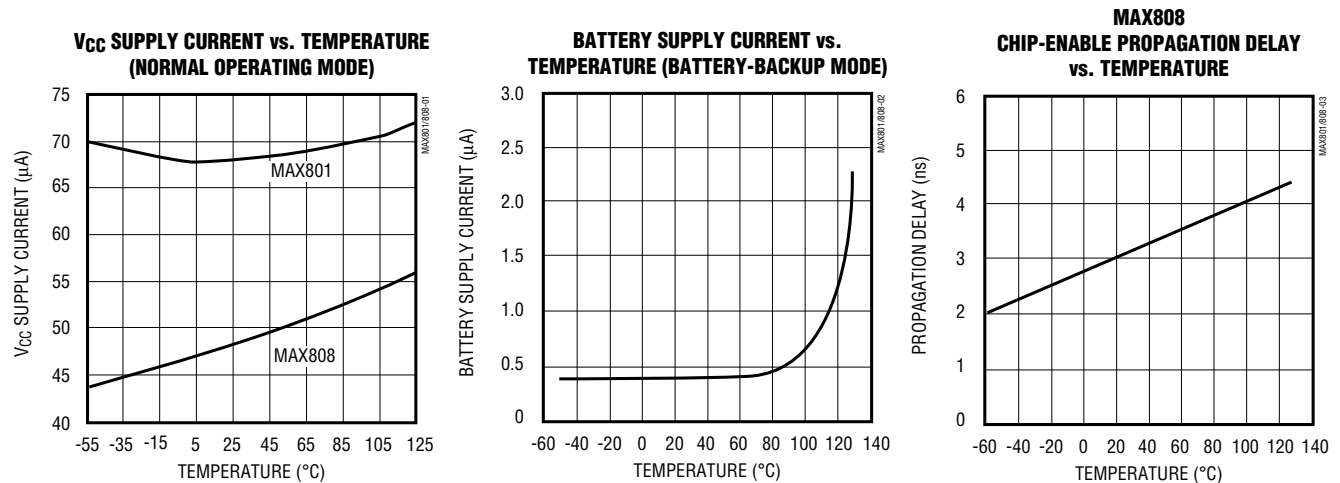
**Note 5:** The chip-enable resistance is tested with  $V_{\overline{CE} IN} = V_{CC} / 2$  and  $I_{\overline{CE} IN} = 1mA$ .

**Note 6:** The chip-enable propagation delay is measured from the 50% point at  $\overline{CE} IN$  to the 50% point at  $\overline{CE} OUT$ .

**Note 7:** If  $\overline{CE} IN$  goes high,  $\overline{CE} OUT$  goes high immediately and stays high until reset is deasserted and  $\overline{CE} IN$  is low.

## Typical Operating Characteristics

( $V_{CC} = 5V, V_{BATT} = 2.8V$ , no load,  $T_A = +25^\circ C$ , unless otherwise noted.)

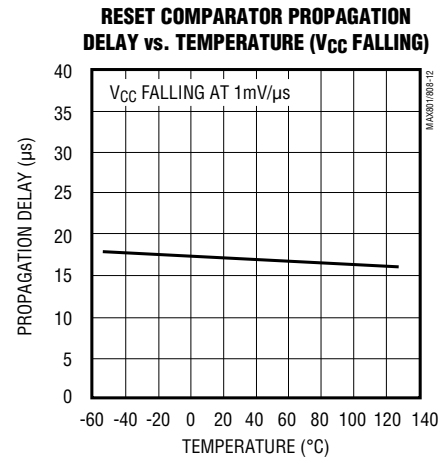
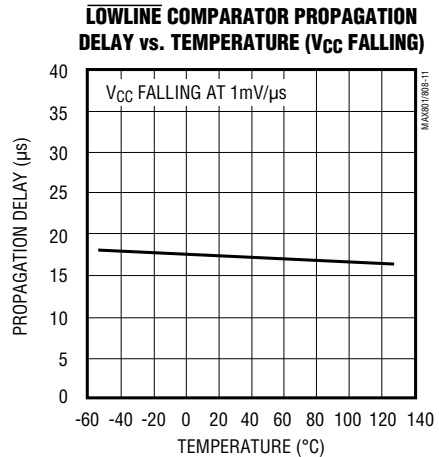
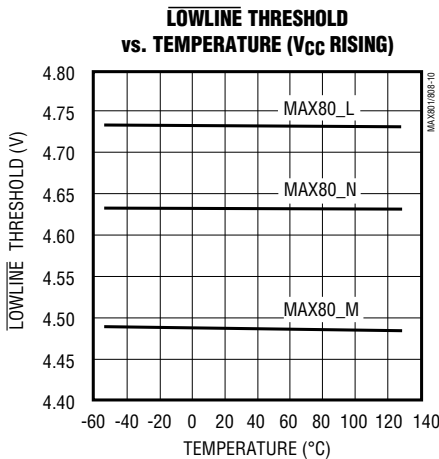
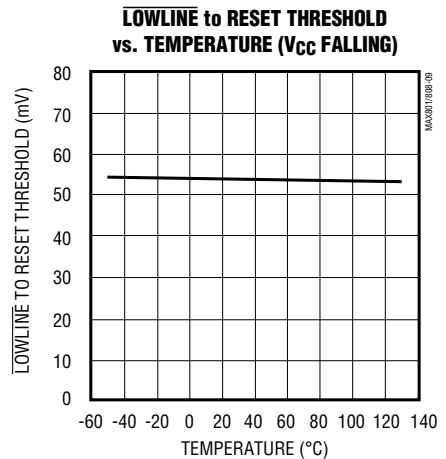
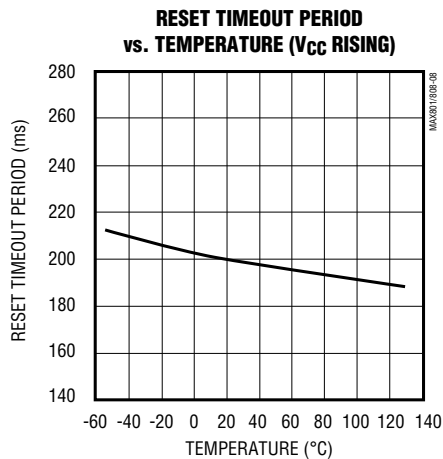
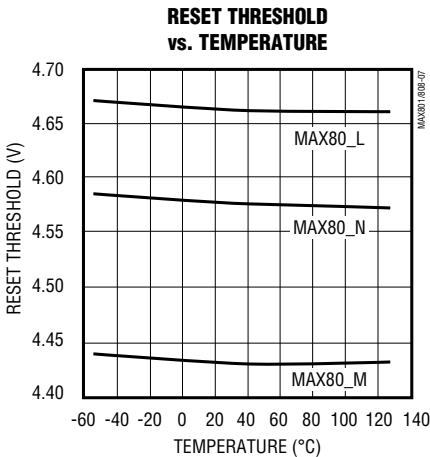
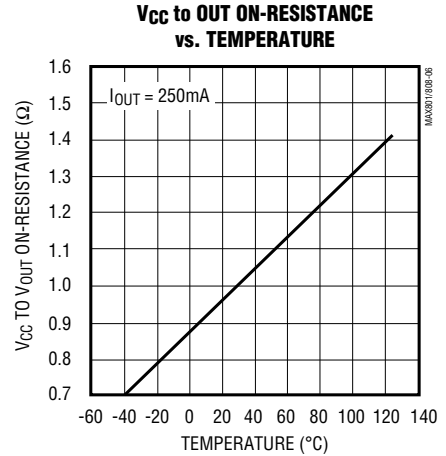
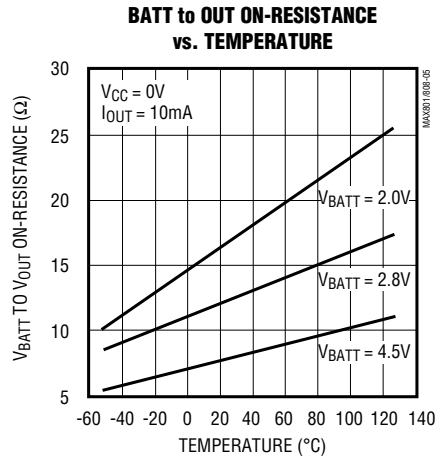
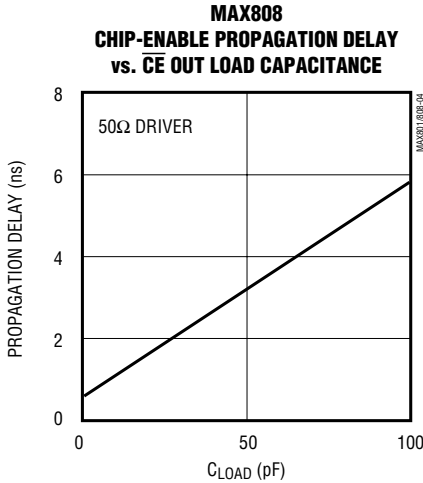


# 8-Pin $\mu$ P Supervisory Circuits with $\pm 1.5\%$ Reset Accuracy

## Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $V_{BATT} = 2.8V$ , no load,  $T_A = +25^\circ C$ , unless otherwise noted.)

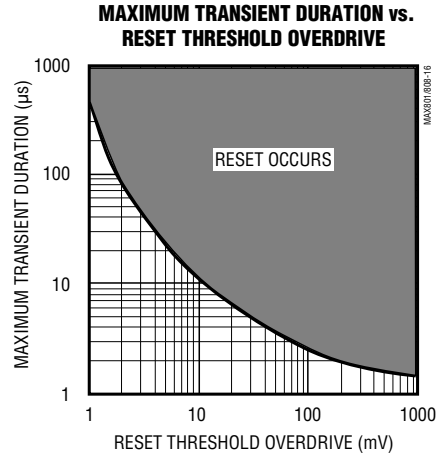
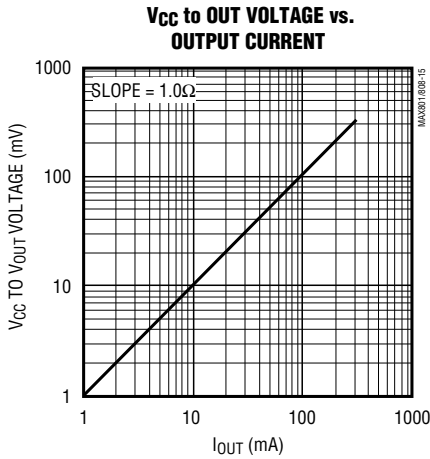
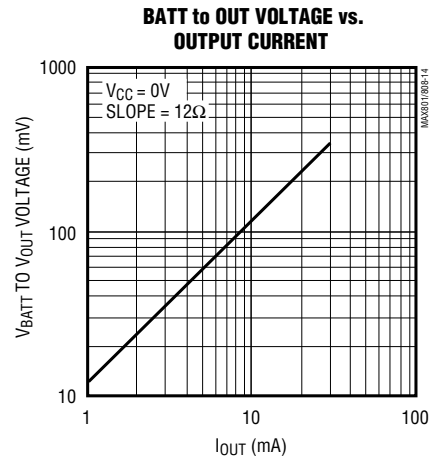
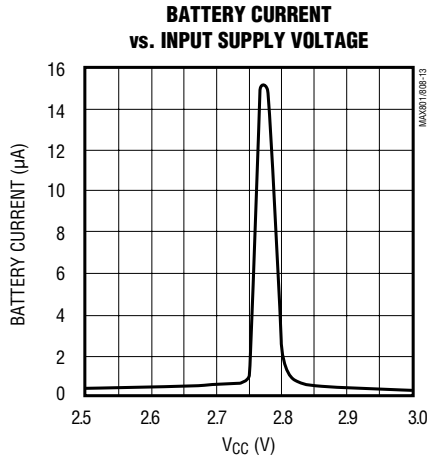
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# 8-Pin $\mu$ P Supervisory Circuits with $\pm 1.5\%$ Reset Accuracy

## Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $V_{BATT} = 2.8V$ , no load,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Description

PIN		NAME	FUNCTION
MAX801	MAX808		
1	1	$V_{CC}$	Input Supply Voltage, nominally +5V. Bypass with a 0.1 $\mu$ F capacitor to GND.
2	2	$\overline{LOWLINE}$	Low-Line Comparator Output. This CMOS-logic output goes low when $V_{CC}$ falls to 52mV above the reset threshold. Use $\overline{LOWLINE}$ to generate an NMI, initiating an orderly shut-down routine when $V_{CC}$ is falling. $\overline{LOWLINE}$ swings between $V_{CC}$ and GND.
3	3	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ is triggered and stays low when $V_{CC}$ is below the reset threshold (or during a watchdog timeout for the MAX801). It remains low 200ms after $V_{CC}$ rises above the reset threshold (or 200ms after the watchdog timeout occurs). $\overline{RESET}$ has a strong pull-down but a relatively weak pull-up, and can be wire-OR connected to logic gates. Valid for $V_{CC} \geq 1V$ . $\overline{RESET}$ swings between $V_{CC}$ and GND.
4	4	GND	Ground

# 8-Pin $\mu$ P Supervisory Circuits with $\pm 1.5\%$ Reset Accuracy

## Pin Description (continued)

PIN		NAME	FUNCTION
MAX801	MAX808		
5	—	RESET	Active-High Reset Output. RESET is the inverse of $\overline{\text{RESET}}$ . It is a CMOS output that sources and sinks current. RESET swings between $V_{CC}$ and GND.
—	5	$\overline{\text{CE}}$ OUT	Chip-Enable Output. Output to the chip-enable gating circuit. $\overline{\text{CE}}$ OUT is pulled up to the higher of $V_{CC}$ or $V_{BATT}$ when the chip-enable gate is disabled.
6	—	WDI	Watchdog Input. If WDI remains high or low longer than the watchdog timeout period (typically 1.6sec), $\overline{\text{RESET}}$ will be asserted for 200ms. Leave unconnected to disable the watchdog function.
—	6	$\overline{\text{CE}}$ IN	Chip-Enable Input
7	7	BATT	Backup-Battery Input. When $V_{CC}$ falls below the reset threshold and $V_{BATT}$ , OUT switches from $V_{CC}$ to BATT. $V_{BATT}$ may exceed $V_{CC}$ . The battery can be removed while the MAX801/MAX808 is powered up, provided BATT is bypassed with a 0.1 $\mu$ F capacitor to GND. If no battery is used, connect BATT to ground and $V_{CC}$ to OUT.
8	8	OUT	Output Supply Voltage to CMOS RAM. When $V_{CC}$ exceeds the reset threshold or $V_{BATT}$ , OUT connects to $V_{CC}$ . When $V_{CC}$ falls below the reset threshold and $V_{BATT}$ , OUT connects to BATT. Bypass OUT with a 0.1 $\mu$ F capacitor to GND.

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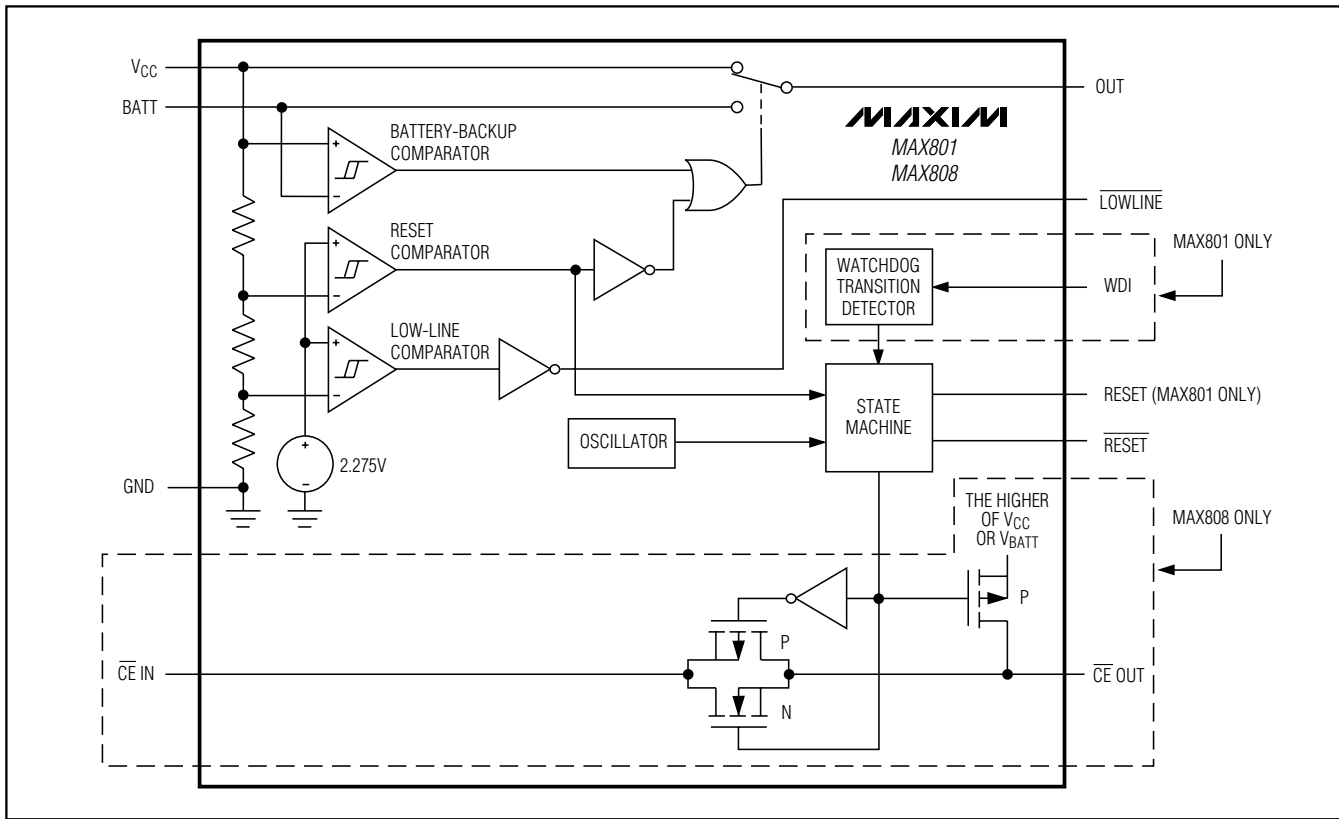


Figure 1. Functional Diagram

## 8-Pin $\mu\text{P}$ Supervisory Circuits with $\pm 1.5\%$ Reset Accuracy

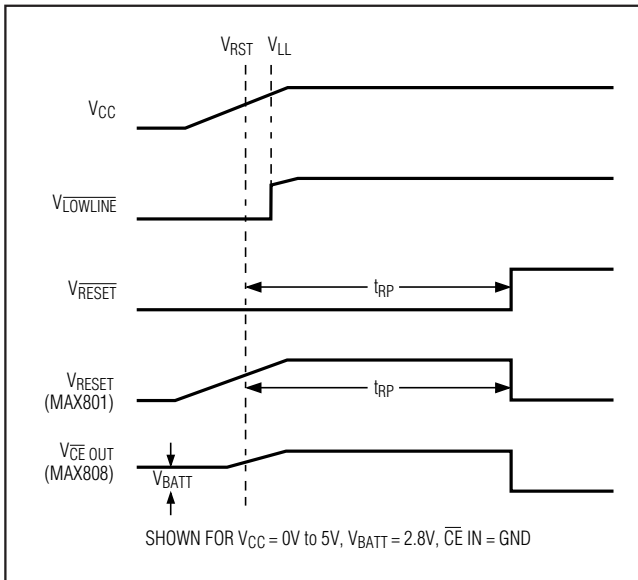


Figure 2a. Timing Diagram, V<sub>CC</sub> Rising

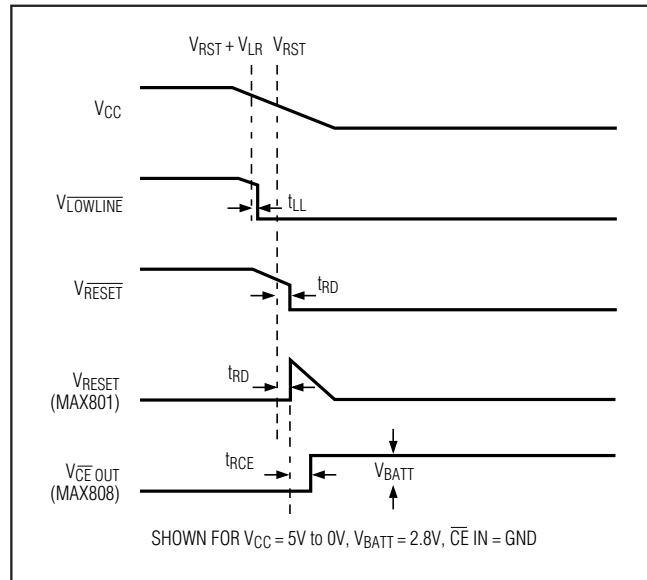


Figure 2b. Timing Diagram, V<sub>CC</sub> Falling

### Detailed Description

The MAX801/MAX808 microprocessor ( $\mu\text{P}$ ) supervisory circuits provide power-supply monitoring and backup-battery switchover in  $\mu\text{P}$  systems. The MAX801 also provides program-execution watchdog functions (Figure 1). Use of BiCMOS technology results in an improved, 1.5% reset-threshold precision while keeping supply currents typically at 68 $\mu\text{A}$  (48 $\mu\text{A}$  for the MAX808). The MAX801/MAX808 are intended for battery-powered applications that require high reset-threshold precision, allowing a wide power-supply operating range while preventing the system from operating below its specified voltage range.

### RESET and RESET Outputs

The MAX801/MAX808's  $\overline{\text{RESET}}$  output ensures that the  $\mu\text{P}$  powers up in a known state, and prevents code-execution errors during power-down and brownout conditions. It does this by resetting the  $\mu\text{P}$ , terminating program execution when V<sub>CC</sub> dips below the reset threshold. Each time  $\overline{\text{RESET}}$  is asserted, it stays low for at least the 200ms reset timeout period (set by an internal timer) to ensure the  $\mu\text{P}$  has adequate time to return to an initial state. The internal timer restarts any time V<sub>CC</sub> goes below the reset threshold (V<sub>RST</sub>) before the reset timeout period is completed. The watchdog timer on the MAX801 can also initiate a reset (see the MAX801 Watchdog Timer section).

The  $\overline{\text{RESET}}$  output is active low, and is implemented with a strong pull-down/relatively weak pull-up structure. It is guaranteed to be a logic low for  $0\text{V} < V_{\text{CC}} < V_{\text{RST}}$ , provided V<sub>BATT</sub> is greater than 2V. Without a backup battery,  $\overline{\text{RESET}}$  is guaranteed valid for V<sub>CC</sub>  $\geq$  1V.

The RESET output is the inverse of the  $\overline{\text{RESET}}$  output; it both sources and sinks current and cannot be wire-OR connected.

### Low-Line Comparator

The low-line comparator monitors V<sub>CC</sub> with a threshold voltage typically 52mV above the reset threshold, with 13mV of hysteresis. Use LOWLINE to provide a non-maskable interrupt (NMI) to the  $\mu\text{P}$  when power begins to fall, initiating an orderly software shutdown routine. In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine once the low-line warning is encountered and before reset asserts. If the system must contend with a more rapid V<sub>CC</sub> fall time (such as when the main battery is disconnected, when a DC-DC converter shuts down, or when a high-side switch is opened during normal operation), use capacitance on the V<sub>CC</sub> line to provide time to execute the shutdown routine (Figure 3). First calculate the worst-case time required for the system to perform its shutdown routine. Then, with worst-case shutdown time, worst-case load current, and minimum low-line to reset threshold (V<sub>LR(min)</sub>),

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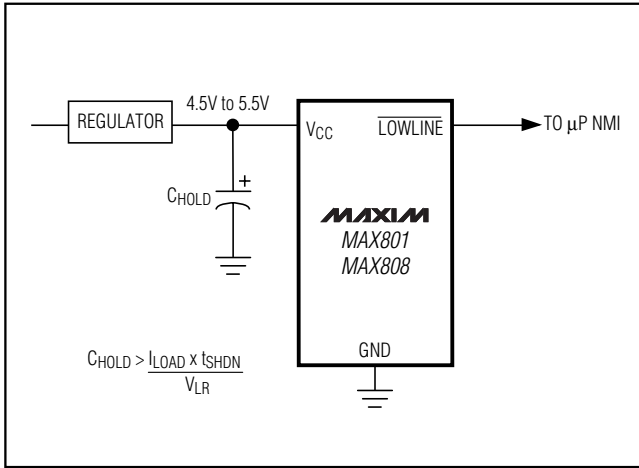


Figure 3. Using LOWLINE to Provide a Power-Fail Warning to the  $\mu$ P

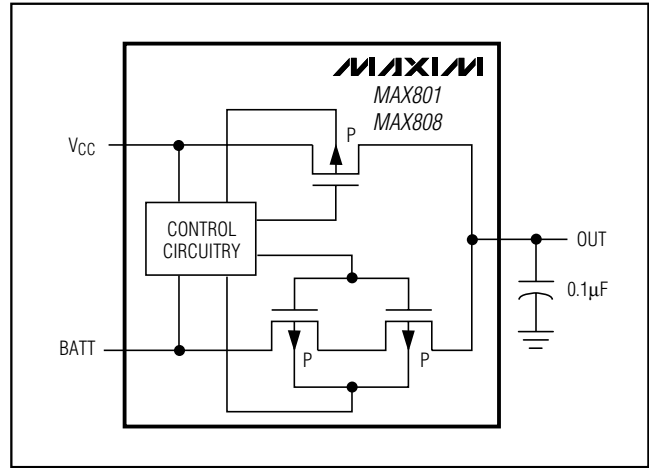


Figure 4. VCC and BATT to OUT Switch

calculate the amount of capacitance required to allow the shutdown routine to complete before reset is asserted:

$$C_{HOLD} = (I_{LOAD} \times t_{SHDN}) / (V_{LR}(\min))$$

where  $t_{SHDN}$  is the time required for the system to complete the shutdown routine (including the  $V_{CC}$  to low-line propagation delay),  $I_{LOAD}$  is the current being drained from the capacitor, and  $V_{LR}$  is the low-line to reset threshold.

### Output Supply Voltage

The output supply (OUT) transfers power from  $V_{CC}$  or BATT to the  $\mu$ P, RAM, and other external circuitry. At the maximum source current of 250mA,  $V_{OUT}$  will typically be 220mV below  $V_{CC}$ . Decouple OUT with a 0.1 $\mu$ F capacitor to ground.

### Battery-Backup Mode

Battery-backup mode preserves the contents of RAM in the event of a brownout or power failure. With a backup battery installed at BATT, the MAX801/MAX808 automatically switches RAM to backup power when  $V_{CC}$  falls. Two conditions are required for switchover to battery-backup mode: 1)  $V_{CC}$  must be below the reset threshold; 2)  $V_{CC}$  must be below  $V_{BATT}$ . Table 1 lists the status of inputs and outputs during battery-backup mode.

BATT is designed to conduct up to 20mA to OUT during battery backup. The PMOS switch on-resistance is approximately 12 $\Omega$ . Figure 4 shows the two series pass elements (between the BATT input and OUT) that facilitate UL recognition.  $V_{BATT}$  can exceed  $V_{CC}$  during normal operation without causing a reset.

Table 1. Input and Output Status in Battery-Backup Mode

PIN		NAME	STATUS
MAX801	MAX808		
1	1	$V_{CC}$	Battery switchover comparator monitors $V_{CC}$ for active switchover.
2	2	$\overline{LOWLINE}$	Logic low
3	3	$\overline{RESET}$	Logic low
4	4	GND	Ground—0V reference for all signals
5	—	RESET	Logic high; the open-circuit voltage is equal to $V_{CC}$ .
—	5	$\overline{CE} OUT$	Logic high. The open-circuit output voltage is equal to $V_{BATT}$ (MAX808).
6	—	WDI	WDI is ignored and goes high impedance.
—	6	$\overline{CE} IN$	High impedance (MAX808)
7	7	BATT	Supply current is 1 $\mu$ A max for $V_{BATT} \leq 2.8V$ .
8	8	OUT	OUT is connected to BATT through two internal PMOS switches in series.

## 8-Pin $\mu$ P Supervisory Circuits with $\pm 1.5\%$ Reset Accuracy

### MAX801 Watchdog Timer

The watchdog monitors the  $\mu$ P's activity. If the  $\mu$ P does not toggle the watchdog input (WDI) within 1.6sec, reset asserts for the reset timeout period. The internal 1.6sec timer is cleared when reset asserts or when a transition (low-to-high or high-to-low) occurs at WDI while reset is not asserted. The timer remains cleared and does not count as long as reset is asserted. It starts counting as soon as reset is released (Figure 5). Supply current is typically reduced by  $10\mu\text{A}$  when WDI is at a valid logic level. To disable the watchdog function, leave WDI unconnected. An internal voltage divider sets WDI to about mid-supply, disabling the watchdog timer/counter.

### MAX808 Chip-Enable Gating

The MAX808 provides internal gating of chip-enable (CE) signals to prevent erroneous data from corrupting CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX808 uses a series transmission gate from the chip-enable input ( $\overline{\text{CE}} \text{ IN}$ ) to the chip-enable output ( $\overline{\text{CE}} \text{ OUT}$ ) (Figure 1). The 8ns max chip-enable propagation from  $\overline{\text{CE}} \text{ IN}$  to  $\overline{\text{CE}} \text{ OUT}$  enables the MAX808 to be used with most  $\mu$ Ps.

The MAX808 also features write-cycle-completion circuitry. If  $V_{\text{CC}}$  falls below the reset threshold while the  $\mu$ P is writing to RAM, the MAX808 holds the CE gate enabled for  $18\mu\text{s}$  to allow the  $\mu$ P to complete the write instruction. If the write cycle has not completed by the end of the  $18\mu\text{s}$  period, the CE transmission gate turns off and  $\overline{\text{CE}} \text{ OUT}$  goes high. If the  $\mu$ P completes the write instruction during the  $18\mu\text{s}$  period, the CE gate turns off (high impedance) and  $\overline{\text{CE}} \text{ OUT}$  goes high as soon as the  $\mu$ P pulls  $\overline{\text{CE}} \text{ IN}$  high.  $\overline{\text{CE}} \text{ OUT}$  remains high, even if  $\overline{\text{CE}} \text{ IN}$  falls low for any reason (Figure 6).

### Chip-Enable Input

$\overline{\text{CE}} \text{ IN}$  is high impedance (disabled mode) while reset is asserted. During a power-down sequence when  $V_{\text{CC}}$  passes the reset threshold, the CE transmission gate disables.  $\overline{\text{CE}} \text{ IN}$  becomes high impedance  $18\mu\text{s}$  after reset asserts, provided  $\overline{\text{CE}} \text{ IN}$  is still low. If the  $\mu$ P completes the write instruction during the  $18\mu\text{s}$  period, the CE gate turns off.  $\overline{\text{CE}} \text{ IN}$  becomes high impedance as soon as the  $\mu$ P pulls  $\overline{\text{CE}} \text{ IN}$  high.  $\overline{\text{CE}} \text{ IN}$  remains high impedance even if the signal at  $\overline{\text{CE}} \text{ IN}$  falls low (Figure 6). During a power-up sequence,  $\overline{\text{CE}} \text{ IN}$  remains high impedance (regardless of  $\overline{\text{CE}} \text{ IN}$  activity) until reset is deasserted following the reset timeout period.

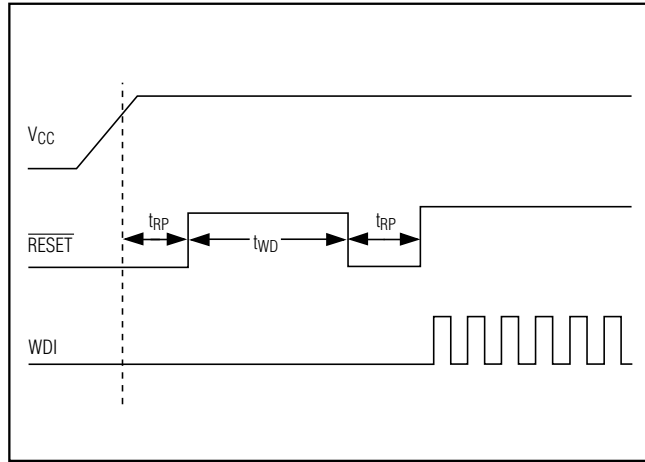


Figure 5. Watchdog Timing

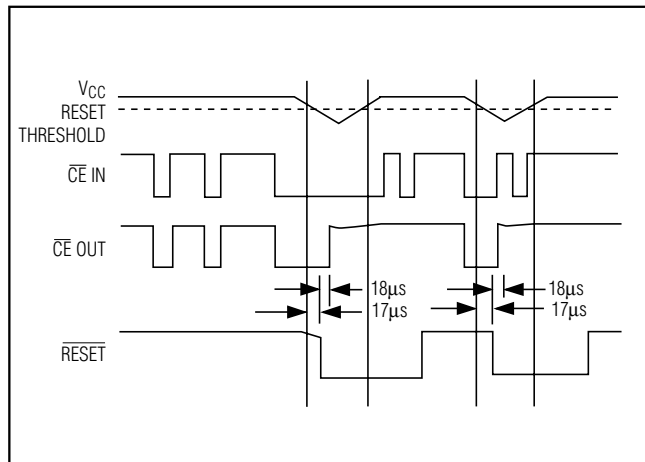


Figure 6. Chip-Enable Timing

In high-impedance mode, the leakage currents into this input are  $\pm 1\mu\text{A}$  max over temperature. In low-impedance mode, the impedance of  $\overline{\text{CE}} \text{ IN}$  appears as a  $75\Omega$  resistor in series with the load at  $\overline{\text{CE}} \text{ OUT}$ .

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to  $\overline{\text{CE}} \text{ IN}$  and the capacitive loading on  $\overline{\text{CE}} \text{ OUT}$  (see the Chip-Enable Propagation Delay vs.  $\overline{\text{CE}} \text{ OUT}$  Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on  $\overline{\text{CE}} \text{ IN}$  to the 50% point on  $\overline{\text{CE}} \text{ OUT}$  using a  $50\Omega$  driver and  $50\text{pF}$  of load capacitance (Figure 7). For minimum propagation delay, minimize the capacitive load at  $\overline{\text{CE}} \text{ OUT}$  and use a low-output-impedance driver.

# 8-Pin $\mu\text{P}$ Supervisory Circuits with $\pm 1.5\%$ Reset Accuracy

MAX801L/M/N, MAX808L/M/N

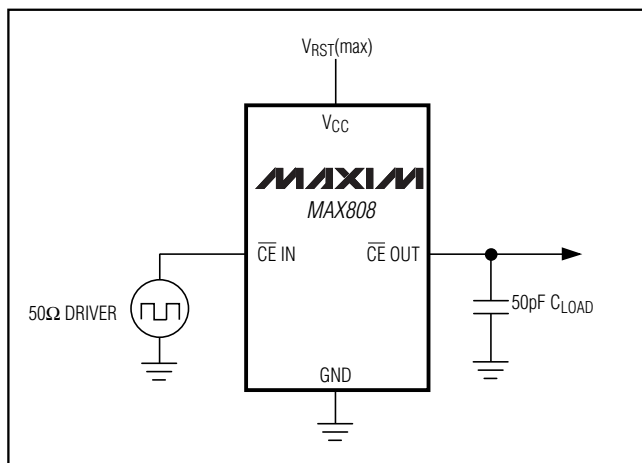


Figure 7. MAX808 CE Gate Test Circuit

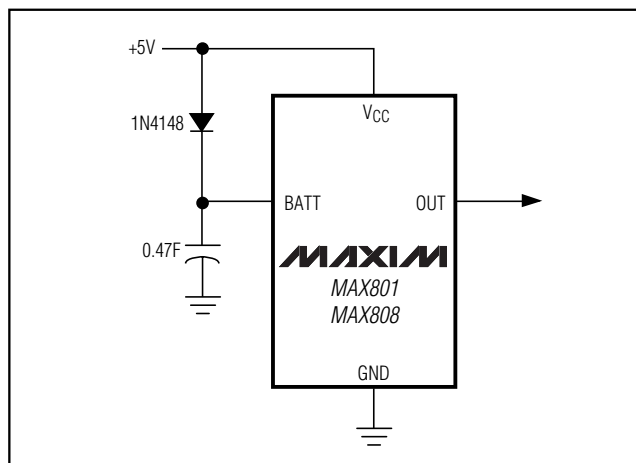


Figure 8. Using the MAX801/MAX808 with a SuperCap

### Chip-Enable Output

In enabled mode,  $\overline{\text{CE}} \text{ OUT}$ 's impedance is equivalent to  $75\Omega$  in series with the source driving  $\overline{\text{CE}} \text{ IN}$ . In disabled mode, the  $75\Omega$  transmission gate is off and  $\overline{\text{CE}} \text{ OUT}$  is actively pulled to the higher of  $V_{\text{CC}}$  or  $V_{\text{BATT}}$ . The source turns off when the transmission gate is enabled.

### Applications Information

The MAX801/MAX808 are not short-circuit protected. Shorting  $\text{OUT}$  to ground, other than power-up transients such as charging a decoupling capacitor, may destroy the device. If long leads connect to the IC's inputs, ensure that these lines are free from ringing and other conditions that would forward bias the IC's protection diodes. Bypass  $\text{OUT}$ ,  $V_{\text{CC}}$ , and  $\text{BATT}$  with  $0.1\mu\text{F}$  capacitors to  $\text{GND}$ .

The MAX801/MAX808 operate in two distinct modes:

- 1) Normal Operating Mode, with all circuitry powered up. Typical supply current from  $V_{\text{CC}}$  is  $68\mu\text{A}$  ( $48\mu\text{A}$  for the MAX808), while only leakage currents flow from the battery.
- 2) Battery-Backup Mode, where  $V_{\text{CC}}$  is below  $V_{\text{BATT}}$  and  $V_{\text{RST}}$ . The supply current from the battery is typically less than  $1\mu\text{A}$ .

### Using SuperCaps™ or MaxCaps™ with the MAX801/MAX808

$\text{BATT}$  has the same operating voltage range as  $V_{\text{CC}}$ , and the battery-switchover threshold voltage is typically  $V_{\text{BATT}}$  when  $V_{\text{CC}}$  is decreasing or  $V_{\text{BATT}} + 0.05\text{V}$  when  $V_{\text{CC}}$  is increasing. This hysteresis allows use of a SuperCap (e.g., around  $0.47\text{F}$ ) and a simple charging

circuit as a backup source (Figure 8). Since  $V_{\text{BATT}}$  can exceed  $V_{\text{CC}}$  while  $V_{\text{CC}}$  is above the reset threshold, no special precautions are needed when using these  $\mu\text{P}$  supervisors with a SuperCap.

### Backup-Battery Replacement

The backup battery can be disconnected while  $V_{\text{CC}}$  is above the reset threshold, provided  $\text{BATT}$  is bypassed with a  $0.1\mu\text{F}$  capacitor to ground. No precautions are necessary to avoid spurious reset pulses.

### Negative-Going Vcc Transients

While issuing resets to the  $\mu\text{P}$  during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration, negative-going  $V_{\text{CC}}$  transients (glitches). It is usually undesirable to reset the  $\mu\text{P}$  when  $V_{\text{CC}}$  experiences only small glitches.

The *Typical Operating Characteristics* show a graph of Maximum Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph was produced using negative-going  $V_{\text{CC}}$  pulses, starting at  $5\text{V}$  and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width that a negative-going  $V_{\text{CC}}$  transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a  $V_{\text{CC}}$  transient that goes  $40\text{mV}$  below the reset threshold and lasts for  $3\mu\text{s}$  or less will not cause a reset pulse to be issued. A  $0.1\mu\text{F}$  bypass capacitor mounted close to the  $V_{\text{CC}}$  pin provides additional transient immunity.

# 8-Pin $\mu$ P Supervisory Circuits with $\pm 1.5\%$ Reset Accuracy

## Watchdog Software Considerations

To help the watchdog timer keep a closer watch on software execution, you can set and reset the watchdog input at different points in the program, rather than “pulsing” the watchdog input high-low-high or low-high-low. This technique avoids a “stuck” loop, where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out.

Figure 9 shows a sample flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, low at the beginning of every subroutine or loop, then high again when the program returns to the beginning. If the program should “hang” in any subroutine, the I/O would be continually set low and the watchdog timer would be allowed to time out, causing a reset or interrupt to be issued.

## Maximum Vcc Fall Time

The Vcc fall time is limited by the propagation delay of the battery switchover comparator and should not exceed  $0.03V/\mu s$ . A standard rule for filter capacitance on most regulators is around  $100\mu F$  per Ampere of current. When the power supply is shut off or the main battery is disconnected, the associated initial Vcc fall rate is just the inverse, or  $1A/100\mu F = 0.01V/\mu s$ .

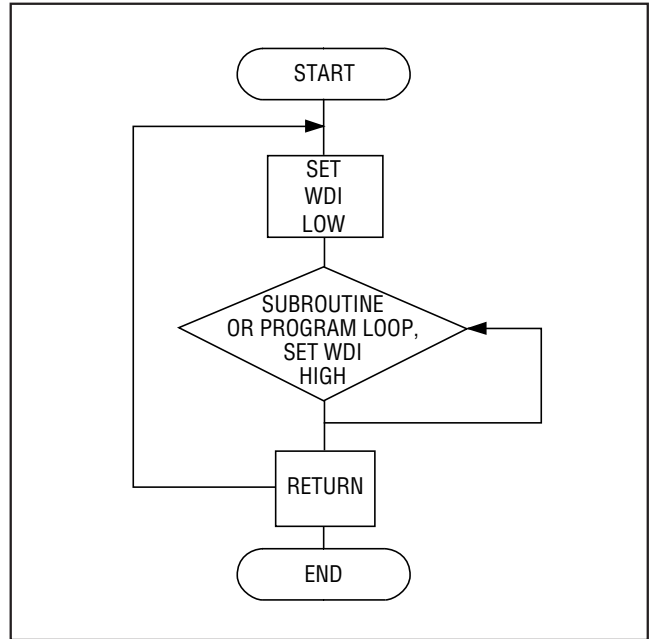
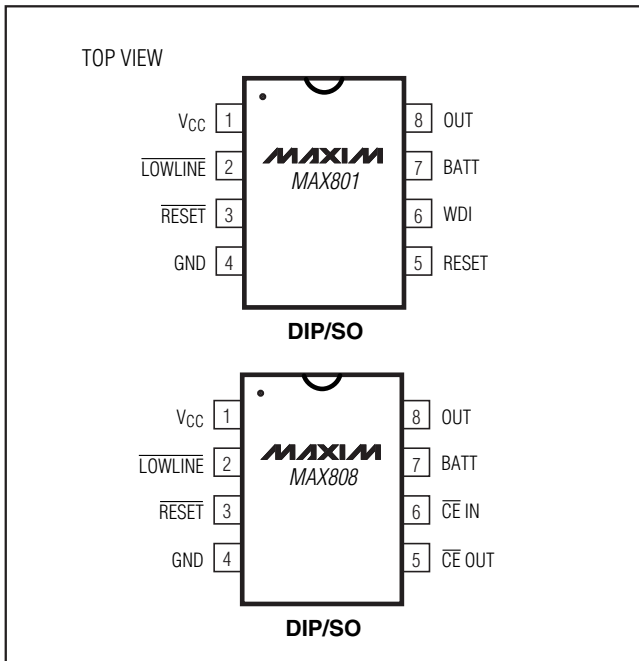


Figure 9. Watchdog Flow Diagram

## Pin Configurations



## Chip Information



TRANSISTOR COUNT: 922

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