THE DATASHEET OF

MAX9268GCM/V+T

www.win-source.net 0086-755-83957316

19-5211; Rev 2; 1/11

EVALUATION KIT AVAILABLE

Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

General Description

The MAX9268 deserializer utilizes Maxim's gigabit multimedia serial link (GMSL) technology. The MAX9268 deserializer features an LVDS system interface for reduced pin count and a smaller package, and pairs with any GMSL serializer to form a complete digital serial link for joint transmission of high-speed video, audio, and bidirectional control data.

The MAX9268 allows a maximum serial payload data rate of 2.5Gbps for a 15m shielded twisted-pair (STP) cable. The deserializer operates up to a maximum output clock rate of 104MHz (3-channel LVDS) or 78MHz (4-channel LVDS). This serial link supports display panels from QVGA (320 x 240) to WXGA (1280 x 800) and higher with 24-bit color.

The 3-channel mode outputs an LVDS clock, three lanes of LVDS data (21 bits), UART control signals, and one I²S audio channel consisting of three signals. The 4-channel mode outputs an LVDS clock, four lanes of LVDS data (28 bits), UART control signals, an I²S audio channel, and auxiliary control outputs. The three audio outputs form a standard I²S interface, supporting sample rates from 8kHz to 192kHz and audio word lengths of 4 to 32 bits. The embedded control channel forms a full-duplex, differential, 100kbps to 1Mbps UART link between the serializer and deserializer. An electronic control unit (ECU), or microcontroller (µC), can be located on the serializer side of the link (typical for video display), on the MAX9268 side of the link (typical for image sensing), or on both sides. In addition, the control channel enables ECU/µC control of peripherals on the remote side, such as backlight control, grayscale gamma correction, camera module, and touch screen. Base-mode communication with peripherals uses either I²C or the GMSL UART format. In addition, the MAX9268 features a bypass mode that enables full-duplex communication using custom UART formats.

The GMSL serializer driver preemphasis, along with the MAX9268 channel equalizer, extends the link length and enhances the link reliability. Spread spectrum is available to reduce EMI on the LVDS and control outputs of the MAX9268. The serial line inputs comply with ISO 10605 and IEC 61000-4-2 ESD protection standards.

The core supply for the MAX9268 is 3.3V. The I/O supply ranges from 1.8V to 3.3V. The MAX9268 is available in a 48-pin TQFP package (7mm x 7mm) with an exposed pad, and is specified over the -40°C to +105°C automotive temperature range.

Features

- **Pairs with Any GMSL Serializer**
- **2.5Gbps Payload-Rate AC-Coupled Serial Link**
- **Scrambled 8b/10b Line Coding**
- **Supports WXGA (1280 x 800) with 24-Bit Color**
- **8.33MHz to 104MHz (3-Channel LVDS) or 6.25MHz to 78MHz (4-Channel LVDS) Output Clock**
- **4-Bit to 32-Bit Word Length, 8kHz to 192kHz I²S Audio Channel Supports High-Definition Audio**
- **Embedded Half-/Full-Duplex Bidirectional Control Channel (100kbps to 1Mbps)**
- **Two 3-Level Inputs Support 9 Device Addresses**
- **Interrupt Supports Touch-Screen Functions for Display Panels**
- **I²C Master for Peripherals**
- **Equalizer for Serial Link Input**
- **Programmable Spread Spectrum on the LVDS and Control Outputs for Reduced EMI**
- **Serial-Data Clock Recovery Eliminates an External Clock**
- **Automatic Data-Rate Detection Allows On-the-Fly Data-Rate Change**
- **Built-In PRBS Generator for BER Testing of the Serial Link**
- **ISO 10605 and IEC 61000-4-2 ESD Protection**
- **-40°C to +105°C Operating Temperature Range**
- **1.8V to 3.3V I/O and 3.3V Core Supplies**
- **Patent Pending**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9268GCM/V+	-40°C to +105°C	48 TQFP-EP*
MAX9268GCM/V+T	-40°C to +105°C	48 TQFP-EP*

/V denotes an automotive qualified product.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Applications

High-Resolution Automotive Navigation

Rear-Seat Infotainment

Megapixel Camera Systems

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.5V to +3.9V
DVDD, IOVDD to AGND.....-0.5V to +3.9V
GND to AGND.....-0.5V to +0.5V
IN+, IN- to AGND .....-0.5V to +1.9V
TXOUT__, TXCLKOUT_ to AGND .....-0.5V to +3.9V
All Other Pins to GND .....-0.5V to (V_{IOVDD} + 0.5V)
TXOUT__, TXCLKOUT_ Short Circuit to Ground or Supply .....Continuous
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 36.2mW/°C above +70°C)....2898.6mW
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
(IN+, IN-) to AGND.....±8kV
(TXOUT__, TXCLKOUT_) to AGND .....±8kV
All Other Pins to GND.....±3.5kV
IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF)
Contact Discharge
(IN+, IN-) to AGND .....±10kV
(TXOUT__, TXCLKOUT_) to AGND.....±8kV
Air Discharge
(IN+, IN-) to AGND.....±12kV
(TXOUT__, TXCLKOUT_) to AGND .....±20kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge
(IN+, IN-) to AGND.....±8kV
(TXOUT__, TXCLKOUT_) to AGND .....±8kV
Air Discharge
(IN+, IN-) to AGND.....±15kV
(TXOUT__, TXCLKOUT_) to AGND .....±30kV
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

48 TQFP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....27.6°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial.**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (BWS, INT, CDS, EQS, MS, $\overline{PWDN}$, SSEN, DRS)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUTS (WS, SCK, SD/CNTL0, CNTL1, CNTL2/MCLK)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA	DCS = 0	V_{IOVDD} - 0.3			V
			DCS = 1	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA	DCS = 0			0.3	V
			DCS = 1			0.2	
Output Short-Circuit Current	I_{OS}	V_{OUT} = V_{GND}, DCS = 0	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
			V_{IOVDD} = 1.7V to 1.9V	3	7	13	
		V_{OUT} = V_{GND}, DCS = 1	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
			V_{IOVDD} = 1.7V to 1.9V	5	10	21	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²C AND UART I/O, OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL, LOCK, $\overline{ERR}$, GPIO_)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0V to V_{IOVDD} (Note 2)	RX/SDA, TX/SCL	-110		+1	µA
			LOCK, $\overline{ERR}$, GPIO_	-80		+1	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
DIFFERENTIAL OUTPUT FOR REVERSE CONTROL CHANNEL (IN+, IN-)							
Differential High Output Peak Voltage, (V_{IN+}) - (V_{IN-})	V_{ROH}	No high-speed data transmission (Figure 1)		30		60	mV
Differential Low Output Peak Voltage, (V_{IN+}) - (V_{IN-})	V_{ROL}	No high-speed data transmission (Figure 1)		-60		-30	mV
DIFFERENTIAL INPUTS (IN+, IN-)							
Differential High Input Threshold (Peak) Voltage, (V_{IN+}) - (V_{IN-})	$V_{IDH(P)}$	Figure 2			40	90	mV
Differential Low Input Threshold (Peak) Voltage, (V_{IN+}) - (V_{IN-})	$V_{IDL(P)}$	Figure 2		-90	-40		mV
Input Common-Mode Voltage ((V_{IN+}) + (V_{IN-}))/2	V_{CMR}			1	1.3	1.6	V
Differential Input Resistance (Internal)	R_I			80	100	130	Ω
THREE-LEVEL LOGIC INPUTS (ADD0, ADD1)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	ADD0 and ADD1 open or connected to a driver with output in high impedance (Note 3)		-10		+10	µA
Input Current	I_{IN}	ADD0 and ADD1 = high or low, $\overline{PWDN}$ = high or low		-150		+150	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
LVDS OUTPUTS (TXOUT__, TXCLKOUT_)							
Differential Output Voltage	V_{OD}	Figure 3		250		450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 3				25	mV
Output Offset Voltage	V_{OS}	Figure 3		1.125		1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 3				25	mV

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DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{OS}	V_{OUT} = 0V or 3.6V	3.5mA LVDS output	-7.5		+7.5	mA
			7mA LVDS output	-15		+15	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	3.5mA LVDS output				7.5	mA
		7mA LVDS output				15	
Output High-Impedance Current	I_{OZ}	ADD0 and ADD1 = high or low, $\overline{PWDN}$ = high or low		-0.5		+0.5	µA
POWER SUPPLY							
Worst-Case Supply Current (Figure 4)	I_{WCS}	BWS = low, $f_{TXCLKOUT_}$ = 16.6MHz			142	180	mA
		BWS = low, $f_{TXCLKOUT_}$ = 33.3MHz			153	200	
		BWS = low, $f_{TXCLKOUT_}$ = 66.6MHz			179	240	
		BWS = low, $f_{TXCLKOUT_}$ = 104MHz			212	280	
Sleep-Mode Supply Current	I_{CCS}				80	130	µA
Power-Down Current	I_{CCZ}	$\overline{PWDN}$ = GND			19	70	µA

AC ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS CLOCK OUTPUTS (TXCLKOUT+, TXCLKOUT-)							
Clock Frequency	$f_{TXCLKOUT_}$	BWS = GND, V_{DRS} = V_{IOVDD}		8.33		16.66	MHz
		BWS = GND, DRS = GND		16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}		6.25		12.5	
		V_{BWS} = V_{IOVDD}, DRS = GND		12.5		78	
I²C/UART PORT TIMING							
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD (Figure 5)		20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD (Figure 5)		20		150	ns
Input Setup Time	t_{SET}	I²C only (Figure 5)		100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 5)		0			ns
SWITCHING CHARACTERISTICS							
CNTL_ Output Rise-and-Fall Time	t_R, t_F	20% to 80%, C_L = 10pF, DCS = 1 (Figure 6)	V_{IOVDD} = 1.7V to 1.9V	0.5		3.1	ns
			V_{IOVDD} = 3.0V to 3.6V	0.3		2.2	
		20% to 80%, C_L = 5pF, DCS = 0 (Figure 6)	V_{IOVDD} = 1.7V to 1.9V	0.6		3.8	
			V_{IOVDD} = 3.0V to 3.6V	0.4		2.4	
LVDS Output Rise Time	t_R	20% to 80%, R_L = 100Ω (Figure 3)			200	350	ps
LVDS Output Fall Time	t_F	80% to 20%, R_L = 100Ω (Figure 3)			200	350	ps

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Output Pulse Position	t_{PPOSN}	N = 0 to 6, t_{CLK} = 1/$f_{TXCLKOUT_}$, $f_{TXCLKOUT_}$ = 104MHz (Figure 7)	$f_{TXCLKOUT_}$ = 12.5MHz	N/7 x t_{CLK} - 250	N/7 x t_{CLK}	N/7 x t_{CLK} + 250	ps
			$f_{TXCLKOUT_}$ = 33MHz	N/7 x t_{CLK} - 200	N/7 x t_{CLK}	N/7 x t_{CLK} + 200	
			$f_{TXCLKOUT_}$ = 78MHz	N/7 x t_{CLK} - 125	N/7 x t_{CLK}	N/7 x t_{CLK} + 125	
			$f_{TXCLKOUT_}$ = 104MHz	N/7 x t_{CLK} - 100	N/7 x t_{CLK}	N/7 x t_{CLK} + 100	
LVDS Output Enable Time	t_{LVEN}	From the last bit of the enable UART packet to V_{OS} = 1125mV				100	µs
LVDS Output Disable Time	t_{LVDS}	From the last bit of the enable UART packet to V_{OS} = 0V				100	µs
Deserializer Delay	t_{SD}	Figure 8 (Note 4)				3540	Bits
Reverse Control-Channel Output Rise Time	t_R	No forward-channel data transmission (Figure 1)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward-channel data transmission (Figure 1)		180		400	ns
Lock Time	t_{LOCK}	Figure 9				3.6	ms
Power-Up Time	t_{PU}	Figure 10				4.1	ms
I²S OUTPUT TIMING							
WS Jitter	t_{AJ-WS}	t_{WS} = 1/f_{WS}, rising (falling) edge to falling (rising) edge (Note 5)	f_{WS} = 48kHz or 44.1kHz		$0.4e^{-3}$ x t_{WS}	$0.5e^{-3}$ x t_{WS}	ns
			f_{WS} = 96kHz		$0.8e^{-3}$ x t_{WS}	$1e^{-3}$ x t_{WS}	
			f_{WS} = 192kHz		$1.6e^{-3}$ x t_{WS}	$2e^{-3}$ x t_{WS}	
SCK Jitter	t_{AJ-SCK}	t_{SCK} = 1/f_{SCK}, rising edge to rising edge	n_{WS} = 16 bits, f_{WS} = 48kHz or 44.1kHz		$13e^{-3}$ x t_{SCK}	$16e^{-3}$ x t_{SCK}	ns
			n_{WS} = 24 bits, f_{WS} = 96kHz		$39e^{-3}$ x t_{SCK}	$48e^{-3}$ x t_{SCK}	
			n_{WS} = 32 bits, f_{WS} = 192kHz		0.1 x t_{SCK}	0.13 x t_{SCK}	
Audio Skew Relative to Video	t_{ASK}	Video and audio synchronized			3 x t_{WS}	4 x t_{WS}	µs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	C_L = 10pF, DCS = 1	0.3		3.1	ns
			C_L = 5pF, DCS = 0	0.4		3.8	
SD, WS Valid Time Before SCK	t_{DVB}	t_{SCK} = 1/f_{SCK} (Figure 11)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{DVA}	t_{SCK} = 1/f_{SCK} (Figure 11)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns

Note 2: Minimum I_{IN} due to voltage drop across the internal pullup resistor.

Note 3: Measured in serial link bit times. Bit time = 1/(30 x $f_{TXCLKOUT_}$) for BWS = GND. Bit time = 1/(40 x $f_{TXCLKOUT_}$) for V_{BWS} = V_{IOVDD}.

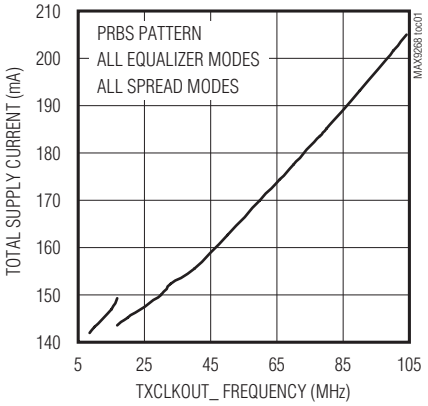
Note 4: Rising to rising-edge jitter can be twice as large.

Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

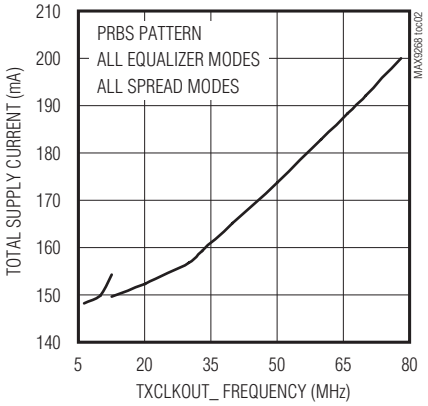
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)

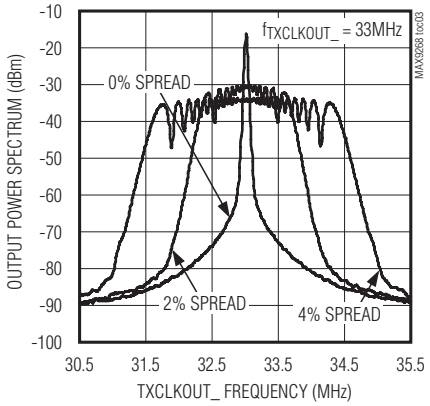
TOTAL SUPPLY CURRENT vs. TXCLKOUT_ FREQUENCY (3-CHANNEL MODE)



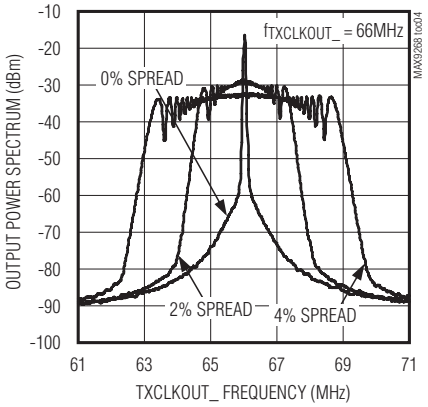
TOTAL SUPPLY CURRENT vs. TXCLKOUT_ FREQUENCY (4-CHANNEL MODE)



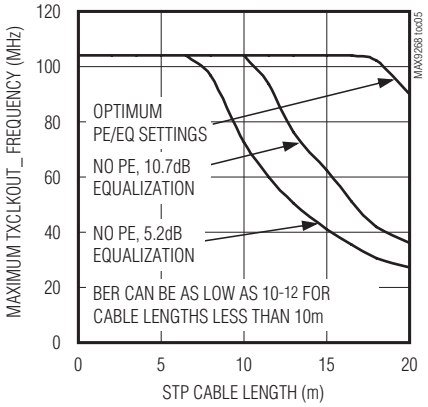
OUTPUT POWER SPECTRUM vs. TXCLKOUT_ FREQUENCY (VARIOUS MAX9268 SPREAD)



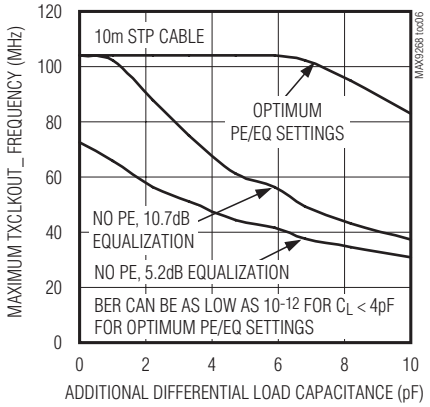
OUTPUT POWER SPECTRUM vs. TXCLKOUT_ FREQUENCY (VARIOUS MAX9268 SPREAD)



MAXIMUM TXCLKOUT_ FREQUENCY vs. STP CABLE LENGTH (BER < 10-9)

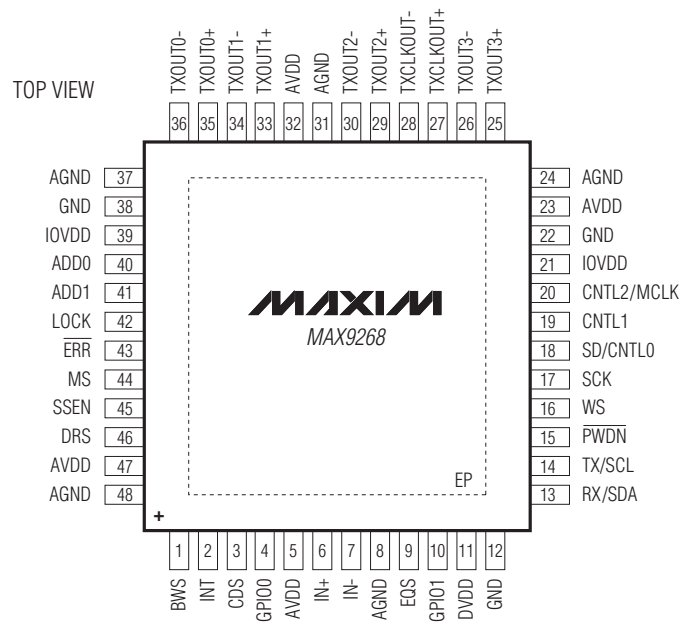


MAXIMUM TXCLKOUT_ FREQUENCY vs. ADDITIONAL DIFFERENTIAL C_L (BER < 10-9)



Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

Pin Configuration



TQFP

Pin Description

PIN	NAME	FUNCTION
1	BWS	Bus-Width Select. Output width selection requires external pulldown or pullup resistor. Set BWS = low for 3-channel mode. Set BWS = high for 4-channel mode.
2	INT	Interrupt Input. Requires external pulldown or pullup resistor. A transition on the MAX9268's INT input toggles the GMSL serializer's INT output.
3	CDS	Control Direction Selection. Control link direction selection input requires external pulldown or pullup resistor. Set CDS = low for µC on the GMSL serializer side of the serial link. Set CDS = high for µC on the MAX9268 side of the serial link.
4	GPIO0	General-Purpose I/O 0. Open-drain, general-purpose input/output with internal 60kΩ (typ) pullup resistor to IOVDD. GPIO0 is high impedance during power-up and when $\overline{PWDN}$ = low.
5, 23, 32, 47	AVDD	3.3V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
6, 7	IN+, IN-	Differential CML Input. Differential input of the serial link.
8, 24, 31, 37, 48	AGND	Analog Ground
9	EQS	Equalizer Select Input. EQS requires external pulldown or pullup resistor. The state of EQS latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set EQS = low for 10.7dB equalizer boost (EQTUNE = 1001). Set EQS = high for 5.2dB equalizer boost (EQTUNE = 0100).

Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

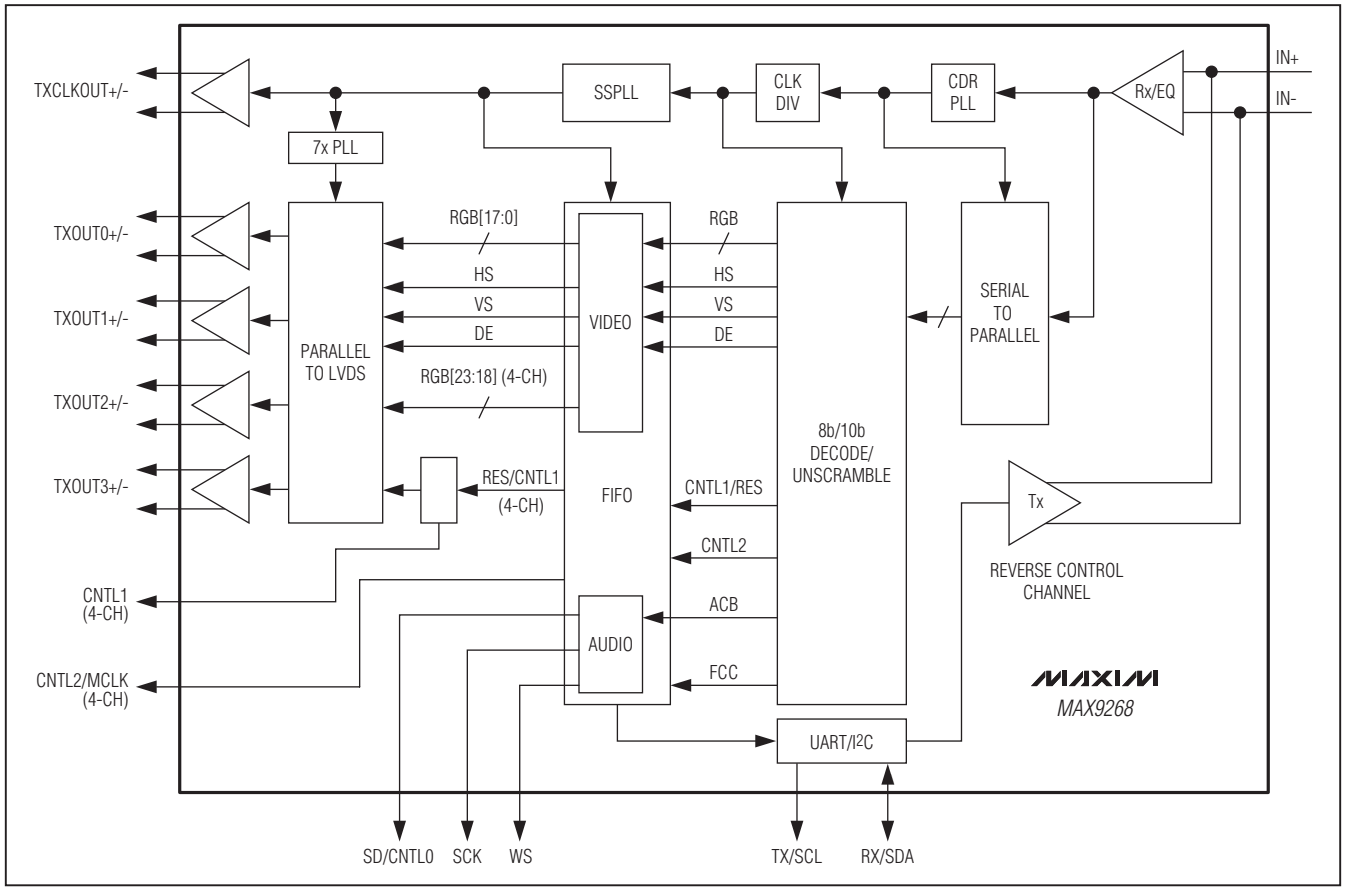
Pin Description (continued)

PIN	NAME	FUNCTION
10	GPIO1	General-Purpose I/O 1. Open-drain general-purpose input/output with internal 60kΩ (typ) pullup resistor to IOVDD. GPIO1 is high impedance during power-up and when $\overline{PWDN}$ = low.
11	DVDD	3.3V Digital Power Supply. Bypass DVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to DVDD.
12, 22, 38	GND	Digital and I/O Ground
13	RX/SDA	Receive/Serial Data. UART receive or I²C serial-data input/output with internal 30kΩ (typ) pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the MAX9268's UART. In I²C mode, RX/SDA is the SDA input/output of the MAX9268's I²C master.
14	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ (typ) pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the MAX9268's UART. In I²C mode, TX/SCL is the SCL output of the MAX9268's I²C master.
15	$\overline{PWDN}$	Power-Down. Active-low power-down input requires external pulldown or pullup resistor.
16	WS	I²S Word-Select Output
17	SCK	I²S Serial-Clock Output
18	SD/CNTL0	I²S Serial-Data/Control Output. Disable I²S to use SD/CNTL0 as an additional control output.
19	CNTL1	Control Output 1. CNTL1 is not active in 3-channel mode and remains low. To use CNTL1, drive BWS high (4-channel mode) and set DISCNTL = 0. CNTL1 is mapped from DOUT27.
20	CNTL2/MCLK	Control 2/MCLK Output. CNTL2/MCLK is not active in 3-channel mode and remains low. To use CNTL2/MCLK, drive BWS high (4-channel mode). CNTL2/MCLK is mapped from DOUT28. CNTL/MCLK can also be used to output MCLK (see the *Additional MCLK Output for Audio Applications* section).
21, 39	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to IOVDD.
25, 26, 29, 30, 33–36	TXOUT_+, TXOUT_-	Differential LVDS Data Outputs. Set BWS = low (3-channel mode) to use TXOUT0_ to TXOUT2_. Set BWS = high (4-channel mode) to use TXOUT0_ to TXOUT3_.
27, 28	TXCLKOUT+, TXCLKOUT-	Differential LVDS Output for the LVDS Clock
40	ADD0	Address Selection Input 0. Three-level input to select the MAX9268's device address (see Table 2). The state of ADD0 latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low).
41	ADD1	Address Selection Input 1. Three-level input to select the MAX9268's device address (see Table 2). The state of ADD1 latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low).
42	LOCK	Open-Drain Lock Output with Internal 60kΩ (typ) Pullup to IOVDD. LOCK = high indicates PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates PLLs are not locked or incorrect serial-word-boundary alignment. LOCK remains low when the configuration link is active. LOCK is high impedance when $\overline{PWDN}$ = low.
43	$\overline{ERR}$	Active-Low, Open-Drain Video Data Error Output with Internal 60kΩ (typ) Pullup to IOVDD. $\overline{ERR}$ goes low when the number of decoding errors during normal operation exceeds a programmed error threshold, or when at least one PRBS error is detected during PRBS test. $\overline{ERR}$ is high impendence when $\overline{PWDN}$ = low.

Pin Description (continued)

PIN	NAME	FUNCTION
44	MS	Mode Select. Control link mode-selection input requires an external pulldown or pullup resistor. Set MS = low to select base mode. Set MS = high to select bypass mode.
45	SSEN	Spread-Spectrum Enable. Serial link spread-spectrum enable input requires an external pulldown or pullup resistor. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±2% spread spectrum on the LVDS and control outputs. Set SSEN = low to use the LVDS and control outputs without spread spectrum.
46	DRS	Data-Rate Select. Data-rate range-selection input requires an external pulldown or pullup resistor. The state of DRS latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set DRS = high for TXCLKOUT_ frequencies of 8.33MHz to 16.66MHz (3-channel mode), or 6.25MHz to 12.5MHz (4-channel mode). Set DRS = low for TXCLKOUT_ frequencies of 16.66MHz to 104MHz (3-channel mode), or 12.5MHz to 78MHz (4-channel mode).
—	EP	Exposed Pad. EP internally connected to AGND. **MUST** externally connect EP to the plane supplying AGND for proper thermal and electrical performance.

Functional Diagram



Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

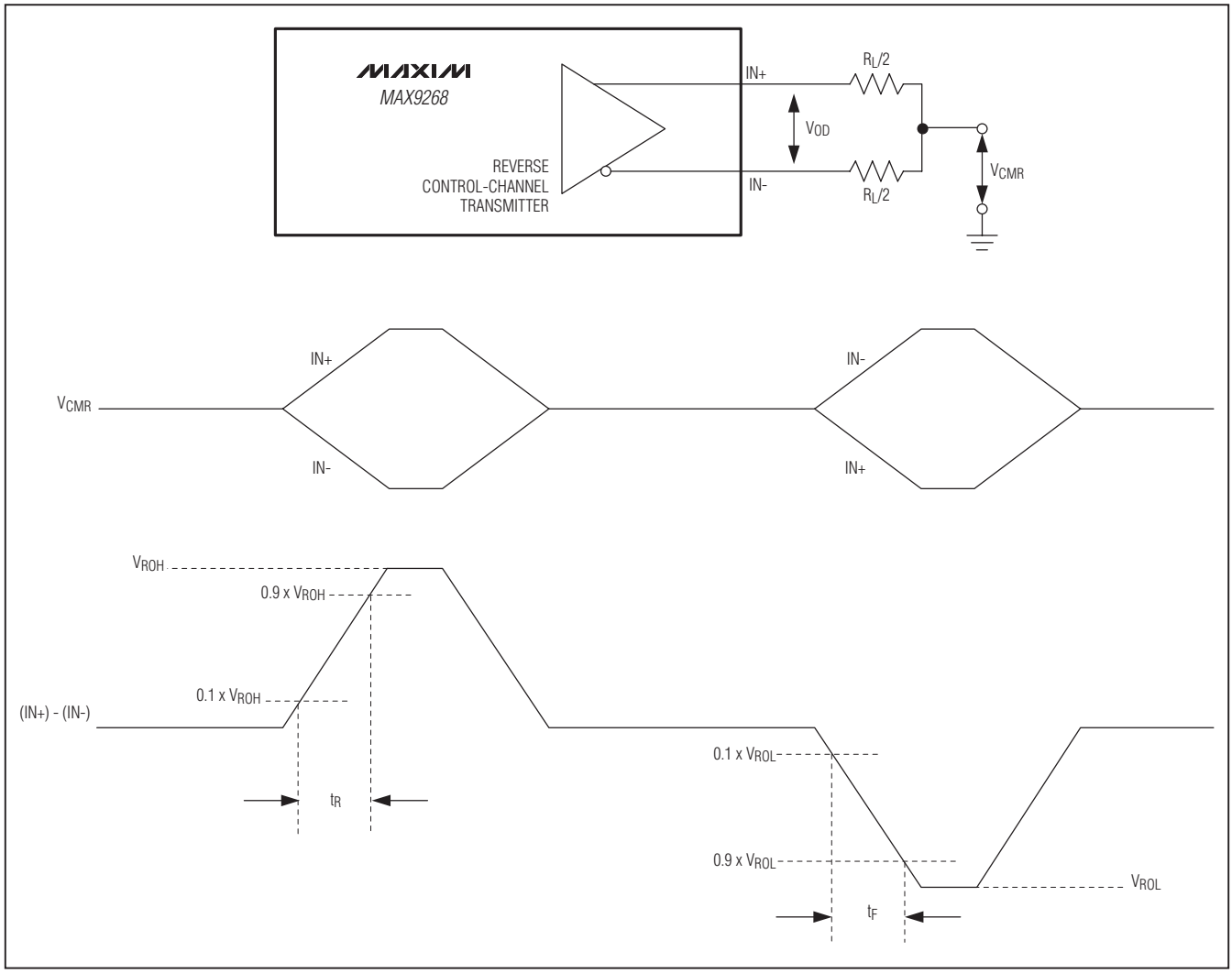


Figure 1. Reverse Control-Channel Output Parameters

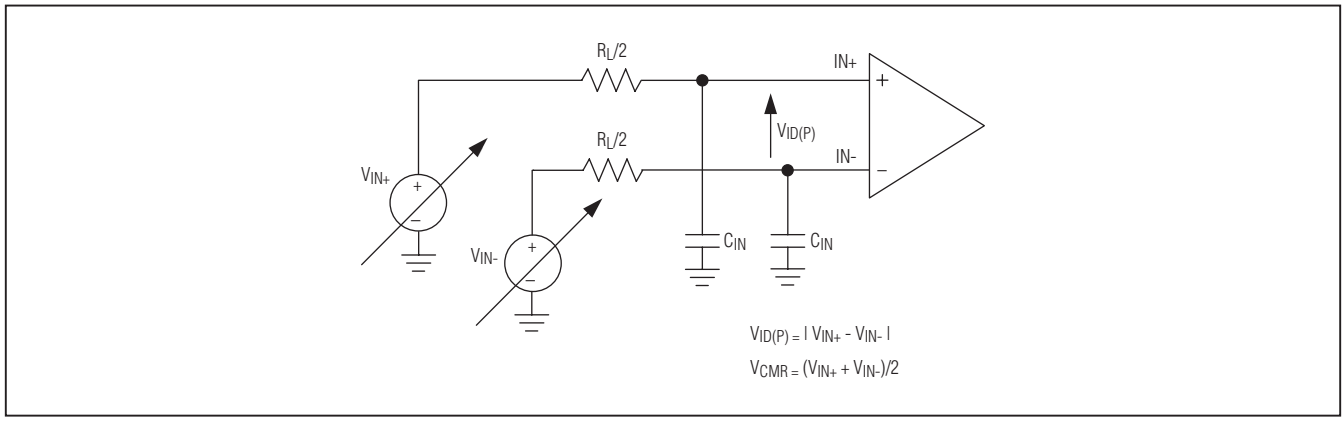


Figure 2. Test Circuit for Differential Input Measurement

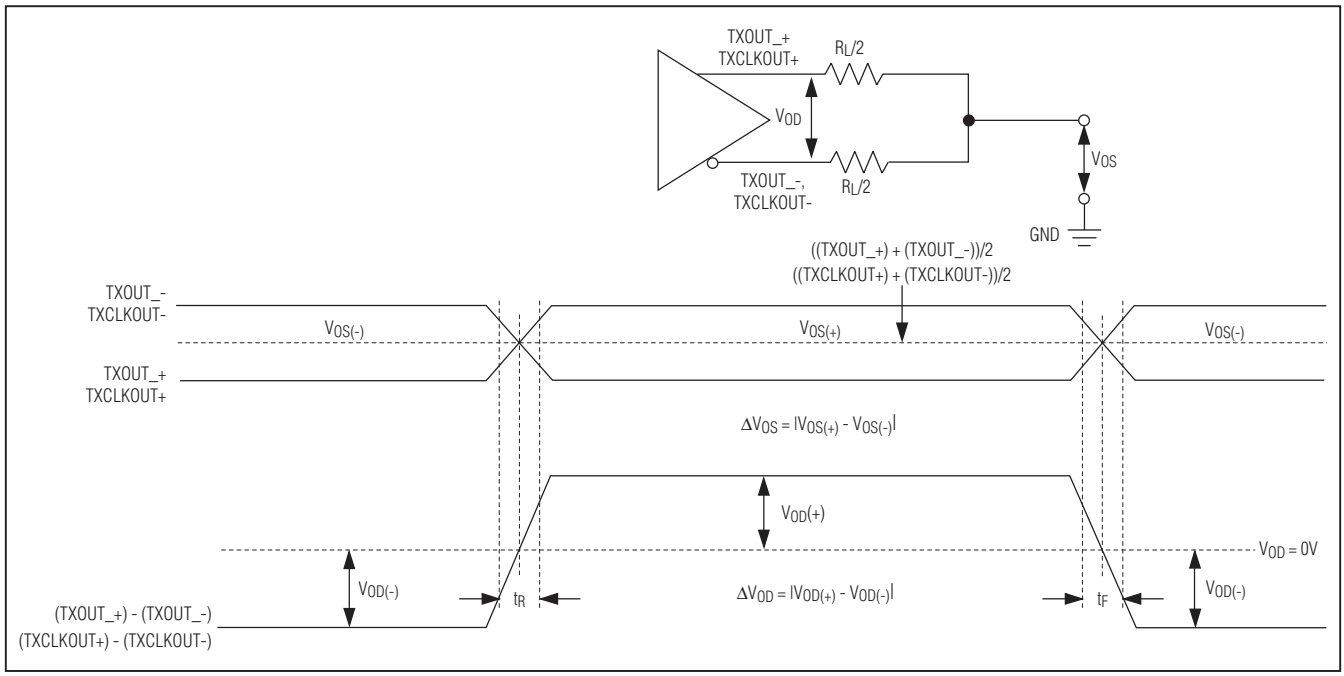


Figure 3. LVDS Output Parameters

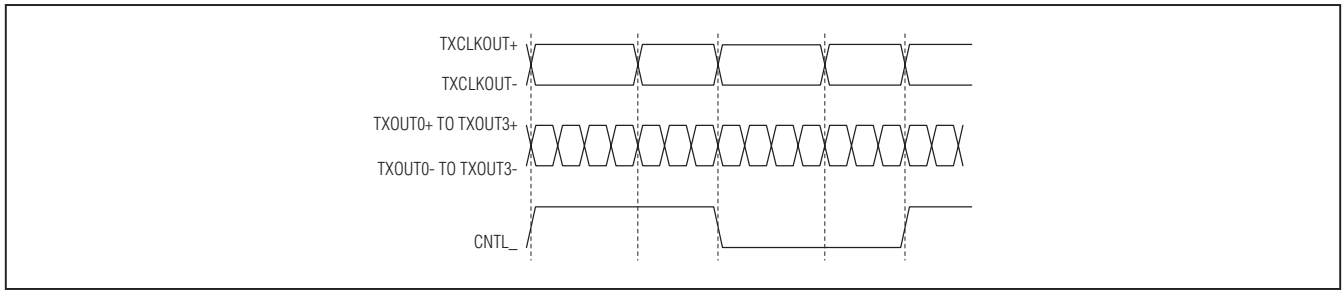


Figure 4. Worst-Case Pattern Output

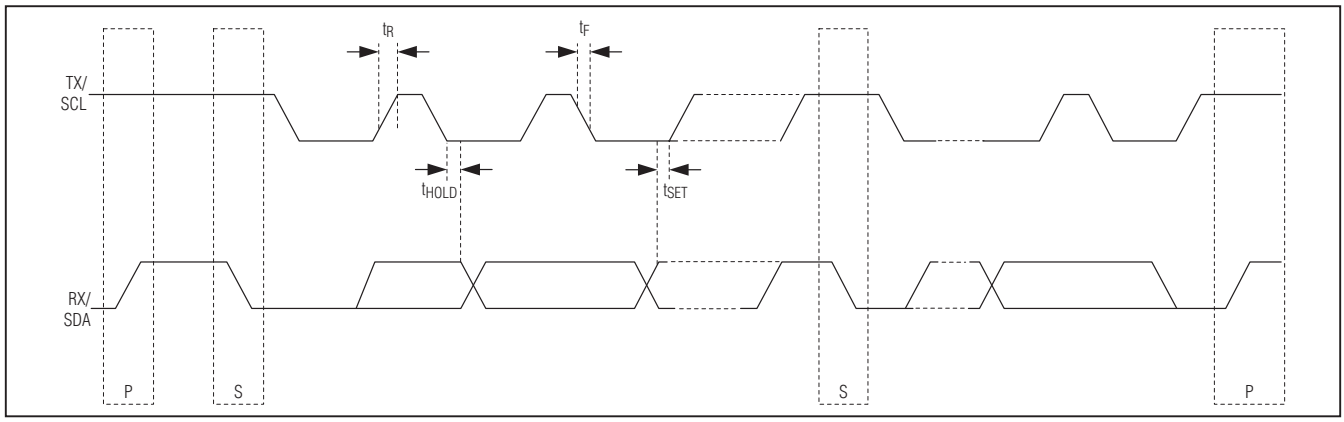


Figure 5. I²C Timing Parameters

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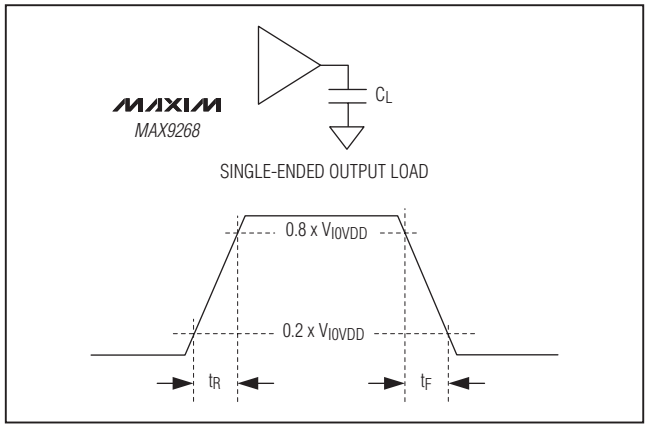

Figure 6. Single-Ended Output Rise-and-Fall Times

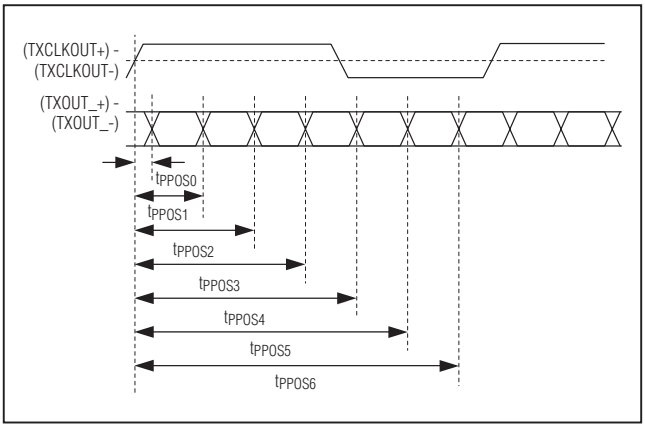

Figure 7. LVDS Output Pulse Position Measurement

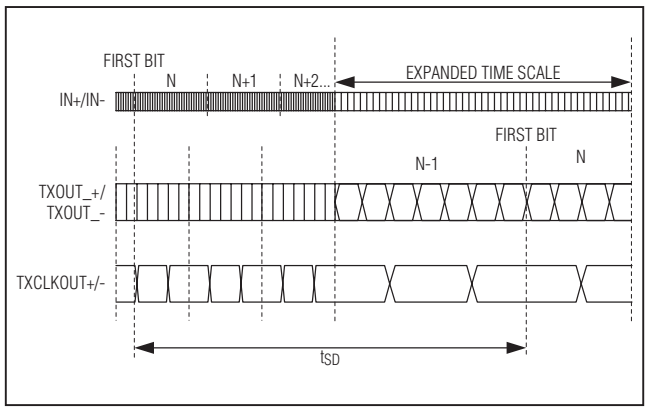

Figure 8. Deserializer Delay

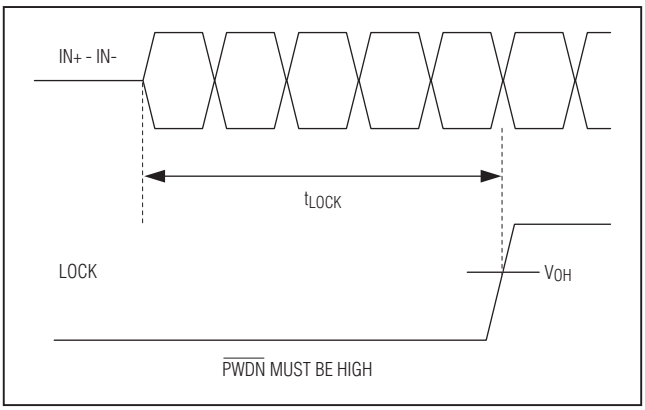

Figure 9. Lock Time

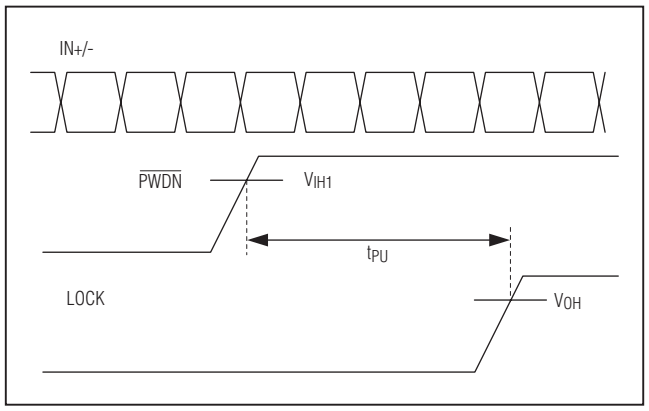

Figure 10. Power-Up Delay

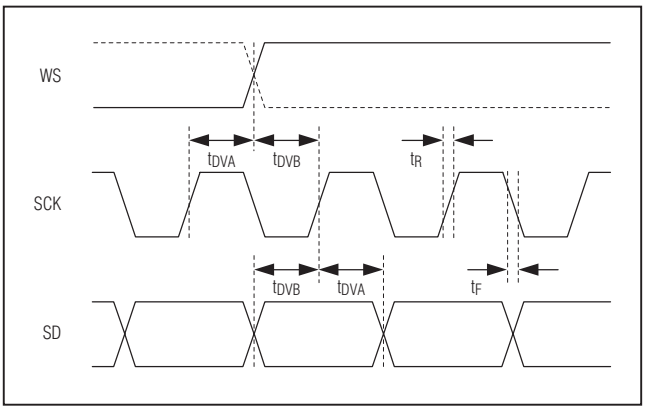

Figure 11. Output I²S Timing Parameters

Detailed Description

The MAX9268 deserializer with LVDS system interface utilizes Maxim's GMSL technology. The MAX9268 deserializer pairs with any GMSL serializer to form a complete digital serial link for joint transmission of high-speed video, audio, and bidirectional control data.

The MAX9268 allows a maximum serial payload data rate of 2.5Gbps for greater than 15m of STP cable. The deserializer operates up to 104MHz for 3-channel LVDS or 78MHz for 4-channel LVDS. The operating frequency range supports display panels from QVGA (320 x 240) up to WXGA (1280 x 800) and higher with 24-bit color.

The 3-channel mode outputs an LVDS clock, three lanes of LVDS data (21 bits), UART control signals, and one I²S audio channel (consisting of three signals). The 4-channel mode outputs an LVDS clock, four lanes of LVDS data (28 bits), UART control signals, one I²S audio channel, and control signals. The I²S interface supports sample rates from 8kHz to 192kHz and audio word lengths of 4 to 32 bits. The embedded control channel forms a full-duplex, differential, 100kbps to 1Mbps UART link between the serializer and deserializer. An ECU or µC can be located on the serializer side of the link (typical for video display), on the MAX9268 side of the link (typical for image sensing), or on both sides. In addition, the control channel enables ECU/µC control of peripherals in the remote side, such as backlight control, grayscale Gamma correction, camera module, and touch screen. Base-mode communication with peripherals uses either I²C or the GMSL UART format. A bypass mode enables full-duplex communication using custom UART formats.

The MAX9268 channel equalizer, along with the serializer preemphasis, extends the link length and enhances the link reliability. Spread spectrum is available to reduce EMI on the LVDS and control outputs of the MAX9268. The serial input complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

The µC configures various operating conditions of the GMSL serializer and the MAX9268 through internal registers. The default device addresses are stored in registers 0x00 and 0x01 of both the GMSL serializer and the MAX9268 (Table 1). Write to the 0x00 and 0x01 registers in both devices to change the device address of the GMSL serializer or the MAX9268.

Table 1. Power-Up Default Register Map (see Table 12)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x40, 0x44, 0x48 0x80, 0x84, 0x88, 0xC0, 0xC4, 0xC8	SERID = XX00XX0, serializer device address is determined by ADD1 and ADD0 (Table 2) RESERVED = 0
0x01	0x50, 0x54, 0x58, 0x90, 0x94, 0x98, 0xD0, 0xD4, 0xD8	DESID =XX01XX0, deserializer device address is determined by ADD1 and ADD0 (Table 2) RESERVED = 0
0x02	0x1F or 0x5F	SS = 00 (SSEN = low), SS = 01 (SSEN = high), spread-spectrum settings depend on SSEN pin state at power-up RESERVED = 0 AUDIOEN = 1, I²S channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking RESERVED = 0 SDIV = 00000, autocalibrate sawtooth divider

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Table 1. Power-Up Default Register Map (see Table 12) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x04	0x03 or 0x13	LOCKED = 0, LOCK output is low (read only) OUTENB = 0, outputs enabled PRBSEN = 0, PRBS test disabled SLEEP = 0 or 1, SLEEP setting default depends on CDS and MS pin state at power-up (see the *Link Startup Procedure* section) INTTYPE = 00, base mode uses I²C REVCCEN = 1, reverse control channel active (sending) FWDCCEN = 1, forward control channel active (receiving)
0x05	0x24 or 0x29	I2CMETHOD = 0, I²C master sends the register address HPFTUNE = 01, 3.75MHz equalizer highpass cutoff frequency PDHF = 0, high-frequency boosting disabled EQTUNE = 0100 (EQS = high, 5.2dB), EQTUNE = 1001 (EQS = low, 10.7dB), EQTUNE default setting depends on EQS pin state at power-up
0x06	0x0F	RESERVED = 0 AUTORST = 0, error registers/output autoreset disabled DISINT = 0, INT transmission enabled INT = 0, INT output is low (read only) GPIO1OUT = 1, GPIO1 output set to high GPIO1 = 1, GPIO1 input = high (read only) GPIO0OUT = 1, GPIO0 output set to high GPIO0 = 1, GPIO0 input = high (read only)
0x07	0x54	RESERVED = 01010100
0x08	0x30	RESERVED = 00110000
0x09	0xC8	RESERVED = 11001000
0x0A	0x12	RESERVED = 00010010
0x0B	0x20	RESERVED = 00100000
0x0C	0x00	ERRTHR = 00000000, error threshold set to zero for decoding errors
0x0D	0x00 (read only)	DECERR = 00000000, zero decoding errors detected
0x0E	0x00 (read only)	PRBSERR = 00000000, zero PRBS errors detected
0x12	0x00	MCLKSRC = 0, MCLK is derived from PCLK (see Table 5) MCLKDIV = 0000000, MCLK output is disabled
0x13	0xX0	RESERVED = XXX RESERVED = 10000
0x14	0x01	RESERVED = 00 FORCELVDS = 0, normal LVDS operation DCS = 0, normal CMOS driver current strength DISCNTL1 = 0, serial-data bit 27 is mapped to CNTL1 DISRES = 0, serial-data bit 27 is mapped to RES ILVDS = 01, 3.5mA LVDS output current

Table 1. Power-Up Default Register Map (see Table 12) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x1E	0x04 (read only)	ID = 00000100, device ID is 0x04
0x1F	0x0X (read only)	RESERVED = 000 CAPS = 0, not HDCP capable REVISION = XXXX

X = Don't care.

Table 2. Deserializer Device Address Defaults (Register 0x01)

PIN		DEVICE ADDRESS* (bin)								SERIALIZER DEVICE ADDRESS* (hex)	DESERIALIZER DEVICE ADDRESS* (hex)
ADD1	ADD0	D7	D6	D5	D4	D3	D2	D1	D0		
Low	Low	1	0	0	X**	0	0	0	R/$\overline{W}$	80	90
Low	High	1	0	0	X**	0	1	0	R/$\overline{W}$	84	94
Low	Open	1	0	0	X**	1	0	0	R/$\overline{W}$	88	98
High	Low	1	1	0	X**	0	0	0	R/$\overline{W}$	C0	D0
High	High	1	1	0	X**	0	1	0	R/$\overline{W}$	C4	D4
High	Open	1	1	0	X**	1	0	0	R/$\overline{W}$	C8	D8
Open	Low	0	1	0	X**	0	0	0	R/$\overline{W}$	40	50
Open	High	0	1	0	X**	0	1	0	R/$\overline{W}$	44	54
Open	Open	0	1	0	X**	1	0	0	R/$\overline{W}$	48	58

**ADD0 and ADD1 affect the default device address values stored in the MAX9268 only. The default device address values stored in the GMSL serializer may differ (see the 3-Level Inputs for Default Device Address section).*

***X = 0 for the serializer address, X = 1 for the deserializer address.*

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Typical Bitmapping and Bus-Width Selection

The LVDS output has two selectable widths: 3-channel and 4-channel. The MAX9268 outputs 3- or 4-channel LVDS (Table 3). Serial data is mapped to outputs on the MAX9268 according to Figures 12 and 13. In 3-channel mode, TXOUT3_ and CNTL1, CNTL2/MCLK are not available. For both modes, the SD/CNTL0, SCK, and WS pins are for I²S audio when audio is enabled. With audio disabled, SD/CNTL0 becomes control signal CNTL0. The MAX9268 outputs clock rates from 8.33MHz to 104MHz for 3-channel mode and 6.25MHz to 78MHz for 4-channel mode.

Serial Link Signaling and Data Format

The GMSL high-speed serial link uses CML signaling with programmable preemphasis and AC-coupling. The GMSL deserializer uses AC-coupling and programmable channel equalization. When using both the preemphasis and equalization, including internally generated overhead bits, the GMSL link operates up to 3.125Gbps over STP cable lengths of 15m or greater. The payload data rate, which is the data rate available to the user or the data rate after subtracting overhead, is 2.5Gbps.

The GMSL serializer scrambles and encodes the input data and sends the 8b/10b coded signal through the serial link. The MAX9268 deserializer recovers the embedded serial clock and then samples, decodes, and descrambles before outputting the data. Figures 14 and 15 show the serial-data packet format after unscrambling and 8b/10b decoding. In 3-channel or 4-channel mode, 21 or 28 bits map to the TXOUT_ _ LVDS outputs. Serial-data bits 27 and 28 map to control outputs in 4-channel mode. The audio channel bit (ACB) contains an encoded audio signal derived from the three I²S signals (SD/CNTL0, SCK, and WS). The forward control-channel (FCC) bit carries the forward control data. The last bit (PCB) is the parity bit of the previous 23 or 31 bits.

Table 3. Bus-Width Selection Using BWS

OUTPUT BITS	3-CHANNEL MODE (BWS = LOW)		4-CHANNEL MODE (BWS = HIGH)	
	TYPICAL BITMAPPING	AUXILIARY SIGNALS MAPPING	TYPICAL BITMAPPING	AUXILIARY SIGNALS MAPPING
DOUT[0:5]	R[0:5]	—	R[0:5]	—
DOUT[6:11]	G[0:5]	—	G[0:5]	—
DOUT[12:17]	B[0:5]	—	B[0:5]	—
DOUT[18:20]	HS, VS, DE	—	HS, VS, DE	—
DOUT[21:22]	Not used	Not used	R6, R7	—
DOUT[23:24]	Not used	Not used	G6, G7	—
DOUT[25:26]	Not used	Not used	B6, B7	—
DOUT27	Not used	Not used	RES*	CNTL1*
DOUT28	Not used	Not used	—	CNTL2/MCLK
SD	—	SD/CNTL0	—	SD/CNTL0

**See the Reserved Bit (RES)/CNTL1 section for details.*

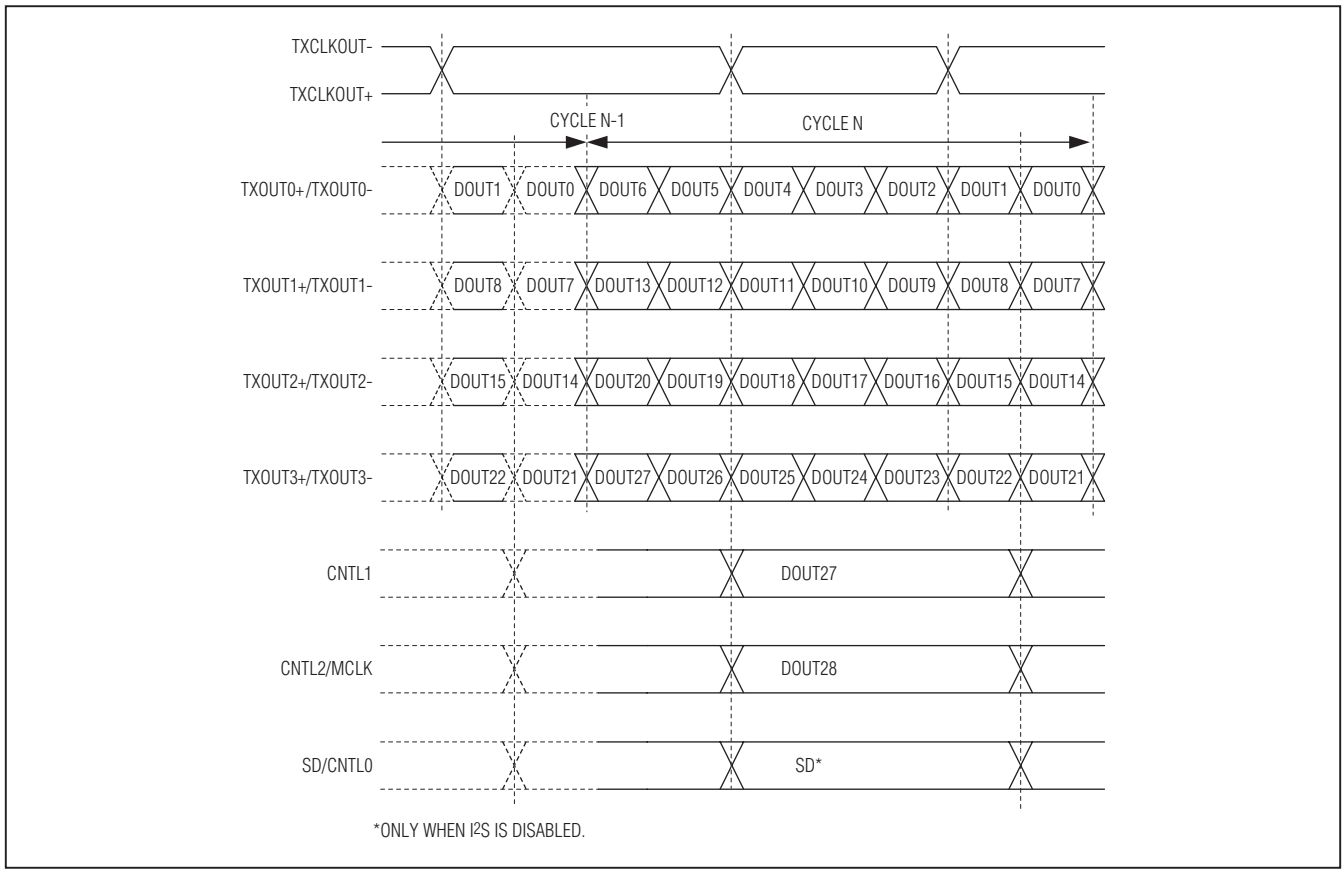

Figure 12. LVDS Output Timing

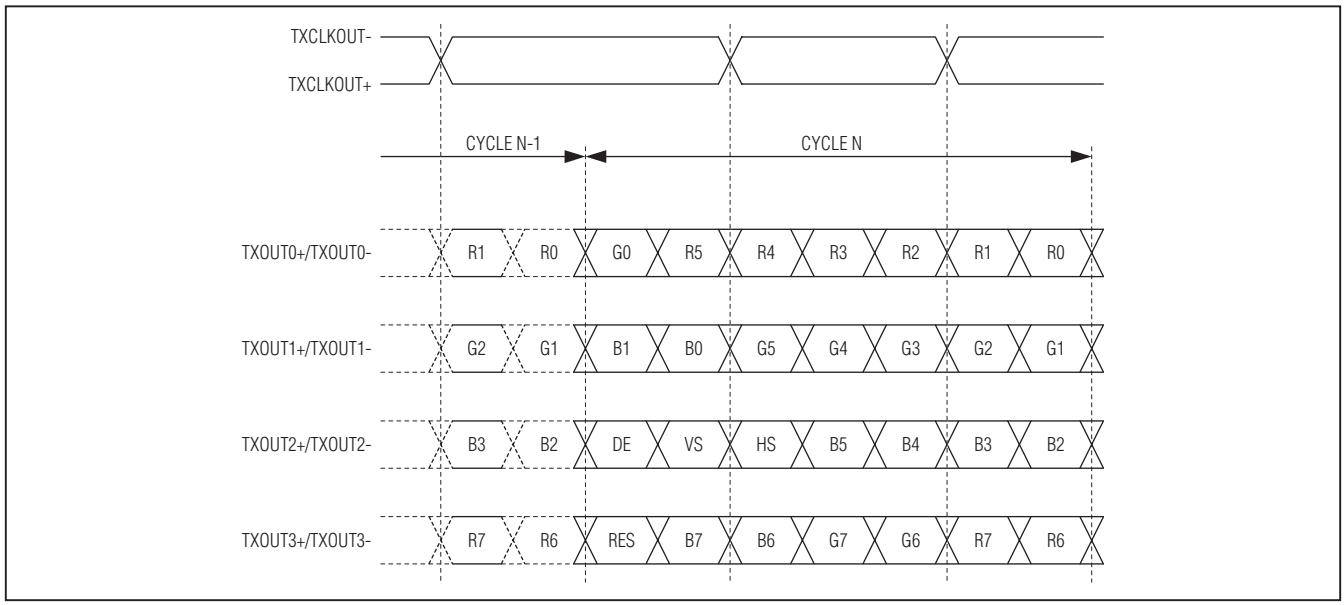

Figure 13. Typical Panel Clock and Bit Assignment

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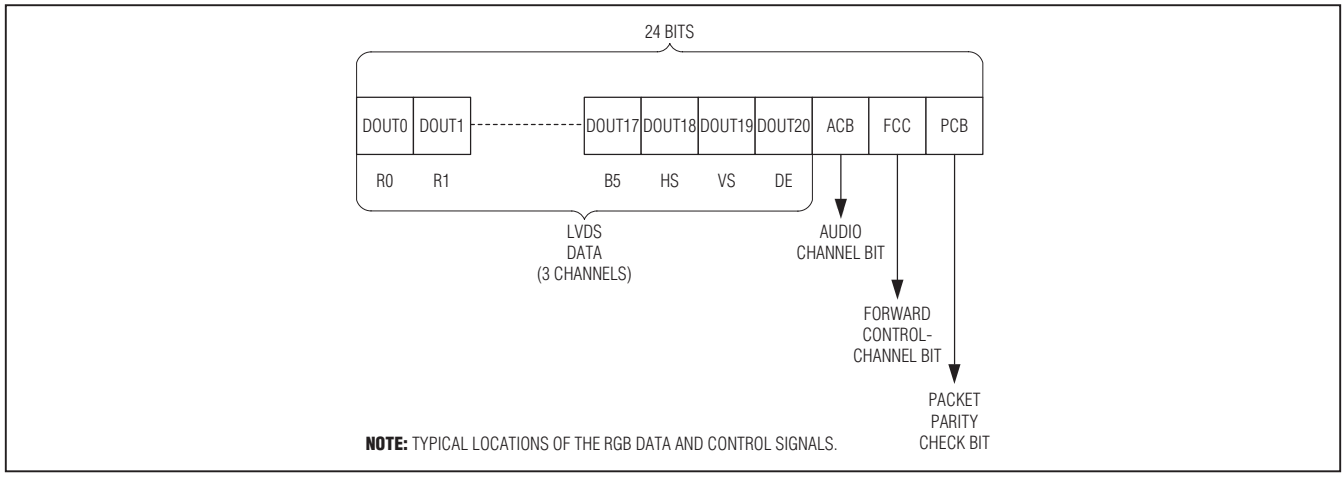

Figure 14. 3-Channel Mode Serial Link Data Format

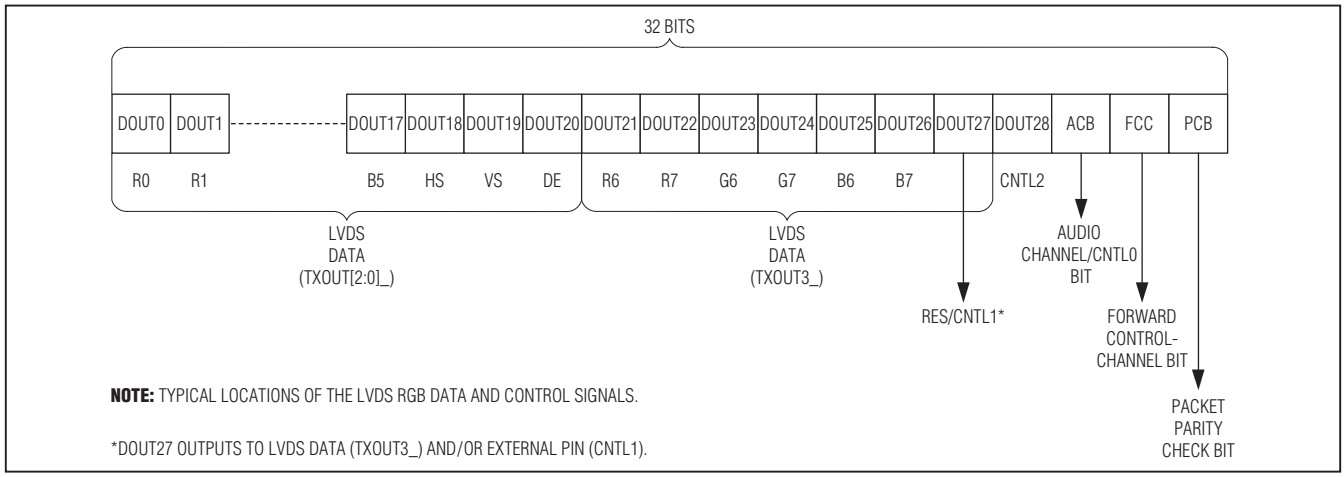

Figure 15. 4-Channel Mode Serial Link Data Format

Reserved Bit (RES)/CNTL1

In 4-channel mode, the MAX9268 deserializes serial-data bit 27 to both RES and CNTL1 by default (both DISCNTL and DISRES = 0). Setting DISRES (D2 of register 0x14) = 1 forces RES low. Setting DISCNTL1 (D3 of register 0x14) = 1 forces CNTL1 low.

Reverse Control Channel

The GMSL serializer uses the reverse control channel to receive I²C/UART and interrupt signals from the MAX9268 in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same twisted pair forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 500µs after power-up. The GMSL serializer temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

Data-Rate Selection

The MAX9268 uses the DRS input to set the TXCLKOUT_ frequency. Set DRS high for a TXCLKOUT_ frequency of 6.25MHz to 12.5MHz (4-channel mode), or 8.33MHz to 16.66MHz (3-channel mode). Set DRS low for normal operation with a TXCLKOUT_ frequency of 12.5MHz to 78MHz (4-channel mode), or 16.66MHz to 104MHz (3-channel mode).

Audio Channel

The I²S audio channel supports audio sampling rates from 8kHz to 192kHz and audio word lengths from 4 bits to 32 bits. The audio bit clock (SCK) does not have to be synchronized with TXCLKOUT_. The GMSL serializer automatically encodes audio data into a single bit stream

synchronous with TXCLKOUT_. The MAX9268 deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I²S format. The audio channel is enabled by default. When the audio channel is disabled, the audio data input (SD) on the serializer becomes a control input (CNTL0) and SD/CNTL0 becomes a control output on the deserializer.

Low TXCLKOUT_ frequencies limit the maximum audio sampling rate. Table 4 lists the maximum audio sampling rate for various TXCLKOUT_ frequencies. Spread-spectrum settings do not affect the I²S data rate or WS clock frequency.

Additional MCLK Output for Audio Applications

Some audio DACs such as the MAX9850 do not require a synchronous main clock (MCLK), while other DACs require MCLK to be a specific multiple of WS. If the audio DAC chip needs the MCLK to be a multiple of WS, use an external PLL to regenerate the required MCLK from WS or SCK.

For audio applications that have WS synchronous to TXCLKOUT_, the MAX9268 provides a divided clock output on CNTL2/MCLK at the expense of one less control line in 4-channel mode (3-channel mode is not affected). By default, CNTL2/MCLK operates as a control data output, and MCLK is turned off. Set MCLKDIV (MAX9268 register 0x12, D[6:0]) to a nonzero value to enable the MCLK output. Set MCLKDIV to 0x00 to disable MCLK and set CNTL2/MCLK as a control data output.

The output MCLK frequency is:

$$f_{MCLK} = \frac{f_{SRC}}{MCLKDIV}$$

where:

f_{SRC} = the MCLK source frequency (Table 5)

MCLKDIV = the divider ratio from 1 to 127

Choose MCLKDIV values such that f_{MCLK} is not greater than 60MHz. MCLK frequencies derived from TXCLKOUT_ (MSCLKSRC = 0) are not affected by spread-spectrum settings in the MAX9268. However, enabling spread spectrum in the GMSL serializer introduces spread spectrum into MCLK. Spread-spectrum settings of either device do not affect MCLK frequencies derived from the internal oscillator. The internal oscillator frequency ranges from 100MHz to 150MHz over all process corners and operating conditions.

Table 4. Maximum Audio WS Frequency (kHz) for Various TXCLKOUT_ Frequencies

WORD LENGTH (BITS)	TXCLKOUT_ FREQUENCY (DRS = LOW) (MHz)				TXCLKOUT_ FREQUENCY (DRS = HIGH) (MHz)			
	12.5	15	16.6	> 20	6.25	7.5	8.33	> 10
8	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
16	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
18	185.5	> 192	> 192	> 192	185.5	> 192	> 192	> 192
20	174.6	> 192	> 192	> 192	174.6	> 192	> 192	> 192
24	152.2	182.7	> 192	> 192	152.2	182.7	> 192	> 192
32	123.7	148.4	164.3	> 192	123.7	148.4	164.3	> 192

Table 5. f_{SRC} Settings

MCLKSRC SETTING (REGISTER 0x12, D7)	DATA-RATE SETTING	BUS-WIDTH SETTING	MCLK SOURCE FREQUENCY (f_{SRC})
0	High speed	3-channel mode	3 x $f_{TXCLKOUT_}$
		4-channel mode	4 x $f_{TXCLKOUT_}$
	Low speed	3-channel mode	6 x $f_{TXCLKOUT_}$
		4-channel mode	8 x $f_{TXCLKOUT_}$
1	—	—	Internal oscillator (120MHz, typ)

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Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data, to program registers on the link serializer/deserializer or to program peripherals. Configuring the CDS pin allows a µC to control the link from the side of the serializer or deserializer, or with dual µCs from both sides, to support a wide variety of applications.

The control channel runs in base mode or bypass mode according to the mode-selection (MS) input of the device connected to the µC. In base mode, the control-channel transactions are half-duplex and in bypass mode they are full-duplex.

Base Mode

In base mode the µC is the host, and in order to access the registers of the serializer or deserializer it must use the GMSL UART format and protocol. The µC accesses peripherals with an I²C interface by sending GMSL UART packets, which are converted to I²C by the serializer or deserializer on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings) using the GMSL UART protocol. The device addresses of the GMSL serializer and MAX9268 in base mode are programmable. The default MAX9268 device address is determined by ADD0 and ADD1 upon power-up, or after returning from a power-down state (Table 2).

When the peripheral interface uses I²C (default), the GMSL serializer/MAX9268 convert packets to I²C that have device addresses different from those of the GMSL serializer or MAX9268. The converted I²C bit rate is the same as the original UART bit rate.

The GMSL serializer embeds control signals going to the MAX9268 in the high-speed forward link. The MAX9268 uses a proprietary differential line coding to send signals back towards the serializer. The speed of the control channel ranges from 100kbps to 1Mbps in both directions. The GMSL serializer and MAX9268 deserializer automatically detect the control-channel bit rate in base mode. Packet bit rates can vary up to 3.5x from the previous bit rate (see the *Changing the Clock Frequency section*). Figure 16 shows the UART protocol for writing and reading in base mode between the µC and the GMSL serializer/MAX9268.

Figure 17 shows the UART data format. Figures 18 and 19 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and interrupt generate transitions on the control channel that should be ignored by the µC. Data written to the GMSL serializer/MAX9268 registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify write commands received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART data rate automatically. If the INT or MS inputs of the MAX9268 toggle while there is control-channel communication, the control-channel communication can be corrupted since INT has priority on the control channel. In the event of a missed acknowledge, the µC should assume there was an error in the packet when the slave device receives it, or that an error occurred during the response from the slave device. In base mode, the µC must keep the UART Tx/Rx lines high for 16 bit times before sending a new packet.

As shown in Figure 20, the remote-side device converts the packets going to or coming from the peripherals from the UART format to the I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C's data rate is the same as the UART data rate.

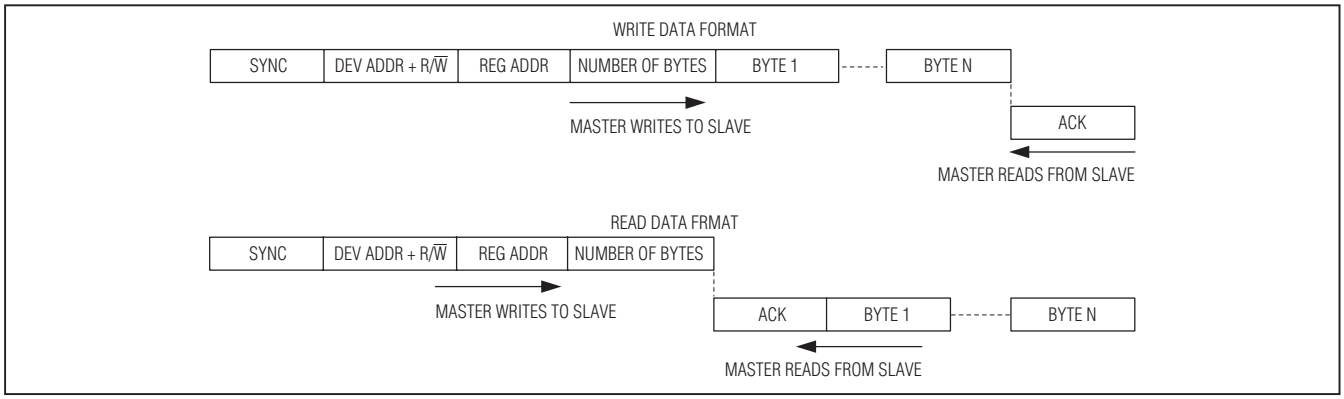

Figure 16. GMSL UART Protocol for Base Mode

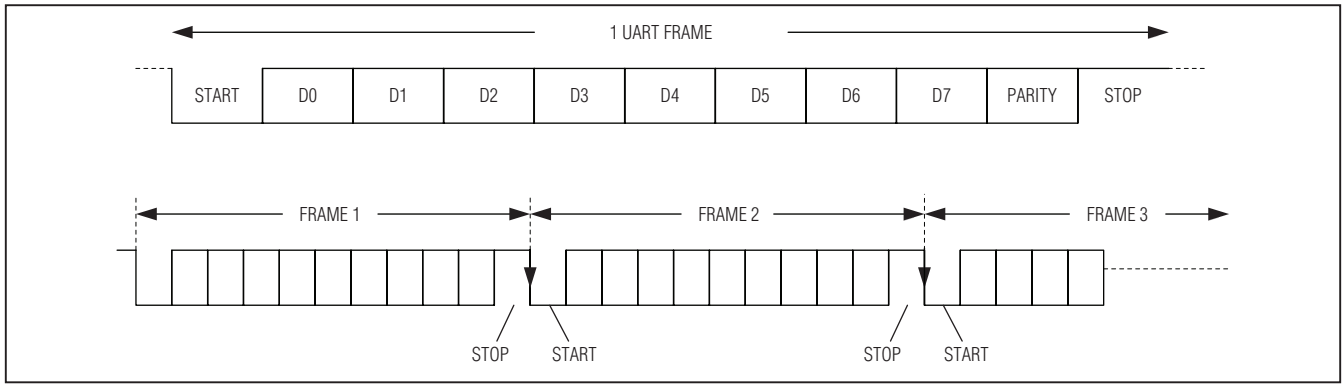

Figure 17. GMSL UART Data Format for Base Mode

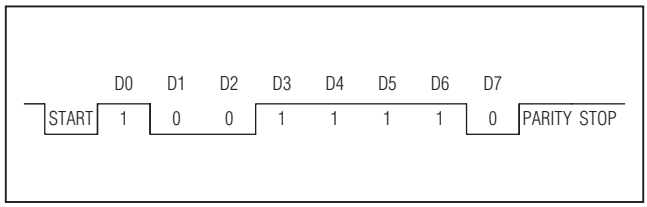

Figure 18. SYNC Byte (0x79)

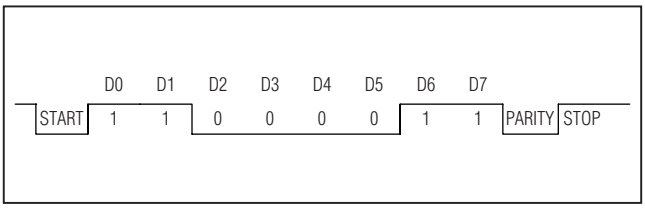

Figure 19. ACK Byte (0xC3)

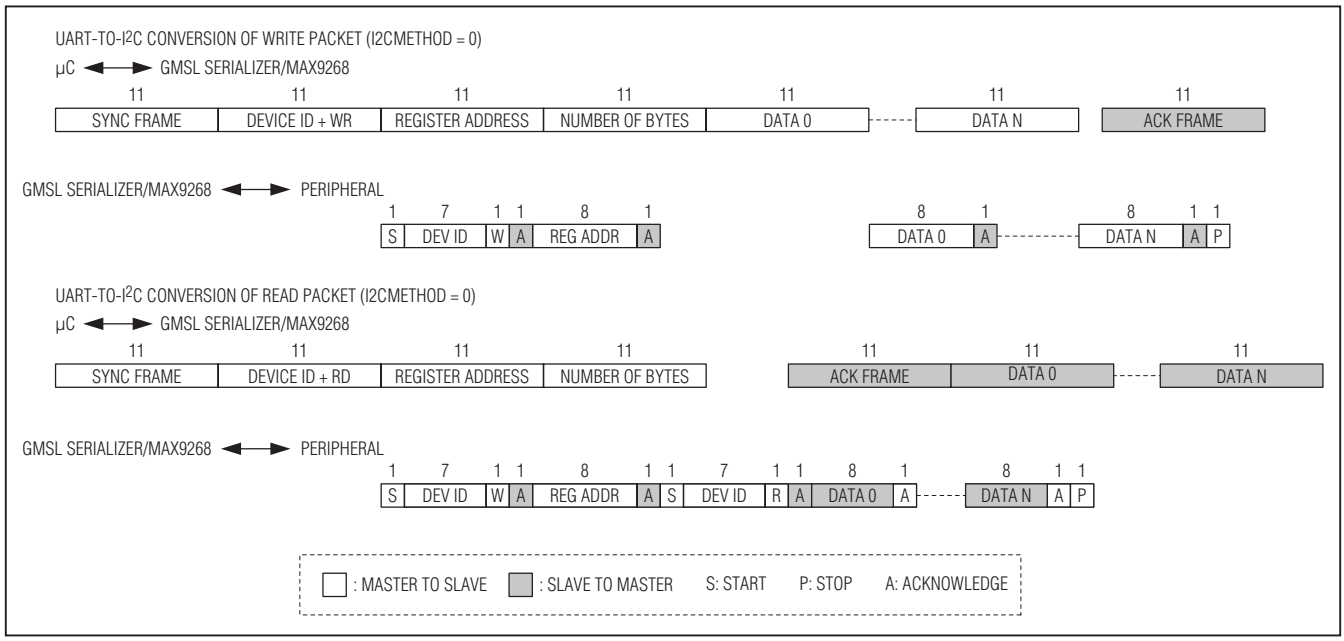

Figure 20. Format Conversion between GMSL UART and I²C with Register Address (I2CMETHOD = 0)

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Interfacing Command-Byte-Only I²C Devices

The GMSL serializer and MAX9268 UART-to-I²C conversion interfaces with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 21). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

Bypass Mode

In bypass mode, the GMSL serializer/MAX9268 ignore UART communications. The µC is thereby free to communicate with the peripherals using its own UART protocol without concern that communication traffic inadvertently misprograms the GMSL serializer or MAX9268. The µC cannot access the GMSL serializer/MAX9268 registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one TXCLKOUT_ period of jitter due to the asynchronous sampling of the UART signal by TXCLKOUT_.

Set MS = high to put the control channel into bypass mode. For applications with the µC connected to the deserializer (CDS is high), there is a 1ms wait time between setting MS high and the bypass control channel being active. There is no delay time when switching to bypass mode when the µC is connected to the serializer (CDS = low). Bypass mode accepts bit rates down to 28kbps in the forward direction (serializer to deserializer), and 7.7kbps in the reverse direction (deserializer to serializer). See the *Interrupt Control* section for interrupt functionality limitations. The control-channel data pattern should not be held low longer than 100µs if interrupt control is used.

Interrupt Control

The INT pin of the GMSL serializer is the interrupt output and the INT pin of the MAX9268 is the interrupt input. The interrupt output on the GMSL serializer follows the transitions at the interrupt input, even during reverse-channel communication or loss of lock. This interrupt function supports remote-side functions such as touchscreen peripherals, remote power-up, or remote monitoring. Interrupts that occur during periods where the reverse control channel is disabled, such as link startup/shutdown, are automatically resent once the reverse control channel becomes available again. Bit D4 of register 0x06 in the MAX9268 also stores the interrupt input state. The INT output of the GMSL serializer is low after power-up. In addition, the µC can set the INT output of the serializer by writing to the SETINT register bit. In normal operation, the state of the interrupt output changes when the interrupt input on the MAX9268 toggles. Do not send a logic-low value longer than 100µs in either base or bypass mode to ensure proper interrupt functionality.

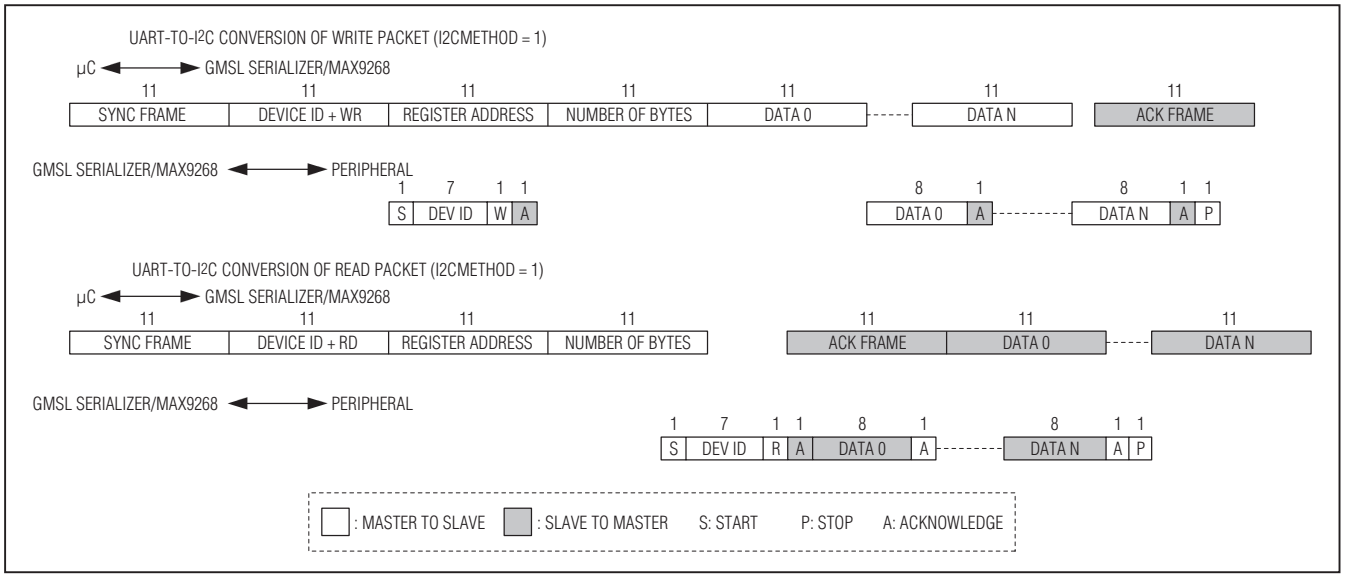

Figure 21. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 1)

Line Equalizer

The MAX9268 includes an adjustable line equalizer to further compensate cable attenuation at high frequencies. The cable equalizer has 12 selectable levels of compensation, from 2.1dB to 13dB (Table 6). The EQS input selects the default equalization level at power-up. The state of EQS is latched upon power-up or when resuming from power-down mode. To select other equalization levels, set the corresponding register bits in the MAX9268 (0x05 D[3:0]). Use equalization in the MAX9268, together with preemphasis in the GMSL serializer, to create the most reliable link for a given cable.

Spread Spectrum

To reduce the EMI generated by the transitions on the serial link and outputs of the MAX9268, both the GMSL serializer and MAX9268 support spread spectrum. Turning on spread spectrum on the GMSL serializer spreads the serial data and the MAX9268 outputs. Do not enable spread for both the GMSL serializer and the MAX9268. The two selectable spread-spectrum rates at the MAX9268 outputs are ±2% and ±4% (Table 7).

Set the MAX9268 SSEN input high to select 2% spread at power-up, and SSEN input low to select no spread at power-up. The state of SSEN is latched upon power-up or when resuming from power-down mode.

Turning on spread spectrum on the GMSL serializer or the MAX9268 does not affect the audio data stream. Changes in the GMSL serializer spread settings only affect the MAX9268 MCLK output if it is derived from TXCLKOUT_ (MCLKSRC = 0).

The MAX9268 includes a sawtooth divider to control the spread-modulation rate. Autodetection or manual programming of the TXCLKOUT_ operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV, 0x03 D[4:0]) allows the user to set a modulation frequency according to the TXCLKOUT_ frequency. Always keep the modulation frequency between 20kHz to 40kHz to ensure proper operation.

Manual Programming of the Spread-Spectrum Divider

The modulation rate for the MAX9268 relates to the TXCLKOUT_ frequency as follows:

$$f_M = (1 + DRS)\frac{f_{TXCLKOUT_}}{MOD \times SDIV}$$

where:

f_M = Modulation frequency

DRS = DRS input value (0 or 1)

$f_{TXCLKOUT_}$ = LVDS clock frequency

MOD = Modulation coefficient given in Table 8

SDIV = 5-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the spread-spectrum settings.

Table 6. Cable Equalizer Boost Levels

BOOST SETTING (0x05 D[3:0])	TYPICAL BOOST GAIN (dB)
0000	2.1
0001	2.8
0010	3.4
0011	4.2
0100	5.2 **Power-up default (EQS = high)**
0101	6.2
0110	7
0111	8.2
1000	9.4
1001	10.7 **Power-up default (EQS = low)**
1010	11.7
1011	13

Table 7. LVDS and Control Output Spread Rates

SS	SPREAD (%)
00	No spread spectrum. **Power-up default when SSEN = low.**
01	±2% spread spectrum. **Power-up default when SSEN = high.**
10	No spread spectrum
11	±4% spread spectrum

Table 8. Modulation Coefficients and Maximum SDIV Settings

SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT (dec)	SDIV UPPER LIMIT (dec)
4	208	15
2	208	30

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Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 8, set SDIV to the maximum value.

Sleep Mode

The GMSL serializer/MAX9268 include low-power sleep mode to reduce power consumption on the device not attached to the µC (the MAX9268 in LCD applications and the GMSL serializer in camera applications). Set the corresponding remote IC's SLEEP bit to 1 to initiate sleep mode. The GMSL serializer sleeps immediately after setting its SLEEP = 1. The MAX9268 sleeps after serial link inactivity or 8ms (whichever arrives first) after setting its SLEEP = 1. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

The µC side device cannot enter into sleep mode. If an attempt is made to program the µC side device for sleep, the SLEEP bit remains 0. Use the power-down mode to bring the µC side device into a low-power state.

Power-Down Mode

The MAX9268 includes a power-down mode to further reduce power consumption. Set $\overline{PWDN}$ low to enter power-down mode. While in power-down mode, the outputs of the device remain high impedance. Entering power-down mode resets the internal registers of the device. In addition, upon exiting power-down mode, the MAX9268 relatches the state of SSEN, EQS, DRS, and ADD_.

Configuration Link Mode

The GMSL includes a low-speed configuration link to allow control-data connection between the two devices in the absence of a valid clock input. In either display or camera applications, the configuration link can be used to program equalizer/preemphasis or other registers before establishing the video link. An internal oscillator provides a clock for establishing the serial configuration link between the GMSL serializer and the MAX9268. Set CLINKEN = 1 on the GMSL serializer to turn on the configuration link. The configuration link remains active as long as the video link has not been enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Startup Procedure

Table 9 lists four startup cases for video-display applications. Table 10 lists two startup cases for image-sensing applications. In either video-display or image-sensing applications, the control link is always available after the high-speed data link or the configuration link is established and the GMSL serializer/MAX9268 registers or peripherals are ready for programming.

Video-Display Applications

For a video-display application with a remote display unit, connect the µC to the GMSL serializer and set CDS = low for both the GMSL serializer and the MAX9268. Table 9 summarizes the four startup cases based on the settings of $\overline{AUTOS}$ and MS.

Case 1: Autostart Mode

After power-up or when $\overline{PWDN}$ transitions from low to high for both the serializer and deserializer, the serial link establishes whether a stable clock is present. The GMSL serializer locks to the clock and sends the serial data to the MAX9268. The MAX9268 then detects activity on the serial link and locks to the input serial data.

Case 2: Standby Start Mode

After power-up or when $\overline{PWDN}$ transitions from low to high for both the serializer and deserializer, the MAX9268 starts up in sleep mode, and the GMSL serializer stays in standby mode (does not send serial data). Use the µC and program the serializer to set SEREN = 1 to establish a video link or CLINKEN = 1 to establish the configuration link. After locking to a stable clock (for SEREN = 1) or the internal oscillator (for CLINKEN = 1), the serializer sends a wake-up signal to the MAX9268. The MAX9268 exits sleep mode after locking to the serial data and sets SLEEP = 0. If after 8ms the MAX9268 does not lock to the input serial data, the deserializer goes back to sleep and the internal sleep bit remains set (SLEEP = 1).

Case 3: Remote Side Autostart Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the remote device (MAX9268) starts up and tries to lock to an incoming serial signal with sufficient power. The host side (GMSL serializer) is in standby mode and does not try to establish a link. Use the µC and program the serializer to set SEREN = 1 (and apply a stable clock signal) to establish a video link, or CLINKEN = 1 to establish the configuration link. In this case, the MAX9268 ignores the short wake-up signal sent from the GMSL serializer.

Case 4: Remote Side in Sleep Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the remote device (MAX9268) starts up in sleep mode. The high-speed link establishes automatically after the GMSL serializer powers up with a stable clock signal and sends a wake-up signal to the MAX9268. Use this mode in applications where the MAX9268 powers up before the GMSL serializer.

Table 9. Startup Selection for Display Applications (CDS = Low)

CASE	$\overline{\text{AUTOS}}$ (GMSL SERIALIZER)	GMSL SERIALIZER POWER-UP STATE	MS (MAX9268)	MAX9268 POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Low	Normal (SLEEP = 0)	Both devices power up with serial link active (autostart).
2	High	Serialization disabled	High	Sleep mode (SLEEP = 1)	Serial link is disabled and the MAX9268 powers up in sleep mode. Set SEREN = 1 or CLINKEN = 1 in the GMSL serializer to start the serial link and wake up the MAX9268.
3	High	Serialization disabled	Low	Normal (SLEEP = 0)	Both devices power up in normal mode with the serial link disabled. Set SEREN = 1 or CLINKEN = 1 in the GMSL serializer to start the serial link.
4	Low	Serialization enabled	High	In sleep mode (SLEEP = 1)	MAX9268 starts in sleep mode. Link autostarts upon GMSL serializer power-up. Use this case when the MAX9268 powers up before the serializer.

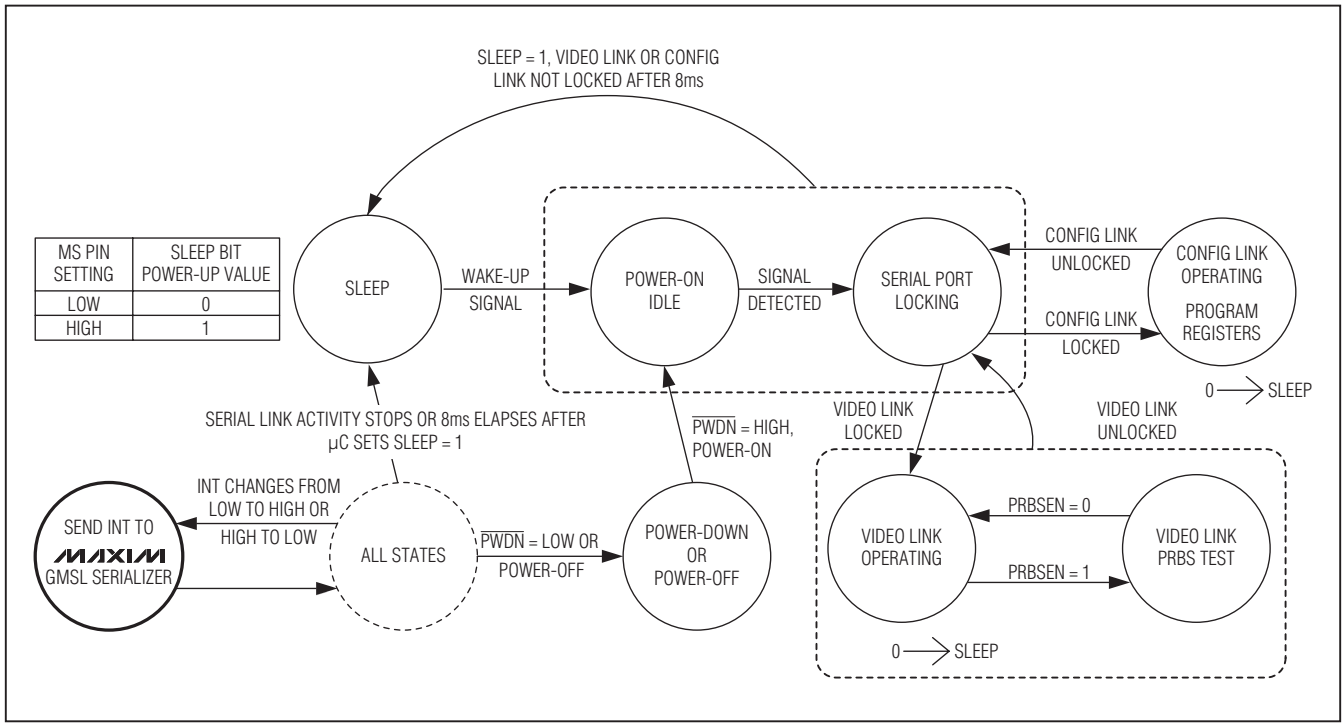

Figure 22. State Diagram, CDS = Low (LCD Application)

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Image-Sensing Applications

For image-sensing applications, connect the µC to the MAX9268 and set CDS = high for both the GMSL serializer and the MAX9268. The deserializer powers up normally (SLEEP = 0) and continuously tries to lock to a valid serial input. Table 10 summarizes both startup cases, based on the state of the GMSL serializer $\overline{AUTOS}$ pin.

Case 1: Autostart Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the GMSL serializer locks to a stable input clock and sends the high-speed data to the MAX9268. The deserializer locks to the serial data and outputs the video data and clock.

Case 2: Sleep Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the GMSL serializer starts up in sleep mode. Use the µC to wake up the serializer by sending a GMSL protocol UART frame containing at least three rising edges (e.g., 0x66), at a bit rate no greater than 1Mbps. The low-power wake-up receiver of the serializer detects the wake-up frame over the reverse control channel and powers up. Reset the sleep bit (SLEEP = 0) of the GMSL serializer using a regular control-channel write packet to power up the device fully. Send the sleep bit write packet at least 500µs after the wake-up frame. The GMSL serializer goes back to sleep mode if its sleep bit is not cleared within 5ms (min) after detecting a wake-up frame.

Applications Information

Error Checking

The MAX9268 checks the serial link for errors and stores the number of detected decoding errors in the 8-bit register DECERR (0x0D). If a large number of decoding errors are detected within a short duration, the deserializer loses lock and stops the error counter. The deserializer then attempts to relock to the serial data. DECERR resets upon successful video link lock, successful readout of DECERR (through UART), or whenever autoerror reset is enabled. The MAX9268 does not check for decoding errors during the internal PRBS test and DECERR is reset to 0x00.

Table 10. Startup Selection for Image-Sensing Applications (CDS = High)

CASE	$\overline{AUTOS}$ (GMSL SERIALIZER)	GMSL SERIALIZER POWER-UP STATE	MAX9268 POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Normal (SLEEP = 0)	Autostart
2	High	Sleep mode (SLEEP = 1)	Normal (SLEEP = 0)	GMSL serializer is in sleep mode. Wake up the serializer through the control channel (µC attached to MAX9268).

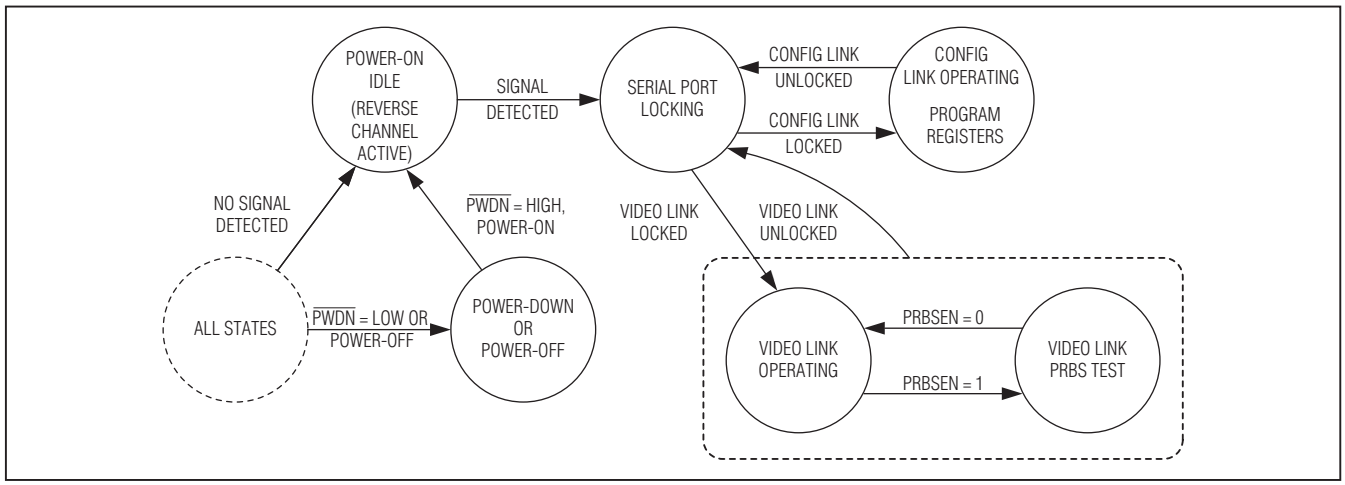

Figure 23. MAX9268 State Diagram, CDS = High (Camera Application)

$\overline{ERR}$ Output

The MAX9268 has an open-drain $\overline{ERR}$ output. This output asserts low whenever the number of decoding errors exceeds the error threshold ERRTHR (0x0C) during normal operation, or when at least one PRBS error is detected during the PRBS test. $\overline{ERR}$ reasserts high whenever DECERR (0x0D) resets due to DECERR readout, video link lock, or autoerror reset.

Autoerror Reset

The default method to reset errors is to read the respective error registers in the MAX9268 (0x0D, 0x0E). Autoerror reset clears the decoding error counter DECERR and the $\overline{ERR}$ output ~1µs after $\overline{ERR}$ goes low. Autoerror reset is disabled on power-up. Enable autoerror reset through AUTORST (0x06 D6). Autoerror reset does not run when the device is in PRBS test mode.

Self-PRBS Test

The GMSL serializer/MAX9268 link includes a PRBS pattern generator and bit-error verification function. Set PRBSEN = 1 (0x04 D5) first in the GMSL serializer and then the MAX9268 to start the PRBS test. Set PRBSEN = 0 (0x04 D5) first in the MAX9268 and then the GMSL serializer to exit the PRBS self-test. The MAX9268 uses an 8-bit register (0x0E) to count the number of detected errors. The control link also controls the start and stop of the error counting. During PRBS mode, the device does not count decoding errors and the MAX9268 $\overline{ERR}$ output reflects PRBS errors only.

Microcontrollers on Both Sides of the GMSL Link (Dual µC Control)

Usually a single µC is used for GMSL device programming and control-channel communications and is located either on the serializer side for video-display applications or on the deserializer (MAX9268) side for image-sensing applications. In the former case, the CDS pins of the serializer/deserializer are set to low; in the latter case, they are set to high. However, if the CDS pin of the serializer is low and the same pin on the deserializer is high, then µCs connected at each device are enabled as masters simultaneously. In such a case, the µC on either side communicates with the GMSL serializer and the MAX9268.

Contention can occur if the µCs attempt to use the control channel at the same time. The serializer/deserializer do not in themselves provide a way to avoid contention. The fact that an acknowledge is not received when contention occurs can be used to trigger a retry. Alternatively, a higher layer protocol can be implemented to avoid contention. In addition, if UART communication across the serial link is not required, the µCs can disable the forward and reverse control channel through the REVCCEN and FWDCCEN bits (0x04 D[1:0]) in the GMSL serializer/MAX9268. UART communication across the serial link is prevented and therefore contention between µCs can no longer occur. During dual µC operation, if one of the CDS pins on either side changes state, the link resumes the corresponding state described in the *Link Startup Procedure* section.

As an example of dual µC use in an image-sensing application, the GMSL serializer can be in sleep mode and waiting for wake-up by the MAX9268. After wake-up, the serializer-side µC sets the GMSL serializer's CDS pin low and assumes master control of the serializer's registers.

Changing the Clock Frequency

Both the video clock rate ($f_{TXCLKOUT_}$) and the control-channel clock rate (f_{UART}) can be changed on-the-fly to support applications with multiple clock speeds. It is recommended to enable the serial link after the video clock stabilizes. Stop the video clock for 5µs and restart the serial link, or toggle SEREN after each change in the video clock frequency, to recalibrate any automatic settings if a smooth frequency change cannot be guaranteed. The reverse control channel remains unavailable for 350µs after serial link start or stop. Limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps and then at 100kbps to have reduction ratios of 3 and 3.333, respectively.

LOCK Output Loopback

For quick loss-of-lock notification, the MAX9268 can loop back its LOCK output to the GMSL serializer using the INT signal. Connect the LOCK output to the INT input of the MAX9268. The interrupt output on the GMSL serializer follows the transitions at the LOCK output. Reverse control-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the video link. LOCK asserts for video link only and not for the configuration link.

GPIOs

The MAX9268 has two open-drain GPIOs available. GPIO1OUT and GPIO0OUT (0x06 D3, D1) set the output state of the GPIOs. The GPIO input buffers are always enabled. The input states are stored in GPIO1 and GPIO0 (0x06 D2, D0). SET GPIO1OUT/GPIO0OUT to 1 when using GPIO1/GPIO0 as an input.

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Programming the Device Addresses

Both the GMSL serializer and the MAX9268 have programmable device addresses. This allows multiple GMSL devices along with I²C peripherals to coexist on the same control channel. The serializer device address is stored in registers 0x00 of each device, while the deserializer device address is stored in register 0x01 of each device. To change the device address, first write to the device whose address changes (register 0x00 of the GMSL serializer for serializer device address change, or register 0x01 of the MAX9268 for deserializer device address change). Then write the same address into the corresponding register on the other device (register 0x00 of the MAX9268 for serializer device address change, or register 0x01 of the GMSL serializer for deserializer device address change).

3-Level Inputs for Default Device Address

ADD0 and ADD1 are 3-level inputs, which set the device addresses stored in the MAX9268 (Table 2). Set the desired device addresses by connecting ADD0/ADD1 through a pullup resistor to IOVDD, a pulldown resistor to GND, or to high impedance. For digital control, use three-state logic to drive the 3-level logic inputs.

ADD0/ADD1 set the device addresses in the MAX9268 only and not the GMSL serializer. Set the GMSL serializer's ADD0/ADD1 inputs to the same settings as the MAX9268; alternatively, write to registers 0x00 and 0x01 of the GMSL serializer to reflect any changes made due to the 3-level inputs.

Choosing I²C/UART Pullup Resistors

Both I²C/UART open-drain lines require pullup resistors to provide a logic-high level. There are trade-offs between power dissipation and speed, and a compromise made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *AC Electrical Characteristics* section for details). To meet the fast-mode rise-time requirement, choose the pullup resistors such that rise time $t_R = 0.85 \times R_{PULLUP} \times C_{BUS} < 300ns$. The waveforms are not recognized if the transition time becomes too slow. The MAX9268 supports I²C/UART rates up to 1Mbps.

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Four capacitors (two at the serializer output and two at the deserializer input) are needed for proper link operation and to provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML receiver termination resistor (R_{TR}), the CML driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is $(C \times (R_{TD} + R_{TR}))/4$. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω). This leaves the capacitor selection to change the system time constant. Use at least 0.2µF high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The MAX9268 uses a 3.0V to 3.6V V_{AVDD} and V_{DVDD}. All single-ended inputs and outputs on the MAX9268 derive power from a 1.7V to 3.6V V_{IOVDD}, which scales with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize any impedance discontinuities. Twisted-pair and shielded twisted-pair cables tend to generate less EMI due to magnetic-field canceling effects. Balanced cables pick up noise as common mode rejected by the CML receiver. Table 11 lists the suggested cables and connectors used in the GMSL link.

Board Layout

Separate the digital signals and CML/LVDS high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/LVDS, and digital signals. Layout PCB traces close to each other for a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together because the impedance goes down when the traces are brought closer.

Route the PCB traces for a CML/LVDS channel (there are two conductors per CML/LVDS channel) in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

ESD Protection

The MAX9268 ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. CML/LVDS I/O are tested for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 24). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 25). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 26).

Table 11. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE
JAE Electronics, Inc.	MX38-FF	A-BW-Lxxxxx
Nissei Electric Co., Ltd.	GT11L-2S	F-2WME AWG28
Rosenberger Hochfrequenztechnik GmbH	D4S10A-40ML5-Z	Dacar 538

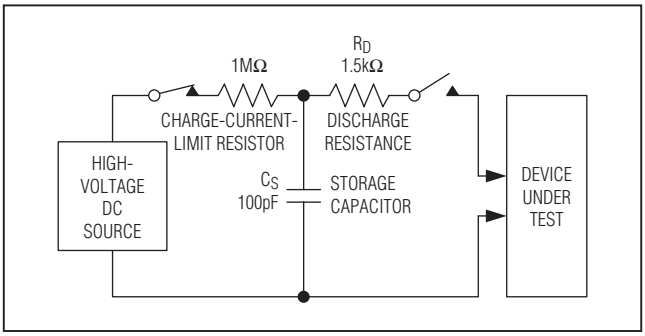


Figure 24. Human Body Model ESD Test Circuit

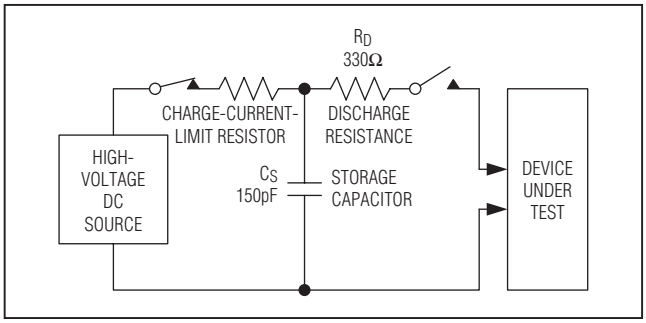


Figure 25. IEC 61000-4-2 Contact Discharge ESD Test Circuit

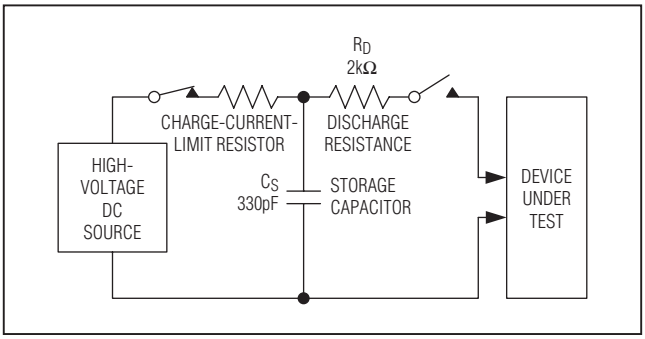


Figure 26. ISO 10605 Contact Discharge ESD Test Circuit

Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

Table 12. Register Table (see Table 1)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address. Power-up default address determined by ADD0 and ADD1 (see Table 2).	XX00XX0
	D0	—	0	Reserved	0
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address. Power-up default address determined by ADD0 and ADD1 (see Table 2).	XX01XX0
	D0	—	0	Reserved	0
0x02	D[7:6]	SS	**00**	No spread spectrum. **Power-up default when SSEN = low.**	00, 01
			01	±2% spread spectrum. **Power-up default when SSEN = high.**	
			10	No spread spectrum	
			11	±4% spread spectrum	
	D5	—	0	Reserved	0
	D4	AUDIOEN	0	Disable I²S channel	1
			1	Enable I²S channel	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock	11
			01	25MHz to 50MHz pixel clock	
			10	50MHz to 104MHz pixel clock	
			11	Automatically detect the pixel clock range	
	D[1:0]	SRNG	00	0.5Gbps to 1Gbps serial-data rate	11
			01	1Gbps to 2Gbps serial-data rate	
			10	2Gbps to 3.125Gbps serial-data rate	
			11	Automatically detect serial-data rate	
0x03	D[7:6]	AUTOFM	00	Calibrate spread-modulation rate only once after locking	00
			01	Calibrate spread-modulation rate every 2ms after locking	
			10	Calibrate spread-modulation rate every 16ms after locking	
			11	Calibrate spread-modulation rate every 256ms after locking	
	D5	—	0	Reserved	0
	D[4:0]	SDIV	00000	Autocalibrate sawtooth divider	00000
			XXXXX	Manual SDIV setting. See the *Manual Programming of Spread-Spectrum Divider* section.	

Table 12. Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x04	D7	LOCKED	0	LOCK output is low	0 (read only)
			1	LOCK output is high	
	D6	OUTENB	0	Enable outputs	0
			1	Disable outputs	
	D5	PRBSEN	0	Disable PRBS test	0
			1	Enable PRBS test	
	D4	SLEEP	0	Normal mode. Default value depends on CDS and MS pin values at power-up).	0, 1
			1	Activate sleep mode. Default value depends on CDS and MS pin values at power-up).	
	D[3:2]	INTTYPE	00	Base mode uses I²C peripheral interface	00
			01	Base mode uses UART peripheral interface	
			10, 11	Base mode peripheral interface disabled	
	D1	REVCCEN	0	Disable reverse control channel to serializer (sending)	1
			1	Enable reverse control channel to serializer (sending)	
	D0	FWDCCEN	0	Disable forward control channel from serializer (receiving)	1
			1	Enable forward control channel from serializer (receiving)	
0x05	D7	I2CMETHOD	0	I²C conversion sends the register address	0
			1	Disable sending of I²C register address (command-byte-only mode)	
	D[6:5]	HPFTUNE	00	7.5MHz equalizer highpass cutoff frequency	01
			01	3.75MHz cutoff frequency	
			10	2.5MHz cutoff frequency	
			11	1.87MHz cutoff frequency	
	D4	PDHF	0	High-frequency boosting enabled	0
			1	High-frequency boosting disabled	
	D[3:0]	EQTUNE	0000	2.1dB equalizer boost gain	0100, 1001
			0001	2.8dB equalizer boost gain	
			0010	3.4dB equalizer boost gain	
			0011	4.2dB equalizer boost gain	
			0100	5.2dB equalizer boost gain. **Power-up default when EQS = high.**	
			0101	6.2dB equalizer boost gain	
			0110	7dB equalizer boost gain	
			0111	8.2dB equalizer boost gain	
			1000	9.4dB equalizer boost gain	
			1001	10.7dB equalizer boost gain. **Power-up default when EQS = low.**	
			1010	11.7dB equalizer boost gain	
			1011	13dB equalizer boost gain	
			11XX	Do not use	

Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

Table 12. Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x06	D7	—	0	Reserved	0
	D6	AUTORST	0	Do not automatically reset error registers and outputs	0
			1	Automatically reset error registers and outputs	
	D5	DISINT	0	Enable interrupt transmission to serializer	0
			1	Disable Interrupt transmission to serializer	
	D4	INT	0	INT input = low (read only)	0 (read only)
			1	INT input = high (read only)	
	D3	GPIO1OUT	0	Output low to GPIO1	1
			1	Output high to GPIO1	
	D2	GPIO1	0	GPIO1 is low	1 (read only)
			1	GPIO1 is high	
	D1	GPIO0OUT	0	Output low to GPIO0	1
			1	Output high to GPIO0	
	D0	GPIO0	0	GPIO0 is low	1 (read only)
			1	GPIO0 is high	
0x07	D[7:0]	—	01010100	Reserved	01010100
0x08	D[7:0]	—	00110000	Reserved	00110000
0x09	D[7:0]	—	11001000	Reserved	11001000
0x0A	D[7:0]	—	00010010	Reserved	00010010
0x0B	D[7:0]	—	00100000	Reserved	00100000
0x0C	D[7:0]	ERRTHR	XXXXXXXX	Error threshold for decoding errors. $\overline{ERR}$ = low when DECERR > ERRTHR.	00000000
0x0D	D[7:0]	DECERR	XXXXXXXX	Decoding error counter. This counter remains zero while the device is in PRBS test mode.	00000000 (read only)
0x0E	D[7:0]	PRBSERR	XXXXXXXX	PRBS error counter	00000000 (read only)
0x12	D7	MCLKSRC	0	MCLK derived from PCLK (see Table 5)	0
			1	MCLK derived from internal oscillator	
	D[6:0]	MCLKDIV	0000000	MCLK disabled	0000000
			XXXXXXX	MCLK divider	
0x13	D[7:5]	—	XXX	Reserved	(read only)
	D[4:0]	—	10000	Reserved	10000

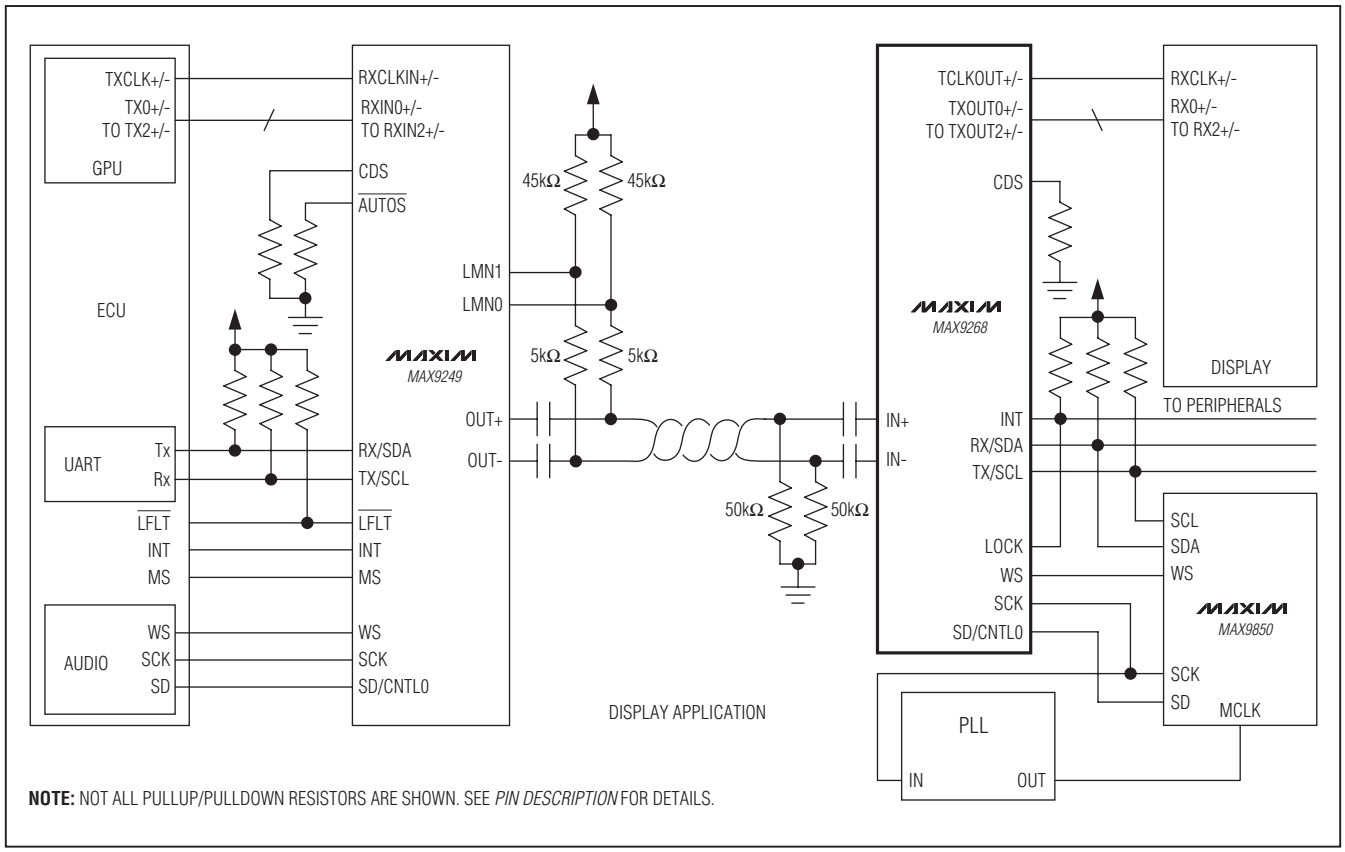
Table 12. Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x14	D[7:6]	—	00	Reserved	00
	D5	FORCELVDS	0	Normal operation	0
			1	Force LVDS outputs low	
	D4	DCS	0	Normal driver current for CMOS outputs (WS, SCK, SD/ CNTL0, CNTL1, CNTL2/MCLK)	0
			1	Strong driver current for CMOS outputs (WS, SCK, SD/ CNTL0, CNTL1, CNTL2/MCLK)	
	D3	DISCNTL1	0	Serial-data bit 27 is mapped to CNTL1	0
			1	CNTL1 forced low	
	D2	DISRES	0	Serial-data bit 27 is mapped to RES	0
			1	RES bit forced low	
	D[1:0]	ILVDS	00	1.75mA LVDS current	01
			01	3.5mA LVDS current	
			10	Do not use	
			11	7mA LVDS current	
0x1E	D[7:0]	ID	00000100	Device identifier (MAX9268 = 0x04)	00000100 (read only)
0x1F	D[7:5]	—	000	Reserved	000 (read only)
	D4	CAPS	0	Not HDCP capable	0 (read only)
			1	HDCP capable	
	D[3:0]	REVISION	XXXX	Device revision	(read only)

X = Don't care.

Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

Typical Application Circuit



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE *PIN DESCRIPTION* FOR DETAILS.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFP-EP	C48E+8	21-0065	90-0138

Gigabit Multimedia Serial Link Deserializer with LVDS System Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/10	Initial release	—
1	5/10	Changed conditions for LVDS output enable/disable times and SCK jitter limits in the AC *Electrical Characteristics* table	5
2	1/11	Added Patent Pending to *Features*	1

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