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FDMC612PZ

P-Channel PowerTrench® MOSFET -20 V, -14 A, 8.4 mΩ

Features

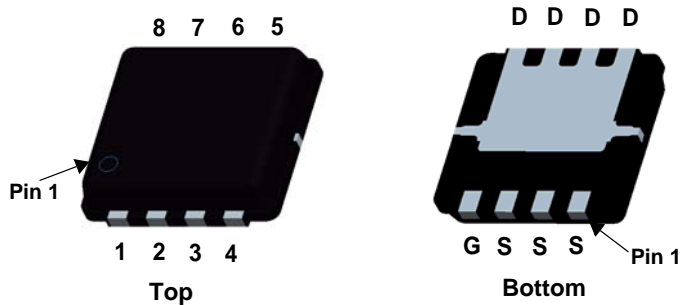
- Max $r_{DS(on)}$ = 8.4 mΩ at $V_{GS} = -4.5$ V, $I_D = -14$ A
- Max $r_{DS(on)}$ = 13 mΩ at $V_{GS} = -2.5$ V, $I_D = -11$ A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Termination is Lead-free and RoHS Compliant
- HBM ESD capability level > 3.6 KV typical (Note 4)

General Description

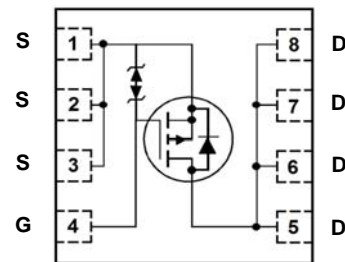
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been optimized for $r_{DS(ON)}$, switching performance and ruggedness.

Applications

- Battery Management
- Load Switch



MLP 3.3x3.3



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units	
V_{DS}	Drain to Source Voltage	-20	V	
V_{GS}	Gate to Source Voltage	±12	V	
I_D	Drain Current -Continuous	$T_C = 25$ °C	A	
	-Continuous	$T_A = 25$ °C (Note 1a)		
	-Pulsed			
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	38	mJ
P_D	Power Dissipation	$T_C = 25$ °C	26	W
	Power Dissipation	$T_A = 25$ °C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC612PZ	FDMC612PZ	MLP 3.3X3.3	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-19		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\text{ }\mu\text{A}$	-0.6	-0.9	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{ V}$, $I_D = -14\text{ A}$		5.9	8.4	m Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -11\text{ A}$		8.2	13	
		$V_{GS} = -4.5\text{ V}$, $I_D = -14\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		8.3	13	
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}$, $I_D = -14\text{ A}$		85		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		5710	7995	pF
C_{oss}	Output Capacitance			1215	1700	pF
C_{rss}	Reverse Transfer Capacitance			1170	1640	pF

Switching Characteristics

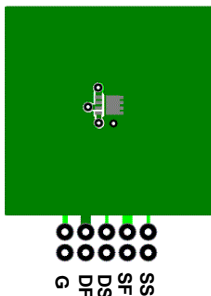
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}$, $I_D = -14\text{ A}$, $V_{GS} = -4.5\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		26	42	ns
t_r	Rise Time			52	83	ns
$t_{d(off)}$	Turn-Off Delay Time			96	154	ns
t_f	Fall Time			81	130	ns
Q_g	Total Gate Charge			53	74	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = -10\text{ V}$, $I_D = -14\text{ A}$, $V_{GS} = -4.5\text{ V}$		9.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			18		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -14\text{ A}$ (Note 2)		-0.8	-1.3	V
		$V_{GS} = 0\text{ V}$, $I_S = -2\text{ A}$ (Note 2)		-0.7	-1.2	
t_{rr}	Reverse Recovery Time	$I_F = -14\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		39	62	ns
Q_{rr}	Reverse Recovery Charge			17	31	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 53 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. 125 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2: Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.

3: E_{AS} of 38 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = -16\text{ A}$, $V_{DD} = -18\text{ V}$, $V_{GS} = -10\text{ V}$.

4: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

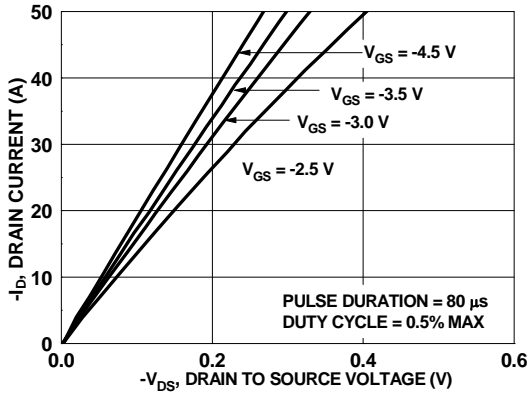


Figure 1. On-Region Characteristics

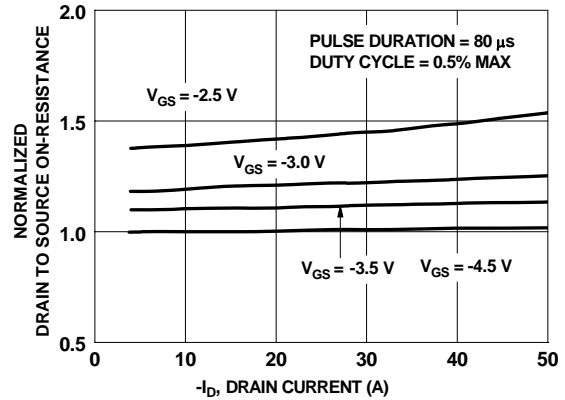


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

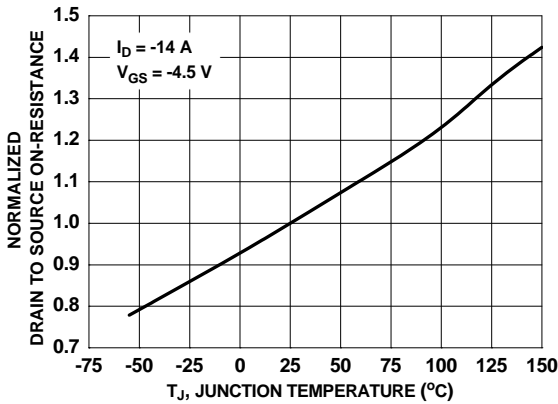


Figure 3. Normalized On-Resistance vs Junction Temperature

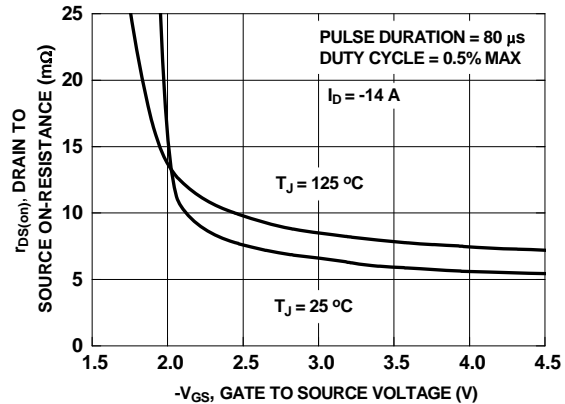


Figure 4. On-Resistance vs Gate to Source Voltage

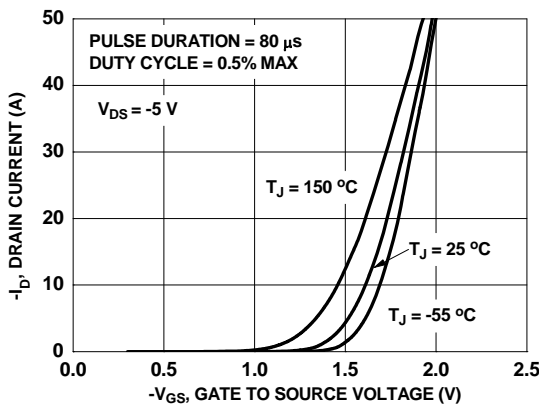


Figure 5. Transfer Characteristics

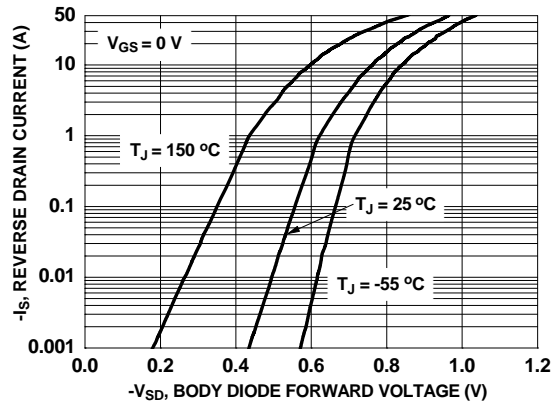


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

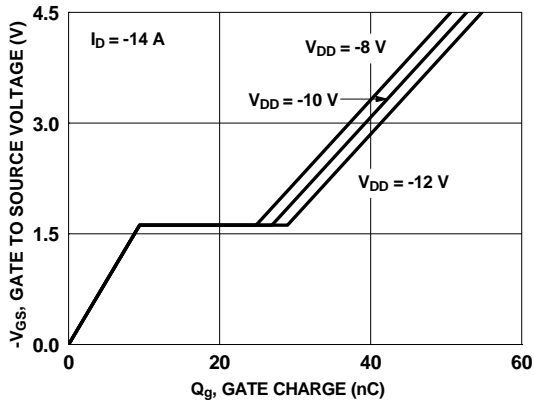


Figure 7. Gate Charge Characteristics

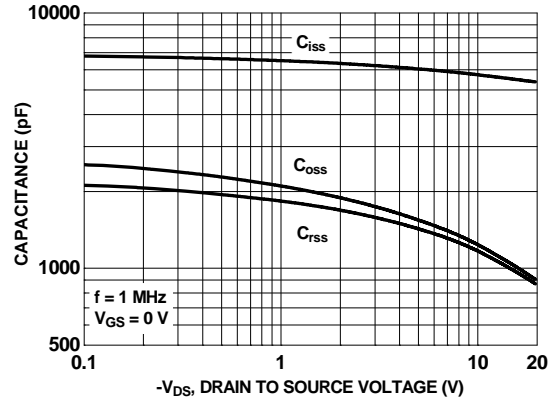


Figure 8. Capacitance vs Drain to Source Voltage

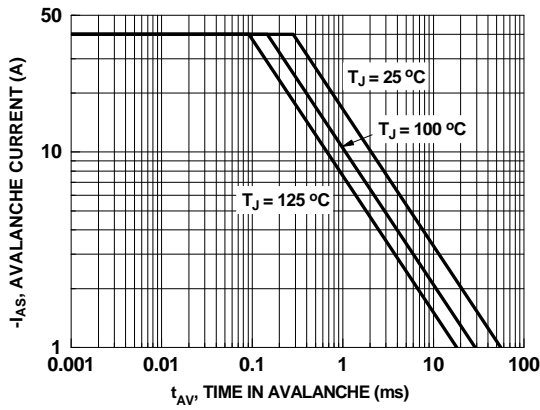


Figure 9. Unclamped Inductive Switching Capability

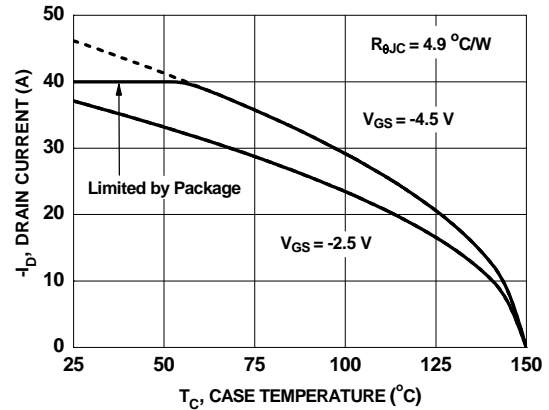


Figure 10. Maximum Continuous Drain Current vs Case Temperature

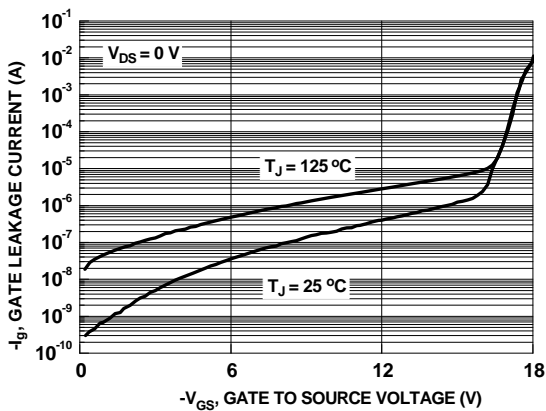


Figure 11. Gate Leakage Current vs Gate to Source Voltage

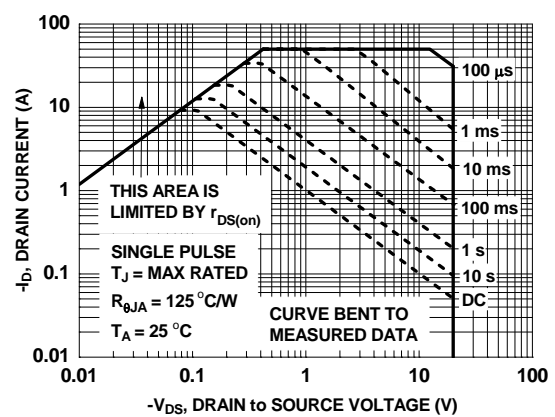


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

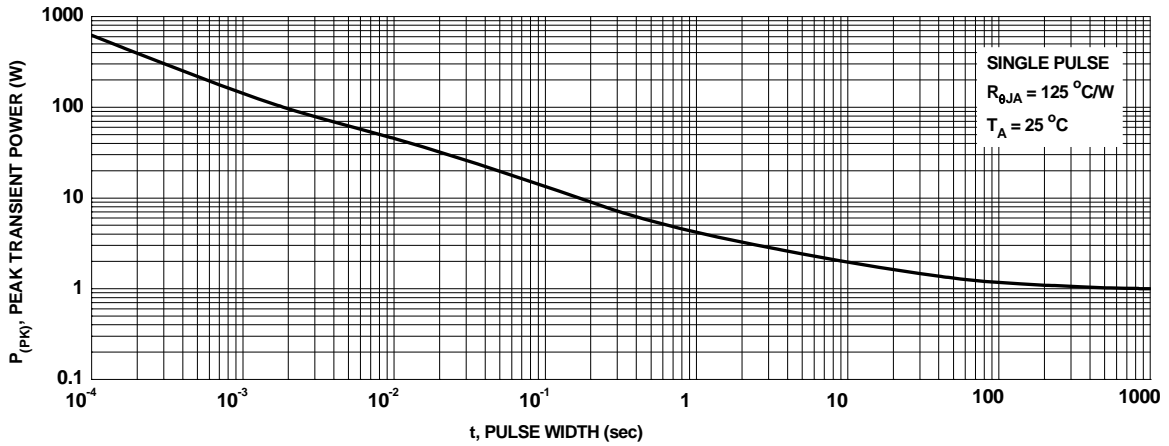


Figure 13. Single Pulse Maximum Power Dissipation

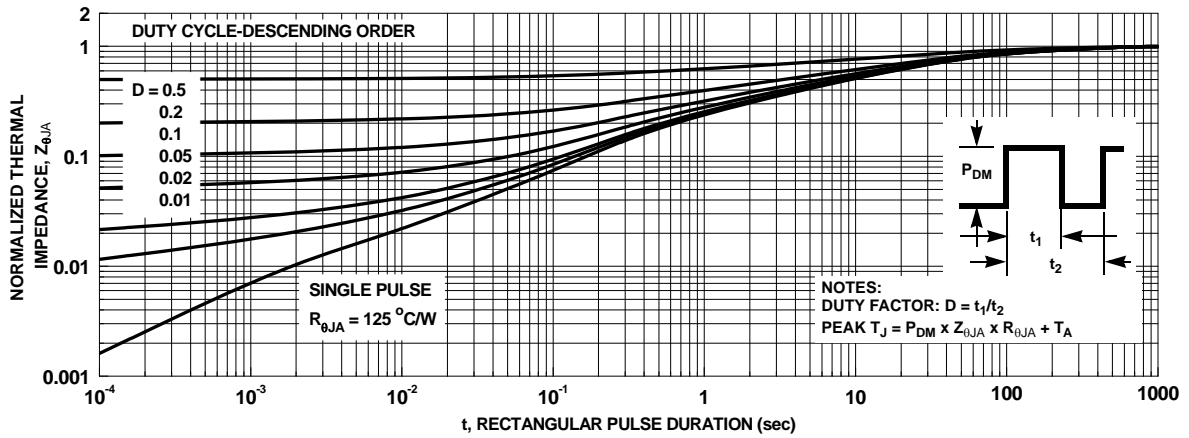
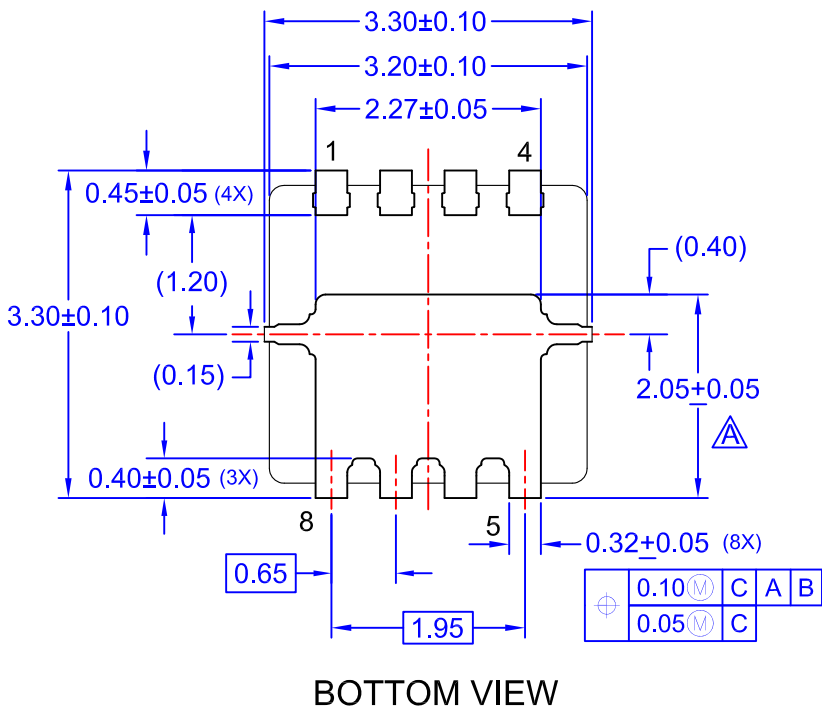
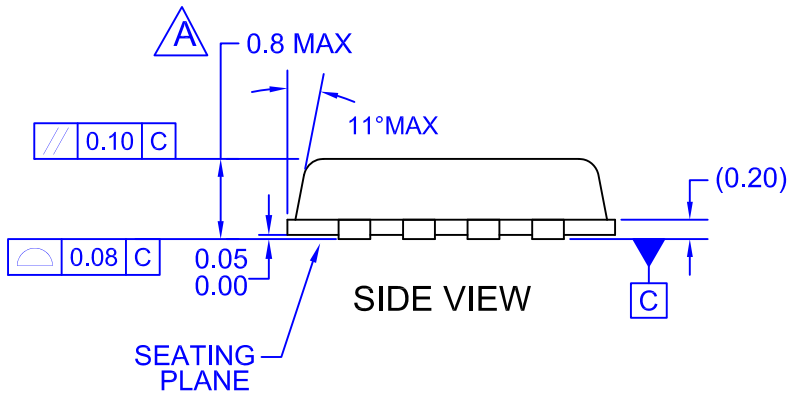
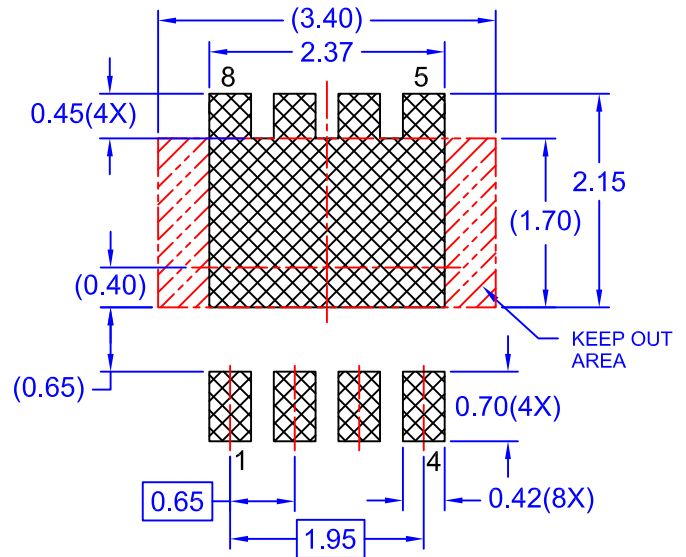
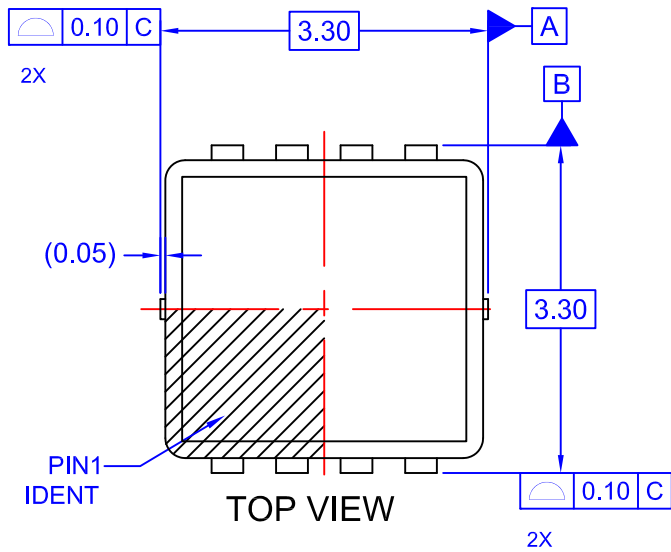


Figure 14. Junction-to-Ambient Transient Thermal Response Curve



NOTES:

- A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.
- F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
- G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.
- H. DRAWING FILENAME: MKT-MLP08Trev4.
- I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.



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