



**THE DATASHEET OF
74LVC2G126GN,115**



74LVC2G126

Dual bus buffer/line driver; 3-state

Rev. 14 — 10 January 2019

Product data sheet

1. General description

The 74LVC2G126 is a dual non-inverting buffer/line driver with 3-state outputs. Each 3-state output is controlled by an output enable input (pin nOE). A LOW-level at pin nOE causes the output to assume a high-impedance OFF-state. Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC2G126 as a translator in a mixed 3.3 V and 5 V environment.

It is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|--------------|-------------------|--------|---|----------|
| | Temperature range | Name | Description | |
| 74LVC2G126DP | -40 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm | SOT505-2 |
| 74LVC2G126DC | -40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |
| 74LVC2G126GT | -40 °C to +125 °C | XSON8 | plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm | SOT833-1 |
| 74LVC2G126GF | -40 °C to +125 °C | XSON8 | extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm | SOT1089 |
| 74LVC2G126GM | -40 °C to +125 °C | XQFN8 | plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm | SOT902-2 |
| 74LVC2G126GN | -40 °C to +125 °C | XSON8 | extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm | SOT1116 |
| 74LVC2G126GS | -40 °C to +125 °C | XSON8 | extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm | SOT1203 |

4. Marking

Table 2. Marking codes

| Type number | Marking code [1] |
|--------------|------------------|
| 74LVC2G126DP | V26 |
| 74LVC2G126DC | V26 |
| 74LVC2G126GT | V26 |
| 74LVC2G126GF | VN |
| 74LVC2G126GM | V26 |
| 74LVC2G126GN | VN |
| 74LVC2G126GS | VN |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

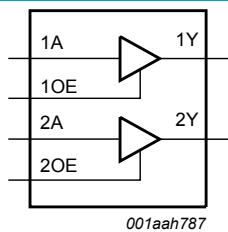


Fig. 1. Logic symbol

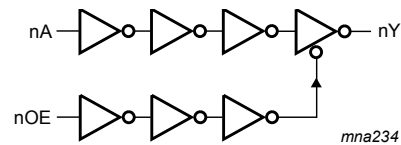
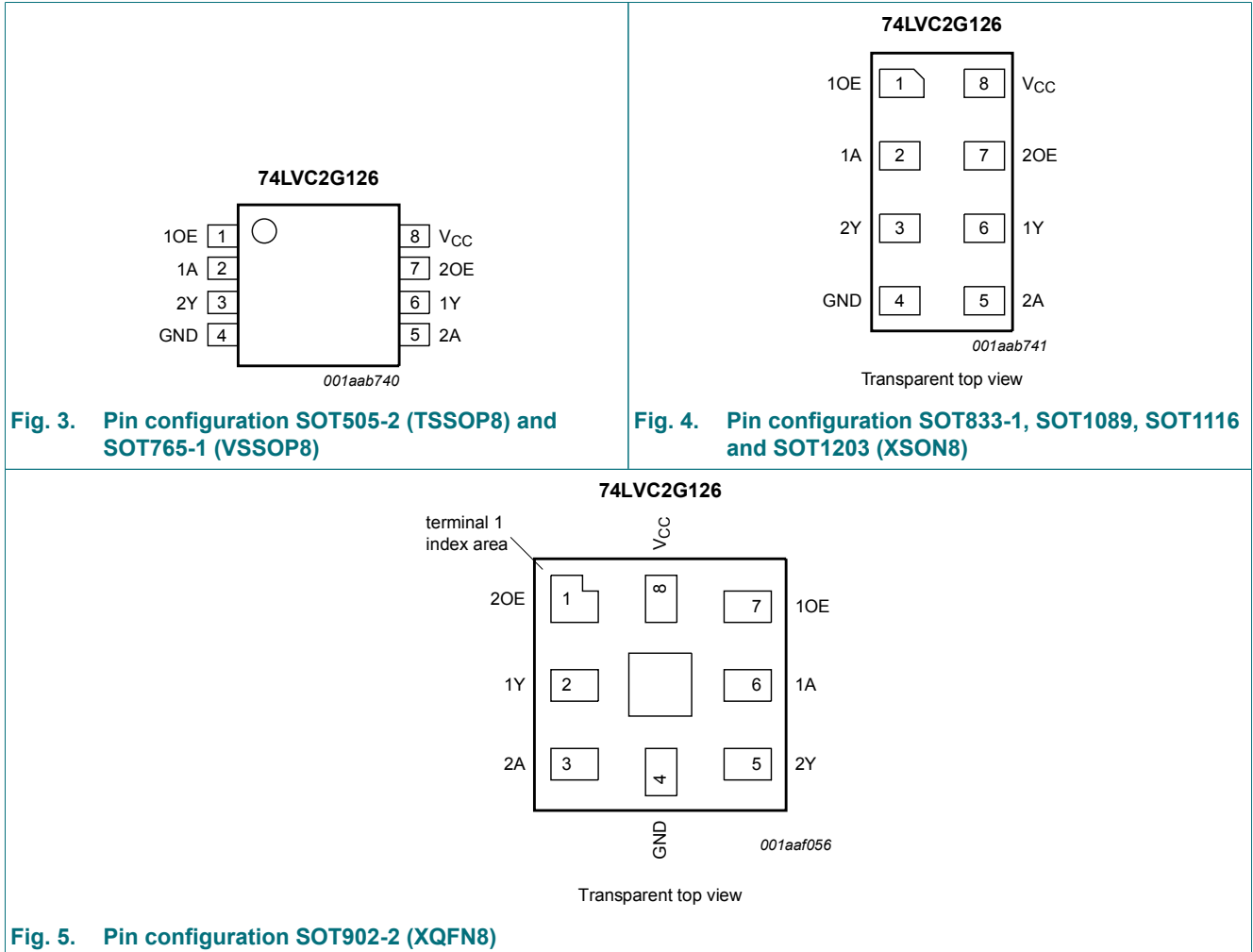


Fig. 2. Logic diagram (one gate)

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

| Symbol | Pin | | Description |
|-----------------|--|----------|-----------------------------------|
| | SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT1116 and SOT1203 | SOT902-2 | |
| 1OE, 2OE | 1, 7 | 7, 1 | output enable input (active HIGH) |
| 1A, 2A | 2, 5 | 6, 3 | data input |
| 1Y, 2Y | 6, 3 | 2, 5 | data output |
| GND | 4 | 4 | ground (0 V) |
| V _{CC} | 8 | 8 | supply voltage |

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

| Input | | Output |
|-------|----|--------|
| nOE | nA | nY |
| H | L | L |
| H | H | H |
| L | X | Z |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---------------------------------|----------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| V_I | input voltage | | [1] -0.5 | +6.5 | V |
| I_{OK} | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ±50 | mA |
| V_O | output voltage | Active mode | [1] -0.5 | $V_{CC} + 0.5$ | V |
| | | Power-down mode; $V_{CC} = 0$ V | [1] -0.5 | +6.5 | V |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ±50 | mA |
| I_{CC} | supply current | | - | +100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to $+125$ °C | [2] - | 300 | mW |
| T_{stg} | storage temperature | | -65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly at 2.5 mW/K.
 For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly at 8.0 mW/K.
 For XSON8 and XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|-------------------------------------|---------------------------------|------|----------|------|
| V_{CC} | supply voltage | | 1.65 | 5.5 | V |
| V_I | input voltage | | 0 | 5.5 | V |
| V_O | output voltage | Active mode | 0 | V_{CC} | V |
| | | $V_{CC} = 0$ V; Power-down mode | 0 | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 5.5 V | - | 10 | ns/V |

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------------------------------------|---------|---------------------|--------------------------------------|---------------------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65V _{CC} | - | - | 0.65V _{CC} | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7V _{CC} | - | - | 0.7V _{CC} | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35V _{CC} | - | 0.35V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 0.3V _{CC} | - | 0.3V _{CC} | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V | - | - | 0.1 | - | 0.1 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.45 | - | 0.70 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.3 | - | 0.45 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.4 | - | 0.60 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | - | 0.55 | - | 0.80 | V |
| | | I _O = 32 mA; V _{CC} = 4.5 V | - | - | 0.55 | - | 0.80 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = -100 µA; V _{CC} = 1.65 V to 5.5 V | V _{CC} - 0.1 | - | - | V _{CC} - 0.1 | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | 1.2 | - | - | 0.95 | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | 1.9 | - | - | 1.7 | - | V |
| | | I _O = -12 mA; V _{CC} = 2.7 V | 2.2 | - | - | 1.9 | - | V |
| | | I _O = -24 mA; V _{CC} = 3.0 V | 2.3 | - | - | 2.0 | - | V |
| | | I _O = -32 mA; V _{CC} = 4.5 V | 3.8 | - | - | 3.4 | - | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | ±0.1 | ±1 | - | ±1 | µA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V | - | ±0.1 | ±2 | - | ±2 | µA |
| I _{OFF} | power-off leakage current | V _I or V _O = 5.5 V; V _{CC} = 0 V | - | ±0.1 | ±2 | - | ±2 | µA |
| I _{CC} | supply current | V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A | - | 0.1 | 4 | - | 4 | µA |
| ΔI _{CC} | additional supply current | per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V | - | 5 | 500 | - | 500 | µA |
| C _I | input capacitance | | - | 2 | - | - | - | pF |

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|-------------------------------------|---------|------|--------------------------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t _{pd} | propagation delay | nA to nY; see Fig. 6 [2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 3.9 | 9.8 | 1.0 | 12.3 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 2.6 | 4.9 | 0.5 | 6.3 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 2.8 | 4.7 | 1.0 | 5.9 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 0.5 | 2.4 | 4.3 | 0.5 | 5.4 | ns |
| t _{en} | enable time | nOE to nY; see Fig. 7 [3] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 4.1 | 10.0 | 1.0 | 12.5 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.6 | 5.0 | 1.0 | 6.3 | ns |
| | | V _{CC} = 2.7 V | 1.0 | 2.8 | 4.7 | 1.0 | 5.9 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.4 | 4.1 | 1.0 | 5.1 | ns |
| t _{dis} | disable time | nOE to nY; see Fig. 7 [4] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 3.3 | 12.6 | 1.0 | 15.4 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 1.9 | 5.7 | 0.5 | 7.5 | ns |
| | | V _{CC} = 2.7 V | 1.5 | 3.0 | 4.8 | 1.5 | 6.2 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.5 | 4.4 | 1.0 | 5.7 | ns |
| C _{PD} | power dissipation capacitance | per buffer; V _I = GND to V _{CC} [5] | | | | | | |
| | | output enabled | - | 17 | - | - | - | pF |
| | | output disabled | - | 5 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] t_{en} is the same as t_{PZH} and t_{PZL}

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

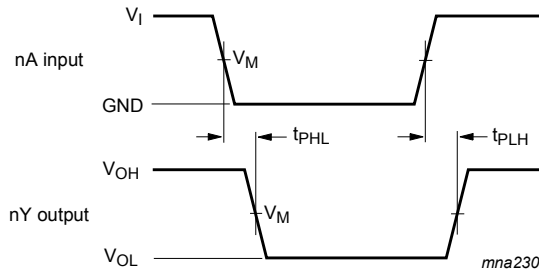
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

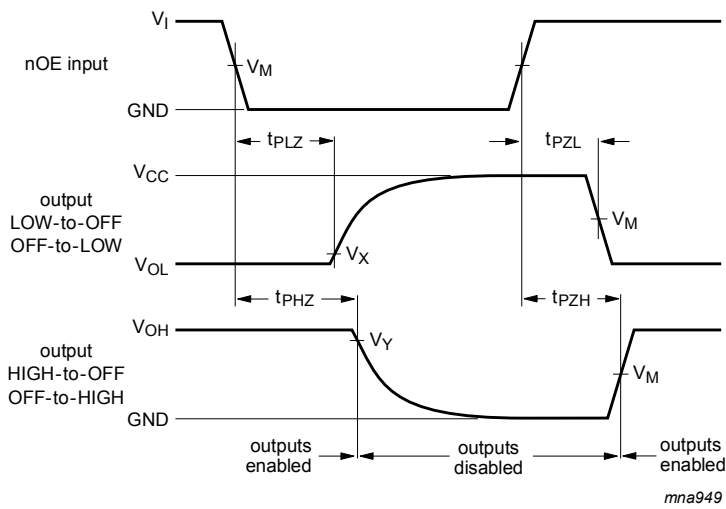
11.1. Waveforms and test circuit



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The data input (nA) to output (nY) propagation delays



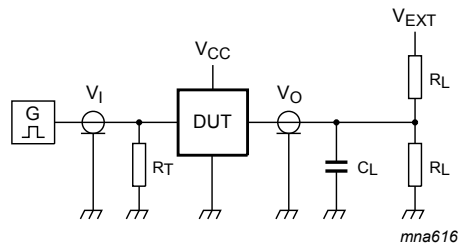
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. 3-state enable and disable times

Table 9. Measurement points

| Supply voltage | Input | Output | | |
|------------------|---------------------|---------------------|---------------------------|---------------------------|
| V_{CC} | V_M | V_M | V_X | V_Y |
| 1.65 V to 1.95 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |
| 2.7 V | 1.5 V | 1.5 V | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |
| 4.5 V to 5.5 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 8. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|------------------|----------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_{CC} | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2.0 ns | 30 pF | 1 k Ω | open | GND | $2 \times V_{CC}$ |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2.0 ns | 30 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 6 V |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 6 V |
| 4.5 V to 5.5 V | V_{CC} | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

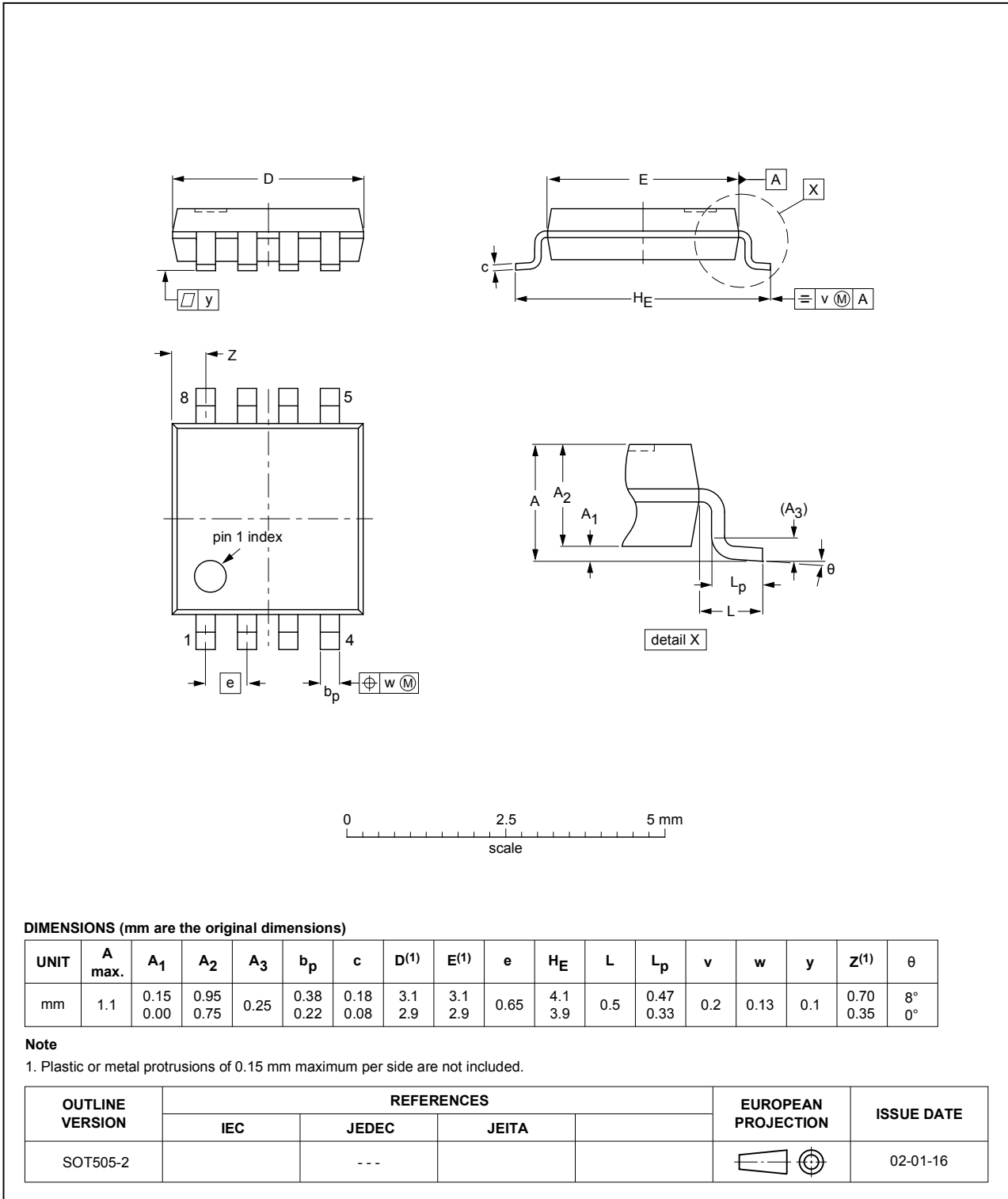


Fig. 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

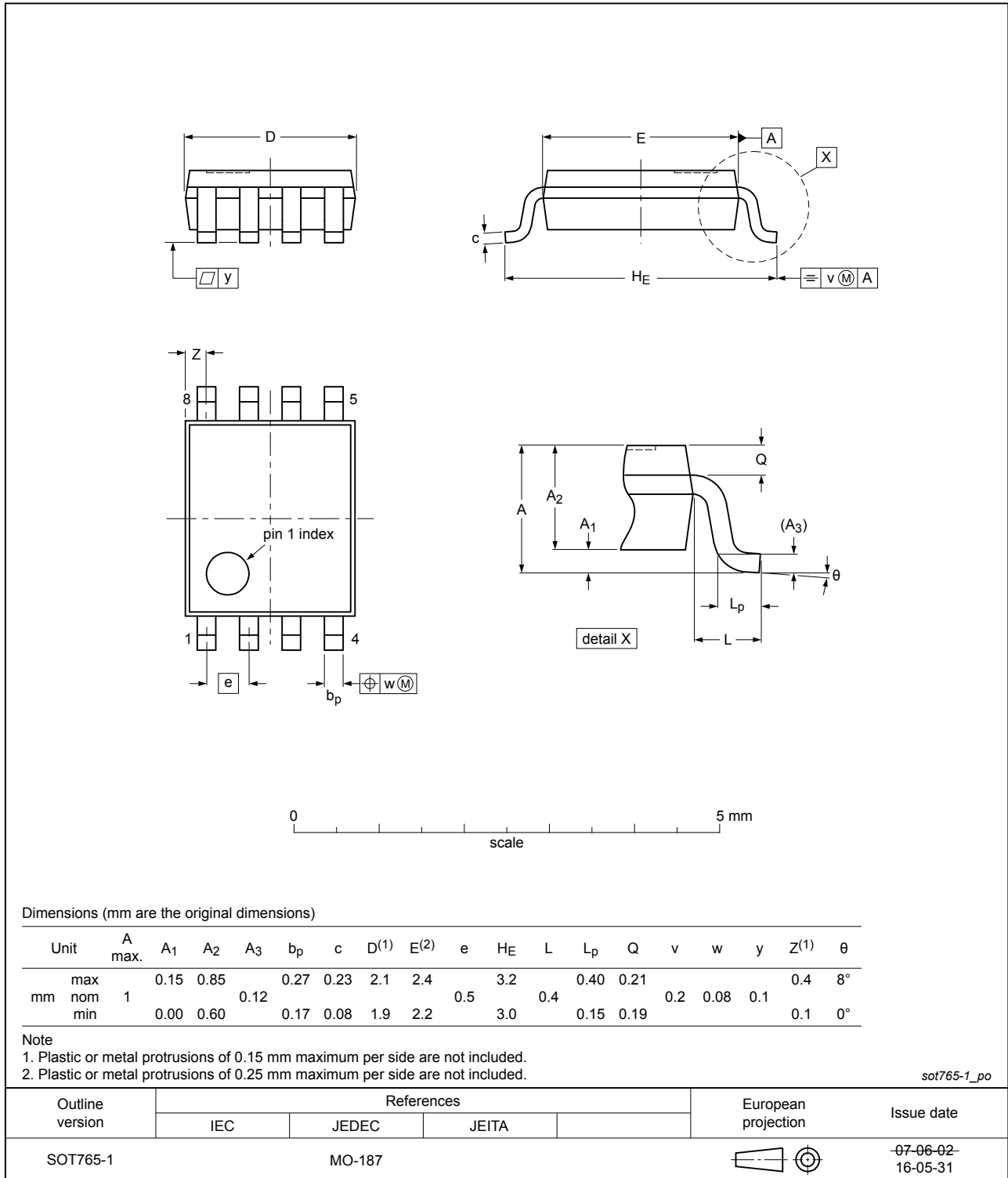


Fig. 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

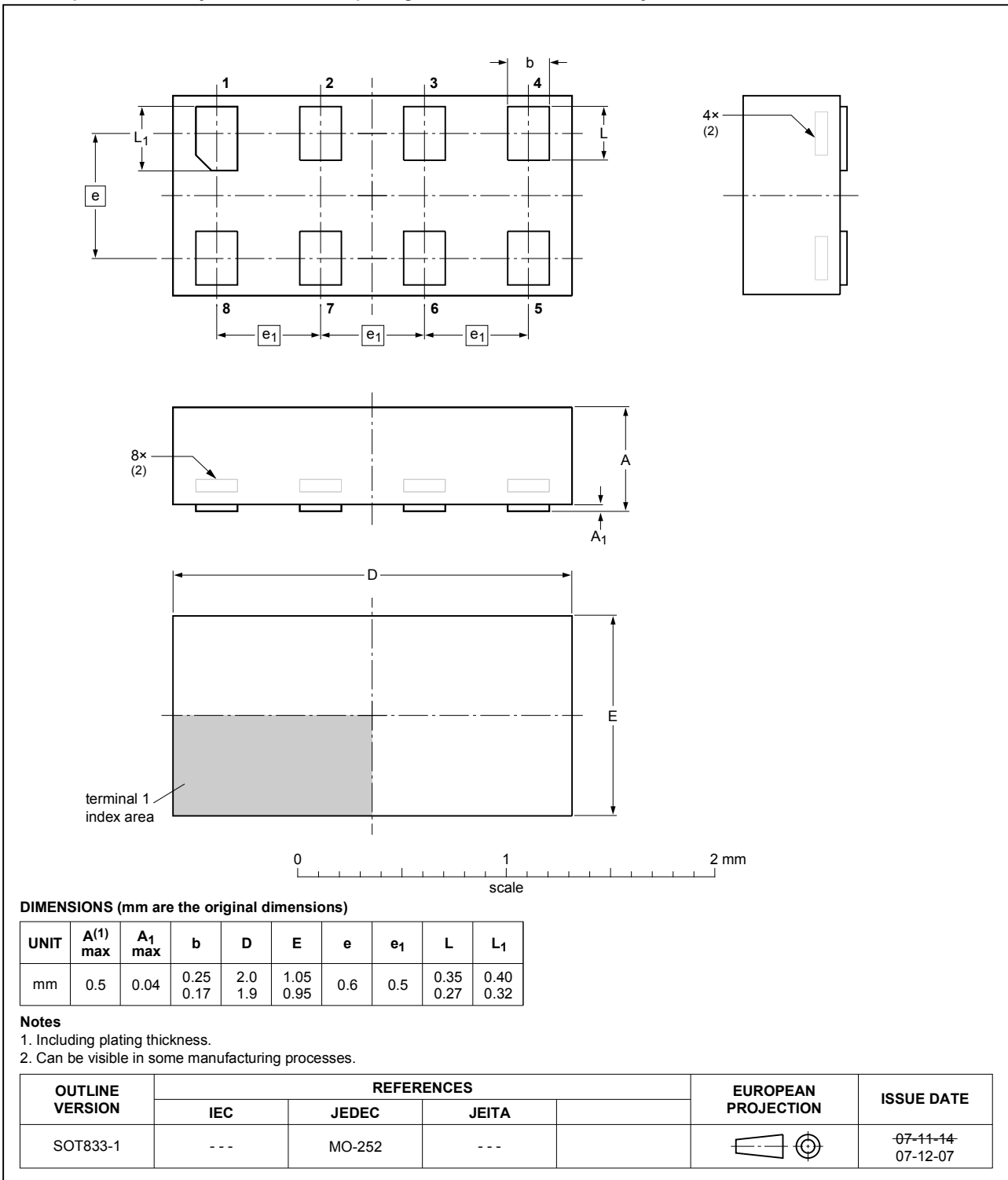


Fig. 11. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089

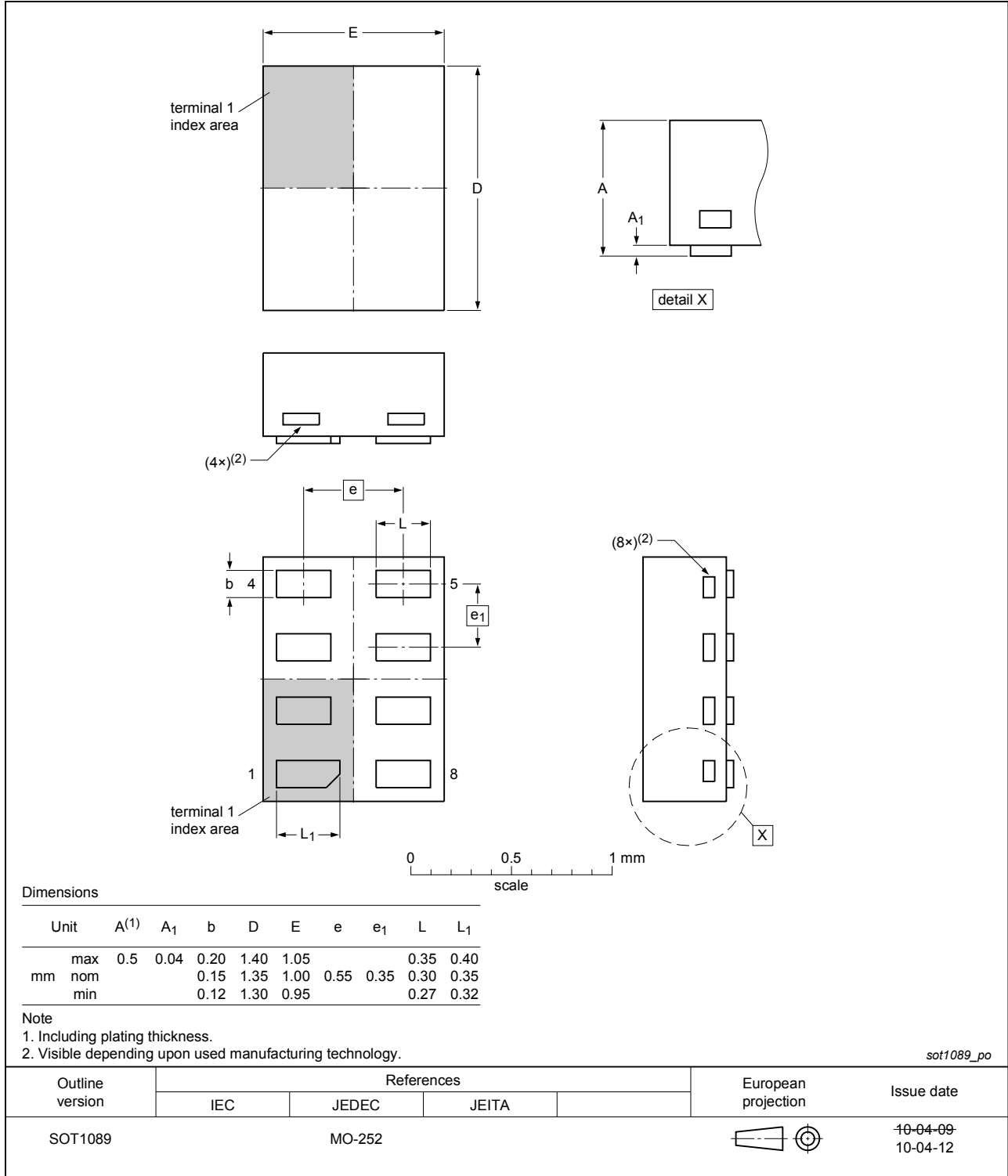


Fig. 12. Package outline SOT1089 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads;
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2

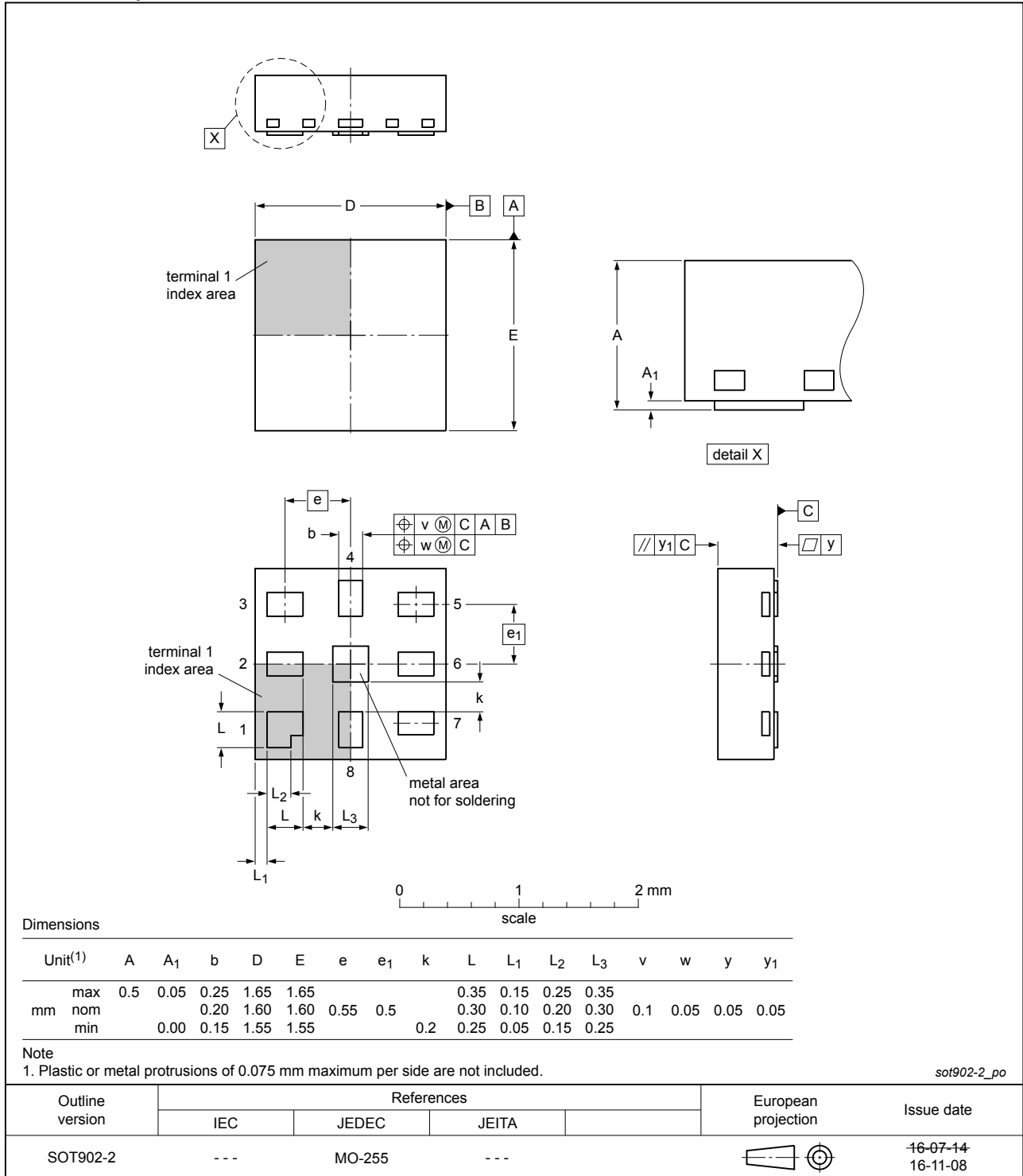


Fig. 13. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

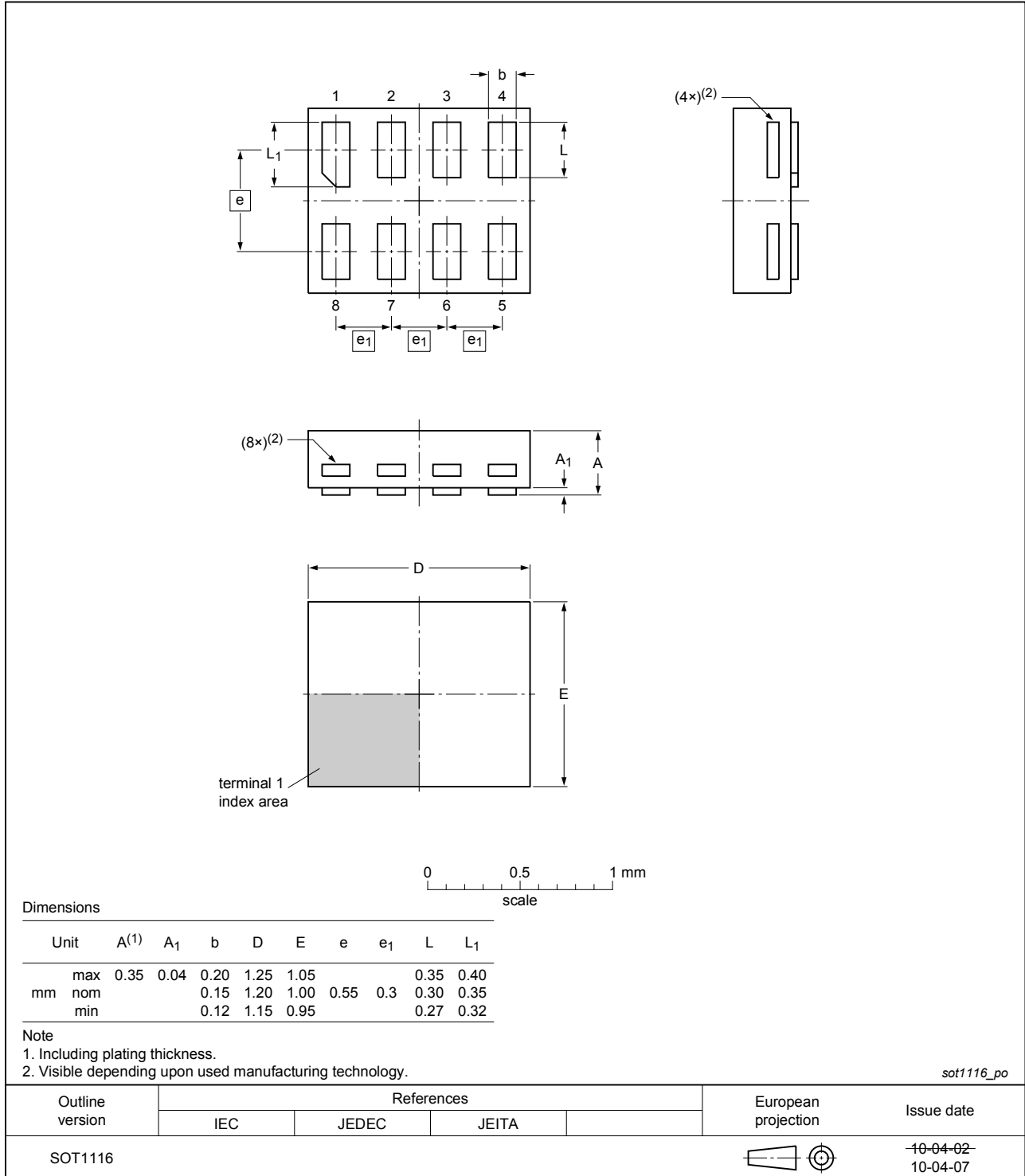


Fig. 14. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

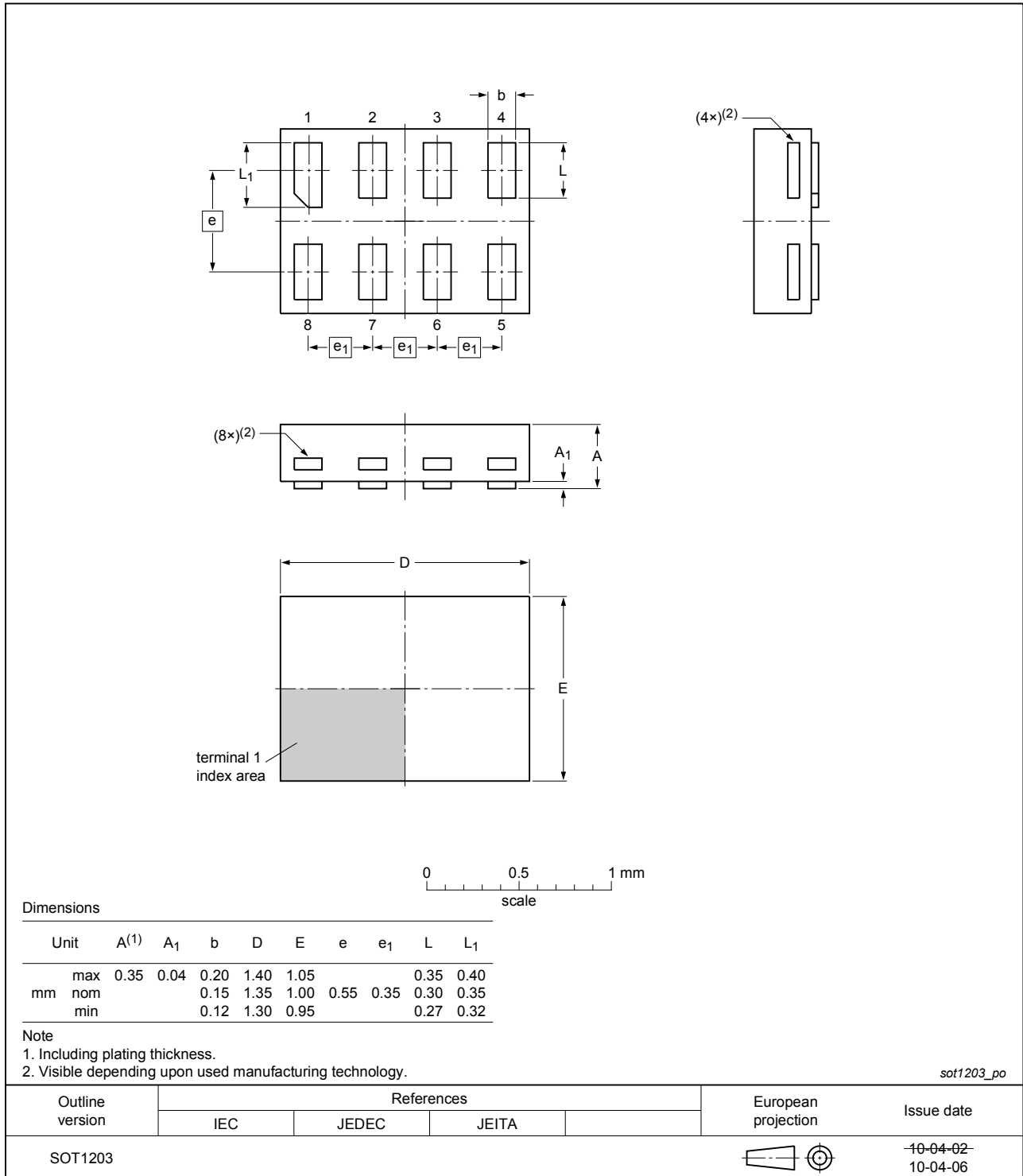


Fig. 15. Package outline SOT1203 (XSON8)

13. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--|-----------------------|---------------|-----------------|
| 74LVC2G126 v.14 | 20190110 | Product data sheet | - | 74LVC2G126 v.13 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74LVC2G126GD (SOT996-2) removed. | | | |
| 74LVC2G126 v.13 | 20161215 | Product data sheet | - | 74LVC2G126 v.12 |
| Modifications: | <ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. | | | |
| 74LVC2G126 v.12 | 20130408 | Product data sheet | - | 74LVC2G126 v.11 |
| Modifications: | <ul style="list-style-type: none"> For type number 74LVC2G126GD XSON8U has changed to XSON8. | | | |
| 74LVC2G126 v.11 | 20120622 | Product data sheet | - | 74LVC2G126 v.10 |
| Modifications: | <ul style="list-style-type: none"> For type number 74LVC2G126GM the SOT code has changed to SOT902-2. | | | |
| 74LVC2G126 v.10 | 20111201 | Product data sheet | - | 74LVC2G126 v.9 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated. | | | |
| 74LVC2G126 v.9 | 20100913 | Product data sheet | - | 74LVC2G126 v.8 |
| 74LVC2G126 v.8 | 20080505 | Product data sheet | - | 74LVC2G126 v.7 |
| 74LVC2G126 v.7 | 20080228 | Product data sheet | - | 74LVC2G126 v.6 |
| 74LVC2G126 v.6 | 20070907 | Product data sheet | - | 74LVC2G126 v.5 |
| 74LVC2G126 v.5 | 20061006 | Product data sheet | - | 74LVC2G126 v.4 |
| 74LVC2G126 v.4 | 20050201 | Product specification | - | 74LVC2G126 v.3 |
| 74LVC2G126 v.3 | 20040922 | Product specification | - | 74LVC2G126 v.2 |
| 74LVC2G126 v.2 | 20030901 | Product specification | - | 74LVC2G126 v.1 |
| 74LVC2G126 v.1 | 20030310 | Product specification | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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