



THE DATASHEET OF LNBP11SP-TR





LNBP20 / LNBP1X series

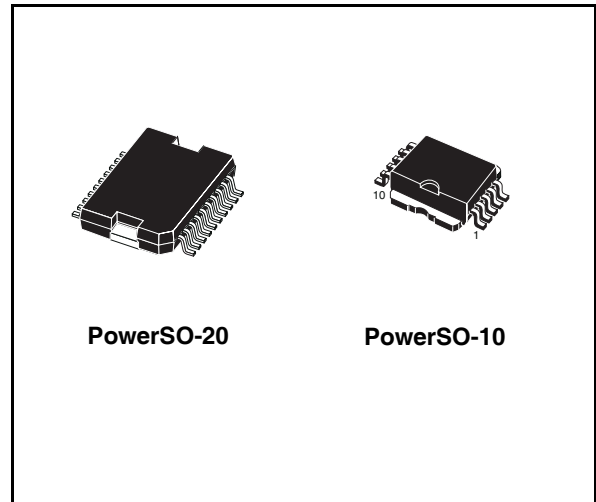
LNBP supply and control voltage regulator (parallel interface)

Feature summary

- Complete interface for two LNBS remote supply and control
- LNB selection and stand-by function
- Built-in tone oscillator factory trimmed at 22KHz
- Fast oscillator start-up facilitates DiSEqC™ encoding
- Two supply inputs for lowest dissipation
- Bypass function for slave operation
- LNB short circuit protection and diagnostic
- Auxiliary modulation input extends flexibility
- Cable length compensation
- Internal over temperature protection
- Backward current protection

Description

Intended for analog and digital satellite receivers, the LNBP is a monolithic linear voltage regulator, assembled in PowerSO-20 and PowerSO-10, specifically designed to provide the powering voltages and the interfacing signals to the LNB downconverter situated in the antenna



via the coaxial cable. Since most satellite receivers have two antenna ports, the output voltage of the regulator is available at one of two logic-selectable output pins (LNBA, LNBB). When the IC is powered and put in Stand-by (EN pin LOW), both regulator outputs are disabled to allow the antenna downconverters to be supplied/controlled by others satellite receivers sharing the same coaxial lines. In this occurrence the device will limit at 3 mA (max) the backward current that could flow from LNBA and LNBB output pins to GND. (See continuous description).

Order codes

| Part number | Package | |
|-------------|-------------|-------------|
| | PowerSO-20 | PowerSO-10 |
| LNBP10 | | LNBP10SP-TR |
| LNBP11 | | LNBP11SP-TR |
| LNBP12 | | LNBP12SP-TR |
| LNBP13 | | LNBP13SP-TR |
| LNBP14 | | LNBP14SP-TR |
| LNBP15 | | LNBP15SP-TR |
| LNBP16 | | LNBP16SP-TR |
| LNBP20 | LNBP20PD-TR | |

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1 Description (continued)

For slave operation in single dish, dual receiver systems, the bypass function is implemented by an electronic switch between the Master Input pin (MI) and the LNBA pin, thus leaving all LNB powering and control functions to the Master Receiver. This electronic switch is closed when the device is powered and EN pin is LOW.

The regulator outputs can be logic controlled to be 13 or 18 V (typ.) by mean of the VSEL pin for remote controlling of LNBs. Additionally, it is possible to increment by 1V (typ.) the selected voltage value to compensate the excess voltage drop along the coaxial cable (LLC pin HIGH).

In order to reduce the power dissipation of the device when the lowest output voltage is selected, the regulator has two Supply Input pins V_{CC1} and V_{CC2} . They must be powered respectively at 16V (min) and 23V (min), and an internal switch automatically will select the suitable supply pin according to the selected output voltage. If adequate heatsink is provided and higher power losses are acceptable, both supply pins can be powered by the same 23V source without affecting any other circuit performance.

The ENT (Tone Enable) pin activates the internal oscillator so that the DC output is modulated by a ± 0.3 V, 22KHz (typ.) square wave. This internal oscillator is factory trimmed within a tolerance of ± 2 KHz, thus no further adjustments neither external components are required.

A burst coding of the 22KHz tone can be accomplished thanks to the fast response of the ENT input and the prompt oscillator start-up. This helps designers who want to implement the DiSEqC™ protocols ^(a).

In order to improve design flexibility and to allow implementation of newcoming LNB remote control standards, an analogic modulation input pin is available (EXTM). An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. When external modulation is not used, the relevant pin can be left open.

Two pins are dedicated to the overcurrent protection/monitoring: CEXT and OLF. The overcurrent protection circuit works dynamically: as soon as an overload is detected in either LNB output, the output is shut-down for a time t_{off} determined by the capacitor connected between CEXT and GND. Simultaneously the OLF pin, that is an open collector diagnostic output flag, from HIGH IMPEDANCE state goes LOW.

After the time has elapsed, the output is resumed for a time $t_{on}=1/15t_{off}$ (typ.) and OLF goes in HIGH IMPEDANCE. If the overload is still present, the protection circuit will cycle again through t_{off} and t_{on} until the overload is removed. Typical $t_{on}+t_{off}$ value is 1200ms when a $4.7\mu F$ external capacitor is used.

This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start up even with highly capacitive loads on LNB outputs.

The device is packaged in PowerSO-20 for surface mounting. When a limited functionality in a smaller package matches design needs, a range of cost-effective PowerSO-10 solutions is also offered. All versions have built-in thermal protection against overheating damage.

a. External components are needed to comply to level 2.x and above (bidirectional) DiSEqC™ bus hardware requirements. DiSEqC™ is a trademark of EUTELSAT.

2 Pin configuration

Figure 1. Pin connections (top view)

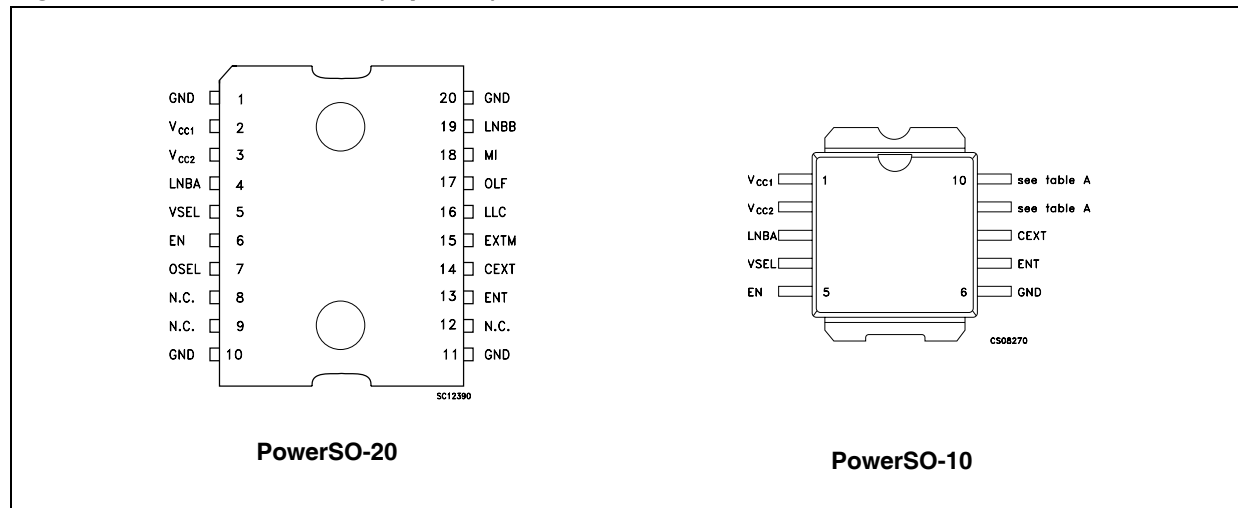


Table 1. Pin Description

| SYMBOL | NAME | FUNCTION | PIN NUMBER vs SALES TYPE (LNBP) | | | | | | | |
|------------------|---|--|---------------------------------|------|------|------|------|------|------|------|
| | | | 20PD | 10SP | 11SP | 12SP | 13SP | 14SP | 15SP | 16SP |
| V _{CC1} | Supply input 1 | 15V to 25V supply. It is automatically selected when V _{OUT} = 13 or 14V | 2 | 1 | 1 | 1 | | 1 | 1 | 1 |
| V _{CC2} | Supply input 2 | 22V to 25V supply. It is automatically selected when V _{OUT} = 18 or 19V | 3 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| LNBA | Output port | See truth table voltage and port selection. In stand-by mode this port is powered by the MI pin via the internal bypass switch | 4 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| V _{SEL} | Output voltage selection: 13 or 18V (typ) | Logic control input: see truth table | 5 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| EN | Port enable | Logic control input: see truth table | 6 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| OSEL | Port selection | Logic control input: see truth table | 7 | 9 | NA | NA | NA | NA | NA | NA |
| GND | Ground | Circuit ground. It is internally connected to the die frame | 1 10 11 20 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |

Table 1. Pin Description

| SYMBOL | NAME | FUNCTION | PIN NUMBER vs SALES TYPE (LNBP) | | | | | | | |
|--------|-------------------------------|---|---------------------------------|------|------|------|------|------|------|------|
| | | | 20PD | 10SP | 11SP | 12SP | 13SP | 14SP | 15SP | 16SP |
| ENT | 22KHz tone enable | Logic control input: see truth table | 13 | 7 | 7 | 7 | 7 | 7 | 7 | 7 |
| CEXT | External capacitor | Timing capacitor used by the dynamic overload protection. Typical application is 4.7 μ F for a 1200ms cycle | 14 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| EXTM | External modulator | External modulation input. Needs DC decoupling to the AC source. if not used, can be left open. | 15 | NA | NA | NA | 9 | NA | 9 | 9 |
| LLC | Line length compens. (1V typ) | Logic control input: see truth table | 16 | NA | NA | 9 | NA | 9 | NA | 10 |
| OLF | Over load flag | Logic output (open collector). Normally in HIGH IMPEDANCE, goes LOW when current or thermal overload occurs | 17 | NA | 9 | NA | NA | 10 | 10 | NA |
| MI | Master input | In stand-by mode, the voltage on MI is routed to LNBA pin. Can be left open if bypass function is not needed | 18 | NA | 10 | 10 | 10 | NA | NA | NA |
| LNBB | Output port | See truth tables for voltage and port selection | 19 | 10 | NA | NA | NA | NA | NA | NA |

Note: The limited pin availability of the PowerSO-10 package leads to drop some functions.

3 Maximum ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------|--|--------------------|------------------|
| V_I | DC Input voltage (V_{CC1} , V_{CC2} , MI) | 28 | V |
| V_O | Output voltage | -0.3 to 28 | V |
| I_O | Output current (LNBA, LNBB) | Internally Limited | mA |
| V_I | Logic input voltage (ENT, EN OSEL, VSEL, LLC) | -0.5 to 7 | V |
| I_{SW} | Bypass switch current | 900 | mA |
| P_D | Power dissipation at $T_{case} < 85^\circ\text{C}$ | 14 | W |
| T_{stg} | Storage temperature range | -40 to +150 | $^\circ\text{C}$ |
| T_{op} | Operating junction temperature range | -40 to +125 | $^\circ\text{C}$ |

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied

Table 3. Thermal data

| Symbol | Parameter | PowerSO-20 | PowerSO-10 | Unit |
|------------|----------------------------------|------------|------------|---------------------------|
| R_{thJC} | Thermal resistance junction-case | 2 | 2 | $^\circ\text{C}/\text{W}$ |

Table 4. Logic Controls Truth Table

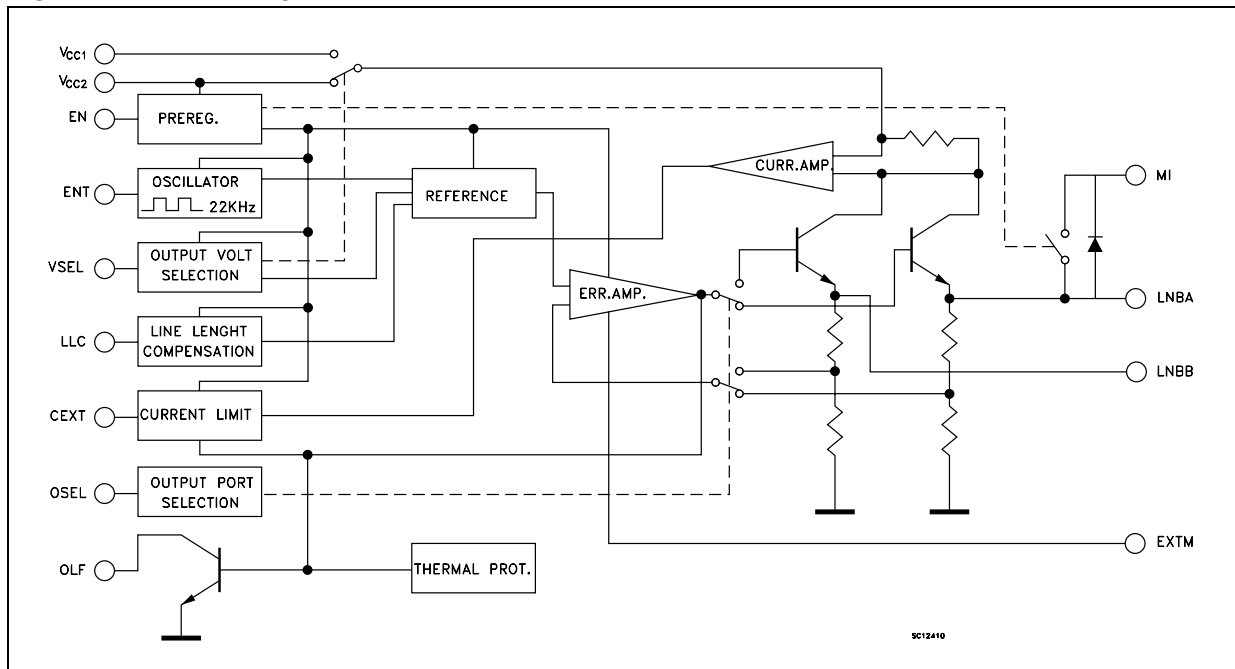
| CONTROL I/O | PIN NAME | L | H |
|-------------|----------|---|----------------------|
| OUT | OLF | $I_{OUT} > I_{OMAX}$ or $T_j > 150^\circ\text{C}$ | $I_{OUT} < I_{OMAX}$ |
| IN | ENT | 22KHz tone OFF | 22KHz tone ON |
| IN | EN | See Table Below | See Table Below |
| IN | OSEL | See Table Below | See Table Below |
| IN | VSEL | See Table Below | See Table Below |
| IN | LLC | See Table Below | See Table Below |

| EN | OSEL | VSEL | LLCO | V_{LNBA} | V_{LNBB} |
|----|------|------|------|-------------------------------|------------|
| L | X | X | X | $V_{MI} - 0.4\text{V}$ (typ.) | Disabled |
| H | L | L | L | 13V (typ.) | Disabled |
| H | L | H | L | 18V (typ.) | Disabled |
| H | L | L | H | 14V (typ.) | Disabled |
| H | L | H | H | 19V (typ.) | Disabled |
| H | H | L | L | Disabled | 13V (typ.) |
| H | H | H | L | Disabled | 18V (typ.) |
| H | H | L | H | Disabled | 14V (typ.) |
| H | H | H | H | Disabled | 19V (typ.) |

Note: All logic input pins have internal pull-down resistor (typ. = 250KW)

4 Diagram

Figure 2. Block diagram



5 Electrical characteristics

Table 5. Electrical characteristics for LNBP Series ($T_J = 0$ to 85°C , $C_1 = 0.22\mu\text{F}$, $C_O = 0.1\mu\text{F}$, $\text{EN}=\text{H}$, $\text{ENT}=\text{L}$, $\text{LLC}=\text{L}$, $V_{\text{IN}1}=16\text{V}$, $V_{\text{IN}2}=23\text{V}$ $I_{\text{OUT}}=50\text{mA}$, unless otherwise specified.)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|---|--|------|---------------------|------|-------------------------|
| $V_{\text{IN}1}$ | $V_{\text{CC}1}$ Supply voltage | $I_O = 500 \text{ mA}$, $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$ | 15 | | 25 | V |
| | | $I_O = 500 \text{ mA}$, $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$ | 16 | | 25 | V |
| $V_{\text{IN}2}$ | $V_{\text{CC}2}$ Supply voltage | $I_O = 500 \text{ mA}$, $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$ | 22 | | 25 | V |
| | | $I_O = 500 \text{ mA}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$ | 23 | | 25 | V |
| $V_{\text{O}1}$ | Output voltage | $I_O = 500 \text{ mA}$, $\text{VSEL}=\text{H}$, $\text{LLC}=\text{L}$ | 17.3 | 18 | 18.7 | V |
| | | $I_O = 500 \text{ mA}$, $\text{VSEL}=\text{H}$, $\text{LLC}=\text{H}$ | | 19 | | V |
| $V_{\text{O}2}$ | Output voltage | $I_O = 500 \text{ mA}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$ | 12.5 | 13 | 13.5 | V |
| | | $I_O = 500 \text{ mA}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$ | | 14 | | V |
| ΔV_O | Line regulation | $V_{\text{IN}1}=15$ to 18V , $V_{\text{OUT}}=13\text{V}$ | | 4 | 40 | mV |
| | | $V_{\text{IN}2}=22$ to 25V , $V_{\text{OUT}}=18\text{V}$ | | 4 | 40 | mV |
| ΔV_O | Load regulation | $V_{\text{IN}1}=V_{\text{IN}2}=22\text{V}$, $V_{\text{OUT}}=13$ or 18V $I_O = 50$ to 500mA | | 80 | 180 | mV |
| SVR | Supply voltage rejection | $V_{\text{IN}1} = V_{\text{IN}2} = 23 \pm 0.5V_{\text{ac}}$, $f_{\text{ac}} = 120 \text{ Hz}$, | | 45 | | dB |
| I_{MAX} | Output current limiting | | 500 | 650 | 800 | mA |
| t_{OFF} | Dynamic overload protection OFF time | Output Shorted, $C_{\text{EXT}} = 4.7\mu\text{F}$ | | 1100 | | ms |
| t_{ON} | Dynamic overload protection ON time | Output Shorted, $C_{\text{EXT}} = 4.7\mu\text{F}$ | | $t_{\text{OFF}}/15$ | | ms |
| f_{TONE} | Tone frequency | $\text{ENT}=\text{H}$ | 20 | 22 | 24 | KHz |
| A_{TONE} | Tone amplitude | $\text{ENT}=\text{H}$ | 0.55 | 0.72 | 0.9 | V_{PP} |
| D_{TONE} | Tone duty cycle | $\text{ENT}=\text{H}$ | 40 | 50 | 60 | % |
| t_r, t_f | Tone rise and fall time | $\text{ENT}=\text{H}$ | 5 | 10 | 15 | μs |
| G_{EXTM} | External modulation gain | $\Delta V_{\text{OUT}}/\Delta V_{\text{EXTM}}$, $f = 10\text{Hz}$ to 40KHz | | 5 | | |
| V_{EXTM} | External modulation input voltage | AC Coupling | | | 400 | mV_{PP} |
| Z_{EXTM} | External modulation impedance | $f = 10\text{Hz}$ to 40KHz | | 400 | | Ω |
| V_{SW} | Bypass switch voltage drop (MI to LNBA) | $\text{EN}=\text{L}$, $I_{\text{SW}}=300\text{mA}$, $V_{\text{CC}2}-V_{\text{MI}}=4\text{V}$ | | 0.35 | 0.6 | V |
| V_{OL} | Overload flag pin logic LOW | $I_{\text{OL}}=8\text{mA}$ | | 0.28 | 0.5 | V |
| I_{OZ} | Overload flag pin OFF state leakage current | $V_{\text{OH}} = 6\text{V}$ | | | 10 | μA |
| V_{IL} | Control input pin logic LOW | | | | 0.8 | V |

Table 5. Electrical characteristics for LNBP Series ($T_J = 0$ to 85°C , $C_I = 0.22\mu\text{F}$, $C_O = 0.1\mu\text{F}$, $\text{EN}=\text{H}$, $\text{ENT}=\text{L}$, $\text{LLC}=\text{L}$, $V_{\text{IN}1}=16\text{V}$, $V_{\text{IN}2}=23\text{V}$ $I_{\text{OUT}}=50\text{mA}$, unless otherwise specified.)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|--------------------------------|---|------|------|------|------------------|
| V_{IH} | Control input pin logic HIGH | | 2.5 | | | V |
| I_{IH} | Control pins input current | $V_{\text{IH}} = 5\text{V}$ | | 20 | | μA |
| I_{CC} | Supply current | Output Disabled ($\text{EN}=\text{L}$) | | 0.3 | 1 | mA |
| | | $\text{ENT}=\text{H}$, $I_{\text{OUT}}=500\text{mA}$ | | 3.1 | 6 | mA |
| I_{OBK} | Output backward current | $\text{EN}=\text{L}$, $V_{\text{LNBA}} = V_{\text{LNBB}} = 18\text{V}$ $V_{\text{IN}1} = V_{\text{IN}2} = 22\text{V}$ or floating | | 0.2 | 3 | mA |
| T_{SHDN} | Temperature shutdown threshold | | | 150 | | $^\circ\text{C}$ |

6 Typical characteristics

(unless otherwise specified $T_J = 25^\circ\text{C}$)

Figure 3. Output voltage vs output current

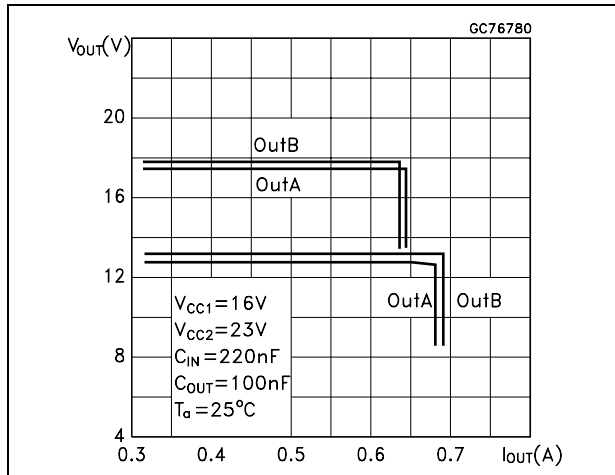


Figure 4. Tone duty cycle vs temperature

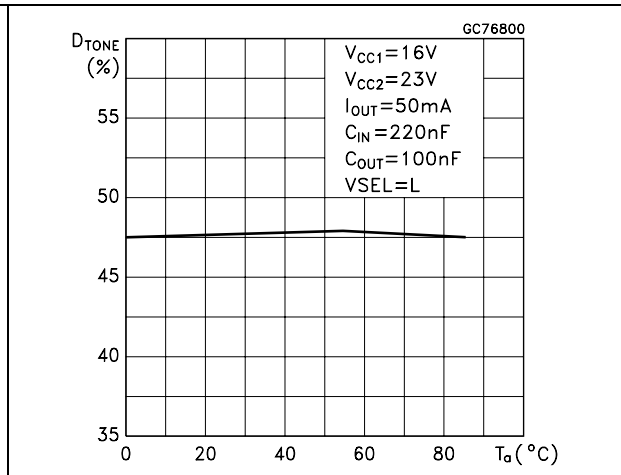


Figure 5. Tone fall time vs temperature

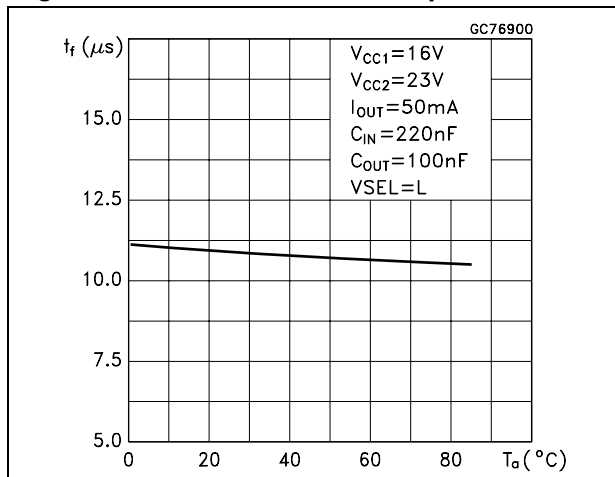


Figure 6. Tone frequency vs temperature

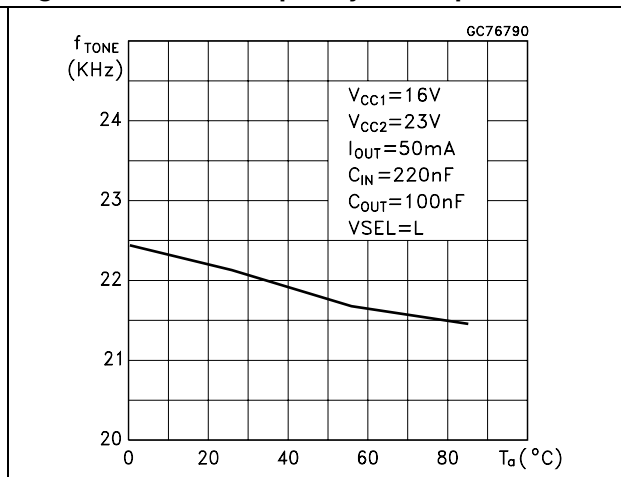


Figure 7. Tone rise time vs temperature

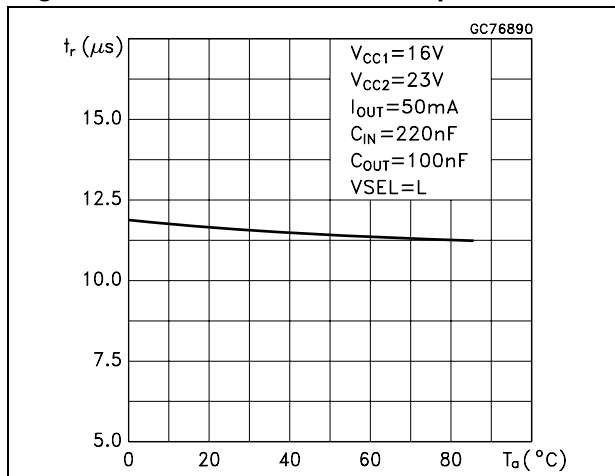


Figure 8. Tone amplitude vs temperature

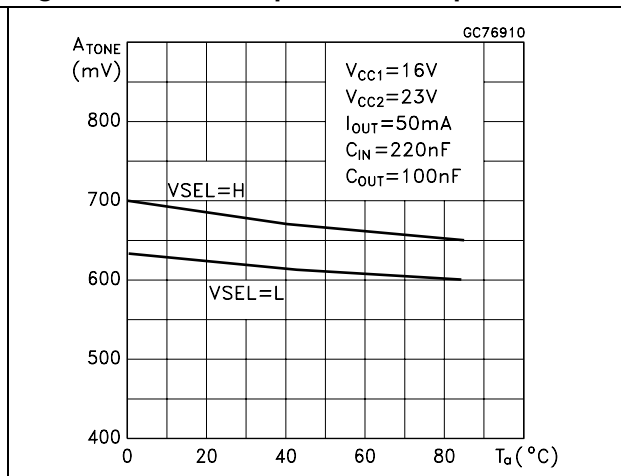


Figure 9. S.V.R. vs Frequency

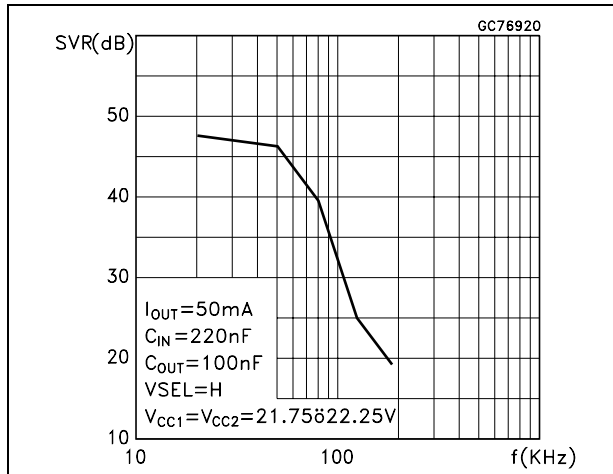


Figure 10. External modulation vs temperature

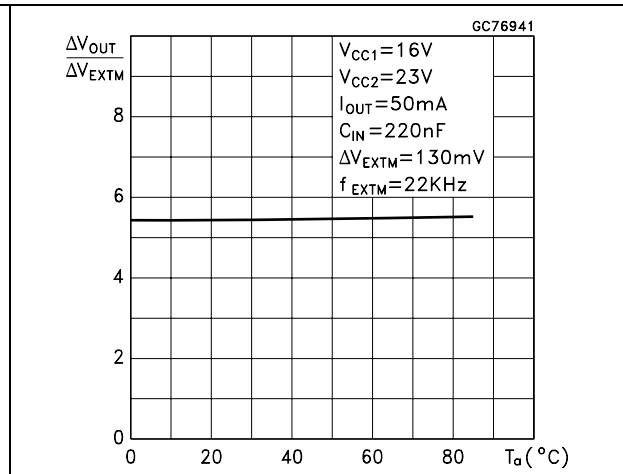


Figure 11. Bypass switch drop vs output current

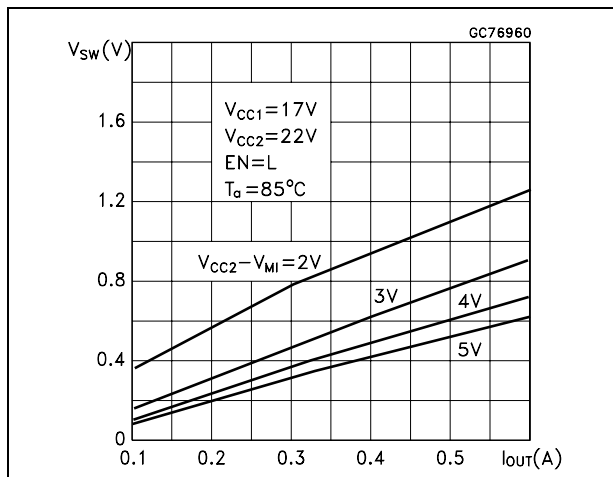


Figure 12. LNBA External modulation gain vs frequency

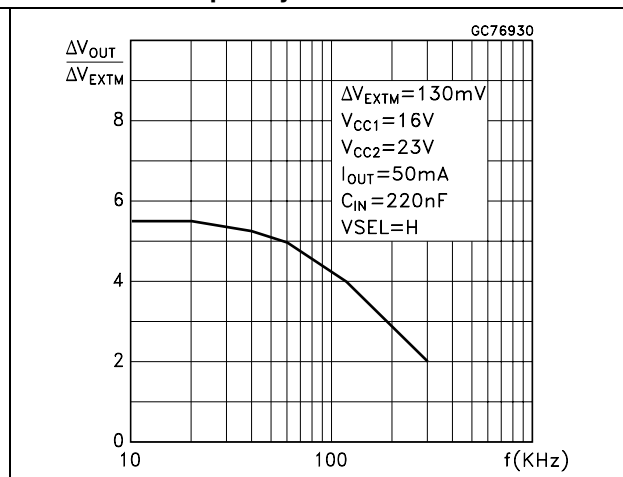


Figure 13. Bypass switch drop vs output current

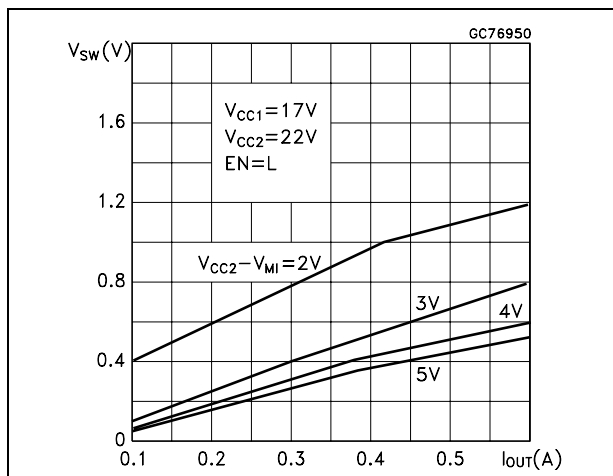


Figure 14. Overload flag pin logic low vs flag current

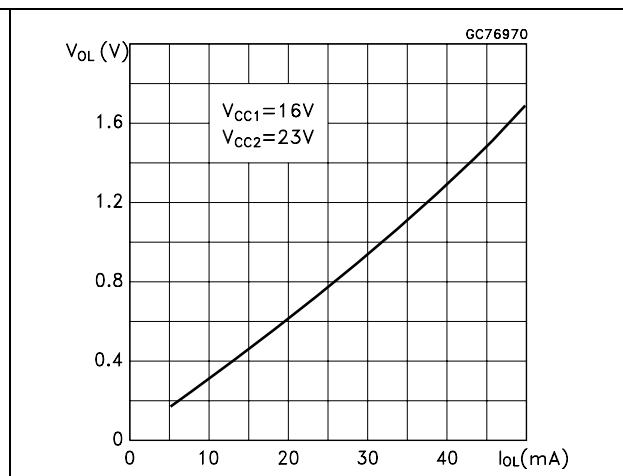


Figure 15. Supply voltage vs temperature

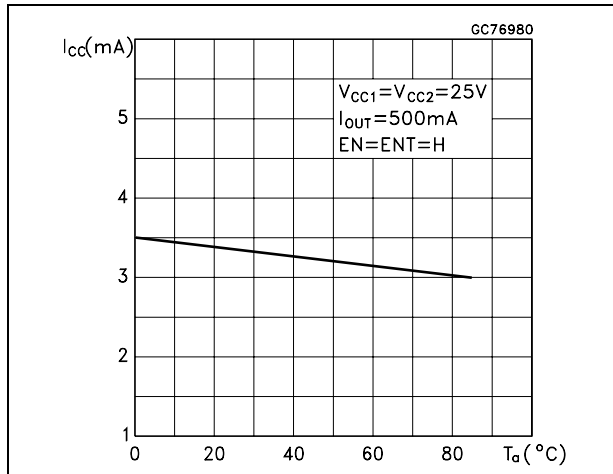


Figure 16. Supply voltage vs temperature

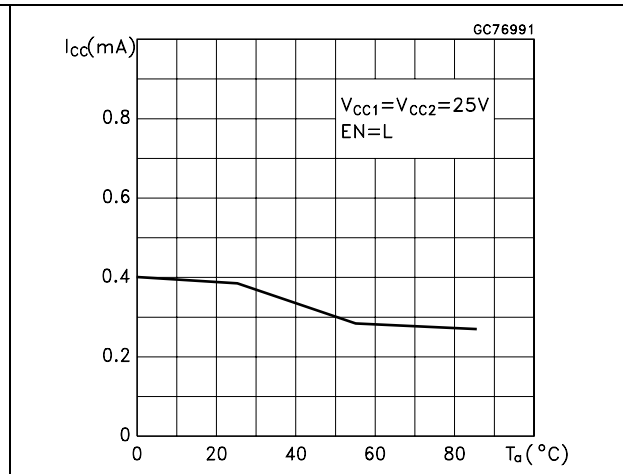


Figure 17. Dynamic overload protection (I_{SC} vs time)

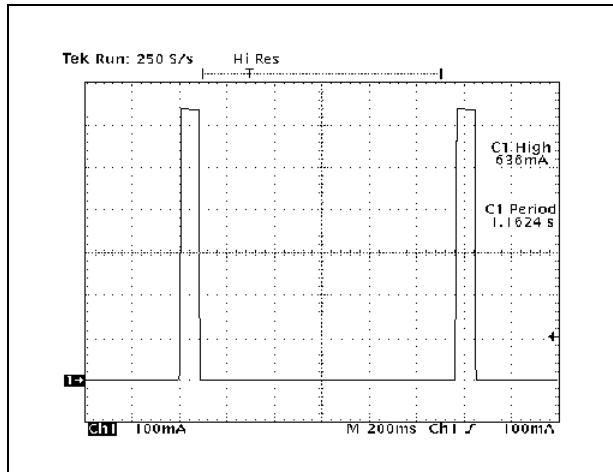


Figure 18. Tone enable

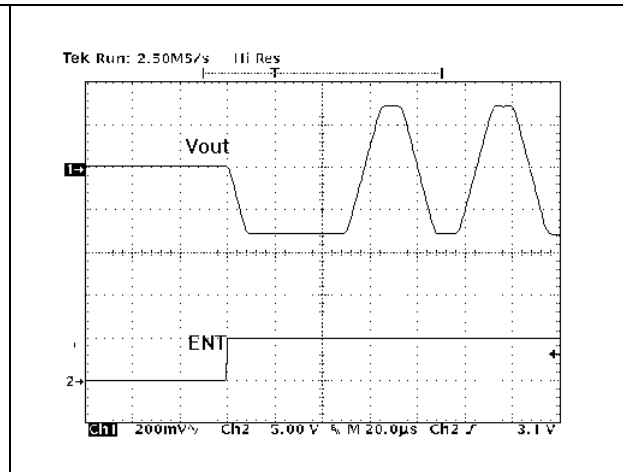


Figure 19. Tone disable

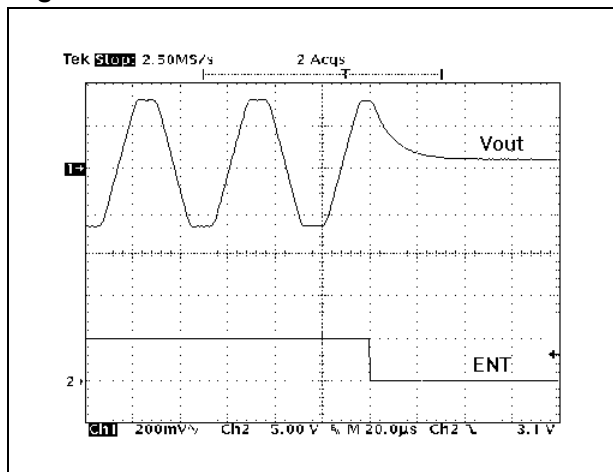


Figure 20. 22KHz Tone

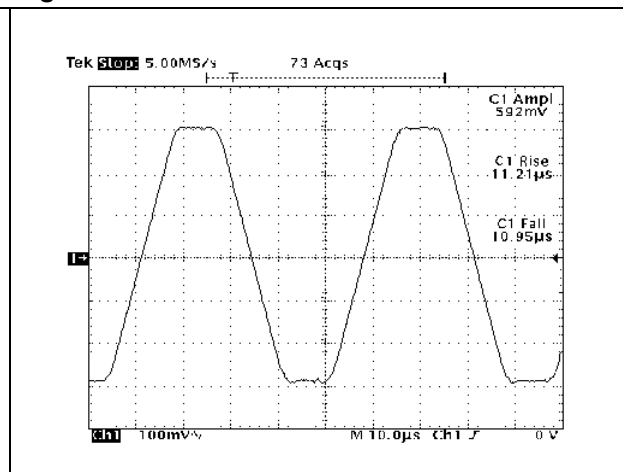


Figure 21. Enable time

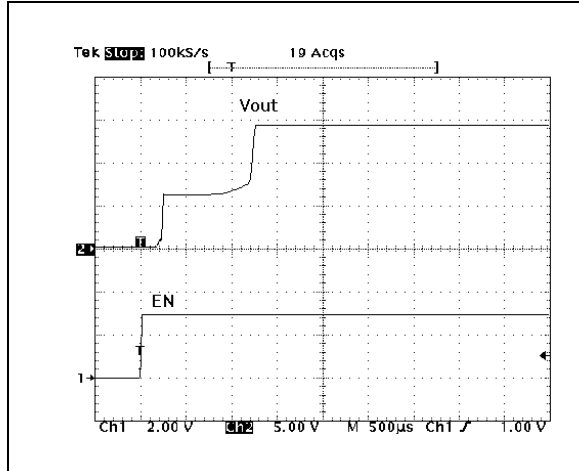


Figure 22. Disable time

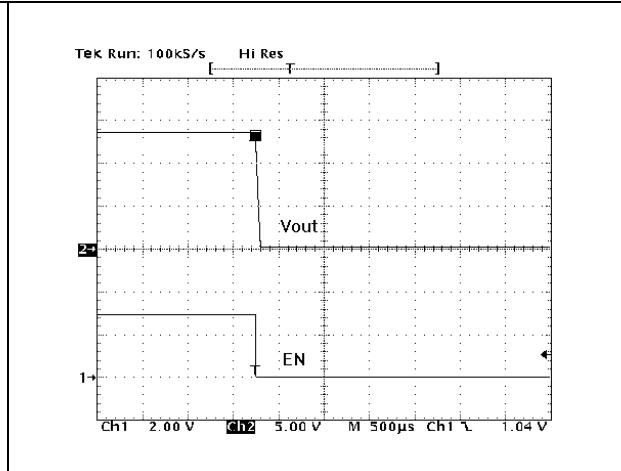


Figure 23. 18V to 13V Change

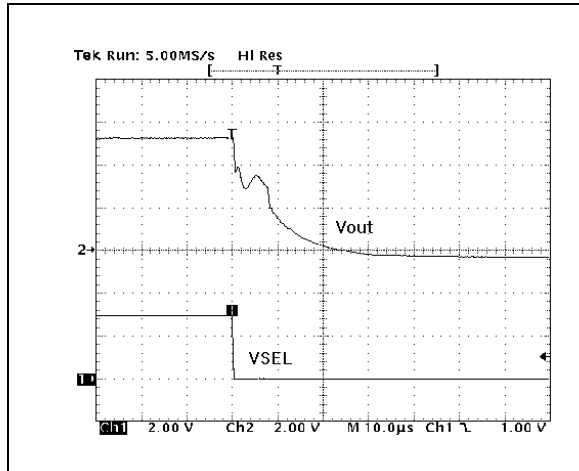
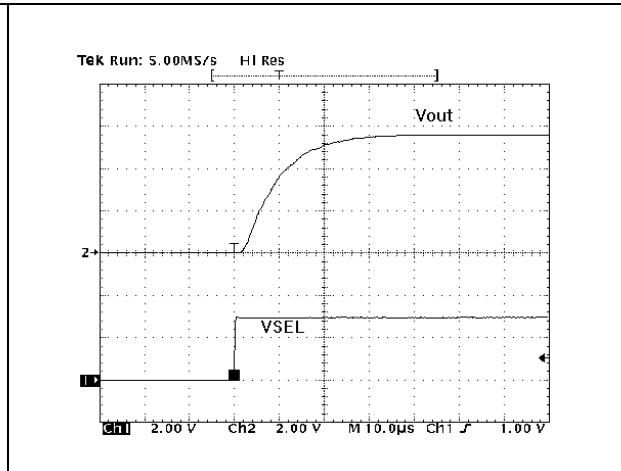


Figure 24. 18V to 13V Change



7 Typical application schematics

Figure 25. Two antenna ports receiver

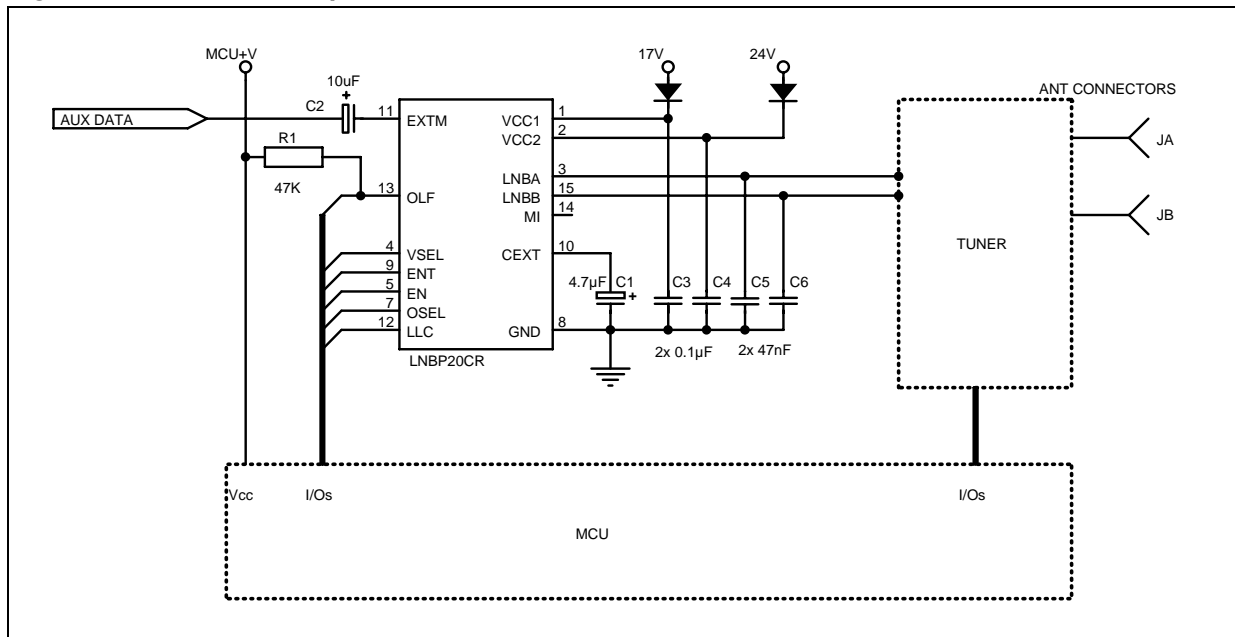


Figure 26. Single antenna receiver with master receiver port

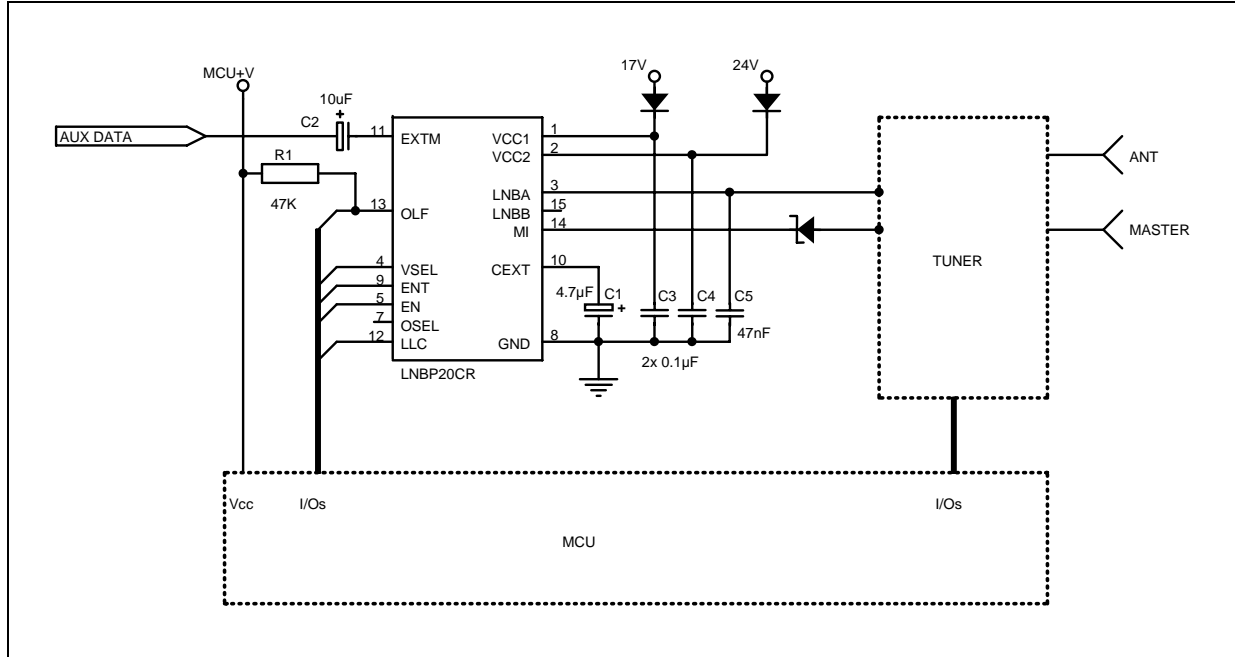


Figure 27. Using serial bus to save MPU I/os

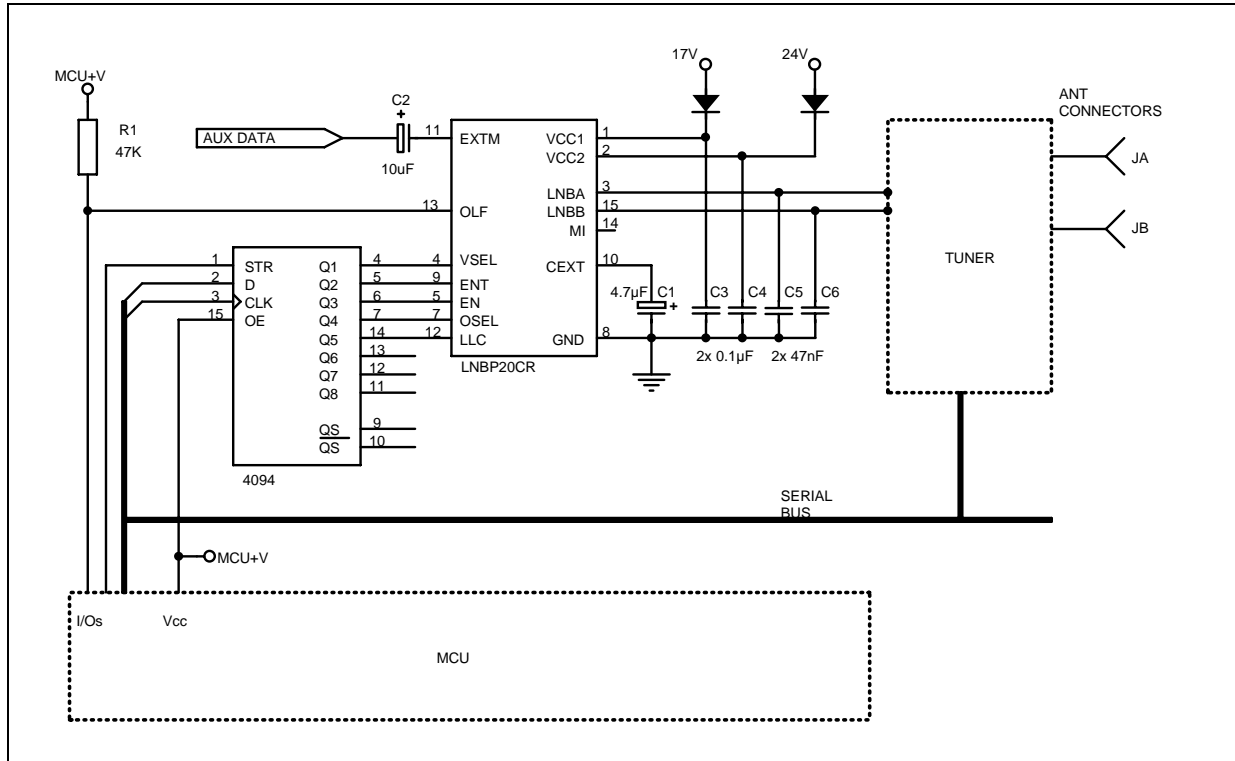


Figure 28. Two antenna ports receiver - low cost solution

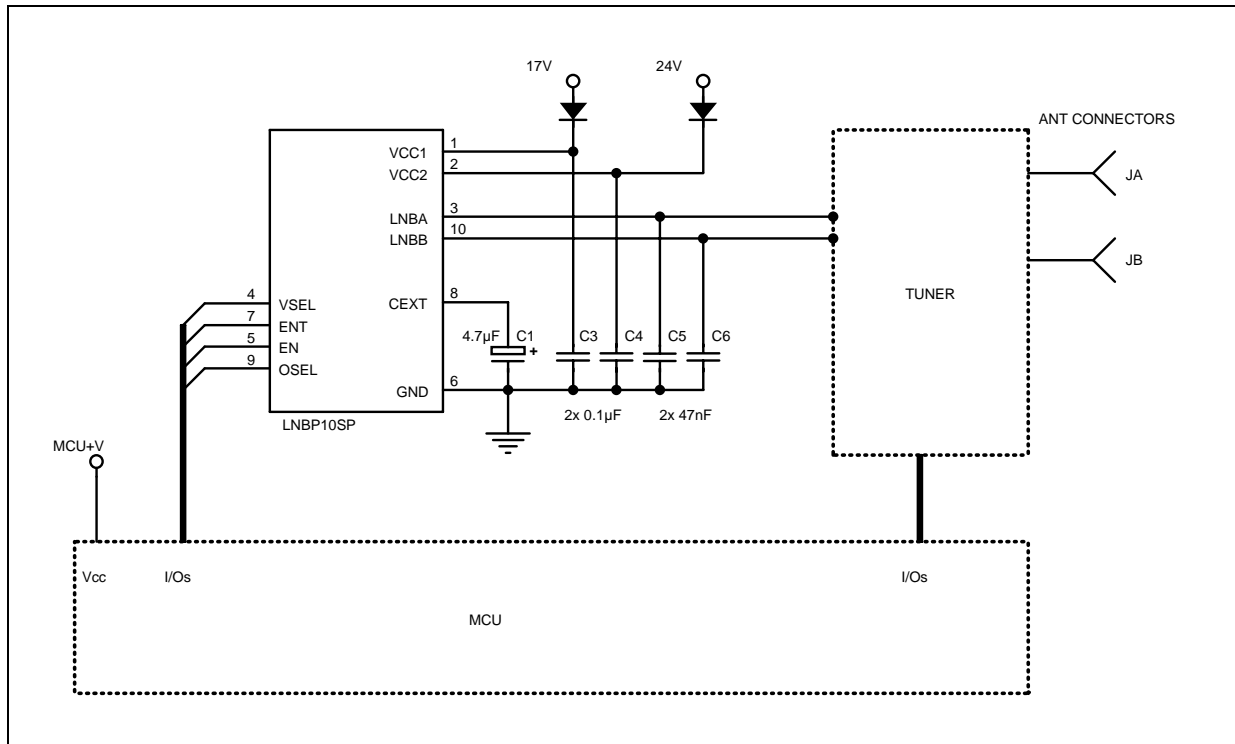


Figure 29. Connecting together V_{CC1} and V_{CC2}

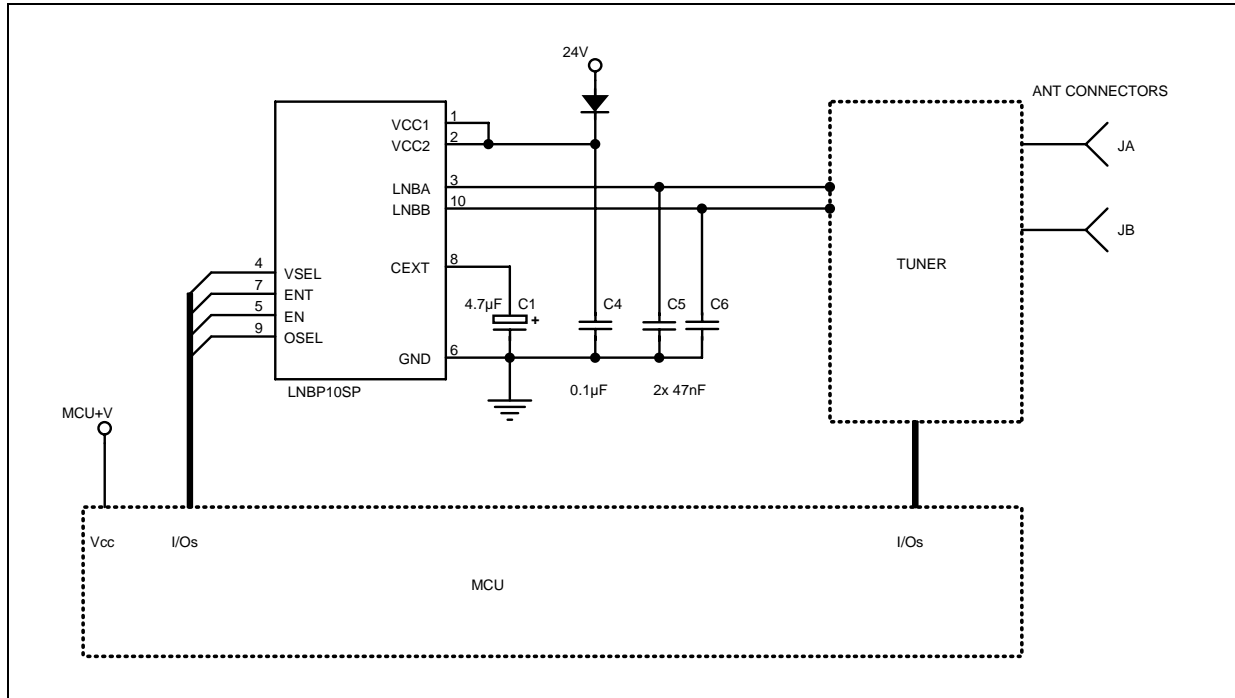


Figure 30. Single antenna receiver with master receiver port - low cost solution

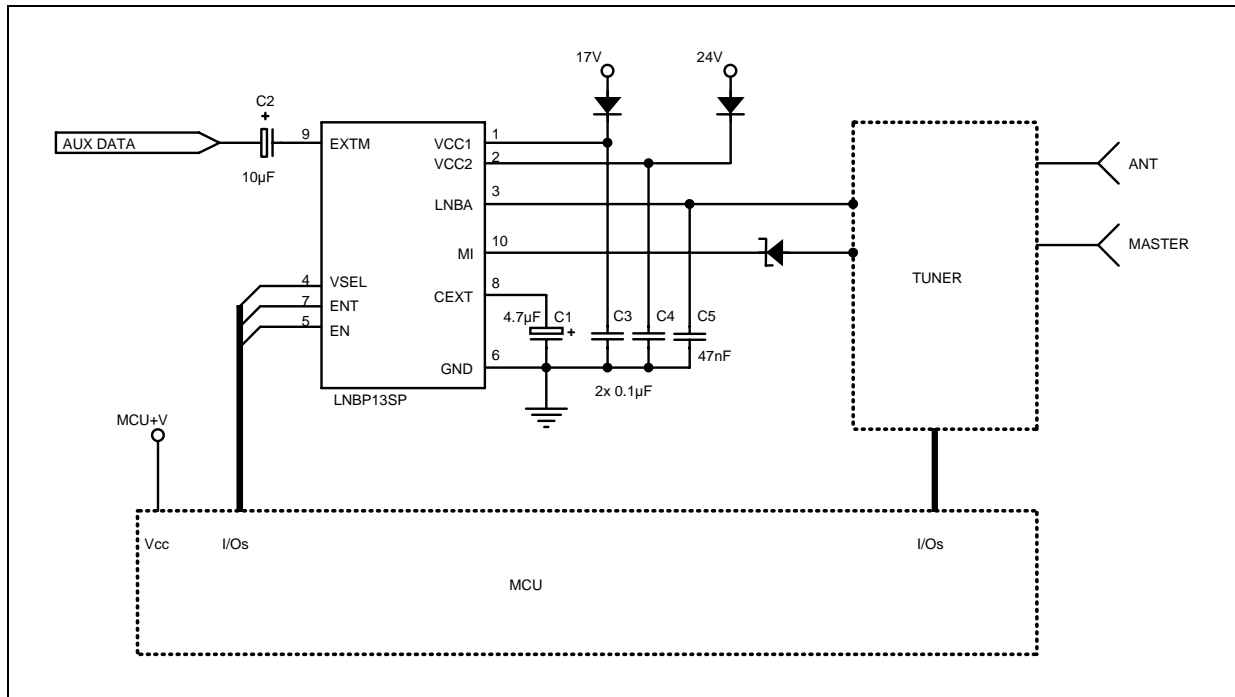
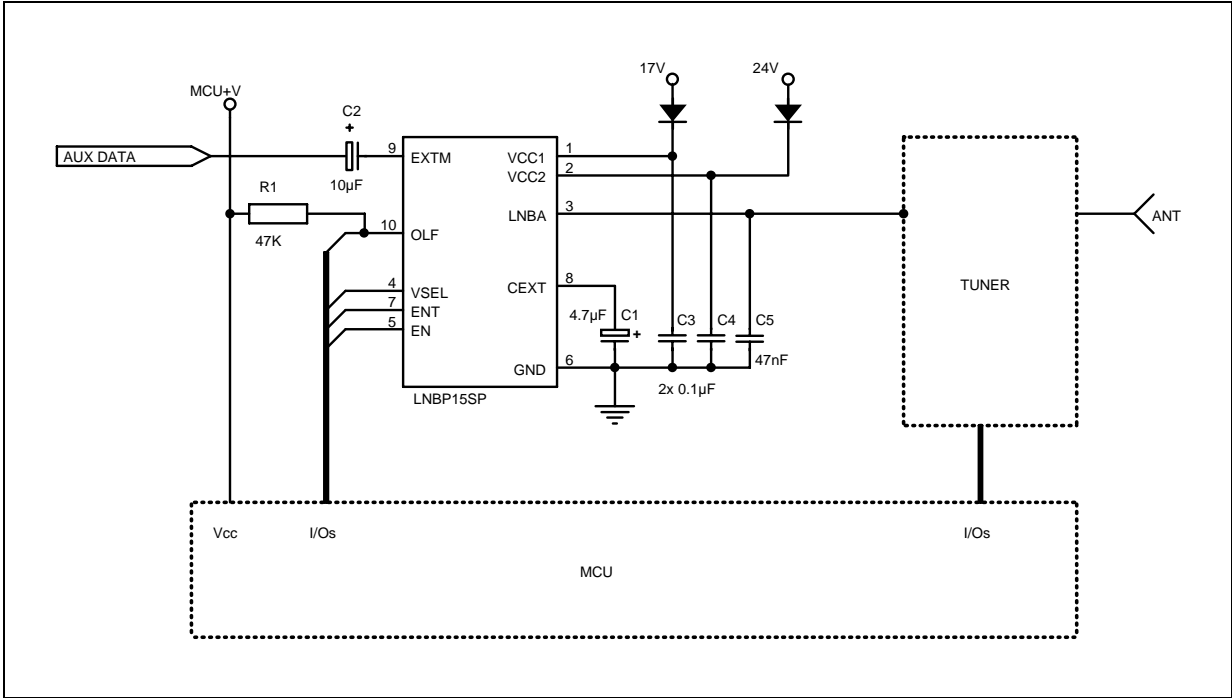


Figure 31. Single antenna receiver with overload diagnostic



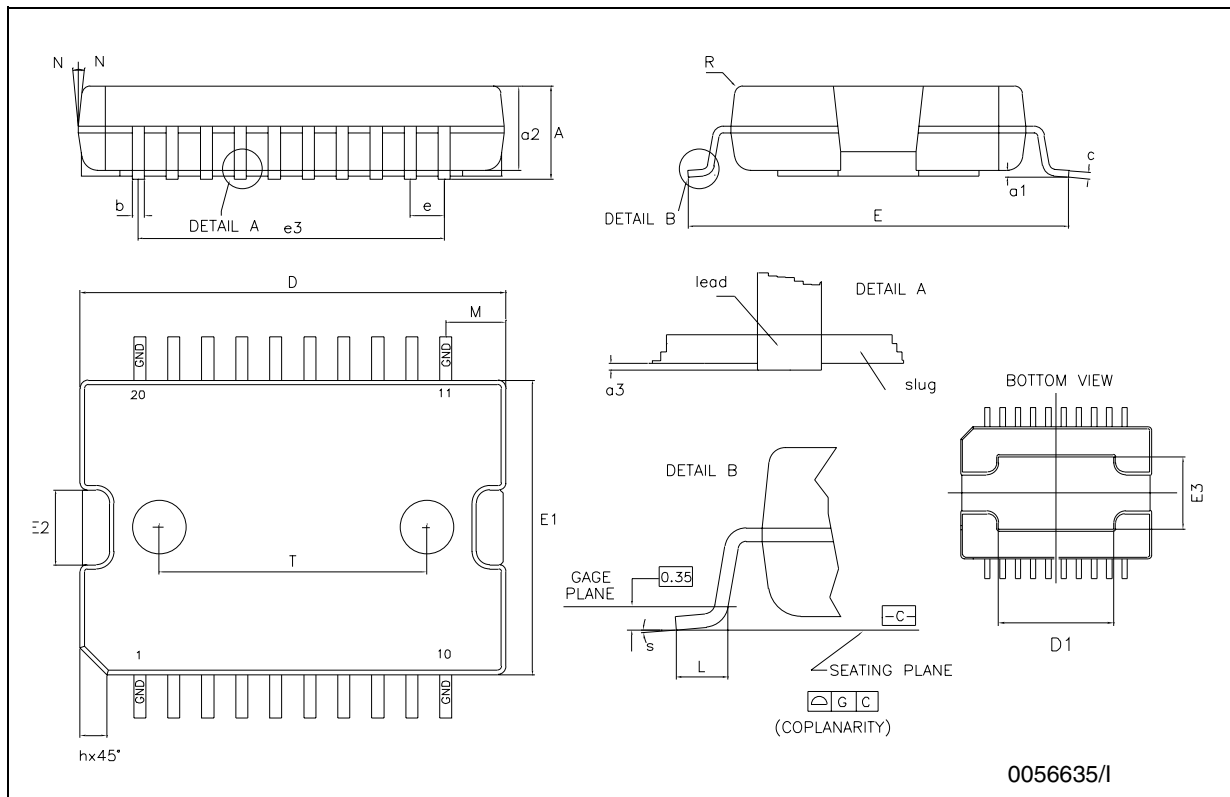
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

PowerSO-20 MECHANICAL DATA

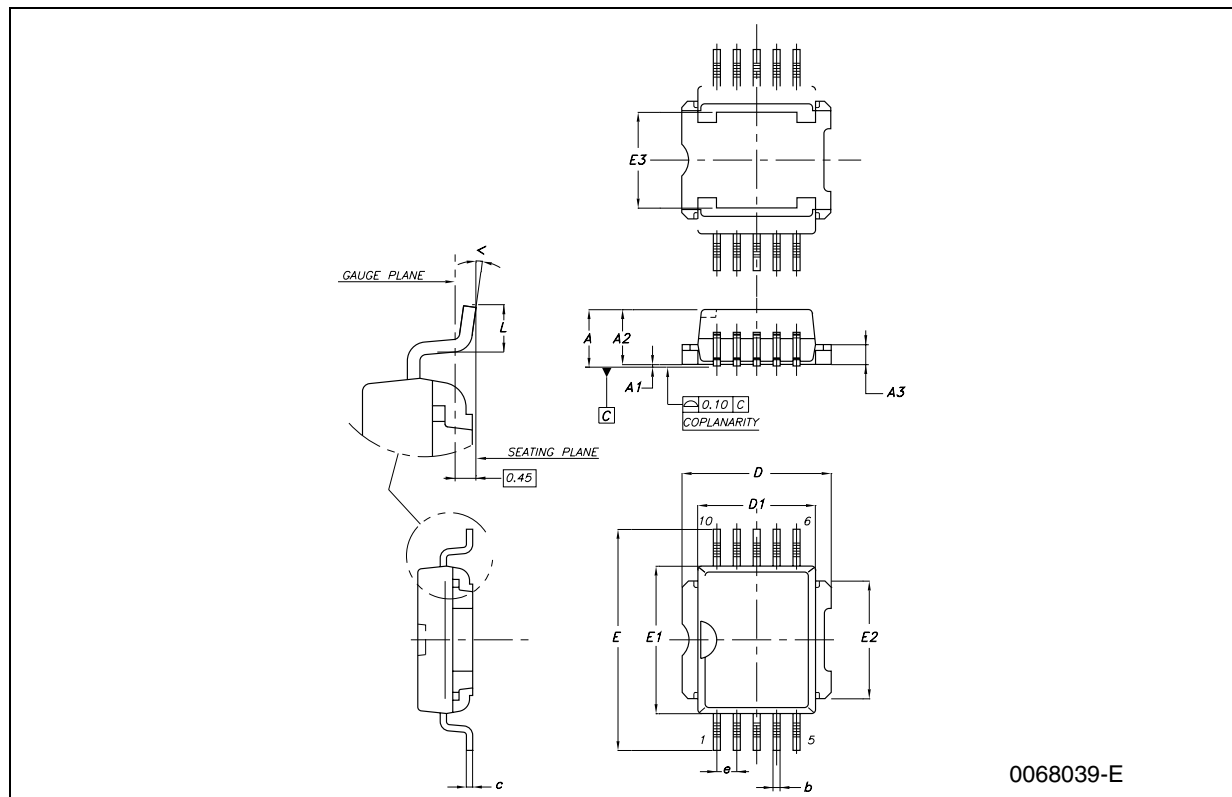
| DIM. | mm. | | | inch | | |
|--------|-------|-------|-------|--------|--------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 3.60 | | | 0.1417 |
| a1 | 0.10 | | 0.30 | 0.0039 | | 0.0118 |
| a2 | | | 3.30 | | | 0.1299 |
| a3 | 0 | | 0.10 | 0 | | 0.0039 |
| b | 0.40 | | 0.53 | 0.0157 | | 0.0209 |
| c | 0.23 | | 0.32 | 0.0090 | | 0.0013 |
| D (1) | 15.80 | | 16.00 | 0.6220 | | 0.630 |
| E | 13.90 | | 14.50 | 0.5472 | | 0.5710 |
| e | | 1.27 | | | 0.0500 | |
| e3 | | 11.43 | | | 0.4500 | |
| E1 (1) | 10.90 | | 11.10 | 0.4291 | | 0.4370 |
| E2 | | | 2.90 | | | 0.1141 |
| E3 | 5.8 | | 6.2 | 0.2283 | | 0.2441 |
| G | 0 | | 0.10 | 0.0000 | | 0.0039 |
| H | 15.5 | | 15.9 | 0.6102 | | 0.6260 |
| h | | | 1.10 | | | 0.0433 |
| L | 0.80 | | 1.10 | 0.0314 | | 0.0433 |
| N | | | 10° | | | 10° |
| S | 0° | | 8° | 0° | | 8° |
| T | | 10.0 | | | 0.3937 | |

(1) "D and E1" do not include mold flash or protusions - Mold flash or protusions shall not exceed 0.15mm (0.006")



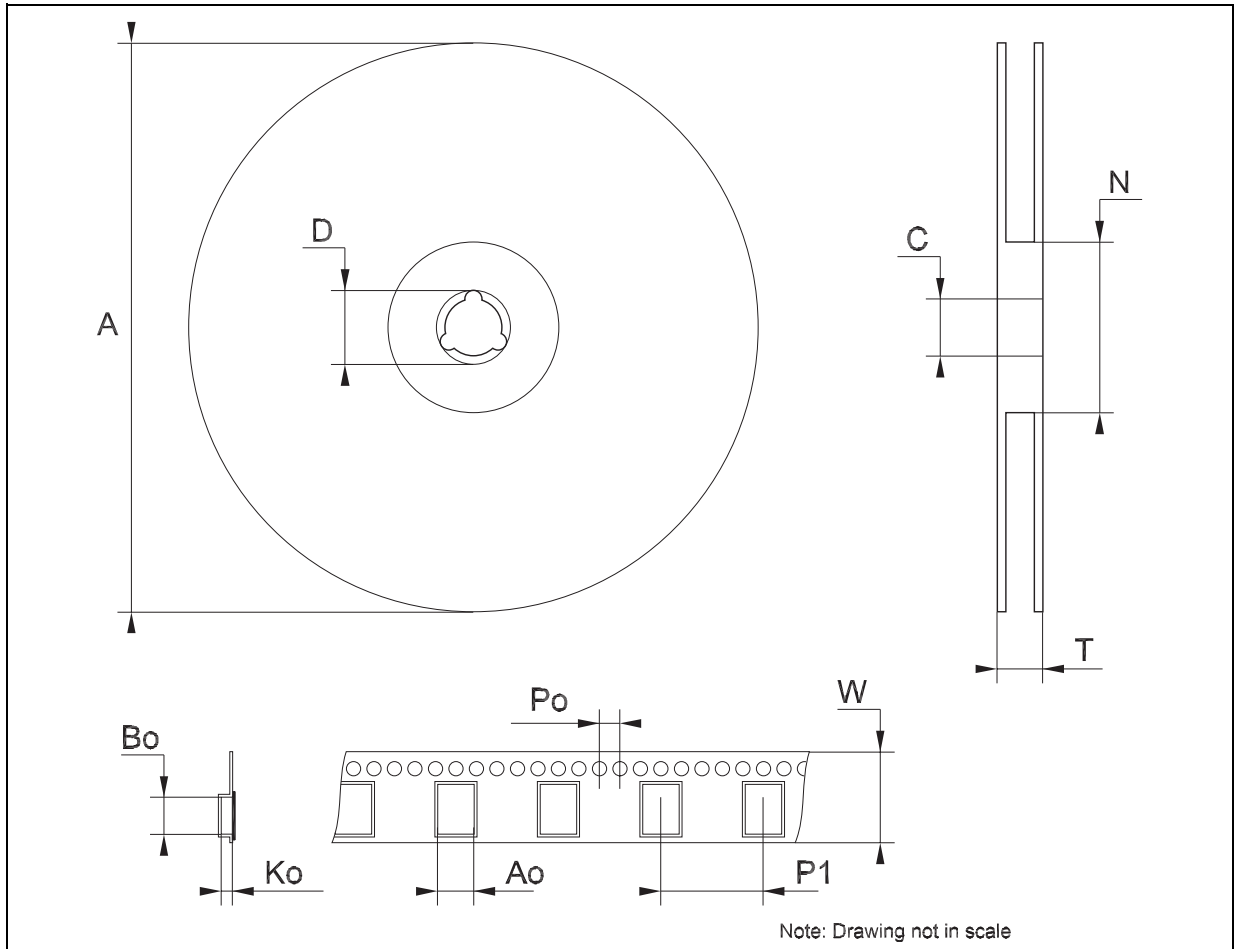
PowerSO-10 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|----------|-------|------|-------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 3.70 | | | 0.146 |
| A1 | | | 0.10 | | | 0.004 |
| A2 | 3.40 | | 3.60 | 0.134 | | 0.142 |
| A3 | 1.25 | | 1.35 | 0.049 | | 0.053 |
| b | 0.40 | | 0.53 | 0.016 | | 0.021 |
| c | 0.35 | | 0.55 | 0.014 | | 0.022 |
| D | 9.40 | | 9.60 | 0.370 | | 0.378 |
| D1 | 7.40 | | 7.60 | 0.291 | | 0.299 |
| E | 13.80 | | 14.40 | 0.543 | | 0.567 |
| E1 | 9.30 | | 9.50 | 0.366 | | 0.374 |
| E2 | 7.20 | | 7.60 | 0.283 | | 0.299 |
| E3 | 5.90 | | 6.10 | 0.232 | | 0.240 |
| e | | 1.27 | | | 0.050 | |
| L | 0.95 | | 1.65 | 0.037 | | 0.065 |
| α | 0° | | 8° | 0° | | 8° |



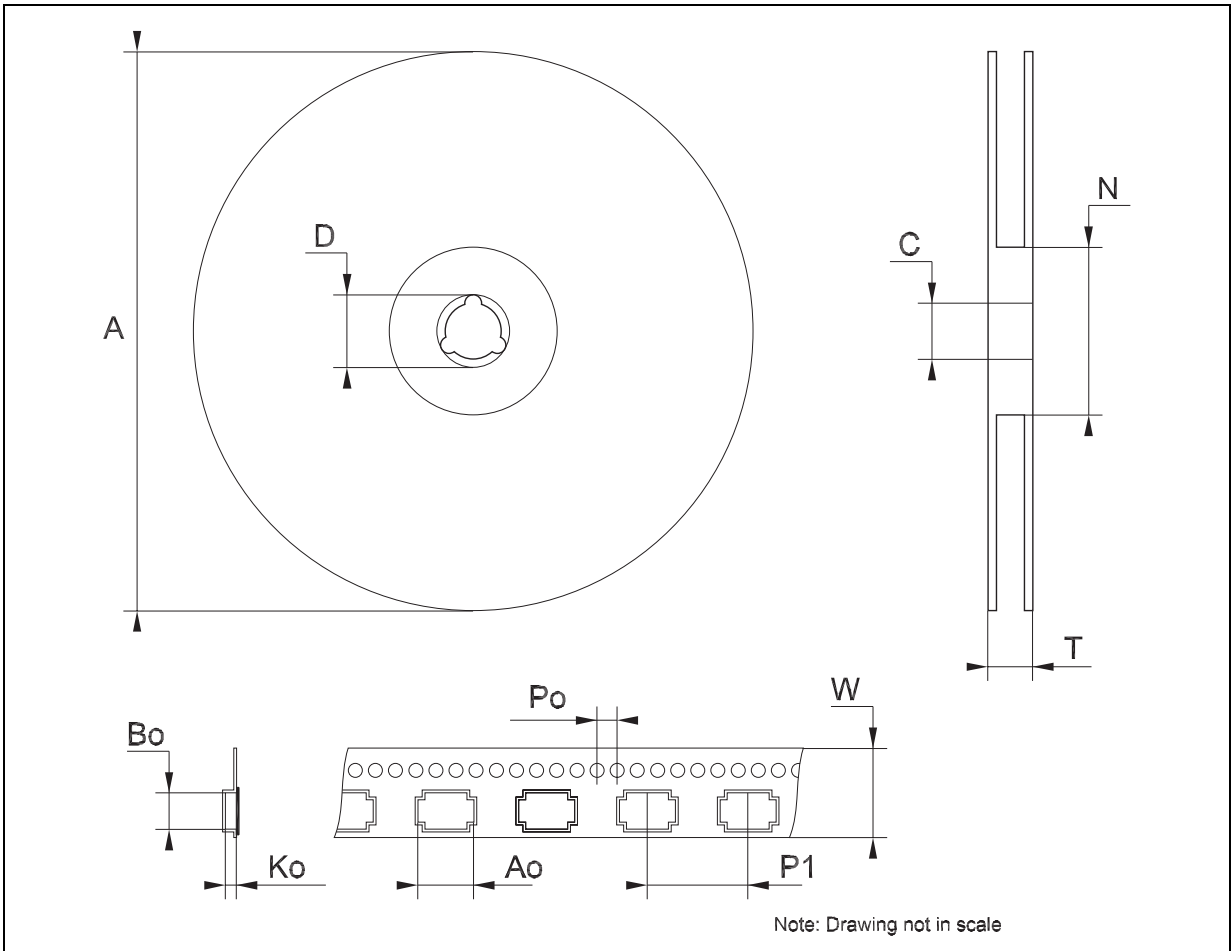
Tape & Reel PowerSO-20 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 30.4 | | | 1.197 |
| Ao | 15.1 | | 15.3 | 0.594 | | 0.602 |
| Bo | 16.5 | | 16.7 | 0.650 | | 0.658 |
| Ko | 3.8 | | 4.0 | 0.149 | | 0.157 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 23.9 | | 24.1 | 0.941 | | 0.949 |
| W | 23.7 | | 24.3 | 0.933 | | 0.957 |



Tape & Reel PowerSO10 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 30.4 | | | 1.197 |
| Ao | 14.9 | | 15.1 | 0.587 | | 0.594 |
| Bo | 9.9 | | 10.1 | 0.390 | | 0.398 |
| Ko | 4.15 | | 4.35 | 0.163 | | 0.171 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 23.9 | | 24.1 | 0.941 | | 0.949 |
| W | 23.7 | | 24.3 | 0.933 | | 0.957 |



9 Revision history

Table 6. Revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 08-Jun-2004 | 7 | Typing Error V_{O1} and V_{O2} on Table 6 - Page 6. |
| 21-Dec-2004 | 8 | Table 2 has been updated on GND row. |
| 07-Sep-2006 | 9 | Add value V_O on table 2 and new template. |
| 03-May-2007 | 10 | Order codes has been updated. |

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